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RESEARCH ARTICLE

High Step-Down Isolated PWM DC–DC Converter Based on Combining a Forward Converter With the Series-Capacitor Structure

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ABSTRACT Incorporating switched-capacitor structures into isolated dc-dc converters is a promising approach to alleviate the limitations of topologies fully based on the use of high step-down transformers. In this paper, the combination of a forward converter with a series-capacitor structure is proposed for applications that require a very high step-down conversion ratio, low output voltage ripple, high output current and isolation. The result of the combination only adds one series-capacitor, one inductor, one switch and one diode (or synchronous rectifier switch) to the component count of a conventional forward converter, thus avoiding the use of a complete second phase. The topology provides high step-down conversion ratio and low output voltage ripple, a characteristic that can be used to decrease the total energy stored by inductors (i.e., higher power density) and/or to reduce the switching frequency (i.e., higher efficiency). Moreover, the converter provides inherent current sharing between the two inductors, natural balance of the voltage across the series-capacitor and lower conduction losses. The converter operation is validated with a 100W and 48V-to-5/3.3/2.5/1.8V prototype that achieves a peak efficiency of 95.8% and a full load efficiency of 91.1%.

INDEX TERMS High conversion ratio, hybrid switched-capacitor converters, isolated converters.

I. INTRODUCTION

Nowadays, many power electronics applications, such as electrical vehicles, renewable energy systems, telecom systems and datacenters, require extremely high dc-dc step-down conversions. Typically, an isolated Pulse-Width Modulated (PWM) dc-dc converter with a high step-down transformer that is responsible for the main part of the voltage conversion is used [1], [2], [3], [4]. However, this transformer is one of the major contributors to the overall loss and size of the converter. Alternatively, isolated resonant dc-dc converters, such as LLC dc-dc converters [5], [6], [7], can be used to increase the efficiency and the power density at the expense of penalizing electromagnetic compatibility due to the variable frequency control. More complex approaches have been explored to minimize the impact of the high step-down transformer, such as splitting it into smaller transformers [8] or combining a non-regulated LLC dc-dc converter with a PWM dc-dc converter [9], [10].

Recently, the interest in Switched-Capacitor (SC) dc-dc converters has increased for very high dc-dc step-down conversions when isolation between input and output ports is not mandatory [11], [12]. A pure SC dc-dc converter performs the voltage conversion without magnetic elements, thus potentially reaching an extremely high power density. In addition, they commonly reduce the voltage stress across the switches, which enables the use of devices with better figure-of-merit ($R_{DS-ON} \cdot Q_G$), thus allowing the converter to

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TABLE 1. DC-DC converters for high step-down conversions.

	SC converters			High step-down transformer		Step-down transformer + SC structure	
	Pure	Resonant	PWM	Resonant	PWM	Resonant	PWM
Power density	Very high	Very high	High	Medium/High	Low	High	Medium/High
Output voltage regulation	No	Variable frequency[*1]	Constant frequency	Variable frequency[*1]	Constant frequency	Variable frequency[*1]	Constant frequency
Isolation	No	No	No	Yes	Yes	Yes	Yes

[*1] Variable frequency control penalizes electromagnetic compatibility.

operate at higher frequencies to further increase the power density. Unfortunately, they suffer from large current spikes during switching transitions because the SCs are directly charged/discharged by other capacitors or voltage sources. This effect reduces efficiency, increases the current stresses of switches, and can cause electromagnetic interference problems. Another drawback is that SC dc-dc converters are only able to perform fixed voltage conversions (i.e., 2-to-1, 4-to-1, 8-to-1, etc.) and there is no lossless method to regulate the output voltage.

An alternative method to avoid the problems resulting from the current spikes of pure SC dc-dc converters is to add one or more inductors. It is important to note that the size of these inductors is much smaller than that of a conventional non-isolated dc-dc converter because they only store the energy needed to achieve the soft charge/discharge of the capacitors. This approach has demonstrated excellent performance in terms of both efficiency and power density when hybrid SC Resonant (SC-R) dc-dc converters are used with fixed conversion ratios [13], [14], [15], [16]. However, the resonant nature of these topologies compromises the electromagnetic compatibility when output voltage regulation is mandatory. An interesting approach to enable output voltage regulation at constant frequency is to increase the energy stored by the inductor and follow a conventional PWM control strategy. In this way, the regulation capability is improved at the expense of reducing the power density. Fortunately, hybrid SC PWM (SC-PWM) dc-dc converters, such as the multi-level flying capacitor buck converter [17], [18], [19], the series-capacitor buck converter [20], [21], [22], [23], [24], or combinations of them [25], [26], still achieve a remarkable improvement over conventional non-isolated dc-dc converters due to the lower voltage swing across inductors.

Considering the limitations of high step-down transformers and the benefits of SC-PWM dc-dc converters, developing novel isolated dc-dc converters by incorporating SC structures is a promising approach for applications that require extremely high dc-dc step-down conversions and isolation (see Table 1). Currently, there are a few studies that have combined SC structures with isolated PWM dc-dc converters. In [27], the flying-capacitor structure is combined with a Half-Bridge (HB) dc-dc converter with Current-Doubler (CD) rectifier. Unfortunately, the flying-capacitor structure does not achieve natural voltage balance, which is mandatory to take advantage of its benefits. Moreover, the current-doubler rectifier does not naturally balance the current that flows through the inductors. As a consequence, active control is mandatory to solve these issues [27]. Furthermore, the leakage inductance of the transformer causes parasitic oscillations on the drain-to-source voltage of the primary side switches. As a result, a ringing suppression circuit must be employed [27]. In [28], an stacked HB dc-dc converter with CD rectifier is proposed. The topology balances the current through the inductors by increasing the number of capacitors. However, the leakage inductance of the transformer also compromises the converter operation. In order to suppress the ringing of the primary side switches, a transformer with interleaved winding structure is used [28]. This technique minimizes the leakage inductance at the expense of increasing the transformer complexity and its cost.

SC structures can also be combined with isolated resonant or quasi-resonant dc-dc converters to reach high step-down conversions and high power density [29], [30], [31], [32], [33], [34], [35]. Unfortunately, these approaches suffer the well-known problems of resonant converters: variable frequency control penalizes the electromagnetic compatibility and the efficiency falls rapidly if they do not operate in the optimal point. A quasi-resonant flying-capacitor HB dc-dc converter with CD rectifier is proposed in [29]. Another approach can be found in [30], where a center-tapped transformer and an output inductor are used to derive a novel isolated resonant dc-dc converter. This converter is modified in [31] by using a full-wave rectifier and by eliminating the output inductor. 3-level LLC dc-dc converters based on staking the HB structure are proposed in [32]. Similarly, the flying-capacitor structure is used in [33] to derive a 3-level LLC dc-dc converter. The series-capacitor structure is combined with the LLC dc-dc converter in [34] and [35].

In this paper, a PWM dc-dc converter is proposed for applications that require a very high step-down conversion ratio, low output voltage ripple, high output current and isolation. The topology is the result of combining a forward converter with the series-capacitor structure. Typically, this SC structure must be combined with two-phase topologies both in non-isolated [20], [21], [22], and isolated resonant [34], [35], dc-dc converters. However, the series-capacitor

forward converter (see Fig. 1) only adds one series-capacitor, one inductor, one switch and one diode (or synchronous rectifier switch) to the component count of a conventional forward converter. The topology has been recently introduced and firstly proposed in [36] as an alternative to parallel-connected converters for solving the temperature problems of output inductors that drive high current. As previously indicated, in this work the topology is proposed for a wider range of applications, which requires a deeper analysis in order to identify the benefits and drawbacks with respect to other topologies with similar target. In comparison to the conventional forward converter, the series-capacitor forward converter achieves a higher step-down conversion ratio and a remarkable reduction of the output voltage ripple, which can be translated into lower total energy stored by inductors (i.e., higher power density for similar efficiency) and/or lower switching frequency (i.e., higher efficiency for similar power density). Moreover, the converter naturally balances both the voltage across the series-capacitor and the inductors currents, thus avoiding the use additional circuitry focused on these issues. Furthermore, it also reduces the conduction losses. These benefits make the series-capacitor forward converter a suitable topology for applications that require a high step-down conversion ratio, isolation and high output current.

The rest of the paper is organized as follows. The topology is described and analyzed in Section II. A comparison to a conventional forward converter is provided in Section III to identify the main benefits and drawbacks. The experimental results are given in Section IV. Finally, Section V concludes this paper.

II. SERIES-CAPACITOR FORWARD CONVERTER

The converter is the result of combining a forward converter with a series-capacitor structure. Fig. 1 shows the different versions of the topology that can be derived depending on the forward converter version considered for the combination [37]. In contrast to previous combinations of a series-capacitor structure with non-isolated [20], [21], [22] or isolated resonant [34], [35], dc-dc converters, the series-capacitor forward converter is not derived from a complete multi-phase converter. As Fig. 1 shows, in all cases, the series-capacitor structure modifies the output side of the topology by only adding a series-capacitor (C_1), an inductor (L_2), a switch (S_{2A}) and a diode (or synchronous rectifier switch, S_{2B}), thus preventing the use of additional transformers (with their reset circuit) and input-side switches. Hence, the input side of the topologies do not suffer any change with respect to the conventional counterparts. This work is focused on the combination with the Active Clamp Forward (ACF) converter due to its benefits with respect to other versions of the forward topology (no extra reset winding, no voltage spikes across the primary side switch caused by the leakage inductance, etc.) [37]. However, the analysis of this work can be extended to the combinations with other versions of the forward converter. Moreover, it is important to note that although the following analysis considers diodes for drawing the rectifier switches, synchronous rectification is recommended to reduce the conduction losses.

A. PRINCIPLE OF OPERATION

The primary side of the Series-Capacitor Active Clamp Forward (SC-ACF) converter is made up of the transformer primary winding, the main switch of the primary side S_{1A}, the clamp switch S_{1B} and the clamp capacitor C_{Cl}. The secondary side comprises two phases connected to the output capacitor C_O and the resistive load R. The first phase is made up of diodes/synchronous rectifier switches S_{1C} and S_{1D}, inductor L_1 and series-capacitor C_1. The second phase comprises the main switch of the secondary side S_{2A}, the diode/synchronous rectifier switch S_{2B} and inductor L_2.

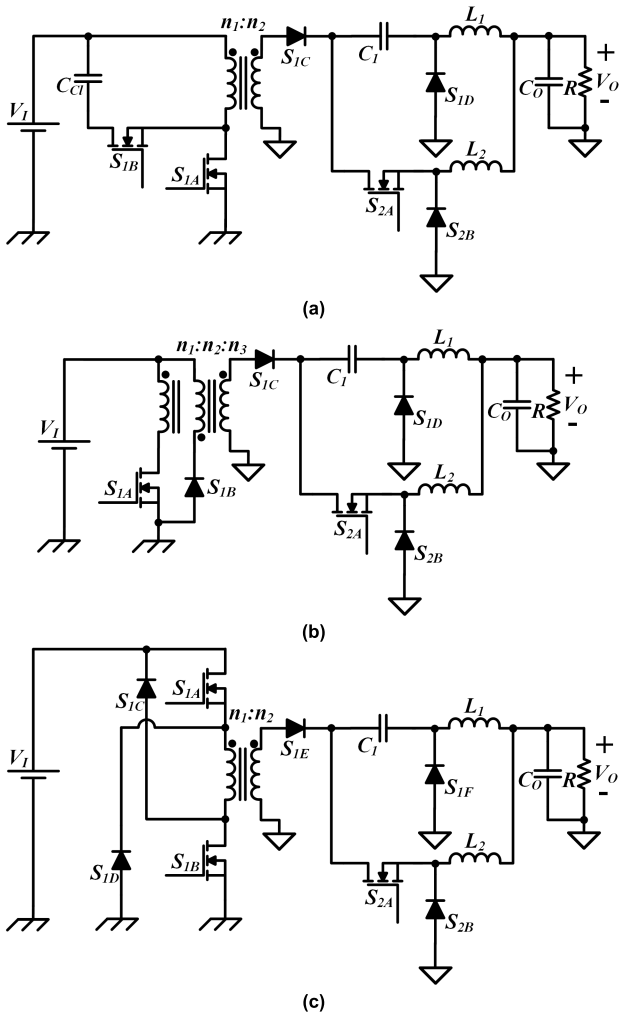

FIGURE 1. Three variants of the series-capacitor forward converter: a) Version derived from the active-clamp forward converter. b) Version derived from the three-winding forward converter. c) Version derived from the two-transistor forward converter.

The description of the converter operation is aided by the sub-circuits shown in Fig. 2, the figure for detailing the voltage and current notation of the topology (i.e., Fig. 3), and the waveforms depicted in Fig. 4. The following analysis assumes that the SC-ACF converter operates in Continuous

Conduction Mode (CCM), the duty cycle d is lower than 0.5 (although higher d values are valid, the operation is different and it is not interesting for high step-down conversion ratios), switches are ideal, the impact of transformer leakage inductance is negligible for describing the operation and the voltage across capacitors is constant. As Fig. 4 shows, the control signals of S_{1A} and S_{2A} have the same d value and a phase shift of 180°. The switching period (T_S) is described through four states (I-IV).

During state I ($0 < t < dT_S$), S_{1A} is ON and S_{2A} is OFF. Consequently, S_{1C} is forward biased because the voltage across the transformer primary winding v_{Pri} is equal to the voltage of the input voltage source V_I. In this way, the transformer secondary winding is connected to L_1 through C_1. As a result, the voltage across the series-capacitor V_{C1} is subtracted to the voltage across the transformer secondary winding v_{Sec}, thus reducing the voltage across the first inductor v_{L1}. During this state, L_1 stores energy and, therefore, its current i_{L1} rises linearly charging C_1. At the same time, the current through the second inductor i_{L2} forward biases S_{2B} connecting L_2 between the ground of the secondary side and the positive output terminal. Hence, L_2 delivers energy to the output and i_{L2} falls linearly. On the primary side, S_{1A} drives the reflected current from L_1 and the magnetizing current i_{LM}.

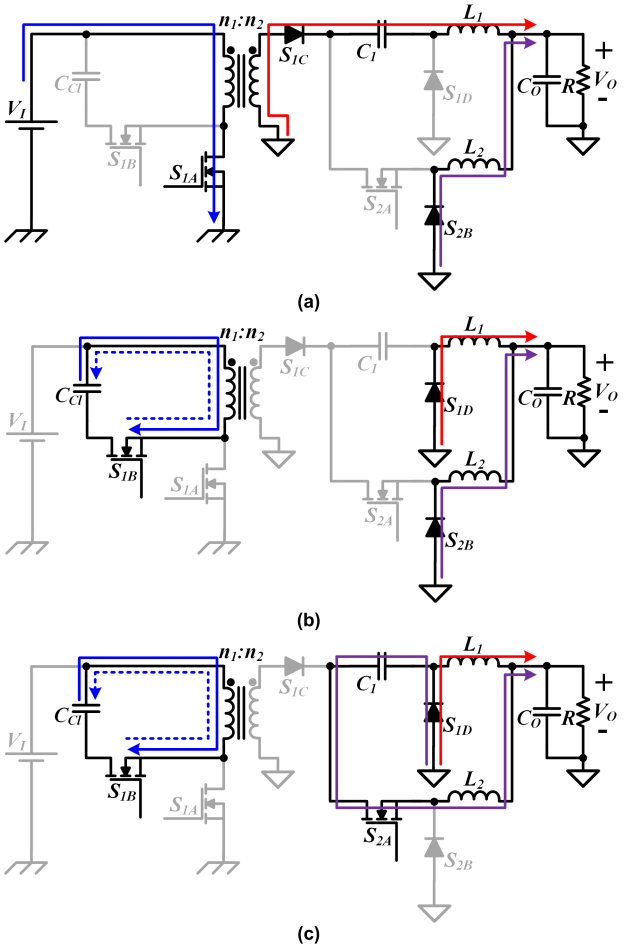

FIGURE 2. Current paths of the series-capacitor active clamp forward converter: a) State I. b) States II and IV. c) State III.

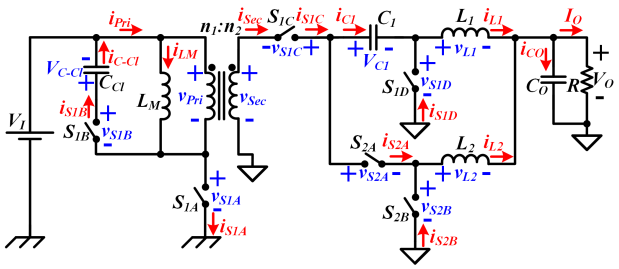

FIGURE 3. Voltage and current notation of the series-capacitor active-clamp forward converter.

During state II ($dT_S < t < T_S/2$), both S_{1A} and S_{2A} are OFF. In this state, i_{LM} forward biases S_{1B} and, consequently, the voltage across the transformer primary winding is negative, thus reverse biasing S_{1C}. At the same time, i_{L1} forward biases S_{1D} connecting L_1 between the ground of the secondary side and the positive output terminal. Therefore, L_1 delivers energy to the output and i_{L1} falls linearly. i_{L2} is still driven by S_{2B} and, consequently, the only change in the second phase with respect to state I is that S_{2A} blocks less voltage (the voltage across the series-capacitor). Since there is no current flowing through C_1, it preserves its charge.

During state III ($T_S/2 < t < T_S/2 + dT_S$), S_{1A} is OFF and S_{2A} is ON. Consequently, there is no change in the primary side and S_{1C} is reverse biased. i_{L1} is still driven by S_{1D} falling linearly and L_1 delivers energy to the output. At the same time, S_{2B} is reverse biased and i_{L2} is driven by S_{2A}, C_1 and S_{1D}. In this state, C_1 supplies the second phase, L_2 stores energy and i_{L2} rises linearly.

State IV ($T_S/2 + dT_S < t < T_S$) is identical to state II because S_{1A} and S_{2A} are OFF. Hence, i_{L1} and i_{L2} are driven by S_{1D} and S_{2B}, respectively.

Regarding the active clamp mechanism, it is identical to that of a conventional ACF converter [37], [38], [39], [40]. At the beginning of state I, i_{LM} is driven by S_{1A} and rises linearly starting with a negative value. When S_{1A} is turned OFF at the end of state I, i_{LM} is positive, thus forward biasing S_{1B}. That switch must be actively turned-on until the end of the switching period to enable i_{LM} to flow later in the opposite direction. It is important to note that i_{LM} falls linearly since the beginning of state II and until the end of the switching period, finishing with a negative value.

B. VOLTAGE CONVERSION RATIO AND VOLTAGE ACROSS THE SERIES-CAPACITOR

Three key elements are responsible for the voltage conversion in the SC-ACF converter. The first one is the transformer, whose contribution to the voltage conversion is determined by the ratio between the turns number of the primary (n_1) and secondary (n_2) windings. The second key element is the PWM control technique, which allows us to regulate part of the voltage conversion with d. The third key element is the series-capacitor, which participates in the voltage

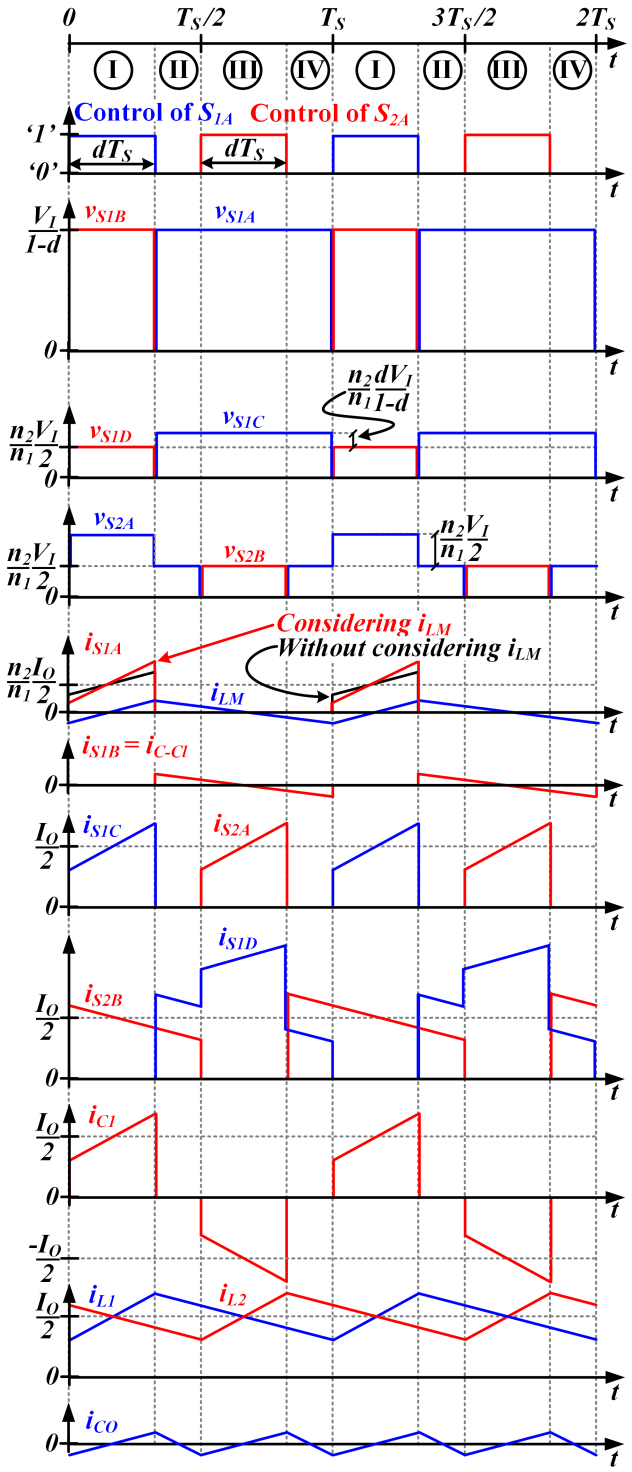

FIGURE 4. Main voltage and current waveforms of the series-capacitor active-clamp forward converter.

conversion process by storing energy during state I and delivering that energy during state III. Therefore, determining the voltage across the series-capacitor V_{C1} is essential to obtain the voltage conversion ratio M. Both V_{C1} and M can be calculated by applying the volt-second balance to L_1 and L_2.

The voltage across L_1 is

$$v_{L1} = \begin{cases} \dfrac{n_2}{n_1} V_I - V_{C1} - V_O, & \textit{in state I}, \\ -V_O, & \textit{in states II, III and IV}. \end{cases} \tag{1}$$

Averaging (1) leads to

$$V_O = d\left(\frac{n_2}{n_1} V_I - V_{C1}\right). \tag{2}$$

The voltage across L_2 is

$$v_{L2} = \begin{cases} -V_O, & \textit{in states I, II and IV}, \\ V_{C1} - V_O, & \textit{in state III}. \end{cases} \tag{3}$$

Averaging (3) leads to

$$V_{C1} = \frac{V_O}{d}. \tag{4}$$

Substituting (4) into (2) allows us to obtain the voltage conversion ratio

$$M = \frac{V_O}{V_I} = \frac{d}{2}\frac{n_2}{n_1}, \tag{5}$$

and the voltage across C_1

$$V_{C1} = \frac{n_2}{n_1}\frac{V_I}{2}. \tag{6}$$

As a conclusion, the voltage across the series-capacitor is naturally balanced, thus avoiding the use of voltage sensors and controls loops focused on that issue.

Considering that d ranges between 0 and 0.5, the available conversion range is

$$M \in \left(0, \frac{1}{4}\frac{n_2}{n_1}\right). \tag{7}$$

According to (6), during state I, the equivalent input voltage of the first phase is half that of a conventional ACF converter because V_{C1} is subtracted from the voltage across the secondary-winding. Moreover, during state III, the equivalent input voltage of the second phase is also half that of a conventional ACF converter because that phase is supplied by the series-capacitor. As a consequence, and according to (5), the voltage conversion ratio of the SC-ACF converter is one half that of a conventional ACF converter considering the same d value and the same transformer. This characteristic makes the SC-ACF converter suitable for applications that require high step-down conversion ratios.

As in the case of the conventional ACF converter, the voltage across the clamp capacitor V_{C-Cl} can be calculated by applying the volt-second balance to magnetizing inductance L_M

$$V_{C-Cl} = \frac{dV_I}{1-d}. \tag{8}$$

C. INDUCTORS CURRENTS AND OUTPUT VOLTAGE RIPPLE

Substituting (5) and (6) into (1) allows us to express v_{L1} as a function of M and V_I

$$v_{L1} = \begin{cases} \left(\frac{1}{2}\frac{n_2}{n_1} - M\right) V_I, & \textit{in state I} \\ -MV_I, & \textit{in states II, III and IV}. \end{cases} \tag{9}$$

During state I, i_{L1} rises linearly, the slope being

$$\left.\frac{di_{L1}}{dt}\right|_I = \frac{\left(\frac{1}{2}\frac{n_2}{n_1} - M\right) V_I}{L_1}. \tag{10}$$

Moreover, i_{L1} falls linearly during states II, III and IV with a slope of

$$\left.\frac{di_{L1}}{dt}\right|_{II,III,IV} = -\frac{MV_I}{L_1}. \tag{11}$$

In the case of L_2, substituting (5) and (6) into (3) allows us to express v_{L2} as a function of d and V_I

$$v_{L2} = \begin{cases} -MV_I, & \textit{in states I, II and IV} \\ \left(\frac{1}{2}\frac{n_2}{n_1} - M\right) V_I, & \textit{in state III}. \end{cases} \tag{12}$$

During state III, i_{L2} rises linearly, the slope being

$$\left.\frac{di_{L2}}{dt}\right|_{III} = \frac{\left(\frac{1}{2}\frac{n_2}{n_1} - M\right) V_I}{L_2}. \tag{13}$$

Moreover, i_{L2} falls linearly during states I, II and IV with a slope of

$$\left.\frac{di_{L2}}{dt}\right|_{I,II,IV} = -\frac{MV_I}{L_2}. \tag{14}$$

The ripple of i_{L1} can be obtained from (10)

$$\Delta i_{L1} = \frac{\left(1 - 2M\frac{n_1}{n_2}\right) MV_I}{L_1 f_S}, \tag{15}$$

where f_S is the switching frequency. The ripple of i_{L2} can be obtained from (13)

$$\Delta i_{L2} = \frac{\left(1 - 2M\frac{n_1}{n_2}\right) MV_I}{L_2 f_S}. \tag{16}$$

The current that flows through the output capacitance i_{CO} is the AC component of the sum of i_{L1} and i_{L2}. Considering $L_1 = L_2 = L$, the ripple of i_{CO} is

$$\Delta i_{CO} = \frac{\left(1 - 4M\frac{n_1}{n_2}\right) MV_I}{Lf_S}. \tag{17}$$

The output voltage ripple can be calculated considering the charge stored and delivered by C_O during a switching period and taking into account that the frequency of i_{CO} is $2f_S$

$$\Delta v_O = \frac{\left(1 - 4M\frac{n_1}{n_2}\right) MV_I}{16LC_O f_S^2}. \tag{18}$$

Although a detailed evaluation of the improvement in comparison to a conventional ACF converter is provided in Section III, at this point, it is important to highlight that the low output voltage ripple is achieved due to three facts. First, the SC-ACF converter reduces Δi_{L1} and Δi_{L2} because, according to (1) and (3), C_1 lowers the swing of the voltage across both inductors during the magnetizing stages. Second, Δi_{CO} is lower than Δi_{L1} and Δi_{L2} due to the 180° phase-shift between i_{L1} and i_{L2}. Third, the effective switching frequency (frequency of i_{CO}) is $2f_S$.

D. AUTOMATIC BALANCE OF PHASE CURRENTS

The SC-ACF converter automatically balances the average inductor currents, thus avoiding the use of current sensors and controls loops focused on that issue. This feature can be explained by analyzing the charging and discharging mechanism of C_1. Since V_{C1} must be constant in steady-state operation, the charge stored by C_1 while i_{L1} rises during state I must be equal to the charge that C_1 delivers while i_{L2} rises during state III. The charge variation of C_1 during state I is:

$$\Delta Q_{C1-I} = < i_{L1} > dT_S, \tag{19}$$

where $<i_{L1}>$ is the average value of i_{L1}. On the other hand, the charge variation of C_1 during state III is:

$$\Delta Q_{C1-III} = - < i_{L2} > dT_S, \tag{20}$$

where $<i_{L2}>$ is the average value of i_{L2}. As previously indicated, the average charge variation must be 0 in steady-state operation, which leads to

$$< i_{L1} > = < i_{L2} > = \frac{I_O}{2}, \tag{21}$$

where I_O is the output current. Intuitively, if $<i_{L1}>$ is higher than $<i_{L2}>$, V_{C1} would rise because the charge of C_1 would be higher at the end of the next switching period. As a result, the voltage across L_1 during state I would fall because the voltage subtracted by C_1 to the secondary winding would be higher. Moreover, the voltage across L_2 during state III would be higher. Consequently, $<i_{L1}>$ would fall and $<i_{L2}>$ would rise, thus eliminating the mismatch.

E. VOLTAGE RIPPLE OF THE SERIES-CAPACITOR

Obtaining the voltage ripple across C_1 is essential because the analysis of the converter's behavior considers that V_{C1} is constant. C_1 is soft charged during state I driving i_{L1}. Similarly, it is soft discharged during state III driving i_{L2}. Therefore, the voltage ripple across C_1 can be modeled as:

$$\Delta v_{C1} = \frac{dI_O}{2C_1 f_S} = \frac{n_1}{n_2}\frac{MI_O}{C_1 f_S}. \tag{22}$$

F. SWITCHES VOLTAGE AND CURRENT STRESSES

The performed analysis allows us to evaluate the switches stresses in terms of maximum voltage and RMS current. Table 2 summarizes the results.

TABLE 2. Maximum voltage and RMS current stresses of the SC-ACF converter switches.

Switch	Maximum Voltage Stress	RMS Current Stress[*1]
S_{1A}	$\frac{V_I}{1-2M\frac{n_1}{n_2}}$	$I_O\sqrt{\frac{M}{2}\frac{n_2}{n_1}}$
S_{1B}	$\frac{V_I}{1-2M\frac{n_1}{n_2}}$	-[*2]
S_{1C}	$\frac{\frac{n_2}{n_1}+2M}{1-2M\frac{n_1}{n_2}}\frac{V_I}{2}$	$I_O\sqrt{\frac{M}{2}\frac{n_1}{n_2}}$
S_{1D}	$\frac{n_2}{n_1}\frac{V_I}{2}$	$\frac{I_O}{2}\sqrt{1+4M\frac{n_1}{n_2}}$
S_{2A}[*3]	$\frac{n_2}{n_1}V_I$	$I_O\sqrt{\frac{M}{2}\frac{n_1}{n_2}}$
S_{2B}	$\frac{n_2}{n_1}\frac{V_I}{2}$	$\frac{I_O}{2}\sqrt{1-2M\frac{n_1}{n_2}}$

[*1] Inductor current ripples are neglected for the RMS current stresses calculation.
[*2] It depends on L_M, which is considered infinite for this analysis.
[*3] The voltage across S_{2A} before the turn-on and after the turn-off is half the maximum voltage stress indicated in this table.

III. COMPARISON TO A CONVENTIONAL ACF CONVERTER

Apart from the higher step-down conversion ratio, the main benefit of the SC-ACF converter in comparison to a conventional ACF converter is the lower output voltage ripple. As will be evaluated in this section, this characteristic is translated into the use of magnetics with lower size and/or the operation at lower switching frequency when a particular output voltage ripple specification must be met.

A. SCENARIO 0: SAME SIZE, SAME SWITCHING FREQUENCY AND LOWER OUTPUT VOLTAGE RIPPLE

In order to perform a comparison that allows us to gather clear conclusions, the following scenario is considered (scenario 0): both converters operate at the same switching frequency and their size (mainly determined by the magnetics) is similar. As will be shown below, in this scenario, the SC-ACF converter achieves lower output voltage ripple and lower conduction loss than the conventional ACF converter. However, the extra switching loss of S_{2A} may penalize the efficiency. Moreover, this section allows us to introduce the well-known model used for estimating power loss [22], [41].

Considering the same transformer for both converters would lead to different core and winding losses because, as indicated in Section II-B, the voltage conversion ratio of the SC-ACF converter is one half that of a conventional ACF converter assuming the same d value. Hence, the transformer considered in this section for each converter will be different in terms of design, but similar in terms of losses and size, thus facilitating the conclusions drawing. In this way, some conditions must be met. Transformer core loss can be modeled as

$$P_{fe} = K_1 f^x B^y V_e, \tag{23}$$

where K_1 is a constant for core material; f is the frequency; x is the frequency exponent; B is the peak ac flux density; y is the flux density exponent; and V_e is the effective core volume. The peak ac flux density can be evaluated as

$$B = \frac{1}{2nA_c}\int_0^{dT_s} v_w dt, \tag{24}$$

where A_c is the core cross-sectional area, n is the turns number of the winding and v_w is the voltage across the winding. Considering (24), the duty cycle of the conventional ACF converter (d_C) must be equal to that of the SC-ACF converter (i.e., $d_C = d$) in order to ensure the same core loss in the transformer of each converter. Moreover, the turns number of the primary windings must be the same for both designs (i.e., $n_{1C} = n_1$). As a consequence, since both converters must provide the same output voltage, the turns number of the secondary winding of the conventional ACF converter (n_{2C}) must be half that of the SC-ACF converter (i.e., $n_{2C} = n_2/2$).

The copper loss of a transformer winding can be evaluated as

$$P_{cu} = R_{cu} i_{cu-RMS}^2, \tag{25}$$

where R_{cu} and i_{cu-RMS} are the resistance of the winding and the root mean square current that flows through it, respectively. Taking into account that $n_{1C} = n_1$, the resistance of the primary winding is the same for both converters. Moreover, the primary winding current of the conventional ACF converter is equal to that of the SC-ACF converter. Consequently, both converters have the same cooper loss in the primary winding of the transformer in scenario 0. The current flowing through the transformer secondary winding of the conventional ACF converter is twice that of the SC-ACF converter. Hence, the wire section of the last one must be half that of the first one in order to ensure the same transformer copper losses and size.

Regarding the inductances, it is considered that the inductance of the conventional ACF converter is implemented by connecting in parallel the two inductances of the SC-ACF converter. As explained below, this approach ensures the same total size and losses. Equation (25) also applies for evaluating the copper loss of each winding. Each inductance of the SC-ACF converter drives $I_O/2$ (current ripple is neglected). In the case of the conventional ACF converter, the inductance drives I_O. However, its copper loss is equal to the total copper loss of the inductances of the SC-ACF converter because the equivalent winding resistance is halved due to the parallel connection. Equations (23) and (24) also apply for evaluating the core loss of each inductance. Taking into account that $n_{1C} = n_1$, that $n_{2C} = n_2/2$ and that $d_C = d$, the voltage excitation of the inductances is the same when they are used in the phases of the SC-ACF converter and when they are parallel connected in the conventional ACF converter. Consequently, the core loss of the equivalent inductance of the ACF converter is equal to the total core losses of the two inductances of the SC-ACF converter.

In this way, the described scenario ensures the same size for both converters and, moreover, the same power losses caused by magnetics. Furthermore, scenario 0 implies that the equivalent inductance of the ACF converter is half that of the SC-ACF converter (i.e., $L_C = L/2$).

It is important to note that the SC-ACF converter has the extra loss of the series-capacitor due to its equivalent series resistance (R_{C1}). Neglecting the current ripple, the loss of C_1 can be evaluated taking into account R_{C1} and the root mean square current that flows through the capacitor

$$P_{C1} = R_{C1} d \frac{I_O^2}{2}, \tag{26}$$

In general, the series-capacitor loss is negligible in comparison to the conduction loss of the secondary side switches and the copper loss of the windings [22].

At this point, a qualitative analysis of switch losses can be addressed. The target of this analysis is to identify the differences between both converters in terms of switch losses rather than accurately estimating them (which typically requires non-analytical approaches, such as TCAD simulations [42], [43]). It is important to note that synchronous rectification is considered in this section and, moreover, inductor current ripples are neglected. The conduction loss of a switch can be evaluated as

$$P_{S-Cond} = R_{DS-ON} i_{S-RMS}^2, \tag{27}$$

where R_{DS-ON} and i_{S-RMS} are the on-resistance of the switch and the root mean square current that flows through it, respectively. Since the currents flowing through the primary side of the ACF converter and the SC-ACF converter are the same in scenario 0, there is no difference in terms of primary side switches conduction losses. In the case of the SC-ACF converter, the RMS current stresses (see Table 2) allow us to determine the total conduction loss of the secondary side switches as follows

$$P_{Sec-Cond} = \frac{R_{DS-ON} I_O^2}{2} \left[3 \frac{n_1}{n_2} M + 1 \right], \tag{28}$$

Note that it is considered that all secondary side switches have the same R_{DS-ON}. In the case of a conventional ACF converter, the total conduction loss of the secondary side switches can be modeled as

$$P_{Sec-Cond-C} = R_{DS-ON} I_O^2. \tag{29}$$

The normalized conduction losses of the secondary side switches for each converter are compared in Fig. 5. The normalization basis is the product of the on-resistance and the output current squared (i.e., conduction losses are divided by $R_{DS-ON} I_O^2$). As can be seen, the two-phase structure of the secondary side allows the SC-ACF converter to reduce conduction loss of the secondary side switches.

The switching loss of a switch can be evaluated considering gate drive loss (negligible in comparison to the other sources of switching loss), transition loss and output capacitance loss

$$P_{S-SW} = C_{iss} V_{drv}^2 f_S + \frac{I_D V_{DS} \left(t_r + t_f \right)}{2} f_S + E_{oss} f_S, \tag{30}$$

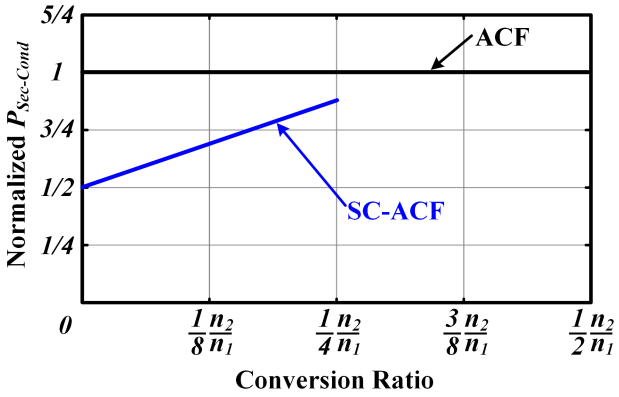

FIGURE 5. Comparison between the normalized conduction loss of the secondary side switches for each converter. Note that the conversion ratio is expressed as a function of the turns ratio of the SC-ACF converter transformer.

where C_{iss} is the switch parasitic input capacitance, V_{drv} is the gate driver supply voltage; I_D is the drain current at turn on; V_{DS} is the drain-to-source voltage the switch blocks before switching; t_r is the rise time of the current through the switch; t_f is the voltage fall time; and E_{oss} is the energy stored by the parasitic output capacitance. If the switch operates with Zero-Voltage Switching (ZVS), the switching loss can be estimated by only computing gate drive loss

$$P_{S-SW} \cong C_{iss} V_{drv}^2 f_S, \tag{31}$$

In a conventional ACF converter, all diodes/synchronous rectifier switches operate with ZVS. Furthermore, the energy stored both in the leakage and in the magnetizing inductor of the transformer is recycled to achieve full or partial ZVS in the main switch and in the clamp switch of the primary side. However, turning-on the main switch with full ZVS is not straightforward. The reason is that part of the energy stored by the magnetizing inductance is transferred to the secondary side during the resonant state instead of being use to discharge the output capacitance of the main switch [38], [39], [40]. In particular, the amount of energy stored by the magnetizing inductance that is used to achieve ZVS in the main switch falls as the output current rises. As a result, ensuring ZVS at low load is more feasible than at full load. Obviously, the magnetizing inductance could be reduced to store more energy and, consequently, to extend the ZVS range to higher output current values. However, that approach increases the conduction losses of the primary side. In summary, the switching losses of a conventional ACF converter is mainly determined by the switching loss of the primary side main switch.

In the SC-ACF converter, as in the case of the conventional counterpart, all diodes/synchronous rectifier switches (i.e., S_{1C}, S_{1D} and S_{2B}) and the clamp switch (i.e., S_{1B}) operate with ZVS. The reasoning regarding the main switch of the conventional ACF converter also applies for the main switch of the SC-ACF converter (i.e., S_{1A}). An intuitive explanation of the ZVS mechanism for the SC-ACF converter is provided

in the appendix section. In this way, S_{2A} would be the only switch without full or partial ZVS (it would require to increase the current ripple of the output inductors as in any buck-derived converter). In summary, the switching losses of the SC-ACF converter are mainly determined by the switching loss of S_{1A} and S_{2A}.

In scenario 0, both converters operate with the same switching frequency and, consequently, both the main switch of the ACF converter and the primary side main switch of the SC-ACF converter (i.e., S_{1A}) have the same switching loss (note that both switches are equivalent in terms of voltage and current stresses). However, the SC-ACF converter suffers the extra switching loss of S_{2A}.

In summary, in scenario 0, the SC-ACF converter exhibits lower conduction loss of secondary side switches, but higher switching loss than the conventional counterpart due to S_{2A}.

At this point, the improvement achieved in terms of output voltage ripple reduction can be evaluated. The output voltage ripple of a conventional ACF converter that has the same output capacitor of the SC-ACF converter is

$$\Delta v_{OC} = \frac{\left(1 - M\frac{n_{1C}}{n_{2C}}\right) MV_I}{8L_C C_O f_{SC}^2}, \tag{32}$$

where L_C and f_{SC} are the inductance and the switching frequency of the conventional ACF converter, respectively. Considering the same switching frequency and the aforementioned transformer design leads to

$$\Delta v_{OC} = \frac{\left(1 - 2M\frac{n_1}{n_2}\right) MV_I}{8L_C C_O f_S^2}, \tag{33}$$

Fig. 6 shows a comparison between the output voltage ripple of a conventional ACF converter and a SC-ACF converter in scenario 0. As can be seen, the SC-ACF converter achieves a remarkable reduction of the output voltage ripple.

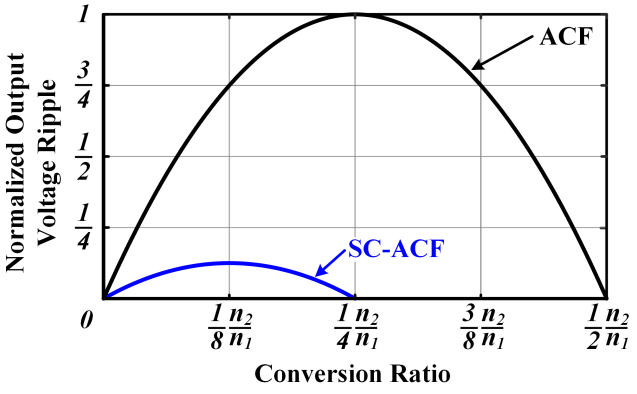

FIGURE 6. Comparison between the output voltage ripple of a conventional ACF converter and a SC-ACF converter in scenario 0. Note that the conversion ratio is expressed as a function of the turns ratio of the SC-ACF converter transformer. The normalization is done dividing the output voltage ripple by the maximum of the conventional ACF converter.

B. COMPARISON CONSIDERING THE SAME OUTPUT VOLTAGE RIPPLE: SCENARIOS I, II AND III

In order to meet a particular output voltage ripple specification, the lower output voltage ripple achieved by the SC-ACF converter can be translated into lowering the energy stored by inductors and/or reducing the switching frequency. Lowering the energy stored by inductors leads to reducing the size of the SC-ACF converter. Reducing the switching frequency leads to higher efficiency because the switching losses of the switches and core losses of magnetics fall. This translation is explored in this section by evaluating three scenarios.

In scenario I, the two inductances of the SC-ACF converter are equal to that of the conventional ACF converter. Hence, the inductance considered for the SC-ACF converter in scenario I is

$$L_I = L_C. \tag{34}$$

The volume occupied by an inductor is proportional to the amount of energy that it is able to store. In the case of the SC-ACF converter, the total volume of the output-filter inductors is proportional to the total stored energy, which can be estimated neglecting the current ripple

$$E_L = E_{L1} + E_{L2} \cong 2\left[\frac{1}{2}L\left(\frac{I_O}{2}\right)^2\right] = \frac{LI_O^2}{4}, \tag{35}$$

where E_{L1} and E_{L2} denote the energy stored by each inductor. In the case of a conventional ACF converter, the total energy stored by its inductor neglecting the current ripple is

$$E_{LC} \cong \frac{L_C I_O^2}{2}. \tag{36}$$

Considering (34)-(36), the total energy stored by the inductors of the SC-ACF converter in scenario I as a function of that of the conventional ACF converter is

$$E_{L-I} = \frac{E_{LC}}{2}. \tag{37}$$

In this scenario, the switching frequency of the SC-ACF converter required to meet an output voltage ripple specification is lower than in the case of the conventional ACF converter and can be expressed as

$$f_{S-I} = \sqrt{\frac{\left(1 - 4M\frac{n_1}{n_2}\right)}{\left(1 - 2M\frac{n_1}{n_2}\right)}}\frac{f_{SC}}{\sqrt{2}}. \tag{38}$$

In Scenario II, both converters have the same open-loop bandwidth. Hence, the inductance considered for the SC-ACF converter in scenario II is:

$$L_{II} = 2L_C. \tag{39}$$

In this case, the total energy stored by the inductors of the SC-ACF converter is

$$E_{L-II} = E_{LC}. \tag{40}$$

Regarding the switching frequency, it is lower than in scenario I

$$f_{S-II} = \sqrt{\frac{\left(1-4M\frac{n_1}{n_2}\right)}{\left(1-2M\frac{n_1}{n_2}\right)}}\frac{f_{SC}}{2}. \tag{41}$$

In Scenario III, both converters operate with the same switching frequency and, consequently, the switching frequency is

$$f_{S-III} = f_{SC}. \tag{42}$$

In this scenario, the output voltage ripple specification is met by reducing the inductances values. In particular, the inductance required by the SC-ACF converter to meet an output voltage ripple specification can be expressed as

$$L_{III} = \frac{\left(1-4M\frac{n_1}{n_2}\right)}{\left(1-2M\frac{n_1}{n_2}\right)}\frac{L_C}{2}. \tag{43}$$

Substituting (43) into (35) and considering (36) leads to:

$$E_{L-III} = \frac{\left(1-4M\frac{n_1}{n_2}\right)}{\left(1-2M\frac{n_1}{n_2}\right)}\frac{E_{LC}}{4}. \tag{44}$$

Fig. 7 shows the improvements achieved by the SC-ACF converter in comparison to the conventional ACF converter in terms of reduction of total energy stored by inductors and reduction of switching frequency for the three scenarios. In scenario I, the total energy stored by inductors is half that of a conventional ACF converter. The switching frequency is lower for the entire conversion range and the improvement rises with the conversion ratio. In scenario II, there is no improvement in terms of inductors size. However, the reduction of the switching frequency is more noticeable than in the case of scenario I. In scenario III, the lower output voltage ripple achieved by the SC-ACF converter is translated completely into lowering the energy stored by inductors and, as can be seen, the improvement rises with the conversion ratio.

C. REDUCTION OF THE OUTPUT VOLTAGE RIPPLE WITH THE EXTENDED VERSION OF THE SC-ACF CONVERTER

As Fig. 8 shows, the SC-ACF converter can be extended by considering N phases in the secondary side of the topology. In this case, the voltage conversion ratio is:

$$M = \frac{V_O}{V_I} = \frac{d}{N}\frac{n_2}{n_1}, \tag{45}$$

Considering that d ranges between 0 and $1/N$, the conversion range is:

$$M \in \left(0, \frac{1}{N^2}\frac{n_2}{n_1}\right). \tag{46}$$

The voltage across the k^{th} series-capacitor is:

$$V_{Ck} = \frac{N-k}{N}\frac{n_2}{n_1}V_I. \tag{47}$$

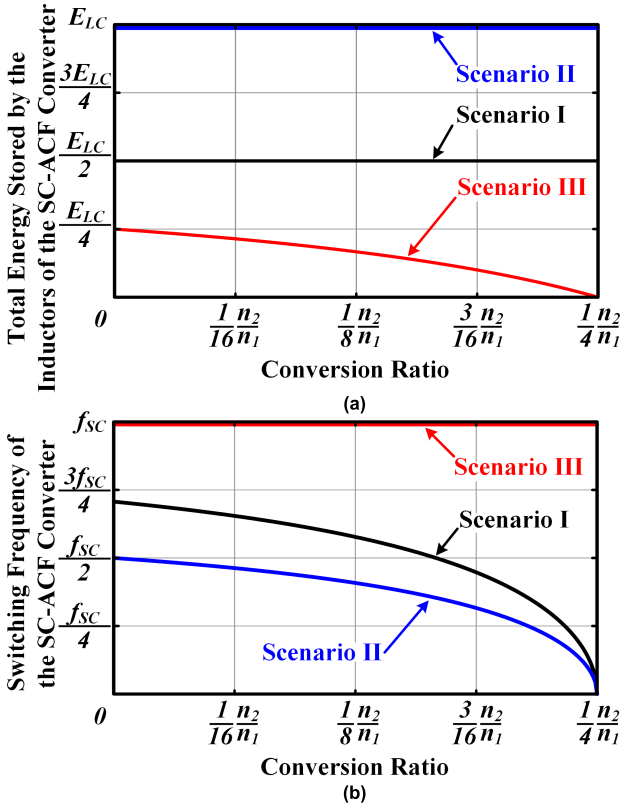

FIGURE 7. Evaluation of the improvements of the SC-ACF converter with respect to a conventional ACF converter considering the same output voltage ripple: a) Total energy stored by inductors. b) Switching frequency. Note that the conversion ratio is expressed as a function of the turns ratio of the SC-ACF converter transformer.

The ripple of the current that flows through the k^{th} inductance L_k is:

$$\Delta i_{Lk} = \frac{\left(1-NM\frac{n_1}{n_2}\right)MV_I}{L_k f_S}. \tag{48}$$

The current that flows through the output capacitance is the AC component of the sum of all inductors currents. Considering $L_1 = L_2 = \ldots = L_N = L$, the ripple of i_{CO} is:

$$\Delta i_{CO} = \frac{\left(1-N^2M\frac{n_1}{n_2}\right)MV_I}{Lf_S}. \tag{49}$$

The output voltage ripple can be calculated considering the charge stored and delivered by C_O during a switching period and taking into account that the frequency of i_{CO} is Nf_S:

$$\Delta v_O = \frac{\left(1-N^2M\frac{n_1}{n_2}\right)MV_I}{8NLC_O f_S^2}. \tag{50}$$

In this way, the extended version of the SC-ACF converter further decreases the output voltage ripple by reducing the ripple of the current that flows through the inductors [see equation (48)], by lowering Δi_{CO} due to the $360°/N$ phase-shift between the phase currents and by increasing the effective switching frequency to Nf_S.

Fig. 9 shows a comparison between the output voltage ripple of a conventional ACF converter and a SC-ACF converter for different N values. As in previous analysis, the comparison considers magnetic designs that are similar in terms of size and losses (i.e., $n_{1C} = n_1$, $n_{2C} = n_2/N$ and $L = NL_C$). Following the reasoning of Section III-B, the improvement in terms of output voltage ripple could be translated into lower inductors size and/or lower switching frequency when a particular output voltage ripple specification must be met.

IV. EXPERIMENTAL SECTION

A. SPECIFICATIONS AND DESIGN GUIDELINES

The SC-ACF converter is a good candidate for applications where a high dc-dc step-down conversion and isolation are mandatory, such as electrical vehicles, renewable energy systems, telecom systems and datacenters. Each application has its own electrical specifications in terms of nominal input voltage, expected input voltage range, maximum output current, bandwidth, etc. Until this section, the SC-ACF converter has been studied in a general way, avoiding particularizations that may restrict the applicability of the carried out analysis. However, setting electrical specifications is mandatory for this experimental section. A SC-ACF converter prototype for a 48V power delivery architecture was implemented (see Fig. 10). This kind of architecture can be found in electric vehicles [44], telecom and datacenters [45], where the implemented prototype could be used as a Point-of-Load (PoL) converter that provides isolation or to generate an isolated and regulated intermediate bus that supplies several PoLs. The implemented prototype has an input voltage of 48V and is able to provide an output voltage between 1.8V and 5V. The maximum output current and the switching frequency of the prototype are 20A (leading to a peak output power of 100W when the output voltage is 5V) and 200kHz, respectively.

At the beginning of the design, the number of phases must be set. As explained in Section III-C, the higher the number of phases, the higher the conversion performed with switched-capacitors and, consequently, lower output voltages could be addressed. However, it also jeopardizes the regulation capability due to the restricted d range [see equation (47)], and increases the design complexity. For the sake of simplicity, the prototype was implemented with $N = 2$. The next step is the transformer selection. Taking into account that d can be adjusted between 0 and 0.5, and considering (5), n_2/n_1 should lead to a nominal d value close to 0.25 in order to maximize the regulation capability (other design approaches could be explored for scenarios with narrow input voltage range). The full or partial ZVS turn-on of S_{1A} can be achieved by reducing the magnetizing inductance. However, as explained in Section III and in the appendix section, reducing the magnetizing inductance leads to higher conduction losses of the primary side. Taking into account that satisfying the ZVS condition for S_{1A} becomes more challenging as the output current rises, trying to ensure full ZVS for high load conditions is not recommended. Another important point is that special attention must be paid for the secondary side winding, which must exhibit low resistance due to the high current it has to drive. Regarding the output inductors, they are selected to ensure a given current ripple specification (typically around 20% of the average current). As indicated in Section III-A, high current ripple would be necessary to achieve ZVS in S_{2A}. However, that design approach is not recommended due the high current levels that flow through the secondary-side of the converter. Moreover, minimizing the Equivalent Series Resistance (ESR) of both inductors is mandatory taking into account the high output current specification. After that, the output capacitor can be selected to meet the output voltage ripple

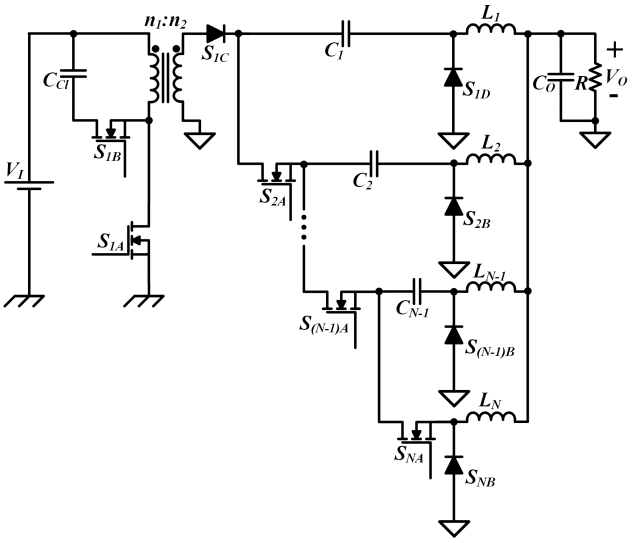

FIGURE 8. Extended version of the SC-ACF converter considering a higher number of phases.

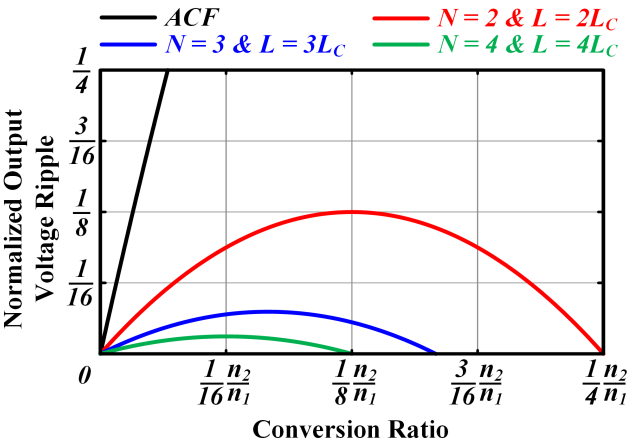

FIGURE 9. Comparison between the output voltage ripple of a conventional ACF converter and the N-phase SC-ACF converter considering the same switching frequency and magnetics with similar size and losses. Note that the conversion ratio is expressed as a function of the turns ratio of the SC-ACF converter transformer when N = 2. The normalization is done dividing the output voltage ripple by the maximum of the conventional ACF converter.

requirement. Equation (22) can be used to select the series-capacitor. In this case, a low ESR is also recommendable due to the high current it drives. Regarding the transistors selection, it is well known that transistors have a tradeoff between switching and conduction losses: in general, fast transistors exhibit higher on-resistance than those optimized for driving high current. Therefore, the transistors selection should be addressed taking into account their voltage and current stresses, and if they act as a switch or as a synchronous rectifier. Since S_{1A} and S_{1B} act as switches that drive low current, fast devices are preferably. Low on-resistance is mandatory for the transistors of the secondary side due to the high current they have to drive. This is especially critical for S_{1D} and S_{2B}, which will be ON during a longer time since the nominal value of d is around 0.25. Regarding the layout, it is mandatory not only to minimize the loops involving switches (in order to minimize the undesired ringing effects due to parasitic inductances), but also all paths of the secondary side due the high conduction losses that could appear due to the high output current specification. Table 3 lists the components and parameters of the experimental prototype, which operates in open loop. D10-Lite board, which includes the Altera MAX 10 Field Programmable Gate Array (FPGA), was used for generating the control signals. As Table 3 indicates, synchronous rectification is used in the prototype. Another important point is that commercial magnetics were selected, thus minimizing the complexity and facilitating the comparison with the prototype of a conventional ACF converter that is detailed in Section IV-D.

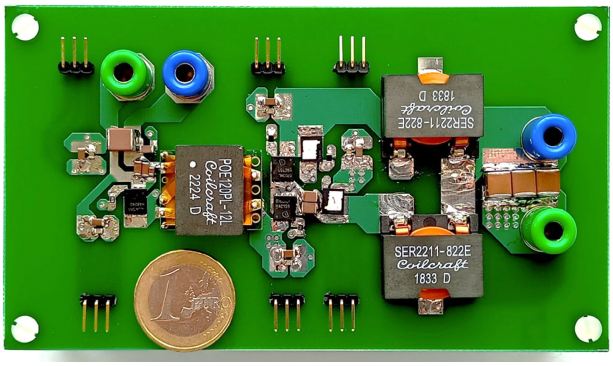

FIGURE 10. Prototype of the SC-ACF converter.

B. MAIN VOLTAGE AND CURRENT WAVEFORMS

Fig. 11 shows the main voltage waveforms for an output voltage of 5V [Fig. 11(a) and (b)] and 2.5V [Fig. 11(c) and (d)]. In particular, the figure shows the signal that drives S_{1A}, the drain-to-source voltage of S_{1A} (i.e., v_{S1A}) and the voltages at the switching nodes of the secondary side (i.e., the drain-to-source voltages of S_{1D} and S_{2B}: v_{S1D} and v_{S2B}, respectively). As can be observed, both S_{1D} and S_{2B} block $(n_2/n_1)(V_I/2)$, which indicates that the series-capacitor voltage is balanced naturally. Moreover, since the active-clamp mechanism recycles the energy stored in the leakage inductor, the overvoltage during the turn-off of S_{1A} is suppressed.

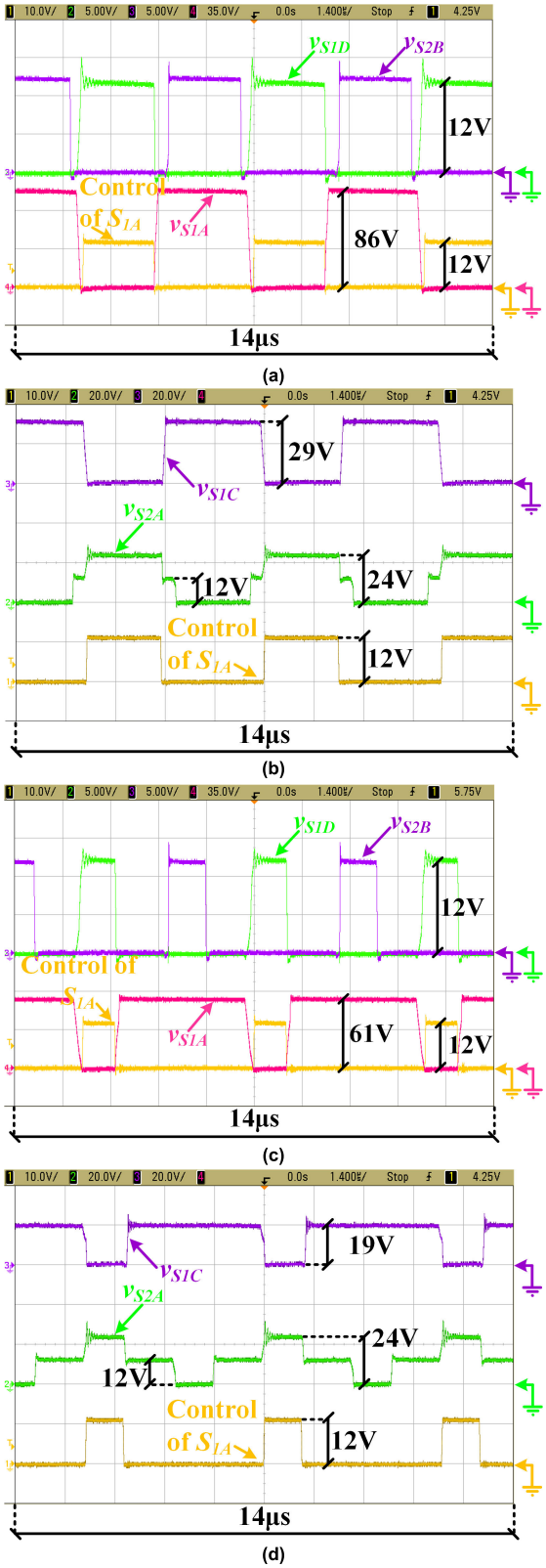

FIGURE 11. Main experimental voltage waveforms: a) $V_O = 5$V (part 1). b) $V_O = 5$V (part 2). c) $V_O = 2.5$V (part 1). d) $V_O = 2.5$V (part 2).

TABLE 3. Prototype components.

Component	Value
Transformer	POE120PL-12L (n_2/n_1 = 1/2, L_M = 50µH, primary/secondary resistance = 18.9mΩ / 6.8mΩ, size = 23.37·20.38·8.94mm^3)
L_1, L_2	SER2211-822MED (8.2µH, resistance = 2.3mΩ, size = 22.5·19.2·10.5 mm^3)
C_1	40µF
C_{C1}	1µF
C_O	300µF
S_{1A}, S_{1B}	BSC160N15NS5 (150V, $R_{DS\text{-}ON,\,max}$ = 16mΩ, Q_G = 19nC)
S_{1C}, S_{2A}	ISC0703NLS (60V, $R_{DS\text{-}ON,\,max}$ = 6.9mΩ, Q_G = 8.7nC)
S_{1D}, S_{2B}	BSC028N06NS (60V, $R_{DS\text{-}ON,\,max}$ = 2.8mΩ, Q_G = 37nC)
Driver	EL7104CSZ

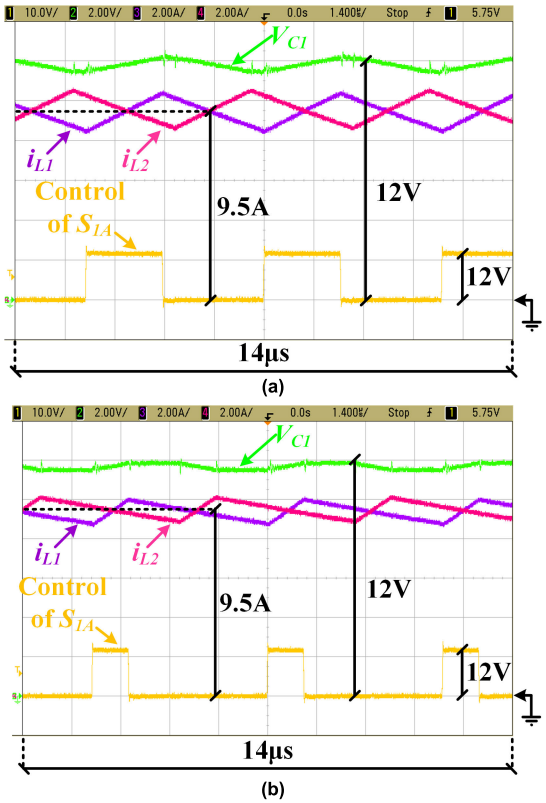

FIGURE 12. Main experimental current waveforms: a) V_O = 5V. b) V_O = 2.5V.

Fig. 12 shows the phase currents (i.e., i_{L1} and i_{L2}), the voltage across the series-capacitor (i.e., V_{C1}) and the signal that drives S_{1A} for an output voltage of 5V [Fig. 12(a)] and 2.5V [Fig. 12(b)] when the output current is 19A. As can be seen, each phase drives half the output current and, therefore, natural current sharing between the phases is achieved. As previously concluded from Fig. 11, the series-capacitor voltage is balanced naturally to $(n_2/n_1)(V_I/2)$. It can be seen [more easily in Fig. 12(b)] that V_{C1} slightly rises during the magnetizing stage of L_1 and it slightly falls during the magnetizing stage of L_2.

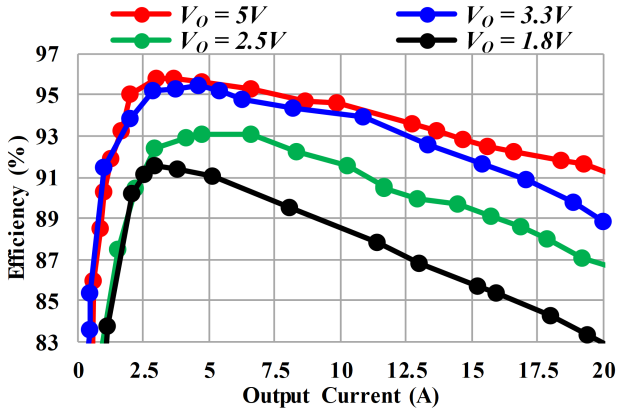

FIGURE 13. Experimental efficiency measurements of the SC-ACF converter for different output voltages.

C. EFFICIENCY

The prototype efficiency was measured for different output voltages. As Fig. 13 shows, the best efficiency is obtained when the output voltage is 5V. In this scenario, the peak efficiency is 95.8% and the efficiency at full load is 91.1%. Reducing the output voltage for a given output current value leads to lower output power. At the same time, secondary side conduction losses, which are predominant in high step-down isolated dc-dc converters, do not suffer a fall as significant as in the case of the output power because they strongly depend on the output current. As a consequence, the efficiency falls significantly as the output voltage is reduced, which is a typical result of low output voltage and high output current converters. Fig. 14 compares the experimental efficiency and the efficiency estimation based on the model of Section III for two output voltage levels.

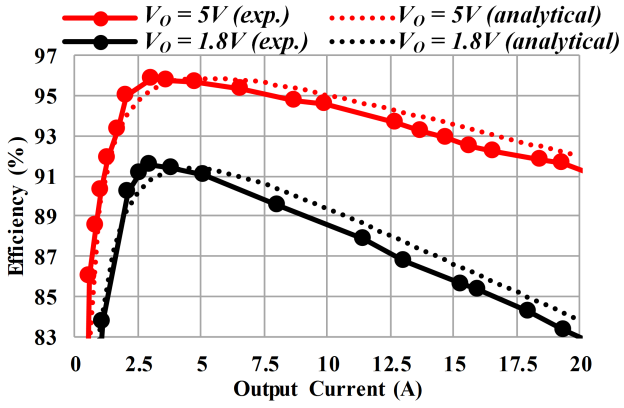

FIGURE 14. Comparison between the experimental efficiency and the efficiency estimated by the analytical model when V_O = 5V and V_O = 1.8V.

Fig. 15 shows an estimation of the losses distributed in the components of the experimental prototype when the output current is 20A. The figure shows the estimation when the

output voltage is 5V [see Fig. 15(a)] and 1.8V [see Fig. 15(b)]. The analysis is based on analytical models [46], [47], the LTspice models provided by the manufacturers, and the online tools they offer to estimate power losses, such as Power Inductor Finder and Analyzer of Coilcraft. As can be seen, conduction losses on the secondary side of the converter are predominant.

D. COMPARISON WITH A CONVENTIONAL ACF CONVERTER

A prototype of a conventional ACF converter was built to compare the efficiencies. In order to perform a comparison as fair as possible, this prototype has the same components of the SC-ACF converter (i.e., same transformer, clamp capacitor, output capacitor, MOSFETs and drivers) and the inductance was built by parallelizing the two inductors of the SC-ACF converter. In this way, the ACF converter prototype has the same open-loop bandwidth (i.e., $L_C = L/2$) and it is similar in terms of volume because the total size of its inductor is equal to the total volume occupied by the two inductors of the SC-ACF converter prototype. Under these conditions, the switching frequency of the conventional ACF converter must be increased in order to achieve the same output voltage ripple. In particular, the required switching frequency can be calculated equaling (18) and (32) taking in account that, in this case, both converters have the same transformer (i.e., $n_{1C} = n_1 = 2, n_{2C} = n_2 = 1$)

$$f_{SC} = \sqrt{\frac{(1-2M)}{(1-8M)}}2f_S. \tag{51}$$

In this way, the switching frequency was set to 459.8kHz, 495.7kHz, 553.8kHz and 871.7kHz when the output voltage was 1.8V, 2.5V, 3.3V and 5V, respectively. As Fig. 16 shows, the SC-ACF converter achieves a remarkable improvement with respect to the conventional ACF converter when they are compared considering the same output voltage level, the same output voltage ripple and similar size. In particular, the efficiency improvement ranges between 7 and 8 points.

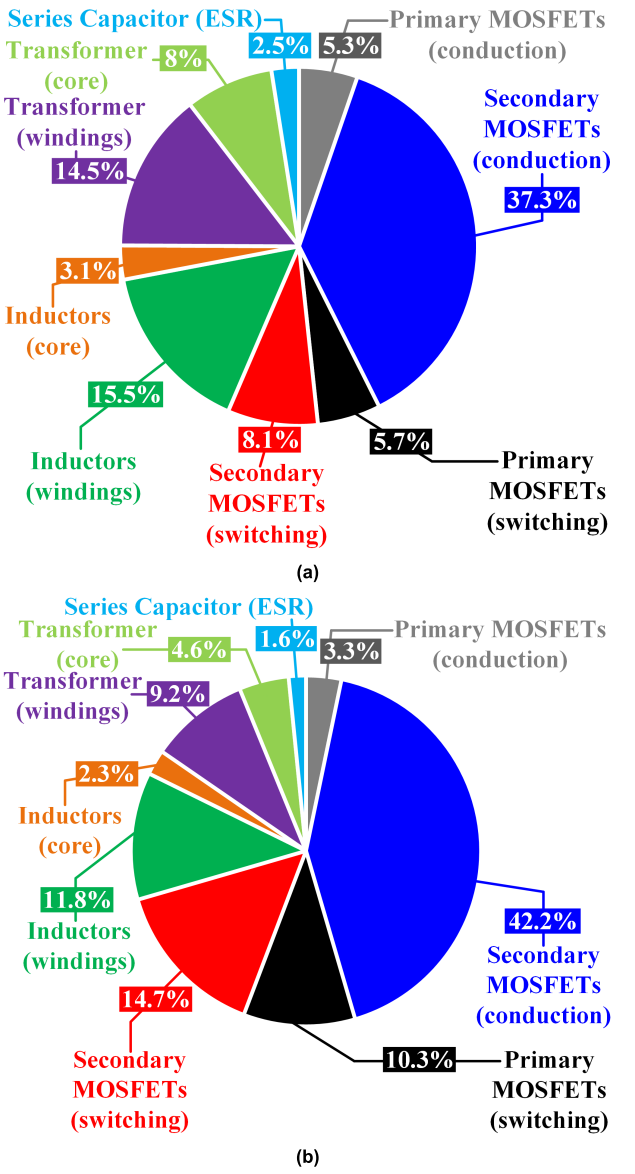

FIGURE 15. Power-loss breakdown of the SC-ACF converter when the output current is 20A: a) $V_O = 5$V. b) $V_O = 1.8$V.

E. COMPARISON TO PREVIOUS WORKS

Table 4 compares from a technical point view the SC-ACF converter with prior works. In order to choose the best dc-dc converter for a given application, aspects that are not typically addressed by technical papers, such as cost, implementation complexity or reliability, should be also considered. Another important point is that for high step-down converters, small changes of output voltage or current lead to remarkable differences in terms of performance. Hence, it is not straightforward to compare prototypes that were designed with different specifications (output voltage ripple, output voltage, output power, etc.) and technology (which directly affects the cost). As an example, if two converters achieve different output voltage ripple, their efficiency and power density cannot be directly compared. Note that, as explained in Section III, the converter that naturally achieves lower output voltage ripple could translate that benefit into higher efficiency (by reducing the switching frequency) and/or higher power density (by reducing the energy stored by inductors). Similarly, if a given prototype is implemented with Gallium Nitride (GaN) switches instead of Silicon (Si) MOSFETs, it would be able to operate at higher switching frequencies. As a result, it could increase the power density by reducing the size of passive components. Hence, comparing different topologies whose prototypes are implemented with different technology is not straightforward because part of the benefits in terms of efficiency or power density could be provided by the technology used for the implementation rather than the topologies. As a conclusion, some aspects of Table 4, such as the component count or the capability to naturally balance the phase currents, can

TABLE 4. Comparison with isolated PWM DC-DC converters with similar voltage specifications.

Ref.	Voltage gain	L_{Leak} impact[*1]	Phase-current balance	V_I (V)	V_O (V)	$I_{O\text{-}Max}$ (A)[*2]	$P_{O\text{-}Max}$ (W)	f_S (kHz)	η (%) Peak	η (%) Full load	Switches[*3] #	Switches[*3] Type	Magnetics Inductors	Magnetics Transformer	Magnetics Type	Capacitors	Power density (W/inch^3)	$\frac{\Delta v_O^{*4}}{V_O}$
[10] Sigma[*5]	-	No	-	48	1	80	80	600/ 1000	93.4	91.6	14	GaN + Si	2	4×10:1	Custom made	4	420	-
[48] HB+CD	$\frac{d}{2}\frac{n_2}{n_1}$	Yes	Active control	36 - 60	1	40	40	400 - 1000	92.9[*6]	89.9[*6]	4	GaN	2	6:1	Custom made[*7]	3	50.6	$5\cdot10^{-4}$ - $1\cdot10^{-4}$
[27] 3-Level HB+CD	$\frac{d}{4}\frac{n_2}{n_1}$	Yes	Active control	48 - 60	0.5 - 1	60	60	333	92.8	85	6[*8]	Si	2	4:1	Custom made	4	-	$15\cdot10^{-4}$
[28] Stacked HB+CD	$\frac{d}{4}\frac{n_2}{n_1}$	Yes	Natural	36 - 60	0.8 - 1.2	45	54	500	92.7	-	6	GaN + Si	2	2:1	Custom made[*7]	6	310	$7\cdot10^{-4}$ - $9\cdot10^{-4}$
[This work] SC-ACF	$\frac{d}{2}\frac{n_2}{n_1}$	No	Natural	48	1.8 - 5	20	100	200	91.6 - 95.8	83.3 - 91.1	6	Si	2	2:1	Commercial	3	123[*9]	$4\cdot10^{-4}$ - $1\cdot10^{-4}$

[*1] It evaluates if the leakage inductance of the transformer causes voltage ringing on the primary side switches and duty cycle loss.
[*2] Maximum output current.
[*3] It also includes synchronous-rectifier switches.
[*4] Output voltage ripple over output voltage: value estimated from the steady-state analysis of each converter neglecting the voltage ripple of the switched-capacitors.
[*5] Although this converter includes a transformer, it does not provide isolation due to the buck converter used to regulate the output voltage.
[*6] At $V_I = 48$V and $f_S = 600$kHz.
[*7] Custom made transformer and commercial inductors.
[*8] There are 8 switches considering the ringing suppression circuit.
[*9] Estimation based on magnetics size and evaluated for $V_O = 5$V.

be compared because they only depend on the topology. However, some of the aspects evaluated in Table 4, such as the efficiency or the power density, cannot be directly compared because each prototype has its own specifications and uses different technologies (i.e., GaN or Si switches, custom made or commercial magnetics, etc.).

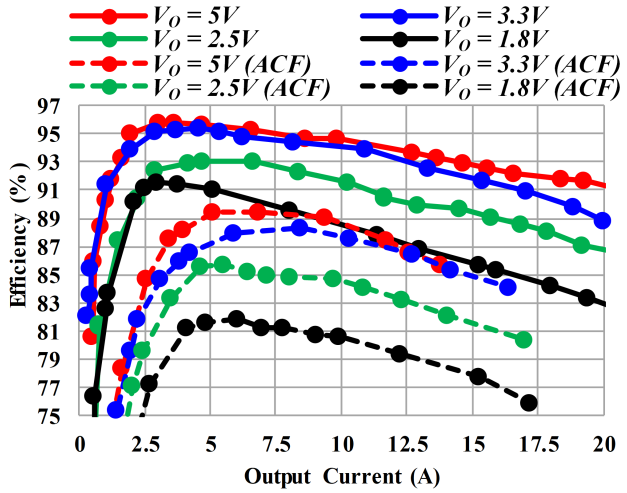

FIGURE 16. Experimental comparison of the efficiency of the SC-ACF converter and a conventional ACF converter with the same output voltage ripple and similar size.

The sigma converter proposed in [10] achieves outstanding results in terms of both efficiency and power density. Its drawback is the complexity: very complex transformer (which is actually made up of four 10:1 transformers that must be carefully designed), high number of switches, GaN technology, etc. Moreover, the converter does not provide isolation due to the buck converter used to regulate the output voltage. The HB dc-dc converter with CD rectifier is another interesting approach for implementing a high step-down isolated dc-dc converter. It was explored in [48] (conventional version), in [27] (version with a flying capacitor on the primary side) and in [28] (version based on stacking HB dc-dc converters). The 3-level HB dc-dc converter with CD rectifier of [27] outperforms the conventional version of [48] in terms of voltage gain at the expense of increasing the number of switches and capacitors. A drawback of both converters is that that active control is mandatory to balance the current of the two phases [27], [47]. The stacked HB dc-dc converter with CD rectifier of [28] solves that problem by increasing the number of capacitors. The converters of [27], [28], and [48] have another drawback: the leakage inductance of the transformer causes parasitic oscillations on the drain-to-source voltage of the primary side switches and duty cycle loss. In order to overcome this problem, interleaved winding structure is recommended for designing the transformer [28]. This well-known technique reduces the leakage inductance at the expense of increasing the transformer complexity and its cost. Alternately, a ringing suppression circuit can be used [27]. However, this approach requires two extra switches.

The prototype implemented for testing the SC-ACF converter was designed pursuing low complexity and a fair comparison with a conventional ACF converter prototype. Therefore, reaching the high power density results achieved by [10] and [28] is out of the scope of the work. As previously

explained, the SC-ACF converter naturally balances the current through the inductors, thus preventing the use of additional control circuitry. In comparison to [28], the active-clamp mechanism allows the SC-ACF converter to avoid any problem derived from the leakage inductance. In this way, it does not suffer parasitic oscillations on the drain-to-source voltage of the primary side switches or duty cycle loss (it can be clearly seen in Fig. 11). The voltage gain of the stacked HB dc-dc converter with CD rectifier of [28] is higher than the one of the SC-ACF converter. However, the number of capacitors of the SC-ACF converter is half that of the stacked HB dc-dc converter with CD rectifier. The efficiency and the power density achieved by the approach of [28] is higher than in the case of the SC-ACF converter. However, $\Delta v_O/V_O$ (i.e., the output voltage ripple over the output voltage) is lower in the case of the implemented SC-ACF converter prototype, thus indicating that the SC-ACF converter would be able to increase the efficiency and/or the power density if it were designed for fulfilling an output voltage ripple requirement similar to that of [28]. Furthermore, GaN switches and a custom-made transformer with interleaved windings are used in the prototype of [28], while the SC-ACF converter prototype uses Si MOSFETs and a commercial transformer. As previously explained, GaN switches would allow us to increase the switching frequency and, consequently, the power density at the expense of increasing cost. Similarly, a custom-made transformer with interleaved windings, such as to one of [28], could be used to increase both efficiency and power density. Unfortunately, that would also lead to higher cost and complexity. In summary, no strong conclusions about the efficiency and the power density of the SC-ACF converter and the one of [28] can be provided by analyzing Table 4. The specifications are different and, moreover, the technologies used for the implementation of the prototypes are not comparable.

V. CONCLUSION

In conventional high step-down isolated dc-dc converters, the transformer is the main responsible of the voltage conversion. However, high step-down transformers highly jeopardize both the power density and the efficiency of the converter. In applications that require isolation, the use of a transformer is mandatory. Fortunately, its penalization can be lowered by incorporating SC structures to aid it in the step-down conversion. In this paper, a PWM dc-dc converter based on combining a forward converter with a series-capacitor structure is proposed for applications that require a very high step-down conversion ratio, low output voltage ripple, high output current and isolation. In contrast to previous topologies that include a series-capacitor, the proposed combination does not need two complete phases: it only adds one series-capacitor, one inductor, one switch and one diode (or synchronous rectifier switch) to the component count of a conventional forward converter. In comparison to other conventional isolated dc-dc converter, the SC-ACF converter increases the step-down conversion ratio and reduces the output voltage ripple at the expense of a higher complexity in terms of hardware and control due to the higher component count. The lower output voltage ripple can be used to decrease the total energy stored by inductors and/or to reduce the switching frequency in order to increase the power density and the efficiency, respectively. In addition, the converter provides inherent current sharing between the two phase, natural balance of the voltage across the series-capacitor and lower conduction losses. These properties make the series-capacitor forward converter a suitable topology for applications where a high step-down conversion ratio, isolation and high output current are mandatory.

The experimental results validated the theoretical analysis with a 100W and 48V-to-5/3.3/2.5/1.8V prototype that achieves a peak efficiency of 95.8% and a full load efficiency of 91.1%. Moreover, a remarkable improvement in terms of efficiency has been reported when it was compared to a conventional forward converter with the same output voltage ripple and similar size.

APPENDIX
ZVS MECHANISM OF THE PRIMARY SIDE

In this section, an intuitive explanation of the mechanism for achieving ZVS on the primary side of the SC-ACF converter is provided. Moreover, the condition to be satisfied in order to ensure the full ZVS operation of S_{1A} is also detailed. The analysis that follows is derived from previous works focused on a conventional ACF converter [38], [39], [40]. For the sake of simplicity, it is considered that the current ripple of the output inductors is negligible (i.e., each inductor drives half the output current), that the ZVS mechanism is only based on the use of the energy stored by the magnetizing inductance, and that S_{1C} and S_{1D} switch instantaneously. These assumptions facilitate the explanation, but will lead to a more restrictive ZVS condition. For instance, the energy stored by the leakage inductance could also be used to facilitate the ZVS operation (further details can be found in [40]).

The ZVS mechanism of S_{1B} begins at the end of state I (i.e., just before $t = dT_S$), when S_{1A} is driving the magnetizing current ($i_{LM} > 0$, close to its maximum value as Fig. 4 shows) and the reflected current from L_1 [i.e., $(n_2/n_1)(I_O/2)$, see Fig. 17(a)]. At $t = dT_S$ [see Fig. 17 (b)], S_{1A} is turned-off and both the magnetizing current and the reflected current from L_1 charge the output capacitance of S_{1A} (C_{1A}) and discharge the output capacitance of S_{1B} (C_{1B}). When the voltage across C_{1A} equals V_I, the voltage across the primary winding of the transformer reaches 0, thus reverse biasing S_{1C}, which stops driving the current of L_1. In this way, the charge and discharge of C_{1A} and C_{1B} continue, but now they only involve the magnetizing current [see Fig. 17(c)]. Finally, when the voltage across C_{1B} equals 0, the body-diode of S_{1B} is forward biased [see Fig. 17(d)], thus enabling the turn-on of the MOSFET with ZVS.

Regarding the ZVS mechanism of S_{1A}, it begins at the end of state IV (i.e., just before $t = T_S$), when, as Fig. 18(a) shows,

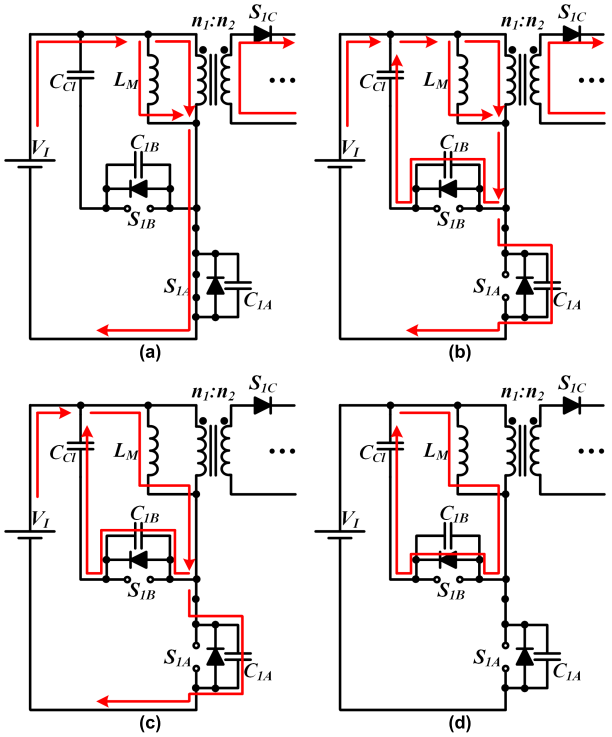

FIGURE 17. Equivalent circuits for analyzing the ZVS mechanism of S_{1B}: a) Initial state. b) Charge of C_{1A} from 0 to V_I. c) Charge of C_{1A} from V_I to $V_I/(1\text{-}d)$. d) Final state.

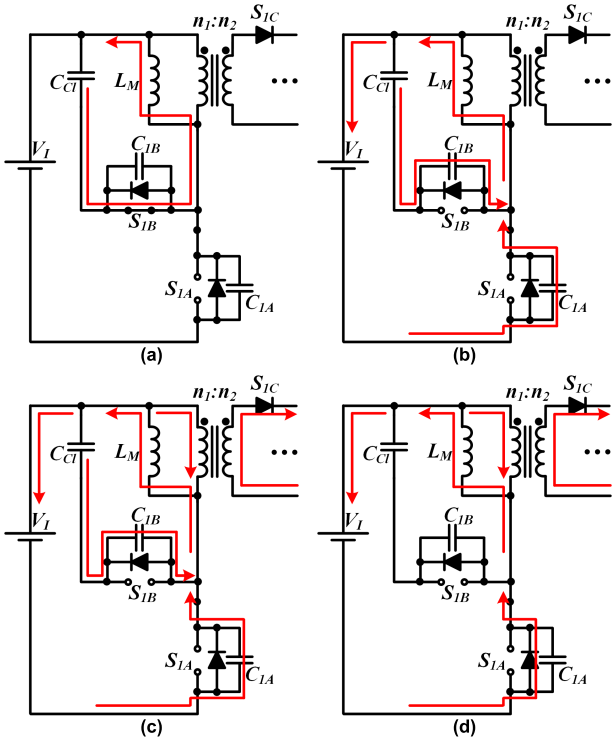

FIGURE 18. Equivalent circuits for analyzing the ZVS mechanism of S_{1A}: a) Initial state. b) Discharge of C_{1A} from $V_I/(1\text{-}d)$ to V_I. c) Discharge of C_{1A} from V_I to 0. d) Final state.

S_{1B} is driving the magnetizing current ($i_{LM} < 0$, close to its minimum value as Fig. 4 shows). At $t = T_S$ [see Fig. 18(b)],

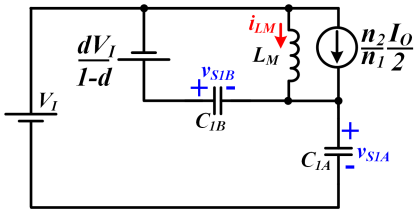

FIGURE 19. Equivalent circuit when the energy stored by the magnetizing inductance discharges C_{1A} from V_I to 0 despite the reflected current from L_1.

S_{1B} is turned-off and, consequently, the magnetizing current charges C_{1B} and discharges C_{1A}. When the voltage across C_{1A} equals V_I, the voltage across the primary winding of the transformer reaches 0, thus forward biasing S_{1C}, which begins to drive the current of L_1. In this way, the charge and discharge of C_{1B} and C_{1A} continue, but now it involves both the reflected current from L_1 and the magnetizing current [see Fig. 18(c)]. Note that, in this case, the reflected current from L_1 hinders the ZVS operation. Finally, when the voltage across C_{1A} equals 0, the body-diode of S_{1A} is forward biased [see Fig. 18(d)], thus enabling the turn-on of the MOSFET with ZVS. Obviously, if the energy stored by the magnetizing inductance is not high enough, the voltage across C_{1A} will not reach 0 and, consequently, partial ZVS instead of full ZVS will be achieved. Fig. 19 shows the equivalent circuit used to obtain the full ZVS condition for S_{1A}. It represents the state when the voltage across C_{1A} has just reached V_I and the energy stored by the magnetizing inductance tries to continue discharging the capacitance despite the reflected current from L_1. In that circuit, the initial current through the magnetizing inductance is

$$I_{LM\_0} = -\frac{dV_I}{2f_S L_M}. \tag{52}$$

The initial voltage across the C_{1A} and C_{1B} are

$$V_{C1A\_0} = V_I. \tag{53}$$

$$V_{C1B\_0} = \frac{dV_I}{1-d}. \tag{54}$$

Solving that circuit allows us to obtain the full ZVS condition for S_{1A}

$$\sqrt{\frac{L_M}{C_{1A}+C_{1B}}}\left(\frac{dV_I}{2f_S L_M} - \frac{n_2}{n_1}\frac{I_O}{2}\right) \geq V_I. \tag{55}$$

Ensuring full ZVS for S_{1A} becomes more difficult as the output load rises. In practice, as previously indicated, aspects that are not considered in this simplified explanation, such as the leakage inductance and the non-instantaneous turn-off of S_{1D}, facilitates the ZVS operation of S_{1A} [38], [39], [40].

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