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RESEARCH ARTICLE

Broadband Monolithic GaN Balanced Amplifier Composed of Mixed Cascade-Tandem Directional Couplers and Cascode Stages

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ABSTRACT In this paper we present a broadband monolithic balanced amplifier reaching 30 dBm output power over a range from 5.7 GHz up to 35.1 GHz. To the best of our knowledge, such broad operational bandwidth has never been reported in literature for balanced topology. The amplifier is composed of broadband tandem-cascade directional couplers and amplifying blocks designed in cascode topology. It is worth noticing that for the first time the mixed tandem-cascade couplers have been integrated in monolithic process, in which only one metallization layer is available for transmission-line structures. The broadband balanced amplifier has been fabricated in high power GH15 gallium nitride (GaN) process offered by United Monolithic Semiconductors (UMS). The measured saturation output power and 1-dB compression point are equal to 30 dBm and 27.8 dBm, respectively.

INDEX TERMS Balanced amplifier, bandwidth enhancement, broadband amplifier, broadband directional coupler, cascode amplifier, GaN amplifier.

I. INTRODUCTION

The balanced amplifier circuit (BA) is a well-known topology in microwave electronics for decades [1]. Due to its advantages, such as good input and output matching, high stability and 3-dB higher linearity compared to a single amplifier [1], [2], the topology is utilized in different applications and technologies, including monolithic ones [3], [4], [5], [6], [7], [8], [9], [10]. Moreover, the BAs are still the subject of intensive research focused on their power efficiency improvement with the use of such solutions as Load-Modulated Balanced Amplifiers (LMBA) [11], [12], [13], [14].

A classic balanced topology is composed of two amplifying blocks placed between two power distribution networks at the input (so-called splitter) and at the output (so-called combiner). These networks are commonly realized by directional couplers or power dividers with phase shifters providing quadrature signals [15], [16]. In [17] and [18] the Authors utilize branch-line couplers which feature narrow operational bandwidth, and therefore, limit the bandwidth of an amplifier. In [19], a single coupled-line section has been used to enhance operational bandwidth of an amplifier, which operates in the range of 33 GHz – 53 GHz. In this case, even though the coupler allows for achieving bandwidth up to one frequency octave, the described amplifier features bandwidth limited to $f_h/f_l = 1.6$. In [20] the Authors have shown an amplifier which is composed of a Lange directional coupler and distributed amplifiers. Although a single-section Lange coupler allows for achieving bandwidths not exceeding one frequency octave, the utilization of distributed amplifiers shown in [20] resulted in the bandwidth of the balanced amplifier equal to $f_h/f_l = 3$. To the best of our knowledge there are no other solutions of monolithic balanced amplifiers that feature wider bandwidths.

It is known that passive distribution networks have significant impact on the width of amplifiers' operational

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bandwidth, and that the widest bandwidths of such power combining/division networks can be achieved with the use of coupled-line directional couplers. Since single-section coupled-line couplers feature maximum bandwidth of one frequency octave, they are not suitable for ultra-broadband applications. To further enhance operational bandwidth, multi-section coupled-line directional couplers have been introduced [21], [22]. In such networks the required coupling of a coupled-line section exceeds the nominal coupling of the entire directional coupler, and the length of such circuits is a multiple of quarterwavelength. Although the problem of strong coupling realization can be approached in PCB technology with the use of multilayer structures, the implementation of strong coupled-line sections in monolithic technologies can be difficult and even not realizable. On the other hand, the reduction of overall size of directional couplers is also very important especially due to the inherent insertion losses. Therefore, different topologies have been proposed, focused on either electrical length minimization or the required coupling reduction. In [23] we have introduced a broadband directional coupler composed of two coupled-line sections connected by uncoupled section, which can be miniaturized in size by increasing coupling of the coupled sections. This idea has been also implemented in monolithic technology [25], where we realized the coupled sections by using a re-entrant structure. On the other hand, in [24] an ultra-broadband solution has been presented, in which directional couplers are composed of coupled-line sections having different values of couplings and electrical lengths. In comparison to classic multisection directional couplers, the considered structure requires significantly reduced couplings of coupled-line sections, which allows for realization of directional couplers with bandwidths exceeding one frequency decade. The described concept has been implemented in monolithic process [26], where a strongly coupled-line section has been designed as a three-strip coupled-line structure using two metallization layers. To the best of our knowledge, the presented in [25] and [26] implementations feature the widest bandwidths that are described for quadrature couplers designed in monolithic technologies reaching one frequency decade. However, both circuits are designed in monolithic technologies that offer two metallization layers for passive circuits' implementations. It has to be underlined that such solutions have never been realized in monolithic processes in which only one metallization layer is available for passive circuit realization.

The bandwidth of balanced amplifiers depends not only on the passive circuit parameters but also on frequency response of amplifying blocks. With this regard two topologies featuring broad frequency response can be mentioned: (i) distributed amplifiers [27], [28], [29], [30] and (ii) cascode amplifiers [31], [32]. Distributed amplifiers are the circuits which operate in broad frequency range, even from 0 Hz up to hundreds of GHz, what has been reported in [30]. However, due to the number of required transistors, the circuit complexity and power consumption can be high. On the other hand, cascode topology is characterized by narrower frequency response in comparison to the disturbed amplifiers, however it is still quite broad and the circuitry is less complex. In [33], the Authors proposed a new approach to improve gain bandwidth of triple cascode amplifier by using resistive feedback and inductive peaking method.

In this paper, we present a design of monolithic balanced amplifier operating in broad bandwidth and having relatively large saturation output power. The requirement related to the bandwidth has been fulfilled by implementing the concept of broadband mixed cascade-tandem directional couplers [34] in monolithic microstrip technology together with amplifying blocks based on cascode topology. It has to be underlined that, this type of directional coupler has been for the first time implemented in the monolithic process in which physical constraints i.e., number of metallization layers, significantly reduce coupling between coupled transmission lines. Moreover, to enhance level of the power gain, an inductive peaking method presented in [33] has been utilized. To the best of our knowledge, for the first this method has been used together with capacitance reduction technique in a cascode amplifier composed of two transistors. Both methods significantly improve frequency response of the amplifier. It is well-known that, the gallium nitride is commonly used technology for high power applications [35]. For instance, in [36] the Authors shown narrowband power amplifier composed of Lange couplers and two-stage amplifying blocks. Therefore, to achieve large output power, we designed our balanced amplifier in GH15 process offered by United Monolithic Semiconductors. However, the chosen process supports only one metallization layer (apart from sub-layer used to form air bridges), which can be used to design transmission-line based structures. The designed broadband balanced amplifier has been fabricated and measured. The results show that the designed circuit operates from 5.7 GHz up to 35.1 GHz, features 30 dBm saturation output power and 1-dB compression point equal to 27.8 dBm at 20 GHz. Moreover, the small-signal gain is not lesser than 8.1 dB in the measured operational bandwidth.

II. BROADBAND GaN AMPLIFIER DESIGN

The concept of a proposed balanced amplifier is presented in Fig. 1. The circuit is composed of two directional couplers acting as power splitter and combiner, and two identical amplifying blocks. The isolated ports of the directional couplers are terminated by matched 50 Ω resistors.

The goal of the presented design was to achieve relatively high output power and broad operational bandwidth of the resulting balanced amplifier. To achieve such a large output power the GaN GH15 process has been chosen, which is dedicated for high power applications. The process offers 150 nm HEMT transistors and it is dedicated for high power applications operating up to 40 GHz. The foundry provides Process Design Kit (PDK) which includes models of all basic

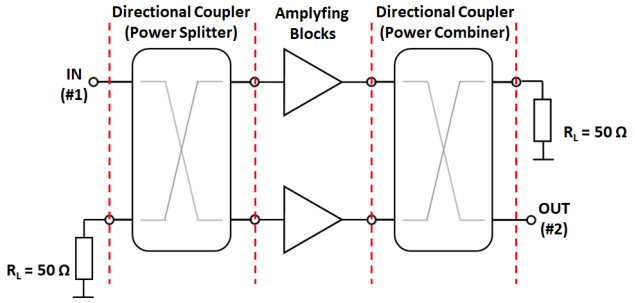


FIGURE 1. Concept of a broadband balanced amplifier composed of two amplifying blocks and microwave directional couplers.

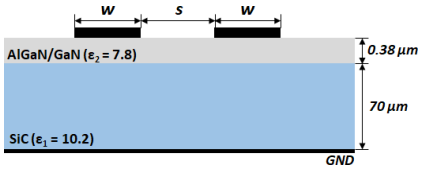


FIGURE 2. Simplified view of the UMS GH15 gallium nitride process.

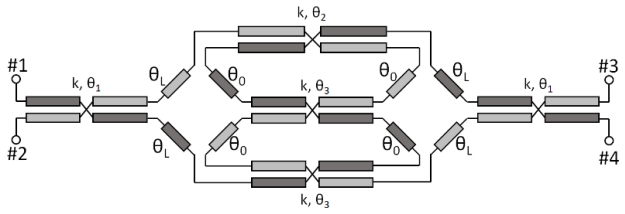


FIGURE 3. Concept of a broadband 3-dB quadrature directional coupler designed in mixed cascade-tandem-connected topology.

TABLE 1. Electrical parameters of the broadband monolithic quadrature directional coupler.

Parameter	Value
$Z_0\,(\Omega)$	50.0
k	0.595
$\theta_1\,(^\circ)$	19.3
$\Theta_2\,(^\circ)$	156.6
$\Theta_3\,(^\circ)$	23.1
$\Theta_L\,(^\circ)$	5.0

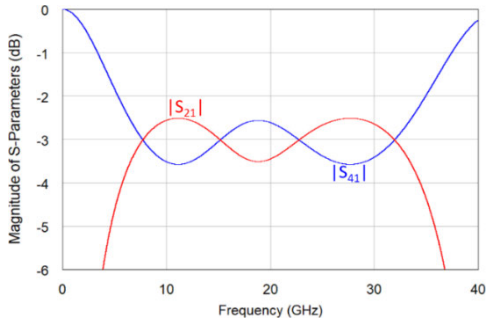


FIGURE 4. Calculated frequency response of the considered broadband directional coupler.

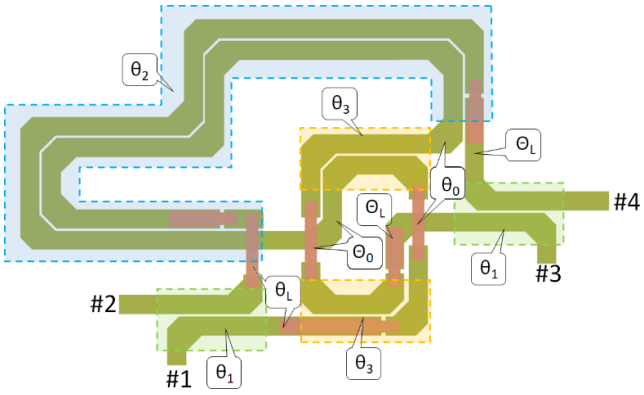


FIGURE 5. Layout of the broadband quadrature directional coupler designed in GH15 UMS process.

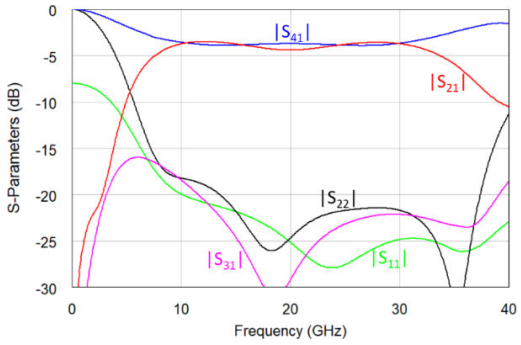


FIGURE 6. Frequency response of the broadband 3-dB directional coupler designed in GH15 MMIC process. Results of electromagnetic calculations.

passive and active components such as capacitors, inductors, resistors, transistors and diodes. Simplified stack-up of the process is presented in Fig. 2. As mentioned above the considered technological process offers only one metallization layer (apart from sub-layer utilized to form air bridges) which can be used to form coupled-line sections. The simplest coupled section can be realized by using two transmission lines having width w, which are separated by gap s. The minimum gap which can be obtained for the process is equal to $s = 4\ \mu$m, which constrains the maximum coupling to $k = 0.595$. Such a value does not allow for realization of even single-section coupled-line 3-dB directional couplers. Therefore, the recently developed idea of the multisection coupler [34] has been implemented for the first time in monolithic technology, to design balanced amplifier having high output power in very broad frequency range exceeding two frequency octaves.

A. MONOLITHIC BROADBAND DIRECTIONAL COUPLER COMPOSED OF CASCADE AND TANDEM-CONNECTED COUPLED-LINE SECTIONS

A schematic diagram of the utilized directional coupler is presented in Fig. 3 [34]. The directional coupler is composed of four coupled-line sections having uniform coupling k and different electrical lengths θ_1, θ_2, θ_3. Coupled sections are connected by transmission lines having equal characteristic impedances Z_0 and electrical lengths θ_0, θ_L. The coupling

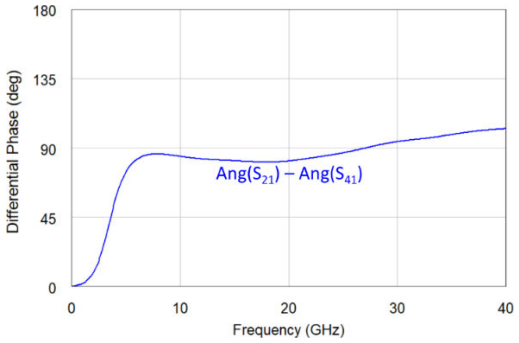


FIGURE 7. Differential phase response of the designed broadband directional coupler. Results of electromagnetic calculations.

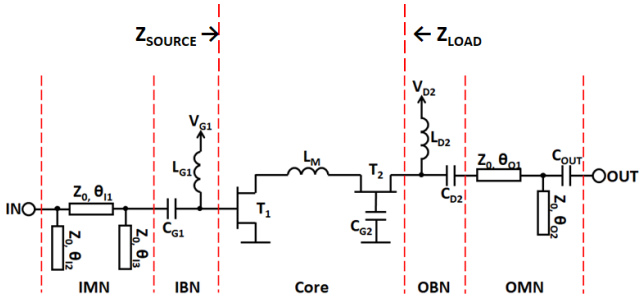


FIGURE 8. Schematic of the designed cascode amplifying block.

coefficient S_{21} and transmission S_{41} can be calculated as follows [34]:

$$S_{21} = C_1 + T_1^2 D^2 \frac{A + C_1 D^2 (B^2 - A^2)}{(1 - AC_1 D^2)^2 - B^2 C_1 D^4} \tag{1}$$

$$S_{41} = \frac{BD^2 T_1^2}{(1 - AC_1 D^2)^2 - B^2 C_1 D^4} \tag{2}$$

where:

$$A = C_2 \left(C_3^2 + T_3^2\right) + 2C_3 T_2 T_3 \tag{3}$$

$$B = T_2 \left(C_3^2 + T_3^2\right) + 2C_2 C_3 T_3 \tag{4}$$

$$D = \cos\theta_L - j \sin\theta_L. \tag{5}$$

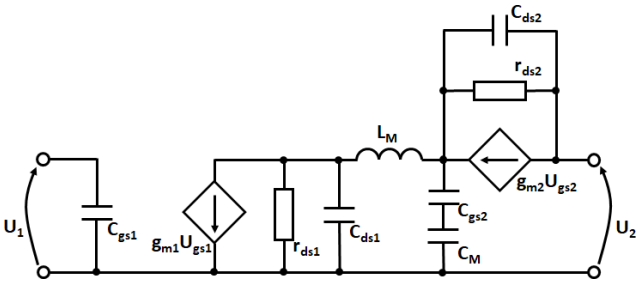


FIGURE 9. Small-signal model of the proposed modified cascode amplifier core composed of two HEMT transistors and additional elements: inductor L_M and capacitor C_M utilized for inductive peaking and capacitance reduction methods.

Coefficients C_i and T_i are coupling and transmission, respectively of the i-th coupled-line section [37]:

$$C_i = \frac{jk \sin\Theta_i}{\sqrt{1 - k^2}\cos\Theta_i + j \sin\Theta_i} \tag{6}$$

$$T_i = \frac{\sqrt{1 - k^2}}{\sqrt{1 - k^2}\cos\Theta_i + j \sin\Theta_i} \tag{7}$$

The frequency response of the considered broadband directional coupler has been calculated from (1) and (2) and presented in Fig. 4, whereas the electrical parameters of the coupler are listed in Table 1.

The monolithic broadband directional coupler has been designed and simulated electromagnetically in AWR Microwave Office environment. In comparison to work presented in [34], the consider directional coupler has been fully designed in microstrip technique which can be easily used in the GH15 process. For the chosen process, the maximum coupling obtained for coupled-line section is equal to $k = 0.595$. Such a value has been calculated for a symmetrical section composed of two transmission-lines having width $w = 41$ um, and the minimum realizable gap $s = 4$ μm. Layout of the structure is presented in Fig. 5, whereas Fig. 6 and Fig. 7 show calculated scattering parameters and differential phase characteristics. As can be seen the directional coupler features a good electrical performance in operational bandwidth, which is equal to $f_H/f_L \approx 6.16$. The isolation is greater than 16.8 dB and return losses are not worse than

$$G'_U = -\frac{R_{ds1} g_{m1} (sR_{ds2}C_{ds2} + R_{ds2}g_{m2} + 1)}{(sR_{ds2}C_{ds2} + 1)(s^3 R_{ds1} L_M C_{ds1} C'_{gs2} + s^2 L_M C'_{gs2} + sR_{ds1}\left(C_{ds1} + C'_{gs2}\right) + 1)} \tag{8}$$

$$Z_{OUT} = \frac{s^3 x^I + s^2 x^{II} + s x^{III} + x^{IV}}{(sR_{ds2}C_{ds2} + 1)(s^3 R_{ds1} L_M C_{ds1} C'_{gs2} + s^2 L_M C'_{gs2} + sR_{ds1}(C_{ds1} + C'_{gs2}))} \tag{11}$$

$$x^I = R_{ds1} R_{ds2} L_M C_{ds1} (C'_{gs2} + C_{ds2}) \tag{12}$$

$$x^{II} = L_M (R_{ds1} C_{ds1} (R_{ds2} g_{m2} + 1) + R_{ds2}(C'_{gs2} + C_{ds2})) \tag{13}$$

$$x^{III} = L_M (R_{ds2} g_{m2} + 1) + R_{ds1} R_{ds2} (C_{ds1} + C'_{gs2} + C_{ds2}) \tag{14}$$

$$x^{IV} = R_{ds1} (R_{ds2} g_{m2} + 1) + R_{ds2}. \tag{15}$$

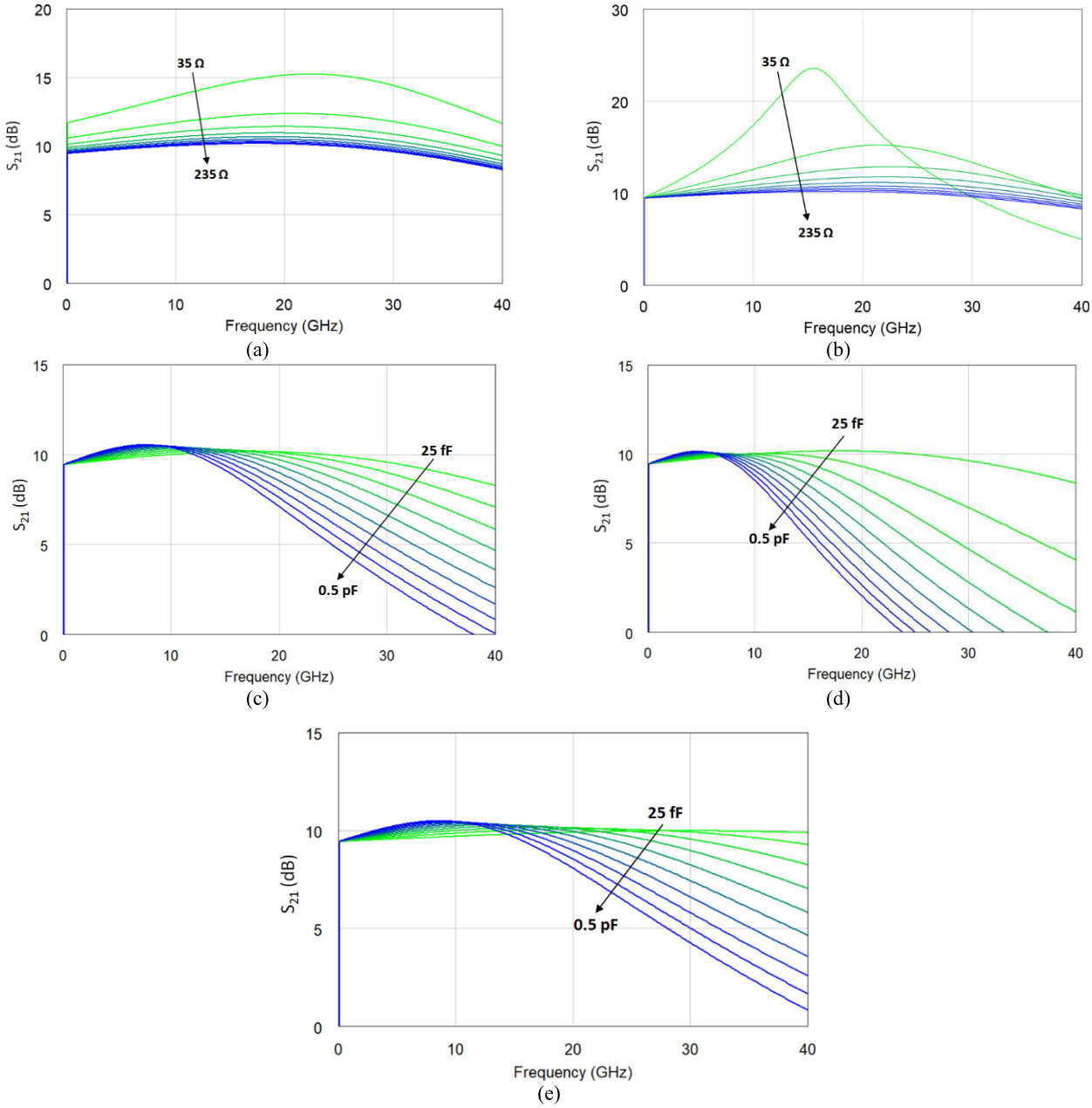


FIGURE 10. Impact of transistor parasticics on matched cascode amplifier frequency response. During the analysis we verified impact of resistances R_{ds1} (a) and R_{ds2} (b), drain-source capacitances C_{ds1} (c), C_{ds2} (d) and gate-source capacitance C_{gs2} (e).

17.2 dB. The imbalance of differential phase between outputs ports #2 and #4 does not exceed 6.3°.

B. BROADBAND CASCODE GaN AMPLIFIERS

To achieve broad operational bandwidth, the amplifying blocks have been realized in cascode topology. The designed circuit is presented in Fig. 8. The core of the block is composed of two HEMT transistors T_1 and T_2, inductor L_M and capacitor C_M. Small-signal model of the circuitry is presented in Fig. 9. It has to be mention that, elements L_M and C_M are used in inductive peaking and capacitive reduction techniques, which significantly improve frequency performance of the cascode amplifier.

For circuitry presented in Fig. 9, the open-load voltage gain G_U' takes form (8), as shown at the bottom of the previous page, where, C'$_{gs2}$ is defined as:

$$C'_{gs2} = \frac{C_{gs2}C_M}{C_{gs2} + C_M} \tag{9}$$

To include influence of load impedance, we can derive voltage gain G_U as

$$G_U = \frac{Z_{LOAD}}{Z_{OUT} + Z_{LOAD}} G'_U \tag{10}$$

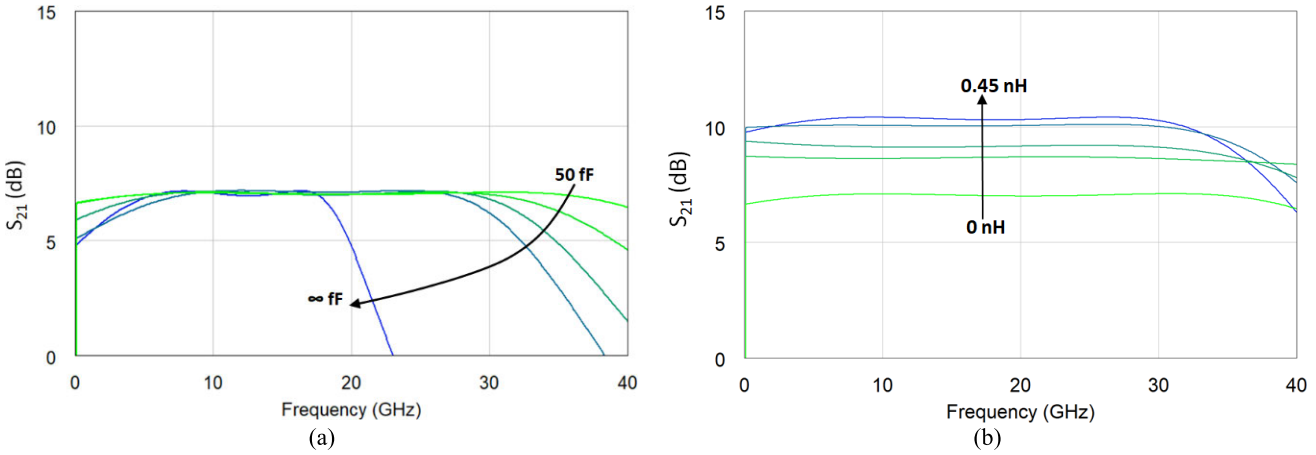


FIGURE 11. Calculation results presenting impact of additional capacitance C_M (a) and inductance L_M (b) on the cascode amplifier frequency response.

TABLE 2. Comparison table presenting parameters of proposed balanced amplifier with other solutions designed in monolithic technologies.

	[3]	[6]	[7]	[20]	[36]	[38]	This work
Amplifying block topology	HEMT GaAs	CMOS 1P6M	HEMT GaAs	HEMT GaN	HEMT AlGaN/GaN	CMOS SiGe	HEMT GaN
Directional coupler topology	Tandem	Lange	Lange	Lange	Lange	Lange	Mixed cascade-tandem
Amplifying block topology	Cascode	Cascade connected stages	Cascode dual-gate	Distributed amplifier	Cascade connected stages	Cascade connected stages	Cascode
Center frequency f_0 (GHz)	180.0	45.4	6.5; 14.5; 30.0	12.0	22.0	180.0	20.0
Bandwidth (f_H/f_L)	2.0	1.04	2.3; 2.2; 2.0	3.0	1.1	1.3	6.16
Power Gain at f_0 (dB)	13.4	21.5	20.5; 17.0; 20.00	9.3	20.0	10.0	9.6
Maximum Output Power at f_0 (dBm)	3.6	---	---; ---; ----	41.1	41.5	---	30.0
1-$dB_{CP(output)}$ (dBm)	---	---	---; +15.0; ---	---	---	-11.1	+27.8
Return Losses at f_0 (dB)	10.0	13.3	10.0; 10.0; 10.0	18.7	10.0	10.2	14.3

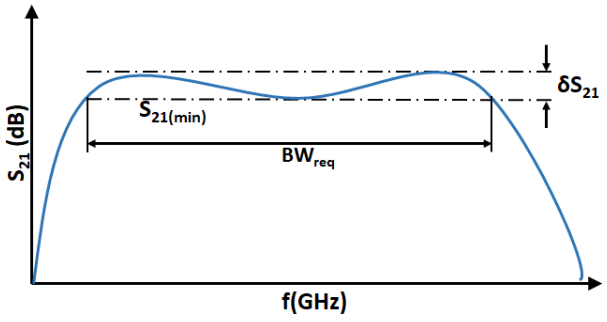


FIGURE 12. Exemplary frequency response of a cascode amplifying block with optimization parameters marked.

where Z_{LOAD} is load impedance and Z_{OUT} is output impedance of cascode core. The output impedance takes form (11), as shown at the bottom of page 4.

For equations (8), (9), (10), and [(11)–(15), as shown at the bottom of page 4], we calculate frequency responses of a matched cascode amplifier for which additional, improving elements L_M and C_M are not taken under consideration. Figure 9 shows impact of particular parameters of the circuit on the operational bandwidth. The broadest frequency responses are obtained for high drain-source resistances R_{ds1}, R_{ds2} and small values of capacitances drain-source C_{ds1}, C_{ds2} and gate-source of the second transistor C_{gs2}. Regarding equation (9) it can be seen that, by adding additional capacitor C_M to the gate of transistor T_2, the overall capacitance C'_{gs2} can be decreased. Such an effect can be used to enhance the operational bandwidth of a cascode amplifier. Simulations presenting impact of C_M on the frequency response are presented in Fig. 10a. On the other hand, to increase small-signal power gain, the inductive peaking method can be used as in [34]. The obtained results are presented in Fig. 10b, where it is clearly seen that, when inductance L_M is increasing, gain level

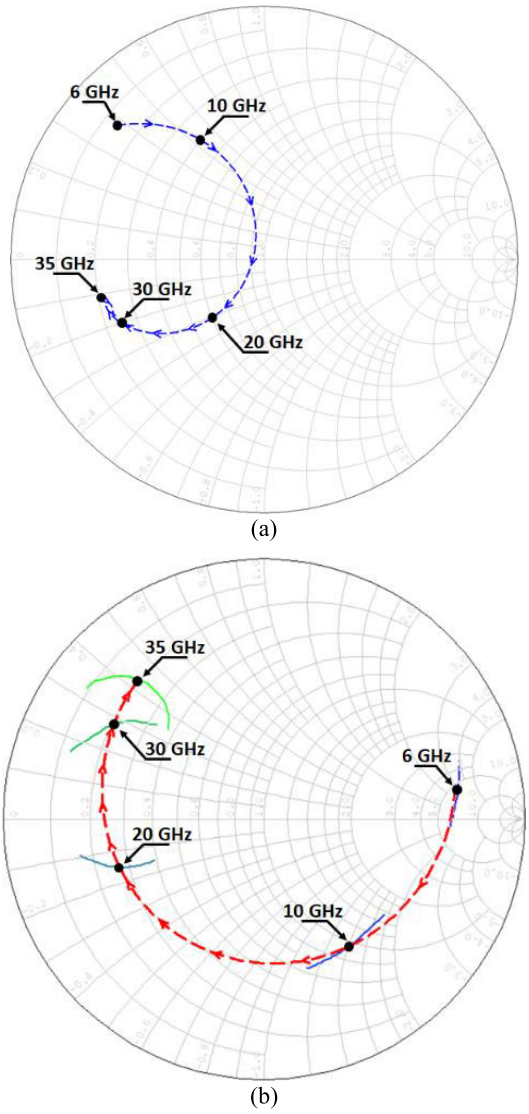


FIGURE 13. The optimum source (a) and load (b) impedance trajectories calculated for the cascode amplifier core composed of two transistors. Results obtained for minimum small-signal power gain $S_{21(min)} = 10$ dB, gain imbalance $\delta S_{21} = 1$ dB and required saturation power $P_{sat(reqx)} = 27$ dBm. Blue and green lines are fragments of power gain contours calculated for value of 10 dB.

is also increased. Both techniques have been used together in the design to improve performance of the cascode amplifying block. To show applicability of the considered techniques, we decide to use the narrowest cascode configuration which is composed of transistor T_1 with four fingers and 50 μm width, and T_2 with eight fingers and 150 μm width. The transistors T_1 and T_2 have been biased by voltages V_{G1} = -2.55 V and $V_{D2} = 15$ V, respectively. Such a biasing point corresponds to Class-B amplifier and sets maximum output power at 27 dBm for a single cascode amplifying block, what gives in total 30 dBm output power for balanced topology. It has to be mention that, the GH15 process allows for achieving greater values of output power. However, due to the power limitations

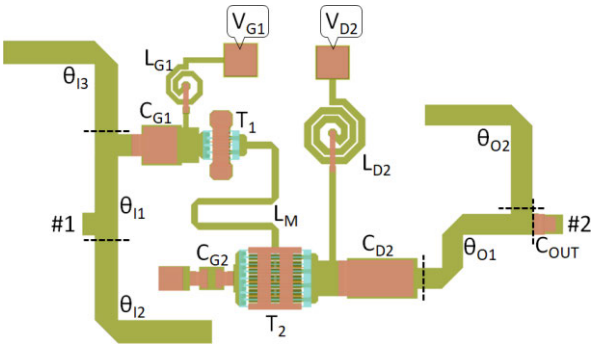


FIGURE 14. Layout of the broadband cascode amplifying block utilized in the broadband GaN balanced amplifier.

of measurement setup and thermal stability which is crucial during long period measurements on bear die chip, we decide to limit maximum power.

Values of additional elements L_M, C_M and source, load impedance trajectories have been found numerically by using Simplex method. The calculations have been obtained using electrical models included in the PDK delivered by the foundry. A simple criterion has been defined as a goal for optimization i.e.;

$$(S_{21(min)} < S_{21}(f) < S_{21(min)} + \delta S_{21})\text{^}P_{sat}(f) = P_{sat(req)}, \tag{16}$$

where $S_{21(\min)}$ is the minimum required small-signal power gain, δS_{21} is the required power gain imbalance and $P_{sat(req)}$ is the required saturation power. Figure 9 present the graphical interpretation of mentioned parameters. The optimization starts from selecting the required operational bandwidth BW_{req}. The procedure is iterative and it goes as long as the assumptions defined in (16) are not fulfilled.

For the considered design, the optimization goals take the following assumptions: $S_{21(min)} = 10$ dB, $\delta S_{21} = 1$ dB, $P_{sat(req)} = 27$ dBm. It is worth nothing that, the optimization procedure has been taken only for a single amplifying block i.e., the single cascode amplifier. Therefore, to achieve 30 dBm saturation power for the balanced amplifier, the single cascode block is designed for $P_{sat(req)} = 27$ dBm. According to optimization results, operational bandwidth of the amplifier in which the mentioned goals are met begin at 6 GHz and ends at 35 GHz. The obtained source and load impedance trajectories together with the calculated small-signal gain contours fragments for 10 dB are presented in Fig. 13. The optimum values for additional inductance and capacitance which have been found are $L_M = 0.45$ nH and $C_M = 0.06$ pF, respectively.

Electrical parameters of input matching network (IMN), output matching network (OMN), input biasing network (IBN) and output biasing network (OBN) have been found numerically by using Simplex method to found overlapping source and load impedance trajectories presented in Fig. 13. We utilize a simple matching circuitry based on a double-stub network at the input of the amplifier and a single-stub circuit

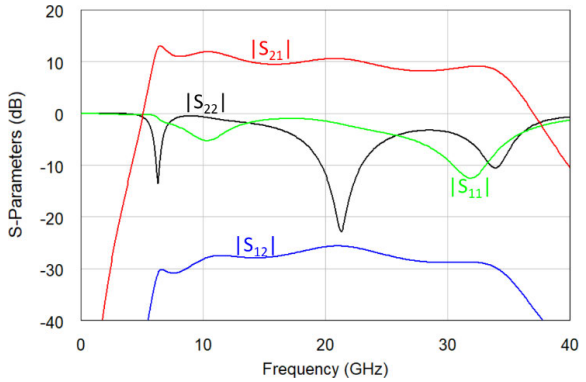


FIGURE 15. Simulated frequency response of a single amplifying block based on the cascode topology.

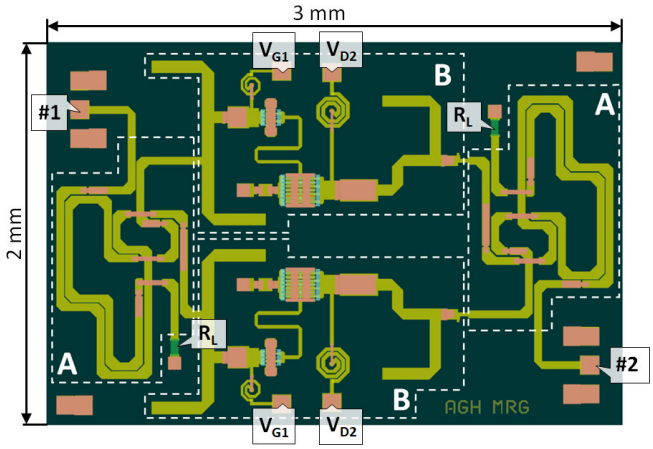


FIGURE 16. Layout of the complete broadband balanced GaN amplifier. The structure is composed of broadband directional couplers (A) and amplifying stages (B).

at its output. It has to be mention that, during the design process of matching networks, we also considered biasing LC circuits composed of inductors L_{G1}, L_{D2} and capacitors C_{G1}, C_{D2}. The final layout of the designed cascode amplifying block is presented in Fig. 14, whereas the simulated frequency response is shown in Fig. 15. The designed stage features small-signal gain greater than 9.4 dB in the entire operational bandwidth, 6.1 GHz up to 35.2 GHz, reverse small signal gain S_{12} is lower than -27 dB.

III. MEASUREMENT RESULTS

The layout of the designed monolithic GaN broadband balanced amplifier is presented in Fig. 16. The amplifier has been fabricated and measured with the use of on-chip measurement setup. The measured frequency responses are presented in Fig. 17, and we can see a good resemblance with the results of simulations. The amplifier operates from 5.7 GHz up to 35.1 GHz, what gives the bandwidth equal to $f_H/f_L \approx 6.15$. The small-signal gain S_{21} is not lower than 8.1 dB. The measured return losses are equal to 14.7 dB at the center frequency. Moreover, the maximum saturation output power is equal to 30 dBm, whereas PAE is equal to

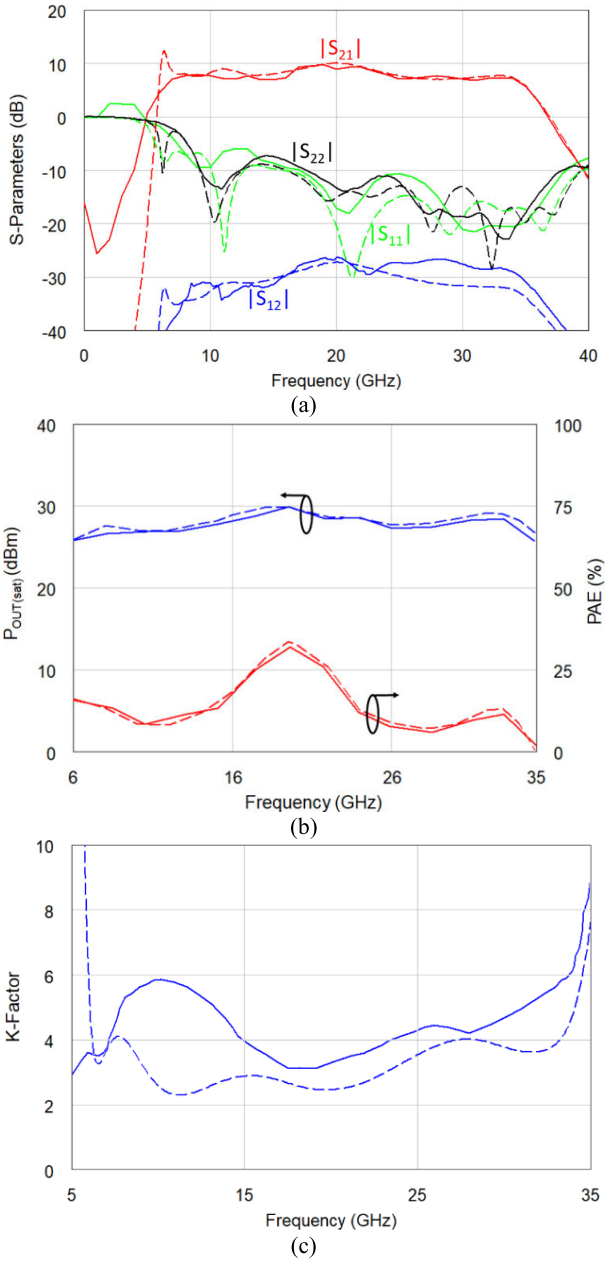


FIGURE 17. Comparison of measured (solid lines) and simulated (dashed lines) frequency response of the broadband amplifier fabricated in GH15 GaN monolithic process. Characteristics (a) shows obtained scattering parameters, (b) presents saturated output power and PAE. The PAE has been simulated and measured for input power $P_{IN} = 23$ dBm, whereas (c) shows stability factor K.

32 %. Both values have been measured at the center frequency equal to 20 GHz. Efficiency of the amplifier has not been taken under consideration during the design process. Therefore, values of PAE in the rest of operational bandwidth are smaller. Value of stability factor K is not smaller than 2.1 in considered wide frequency range and therefore, the device is unconditionally stable. Figures 18 and 19 shows power transfer function and PAE characteristics obtained for different values of frequencies. The compression point for output

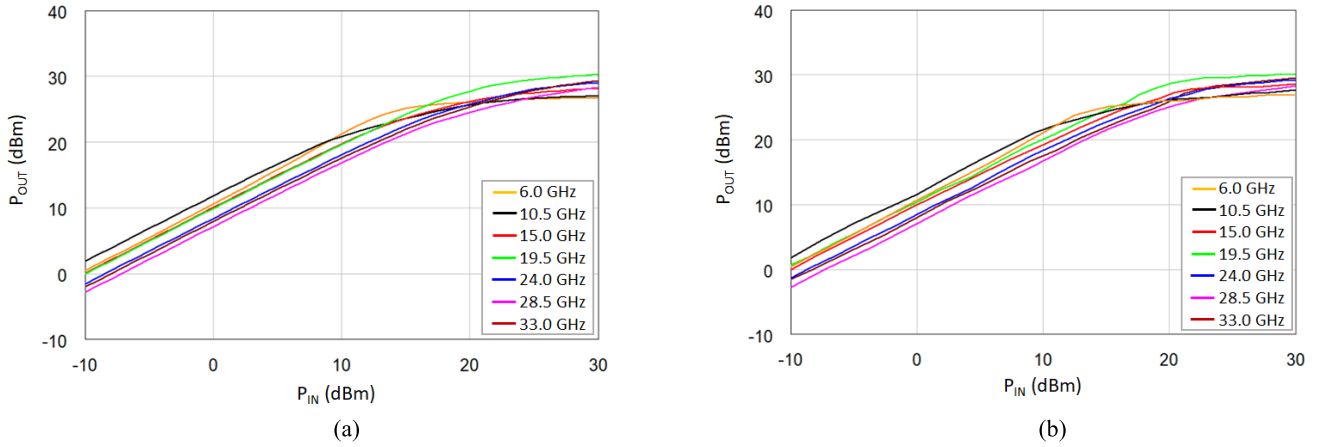


FIGURE 18. Simulated (a) and measured (b) power transfer ($P_{OUT} = f(P_{IN})$) characteristics of the broadband balanced amplifier designed in GH15 process.

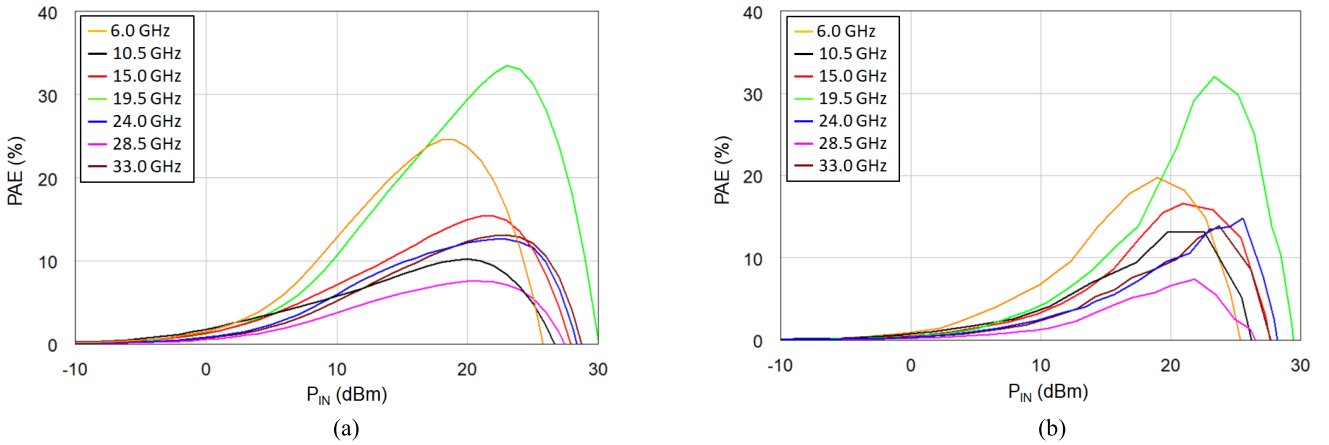


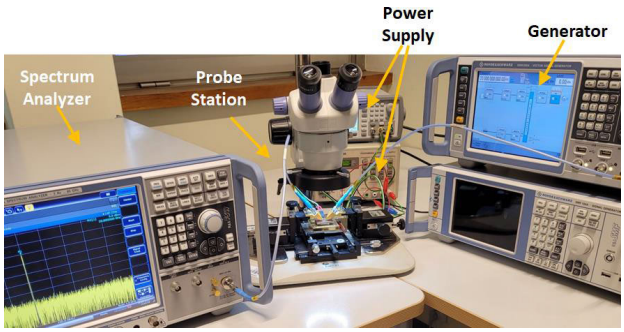
FIGURE 19. Characteristics showing relation between *PAE* and input power ($PAE = f(P_{IN})$). Results obtained during simulations (a) and measurements (b) of the fabricated broadband amplifier.

power measured at 20 GHz is equal to $1dB_{CP} = 27.8$ dBm. The maximum PAE can be observed at the same frequency and it is equal to 32 % for 23 dBm of input power. The obtained results have been collected in Table 2, to compare the proposed solution with other designs presented in literature. It can be seen that the proposed amplifier features the broadest operational bandwidth among all the designs presented elsewhere. In terms of the obtained return losses and small signal power gain, the achieved values are comparable to results presented in [20]. However, the amplifier discussed in [20] features significantly narrower bandwidth. Moreover, the design is composed of two distributed amplifiers with total number of 14 transistors what makes it more complex in comparison to our solution having only 4 transistors.

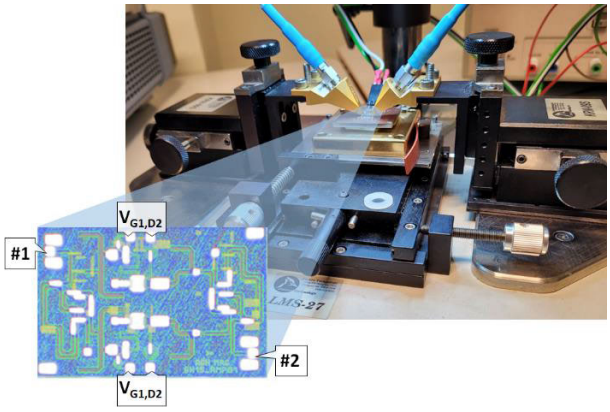
Figure 20a shows the measurement setup used during measurements of transfer functions and PAE which is composed of Rohde & Schwarz SMF 100A Signal Generator operating from 100kHz up to 43.5 GHz, Rohde & Schwarz FSW Signal & Spectrum Analyzer operating from 2Hz up to 85GHz. For measurements of *S*-parameters and stability we used Agilent Technologies 4-port PNA Network Analyzer N5224A operating in 10MHz – 43.5 GHz frequency range. The amplifier has been measured by on-chip method, with the use of a dedicated LMS-27 probe station. Picture showing the manufactured chip during measurements is presented in Fig. 20b.

IV. CONCLUSION

In this paper, we have presented a broadband balanced amplifier designed in monolithic GH15 GaN process, which is composed of broadband mixed cascade-tandem directional couplers and cascode amplifying blocks. The proposed amplifier has the broadest operational bandwidth in comparison to other balanced monolithic circuits reported in literature. Moreover, for the first time the mixed cascade-tandem directional coupler has been used and integrated in monolithic structure, in which only one metallization layer for passive circuit realization is available. The designed balanced amplifier features good electrical performance in terms of return losses, small signal reverse gain, power gain and 1dB compression point, and features bandwidth as wide as $f_h/f_l = 6.16$,



(a)



(b)

FIGURE 20. Pictures showing the measurement setup of the fabricated broadband balanced amplifier (a) and the designed chip (b).

which has never been reported up to date. It can be noted that, the obtained maximum output power reaches 30 dBm, what makes the amplifier suitable for medium power applications.

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