IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 14 October 2023, accepted 8 November 2023, date of publication 16 November 2023,
date of current version 15 December 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3333363

RESEARCH ARTICLE

A 7L and 11L High Step-Up SCMLI Topology With Reduced Component Voltage Stress

JAGABAR SATHIK MOHAMED ALI[1,2], (Senior Member, IEEE), AMJAD REHMAN KHAN[2], (Senior Member, IEEE), GOPINATH NARAYANAN PANDURANGAN[1], PREM PONNUSAMY[3], FATEN S. ALAMRI[4], AND SAEED ALI BAHAJ[5]

[1]Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology (SRMIST), Kattankulathur Campus, Chennai, Tamil Nadu 603203, India
[2]Artificial Intelligence Data Analytics Laboratory (AIDA), College of Computer and Information Sciences (CCIS), Prince Sultan University, Riyadh 11586, Saudi Arabia
[3]Department of Electrical Engineering, St. Thomas' College of Engineering and Technology, Kolkata 700023, India
[4]Department of Mathematical Sciences, College of Science, Princess Nourah bint Abdulrahman University, Riyadh 11671, Saudi Arabia
[5]MIS Department College of Business Administration, Prince Sattam Bin Abdulaziz University, AlKharj 11942, Saudi Arabia

Corresponding author: Faten S. Alamri (fsalamri@pnu.edu.sa)

This research was funded by Princess Nourah bint Abdulrahman University and Researchers Supporting Project number (PNURSP2023R346), Princess Nourah bint Abdulrahman University, Riyadh, Saudi Arabia.

ABSTRACT This article proposes a new capacitor-based multilevel inverter topology (CBMLI) with fewer devices and reduced voltage stress on capacitors and switches. In addition, the proposed topology can be configured as either a 7-level (7L) or 11L circuit with a maximum voltage gain of 3 and 2.5 times, respectively. Comparisons are made between the proposed topology and existing recent CBMLI topologies, and various power loss analyses are presented. The capacitance values are determined by selecting the maximum discharging period, and the associated analysis is presented. Using the simulation software MATLAB/Simulink, the performance of the proposed circuit topology is validated, and the same is tested in the hardware setup. The various dynamic performance characteristics, such as loading changes, input variations, and modulation index, are validated, and the resulting data is discussed.

INDEX TERMS Switched capacitor, multilevel inverter, voltage boost, technological development.

I. INTRODUCTION

Earlier, two-level inverters with suitable modulation schemes were used for harmonic reduction and fundamental voltage control for various applications, including AC drives, Grid-tied renewable energy systems, etc. However, it requires a front high-voltage gain DC-DC boost converter or transformer with a rectifier unit on the source side for high-voltage applications. Also, the grid-tied system requires a complicated filter design at the load side. Conventional multilevel inverters such as cascaded, flying capacitors, and neutral point clamped topologies were proposed to improve the efficiency of the motor drive systems [1], [2]. Later, the explorations grew in a wide span, increasing the number of levels, reducing the power components, incorporating voltage boosting ability, etc., The prominent issues in the conventional multilevel inverters are i) they are buck converters, ii) achieving the voltage balance between the capacitors requires dedicated circuitry, making the system and control complex, iii) if a higher number of levels are required in the terminal voltage, the component count will increase drastically, that is for 'n' capacitors, the components required will be four times 'n' in [3] and [4] and iv) it requires multiple dc source or dc-link capacitors.

The recent research is focused on overcoming the aforementioned issues in conventional neutral point-clamped inverters. The two other types of multilevel inverters, viz., Flying Capacitor Multilevel inverters and Cascaded H- Bridge Multilevel inverters, are hybridized to reduce the component count. The Active Neutral Point Clamped

The associate editor coordinating the review of this manuscript and approving it for publication was Gustavo Callico.

Multilevel inverter topologies are suggested to achieve voltage gain and self-voltage balancing abilities. These topologies are formed by replacing the clamping diodes with active power switches [5]. Additional voltage levels can be obtained by using floating capacitors, and further, reducing clamping diodes may result in reduced conduction losses. These floating capacitors can be used with an H-Bridge to form a hybrid topology with Active Neutral Point clamped inverters. The number of such floating capacitors employed should be optimized, or the voltage balancing issue will arise. In a hybrid voltage source converter that combines three-level neutral point clamped and flying capacitor structures, the voltage balancing issue still needs to be addressed, even though the topology is compact [6]. The number of components is significantly reduced compared to the classical topologies, but voltage boosting and capacitor voltage balancing are still a concern [7]. A switched capacitor based 5LANPC topology is presented in [8] for DC-AC power conversion with inherent self-balancing ability and charging current attenuation. However, they need to have the dc-link voltage equal to the input voltage making the system to add front end boost converter for grid connected applications. Another 9L topology using three switched capacitor is discussed in [9], capable of quadratic voltage gain and inherent voltage balancing. However, it requires a tiny inductor to suppress the inrush current. The topologies presented in [10], [11], [12], and [13], are capable of synthesizing 7 levels with a voltage gain of 1.5, but the component to gain ratio is much higher ranging from 13.3 to 15.3, thus jeopardizing the reliability of the topologies. A reduced switch count based N-Level boost inverter topology has been proposed in [14], with a boosting ability of 2, but its total standing voltage (TSV) and components to gain ration are high. The reduction is components to gain ratio is attempted in [15], [16], [17], [18], and [19] for seven level output by increasing the gain to 3, but the Total standing voltage in the circuit has been compromised. Recently attempts had been made to derive different voltage levels from a single topology through symmetric or asymmetric operation. An UXE-type inverter is proposed in [20], it is capable of giving 9,11 and 13-level operations without any structural modification. However, the topology could achieve only a 1.25 voltage gain during 11-level operation. The proposed high step-up switched capacitor multilevel inverter addresses the component count, voltage gain, and modes of operation. The salient features of the proposed topology are listed as follows:

(i) 7L operation with a voltage gain of 3 and a TSV of 4.6 p.u.
(ii) 11L operation with a voltage gain of 2.5 and a TSV of 4.4 p.u.
(iii) It uses only 10 switches for 7L and 11L output voltage generation.
(iv) Reduced voltage stress on switches.
(v) Both 7 and 11-level operations can be achieved by changing the charging voltage of the capacitor rather than their rating.

TABLE 1. Switching pattern of switches and status of capacitors of 7L operation.

Level	Active Switches	V_o	Capacitor Status			
			C_a	C_b	C_1	C_2
1	$S_1, S_2, S_3', S_4', S_5$	$+V_{in}$	N	C	C	N
2	$S_1', S_2, S_3', S_4', S_5$	$+2V_{in}$	C	D	C	N
3	$S_1', S_2', S_3, S_4', S_5$	$+3V_{in}$	C	D	D	C
4	S_1, S_3, S_4', S_5'	0	N	D	N	D
5	$S_1', S_2', S_3, S_4, S_5'$	$-V_{in}$	C	N	N	D
6	$S_1', S_2, S_3', S_4, S_5'$	$-2V_{in}$	C	N	C	D
7	$S_1, S_2, S_3', S_4, S_5'$	$-3V_{in}$	D	C	C	D
C: Charging, **D:** Discharging, **N:** No effect						

(vi) Self-balancing capacitors, free from any separate control algorithms and sensing elements.

II. PROPOSED TOPOLOGIES

A. CIRCUIT DIAGRAM DESCRIPTION AND WORKING PRINCIPLE OF PROPOSED TB-7LI

As shown in Fig. 2 (a), the proposed topology consists of a single dc source, four switched capacitors, two diodes, eight switches with antiparallel diodes (S_1, S_3-S_5,and S_1', S_3'-S_5'), and two switches (S_2 and S_2') without anti-parallel diode. The voltage across each SCs is given in (1)

$$V_{C_a} = V_{C_b} = V_{C_1} = V_{C_2} = V_{in} \tag{1}$$

±L1 (V_{in})- During the first level, the capacitor C_a and C_1 get charged to vin through the switches S_1, S_2, S_4' S_5, and $D_{1,2}$ for positive level and S_4, S_1', S_3, S_5', and S_2 for the negative cycle as shown in Fig. 2 (b) and (c), respectively. The input voltage is supplied to the load, i.e., $V_o = V_{in,}$ for both the half cycle.

±L_2 ($2V_{in}$)- the charged capacitor is discharged to the load by adding the source voltage together, as shown in Fig. 2 (d) and (e). However, the upper capacitor, i.e., C_a and C_1, is charging, and C_b and C_2 are discharging for the positive and negative cycle, respectively. The voltage across the load will be the sum of the source voltage and the capacitor, either C_b or C_2 voltage, with respect to the polarity of the load voltage.

±L3 ($3V_{in}$)-the top level, i.e., third level, produces the output voltage equal to three times the source voltage, which is achieved by summing the voltage across the C_b, C_1, and source voltage for the positive cycle and the negative cycle the C_a, C_2 is added with vin as shown in Fig. 2 (f) and (g) respectively. Finally, the zero states with a maximum output voltage of $0V_{in}$ are achieved by subtracting the C_a and C_1 or C_b and C_2, as shown in Fig. 2 (h). The switching sequences of the 7L operation, voltage stress and current stress of all switches during each voltage levels are presented in Table 1, 2 and 3.

B. WORKING PRINCIPLE OF PROPOSED TB-11LI

The 11L can be obtained by changing the switching operation. For 7L operation, all four capacitors were charged to a voltage equivalent to the input voltage. But in 11L operation,

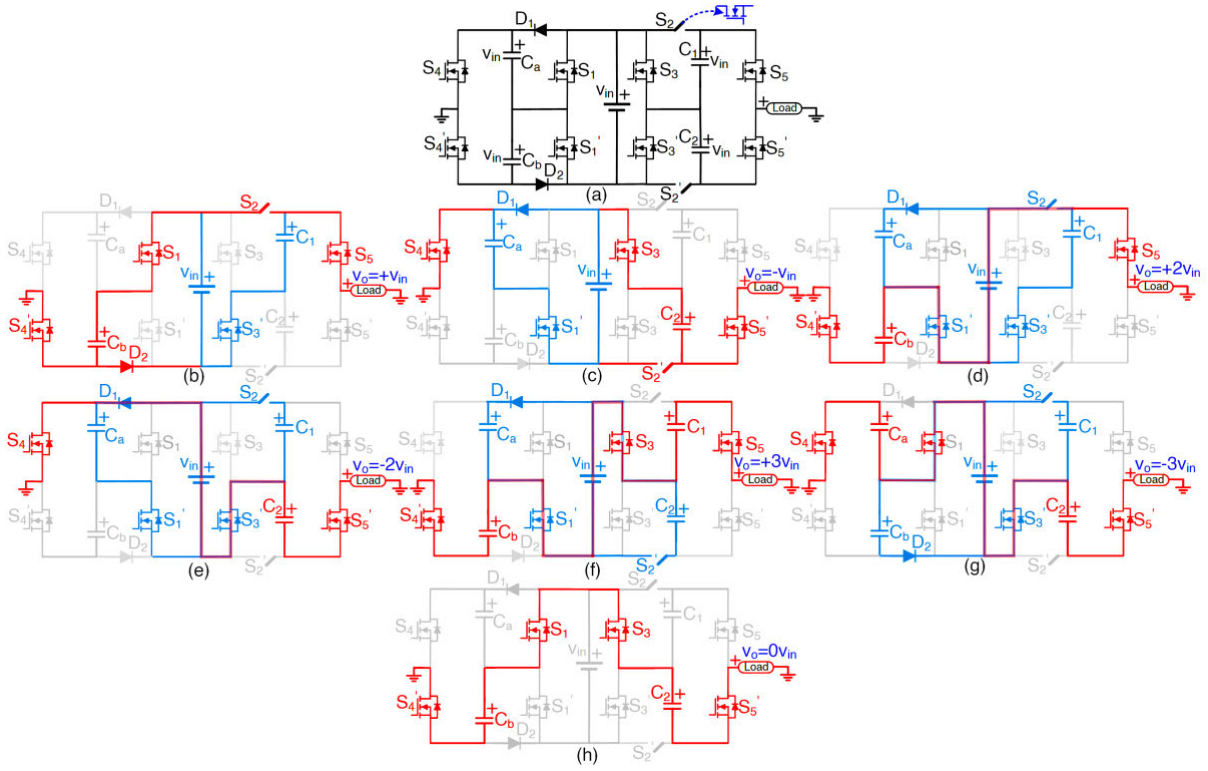


FIGURE 1. Proposed 7L topology (a) Circuit diagram of the proposed and (b)-(h) Modes of operations with corresponding current paths.

TABLE 2. Voltage stress of switches during 7L operation.

Level	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	S_5	S_5'	V_o
1	0	V_{in}	V_{in}	V_{in}	V_{in}	V_{in}	$2V_{in}$	0	$2V_{in}$	$2V_{in}$	$+V_{in}$
2	V_{in}		0			0			0		$+2V_{in}$
3		0	V_{in}			V_{in}			$2V_{in}$	0	$+3V_{in}$
4	0	V_{in}		0	0			$2V_{in}$			0
5	V_i		V_{in}				0		$2V_{in}$		$-V_{in}$
6		0		V_{in}	V_{in}	0				0	$-2V_{in}$
7		V_{in}	0			0	0				$-3V_{in}$
MBV	V_{in}	V_{in}	V_{in}	V_{in}	V_{in}	V_{in}	$2V_{in}$	$2V_{in}$	$2V_{in}$	$2V_{in}$	-

TABLE 3. Current stress of switches during 7L operation.

Level	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	S_5	S_5'	V_o
1	i_{cb}	-	$i_{c1}+i_o$	-	-	i_{c1}	-	i_o	i_o	-	$+V_{in}$
2	-	$i_{ca}+i_o$				i_{c1}					$+2V_{in}$
3			-	i_{c2}	i_o	-					$+3V_{in}$
4	i_o	-		-					-	i_o	$0\ V_{in}$
5	-	i_{ca}		$i_{c2}+i_o$	i_{c2}		i_o	-			$-V_{in}$
6			i_{c1}	-	-	$i_{c1}-i_o$					$-2V_{in}$
7	i_{cb}	-									$-3V_{in}$

the capacitors C_1 and C_2 are operated in clamping mode. The input voltage is evenly divided between the capacitors C_1 and C_2. With this and switching sequence modification, the topology can synthesize 11L without structural modifications. The respective switching sequences of the 11L operation, voltage stress, and current stress of all switches during each voltage level are given in Tables 4, 5, and 6.

TABLE 4. Switching pattern of switches and status of capacitors of 11L operation.

Level	Active Switches	V_o	Capacitor Status			
			C_a	C_b	C_1	C_2
1	S_1, S_3', S_4', S_5	$+V_{in}/2$	N	C	D	N
2	S_1, S_2, S_2', S_4', S_5	$+2V_{in}$	N	C	C	C
3	S_1, S_3, S_4', S_5	$+3V_{in}$	N	C	D	N
4	S_1', S_2, S_2', S_4', S_5	$+4V_{in}$	C	D	C	C
5	S_1', S_3, S_4', S_5	$+5V_{in}$	C	D	D	N
6	S_1, S_2, S_2', S_4', S_5'	0	C	C	C	C
7	S_1', S_3, S_4, S_5'	$-V_{in}/2$	C	N	N	D
8	S_1, S_2, S_2', S_4, S_5'	$-2V_{in}$	C	N	C	C
9	S_1', S_3', S_4, S_5'	$-3V_{in}$	C	N	N	D
10	S_1, S_2, S_2', S_4, S_5'	$-4V_{in}$	D	C	C	C
11	S_1, S_3', S_4, S_5'	$-5V_{in}$	D	C	N	D

C: Charging, **D:** Discharging, **N:** No effect

C. CAPACITOR SIZING

The optimum value of the capacitor to be connected to the circuit can be obtained by using the equation below [21]

$$C_{opt} = {Q_{Ci}}/{k \times V_{in}} \tag{2}$$

where Q_{Ci} and k represent the net charge of ith capacitor and ripple factor.

For the 7L and 11L operations, the optimum value of capacitance is to be chosen based on the lower ripple voltage,

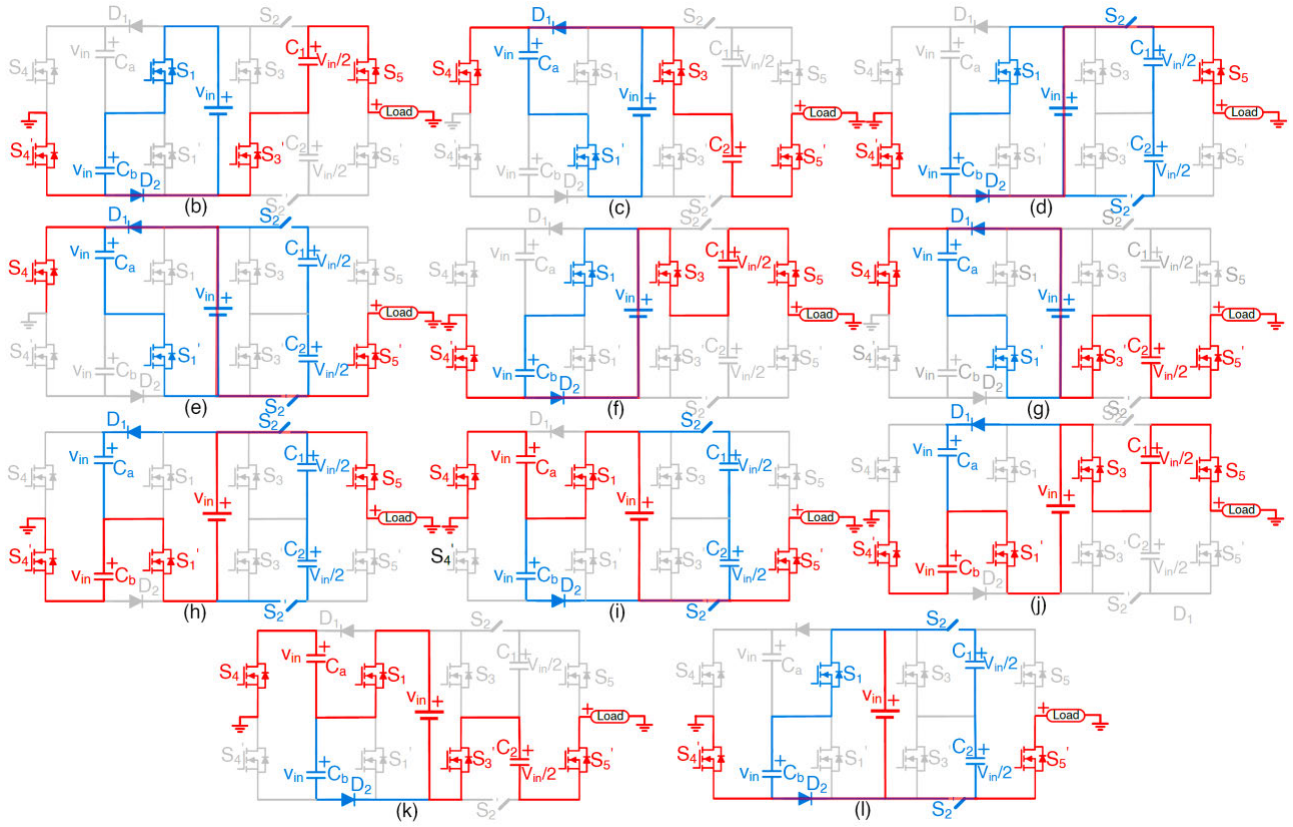


FIGURE 2. Proposed 11L topology (a) Circuit diagram and (b)-(l) Modes of operations with corresponding current paths.

TABLE 5. Voltage stress of switches during 11L operation.

Level	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	S_5	S_5'	V_o
1									V_{in}		$+V_{in}/2$
2	0		$0.5V_{in}$	0	V_{in}	$0.5V_{in}$	V_{in}				$+V_{in}$
3		V_{in}						0	0	V_{in}	$+3V_{in}/2$
4	V_{in}			$0.5V_{in}$	$0.5V_{in}$	V_{in}	$2V_{in}$				$+2V_{in}$
5		0	0								$+5V_{in}/2$
6	0	V_{in}		0	0	$0.5V_{in}$		0	V_{in}	0	0
7				$0.5V_{in}$	$0.5V_{in}$	V_{in}					$-V_{in}/2$
8	V_{in}	0					0	$2V_{in}$			$-V_{in}$
9			$0.5V_{in}$	0	V_{in}	$0.5V_{in}$					$-3V_{in}/2$
10		V_{in}									$-2V_{in}$
11	0										$-5V_{in}/2$
MBV	V_{in}	V_{in}	$0.5V_{in}$	$0.5V_{in}$	V_{in}	V_{in}	$2V_{in}$	$2V_{in}$	V_{in}	V_{in}	-

TABLE 6. Current stress of switches during 11L operation.

Level	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	S_5	S_5'	V_o
1			-	-	-	i_o					$+V_{in/2}$
2	i_{cb}	-	$(i_{c1,2})+i_o$	$(i_{c1}=i_{c2})$							$+V_{in}$
3			-	-	i_o						$+3V_{in}/2$
4	-	$i_{ca}+i_o$	$(i_{c1,2})+i_o$	$(i_{c1}=i_{c2})$	-		-	i_o	i_o	-	$+2V_{in}$
5			-	-	i_o	-					$+5V_{in}/2$
6	i_{cb}	-	$(i_{c1}=i_{c2})$	$(i_{c1,2})-i_o$	-						0
7			-	-	i_o						$-V_{in}/2$
8	-	i_{ca}	$(i_{c1}=i_{c2})$	$(i_{c1,2})-i_o$							$-V_{in}$
9			-	-	-	i_o	i_o	-	-	i_o	$-3V_{in}/2$
10	i_o	-	$(i_{c1}=i_{c2})$	$(i_{c1,2})-i_o$		-					$-2V_{in}$
11			-	-		i_o					$-5V_{in}/2$

nominal frequency, high gain, and longest discharging time (*LDT*). The *LDT* for each cycle should be determined based on the charging and discharging chart shown in Fig.3.

During seven-level operation, the *LDT* of the capacitors C_a and C_1 is between t_c and π-t_c. Thus, the net charge of capacitors $C_a$and C_1 can be mathematically expressed in the (3),

$$Q_{C_a}\left(Q_{C_1}\right) = \int_{t_c}^{(\pi - t_c)} I_L(t)\, d\omega t \tag{3}$$

where, IL(t) denotes load current. F or an RL load, the net charge of capacitors C_a and C_1 can be mathematically expressed in the (4),

$$Q_{C_a}\left(Q_{C_1}\right) = \int_{t_c}^{(\pi - t_c)} I_m \sin\left(\omega t - \phi\right)\ d\omega t \tag{4}$$

where, Im is the maximum value of the load current. On simplification, the charge in capacitors C_a and C_1 can be estimated using the (5) below,

$$Q_{C_a}\left(Q_{C_1}\right) = \frac{I_m}{\omega}\left[cos\left(\omega t_c\right) - cos\omega\left(\pi - t_c\right)\right] \tag{5}$$

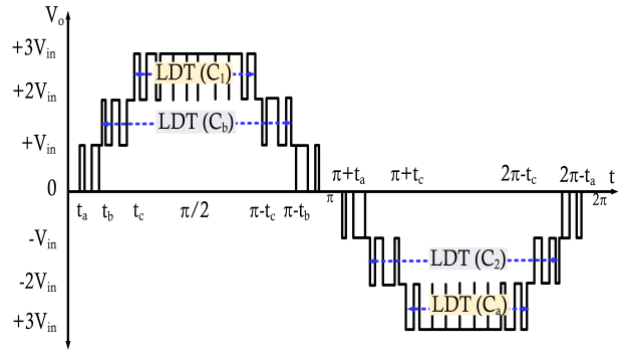


FIGURE 3. Charging and discharging time of the capacitors for synthesizing 7L voltage waveform.

By substituting the calculated charge in the equation (3), the optimum value of capacitance can be found in the (6),

$$C_{a-opt/1-opt} = \frac{Q_{C_a}\left(Q_{C_1}\right)}{k \times V_{in}} = \frac{I_m}{k \times V_{in} \times \omega}\left[cos\left(\omega t_c\right) - cos\,\omega\left(\pi - t_c\right)\right] \tag{6}$$

Similar to the capacitors C_a and C_1, the optimum values of C_b and C_2 are also calculated. Considering the LDT of C_b and C_2, which is in between t_b and π-t_b, the value of net charge and the optimum value of capacitance is calculated as (7),

$$Q_{C_b}\left(Q_{C_2}\right) = \frac{I_m}{\omega}\left[cos\left(\omega t_c\right) - cos\,\omega\left(\pi - t_c\right)\right] \tag{7}$$

$$C_{b-opt/2-opt} = \frac{Q_{C_b}\left(Q_{C_2}\right)}{k \times V_{in}} = \frac{I_m}{k \times V_{in} \times \omega}\left[cos\left(\omega t_b\right) - cos\,\omega\left(\pi - t_b\right)\right] \tag{8}$$

where, $t_a = 0$; $t_b = {}^{19.47}/_{\omega}$; $t_c = {}^{41.81}/_{\omega}$

D. LOSS EQUATIONS

There are three significant losses in the inverters they are conduction losses, switching losses, and capacitor ripple losses. The conduction losses are the losses due to the internal resistance of the capacitor and switches while synthesizing different voltage levels. From Fig.3, the equivalent circuits are constructed for synthesizing each level, shown in Table 7. In the equivalent circuits, RS-is the switch resistance, V_d-is the forward voltage drop across the diode, Rd-is the diode resistance, and V_{Cx} (x = 1/2/a/b)-is the capacitor voltage. To estimate the conduction loss, the equivalent circuits of each level have been utilized, and the respective expressions for instantaneous and average conduction loss are presented in the fourth column of Table 7. The same method can be used for deducing the conduction losses for the proposed topology when operated in 11L output voltage generation. These are the losses while synthesizing each level, to compute

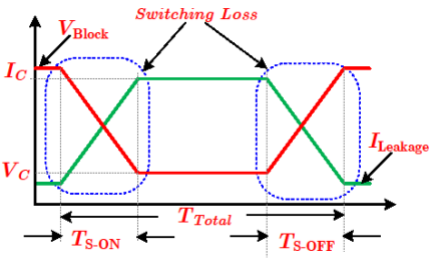


FIGURE 4. Linearized switching model of a power electronic switch.

the average losses, the number of times each level occurs over a cycle is multiplied and divided by the period T.

From Table 7, the total conduction losses can be computed is given in (9)

$$P_{con} = \sum_{i=0}^{N_{Level}} P_{Ci}^{+} + P_{Ci}^{-} \tag{9}$$

The switching characteristics of a practical switch are shown in Fig. 4. The turn-on and turn-off delay times result in energy losses in each switch according to their switching sequence. The energy lost while turning on a power electronic switch can be estimated by the (10),

$$E_{ON} = \frac{V_C i_C}{6} t_{on} \tag{10}$$

Here V_C is the voltage drop across the internal resistance of the switch during conduction. i_C is the current through the switch during the conduction level concerned. Ton is the finite turn-on time. Similarly, from the linearized switching model, the energy dissipated in a switch when it is turned OFF can be determined using the (11)

$$E_{OFF} = \frac{V_{Block} i_C}{6} t_{off} \tag{11}$$

Here V_{Block} is the blocking voltage of the switch, and toff is the time taken for the switch to turn off. The average switching loss can be determined using the (12) and (13). Where f is the frequency, and 'n' is the number of switching instants per cycle.

$$P_{SL} = n \times f\left(E_{on} + E_{OFF}\right) \tag{12}$$

$$P_{SL} = \sum_{i=1}^{N_{Switch}} P_{SL-i} \tag{13}$$

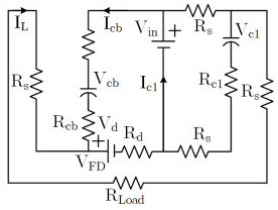
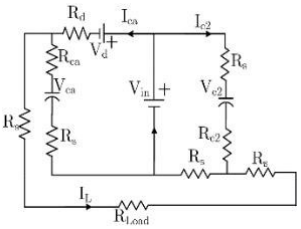
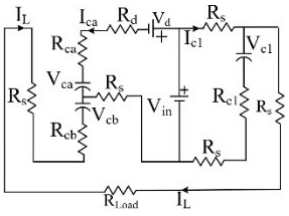
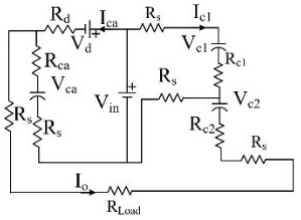
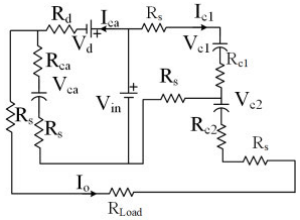
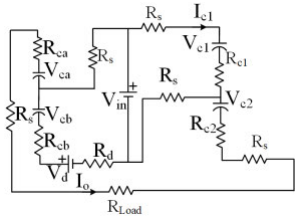
The capacitor ripple voltage arises due to the difference between the desired and actual voltage at its terminals at any instant. If icn is the current through the capacitor 'n' and C_p is the capacitance of capacitor 'p', then the voltage ripple can be estimated using the (14) as given in [22]

$$\Delta V_{cp} = \frac{1}{2\pi f C_p}\int_{\alpha_m}^{\alpha_n} i_{cp}\left(t\right) dt \tag{14}$$

The total ripple loss is the sum of the losses incurred across the capacitors C_1 to C_4, and it can be expressed in (15)

$$P_{R-L} = \frac{1}{2\pi}\sum_{k=1}^{4} C_k \Delta V_{cp}{}^2 \tag{15}$$

TABLE 7. Conduction loss equations for the 7-level topology.

V_o	Equivalent Circuit	Expressions for charging and Load Current	Expressions for instantaneous and average conduction loss
$+V_{in}$		$i_{C_1} = \frac{V_{in} - V_{C_1}}{2R_s + R_{C_1}};$ $i_{C_b} = \frac{V_{in} - V_{C_b} - V_{D2}}{R_s + R_d + + R_{cb}};$ $i_{C_2} = i_{C_a} = 0;$ $i_o = \frac{V_{C_b}}{4R_s + R_{C_b} + R_L};$	$p_{C_1} = i_{C_1}^2(2R_s + R_{C_1}) + i_o^2(4R_s + R_{C_b}) + i_{C_b}^2(R_s + R_{C_b} + R_d)$ $P_{C_1} = \frac{2(t_b - t_a)' \; p_{C_1}}{T}$
$-V_{in}$		$i_{C_2} = \frac{V_{in} - V_{C_2}}{2R_s + R_{C_2}};$ $i_o = \frac{V_{C_a}}{4R_s + R_{ca} + R_L};$ $i_{C_a} = \frac{V_{in} - V_{D1} - V_{C_a}}{R_s + R_d + + R_{C_a}};$ $i_{C_2} = i_{C_b} = 0;$	$p_{C_1}' = i_{C_2}^2(2R_s + R_{C_2}) + i_0^2(4R_s + R_{C_a}) + i_{C_a}^2(R_s + R_{C_a} + R_d)$ $P_{C_1} = \frac{2(t_b - t_a)' \; p_{C_1}'}{T}$
$2V_{in}$		$i_{C_2} = \frac{V_{in} - V_{C_1}}{2R_s + R_{C_2}};$ $i_o = \frac{V_{in} + V_{C_b}}{4R_s + R_{C_b} + R_L};$ $i_{C_a} = \frac{V_{in} - V_{D1} - V_{C_a}}{R_s + R_d + + R_{C_a}};$ $i_{C_1} = i_{C_b} = 0;$	$p_{C_2} = i_{C_2}^2(2R_s + R_{C_1}) + i_o^2(4R_s + R_{C_b}) + i_{C_a}^2(R_s + R_{C_a} + R_d)$ $P_{C_2} = \frac{2(t_c - t_b)' \; p_{C_2}}{T}$
$-2V_{in}$		$i_{C_1} = \frac{V_{in} - V_{C_1}}{2R_s + R_{C_1}};$ $i_o = \frac{V_{in} + V_{C_b} + V_{C_2}}{4R_s + R_{C_b} + R_L};$ $i_{C_a} = \frac{V_{in} - V_{D1} - V_{C_a}}{R_s + R_d + + R_{C_a}};$	$p_{C_2}' = i_{C_1}^2(2R_s + R_{C_1}) + i_o^2(3R_s + R_{C_2} + R_d) + i_{C_a}^2(R_s + R_{C_a} + R_d)$ $P_{C_2} = \frac{2(t_c - t_b)' \; p_{C_2}'}{T}$
$3V_{in}$		$i_o = \frac{V_{C_b} + V_{in} + V_{C_1}}{4R_s + R_{C_1} + R_{C_b} + R_L};$ $i_{C_b} = \frac{V_{in} - V_{C_a} - V_{D1}}{R_s + R_d + R_{C_a}};$ $i_{C_2} = \frac{V_{in} - V_{C_1}}{2R_s + R_{C_2}};$	$p_{C_3} = i_{C_2}^2(2R_s + R_{C_2}) + i_o^2(4R_s + R_{C_b} + R_{C_1}) + i_{C_a}^2(R_s + R_{C_a} + R_d)$ $P_{C_3} = \frac{(p - 2t_c)' \; p_{C_3}}{T}$
$-3V_{in}$		$i_o = \frac{V_{C_a} + V_{in} + V_{C_2}}{4R_s + R_{C_2} + R_{C_a} + R_L};$ $i_{C_b} = \frac{V_{in} - V_{C_b} - V_{D2}}{R_s + R_d + R_{C_b}};$ $i_{C_1} = \frac{V_{in} - V_{c1}}{2R_s + R_{C_1}};$	$p_{C_3}' = i_{C_1}^2(2R_s + R_{C_1}) + i_o^2(4R_s + R_{C_a} + R_{C_2}) + i_{C_b}^2(R_s + R_{C_b} + R_d)$ $P_{C_3} = \frac{(p - 2t_c)' \; p_{C_3}'}{T}$

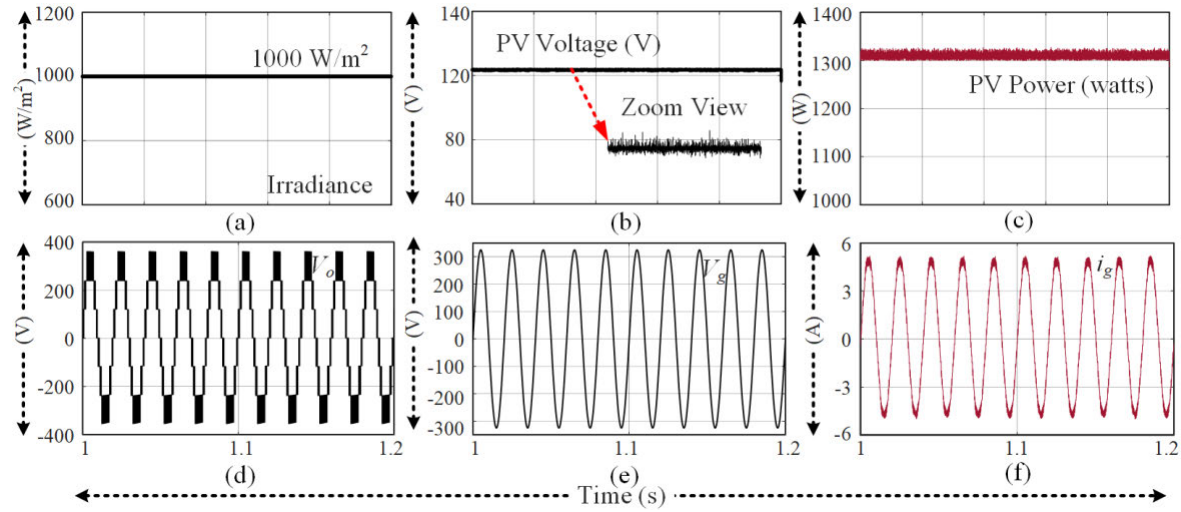


FIGURE 5. Simulation results of (a)-(c) Irradiance level, PV voltage, and PV power, (d) Inverter voltage (V_o), (e) Grid voltage (v_g), and (f) Grid current (i_g).

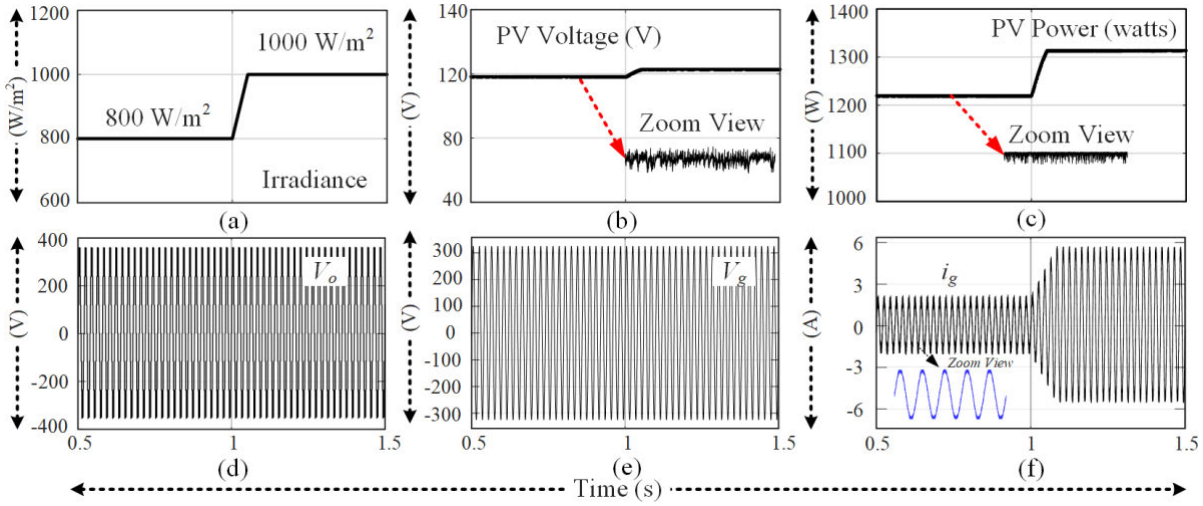


FIGURE 6. Simulation results during a change in irradiance level (a)-(c) Irradiance, PV voltage and PV power, (d) Inverter output voltage (V_o), (e) Grid voltage (v_g), and (f) Grid current (i_g).

The energy loss in a practical switch while turning ON and turning OFF can be estimated using the loss equations explained in [15]. The average power loss can be estimated using the frequency and number of switching instants from the energy loss. Thus, the net loss in any inverter can be expressed in (16) and (17),

$$P_{Loss} = P_{con} + P_{sw} + P_{R-L} \tag{16}$$

$$\eta = \frac{P_{out}}{P_{in} + P_{Loss}} \tag{17}$$

E. CAPACITOR VOLTAGE BALANCING

The prominent setback in conventional multilevel inverter topologies like neutral point clamped and flying capacitor multilevel inverters is that, with the increase in the number of levels in the terminal voltage, the capacitor voltage unbalance will occur [23], [24]. To overcome this setback, there are separate voltage balancing circuits need to be deployed, which makes the circuit bulky and reduces reliability. In the proposed topology, during 7L operation all four capacitors, C_1, C_2, C_a, and C_b are connected individually to the voltage source. The voltage of the source is not divided among the capacitors; hence, the balance is inherently achieved during the 7L operation. In 11L operation, the capacitors C_a and C_b are always connected individually in parallel to the voltage source; hence, their voltage is always equal to the source voltage. But the capacitors C_1 and C_2 are connected in series and then clamped parallel to the voltage source. In this case, the capacitor C_1 conducts for the positive voltage levels, and C_2 conducts for the corresponding negative voltage level, so if the current through the two capacitors C_1 and C_2 over a cycle is summed up, the value will be zero.

TABLE 8. Prototype Specifications.

Parameters / Components	Type and Description
Input Voltage (V_{dc})	100 V
Output Voltage (V_o)	300 V (7L) & 250 V (11L)
Switching (f_{cr})	5 kHz
Output Frequency (f)	50 Hz
Capacitor C_1, C_2, C_3 & C_4	2700 µF, 160 V
Switch	IXXH50N60C3D1 / 600 V, 50 A
Gate Driver	HCPL-J312
Digital Controller	TMS320F28379D
Diode	VS-60EPU02-N3 / 200V, 60 A
Load Parameters	50 Ω, 50+j80 Ω, 80+j50 Ω

This implies that the capacitors C_1 and C_2 are inherently balanced.

III. RESULT AND DISCUSSIONS

The proposed 7L and 11L has been simulated in MATLAB/Simulink platform to test its operability. Initially, the performance has been checked considering the constant irradiance of 1000 W/m^{2}and 25°C, and the respective results are illustrated in Fig. 5(a)-(f). Further the performance has been tested by varying the irradiance level from 800 W/^{m2} to 1000 W/m2 at 25°C, and the corresponding results are depicted in Fig. 6(a)-(f).

The proposed 7L and 11L topologies have been experimentally validated using a laboratory setup of 900 W. The circuit devices and their specification for the experimental prototype are listed in Table 8. Both 7L with triple voltage gain and 11L with a voltage gain of 2.5 topologies have been tested under static and dynamic operating conditions, such as input change, different load conditions, and modulation index variations. Based on the design calculations in equations (6) and (8), the capacitor model SLPX272M160H9P3 has been considered, with an ESR value of 0.074 Ω. Initially, a resistive load of R=50 Ω is chosen for an input voltage of 100 V, a 7L stepped waveform with a peak value of 300 V is obtained, and the load current is 6 A peak as illustrated in Fig. 7(a). The proposed topology is subjected to two different RL loads, R=50 Ω and L = 80 mH and R=80 Ω and L = 50 mH and their performance is tested. The terminal voltage, load current, and capacitor voltages obtained at the above load conditions are portrayed in Fig. 7(b) and Fig. 7(c). For a source voltage of 100 V, the terminal voltage is 300 V, verifying its voltage boosting ability, i.e., voltage gain is 3. The load currents are observed as 5.4 and 3.6 A for the said loads. In both loads, it is observed that the voltages across the capacitors are inherently balanced at 100 V. Further, when compared to the resistive load, the load current is smoothened in the inductive loading, with the inductance being a ripple filter. Fig. 8(a) shows the experimental waveforms of, terminal voltage, load current, and capacitor voltages V_{Ca} and V_{C2} when an input voltage change of 80 V to 100 V is considered. It is observed that the load and capacitors smoothly accommodate the input change. At time t=1.5 s, the load demand is varied from R= 50Ω to R-L Load (50+j80) Ω, and the respective experimental results of terminal voltage, load current, and capacitor voltages V_{Cb} and V_{C1} are depicted in Fig. 8(b). It can be observed that the capacitor voltage is well-balanced, confirming its self-balancing nature, while the load demand is varied. Fig. 9(a) and 9(b) show the experimental results when the modulation index is altered to test the performance of the proposed 7L inverter. While changing the modulation index from 1 to 0.8 and from 0.8 to 0.3, it is observed intact during the above variations with a smooth changeover of terminal voltage and load current. Similar to the 7L operation, the performance of the 11L with a voltage gain of 2.5 is also tested with different scenarios. The waveforms of terminal voltage, load current, and capacitor voltages V_{Ca} and V_{Cb} are shown in Fig. 10(a) when a load of R=50 Ω and an input of 100 V is applied. The proposed topology delivers a terminal voltage with a 250 V peak for an input voltage of 100 V, i.e., a voltage boost 2.5. The capacitor voltages shown in Fig. 10(c) indicate that the capacitor voltagesV_{C1} and V_{C2} are balanced with input voltage equally divided, wherein the capacitor voltages ofV_{Ca} and V_{Cb} are 100 V each. The response of the 11L operation, when subjected to an input change of 80 V to 100 V and during the transient load demand of 50Ω to (50+j80) Ω, is depicted in Fig. 11(a) and 11(b). Furthermore, while varying the modulation index values from 1 to 0.8 and from 0.8 to 0.5, the proposed topology's response is shown in Fig. 12(a) and 12(b).

The PLECS (Piecewise Linear Electrical Circuit Simulation) software tool has been used to analyse the power loss of the proposed 7L and 11L configurations. For this purpose, the thermal modelling of the proposed topologies has been done using the Infineon IGBT switch model IKW50N60DTP with its anti-parallel diode, and the maintained ambient temperature value is 25° C. The efficiency is obtained by considering the input of 100 V with different load values. Figures 13(a) and 13(b) show the efficiency graph of 7L and 11L configurations for different output powers. It is observed that the maximum simulation efficiency when the topology performs 7L operation is 98.5% at 0.4 kW, whereas it is 96.74% for 11L operation. Further, Fig. 13(c) depicts the filled radar chart of loss distribution among semiconductor switches and diodes at 0.9 kW output power during 7L and 11L operations.

IV. COMPARISON WITH OTHER RECENT TOPOLOGIE

Recent topologies with 7L and 11L have been compared with the proposed topology to highlight their unique benefits. Table 9 shows that the 7L topologies are first compared, followed by a comparison of the 11L topologies.

The comparative assessment is performed using the key metrics such as components used (number of switches, drivers, diodes, capacitors, and inductors), voltage gain, maximum blocking voltage per unit ($MBV_{p.u.}$), total standing voltage per unit ($TSV_{p.u.}$/NL), different ratios $MBV_{p.u.}$/Gain, $TSV_{p.u.}/N_L$, T_C /N_L, T_C/Gain), variety of capacitors utilized, and efficiency. The following observations are made

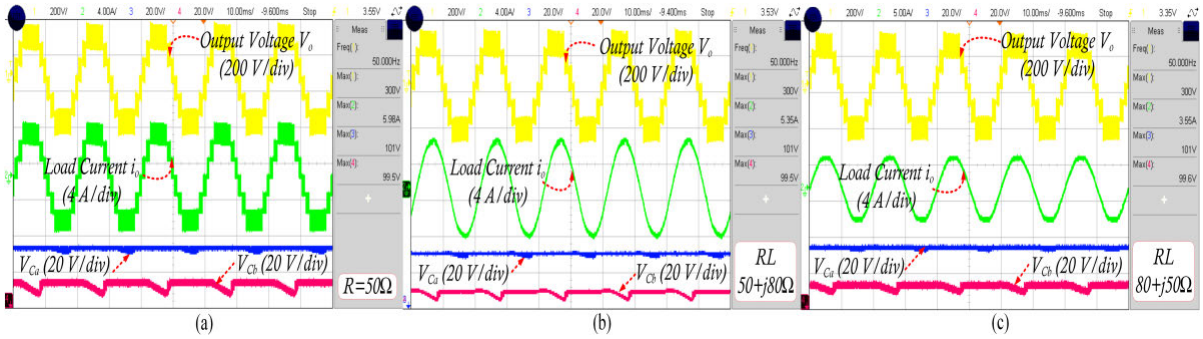


FIGURE 7. 7L operation, (a) R-Load (50 Ω), (b) R-L Load (50+j80) Ω, (c) R-L Load (80+j50) Ω.

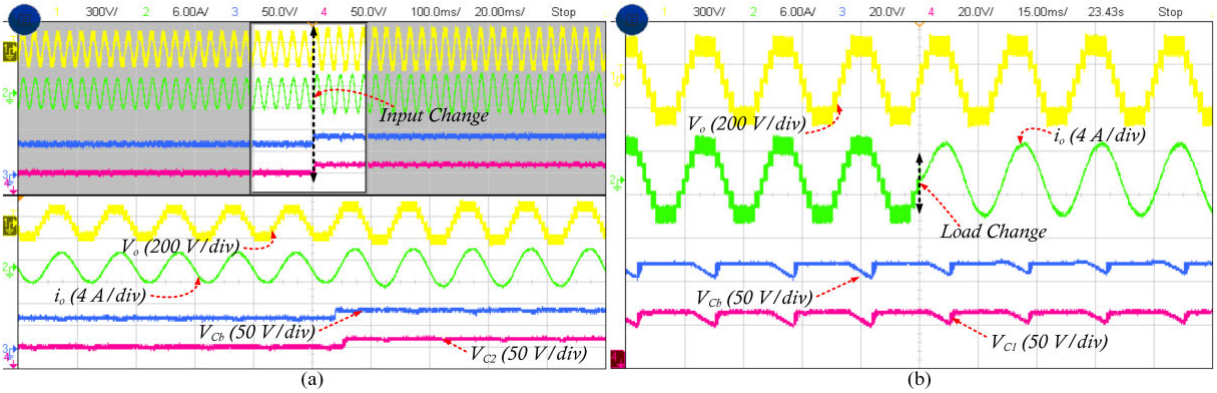


FIGURE 8. 7L operation, (a) Step change in input 80 V to 100 V, (b) Load change from R to R-L Load (50+j80) Ω.

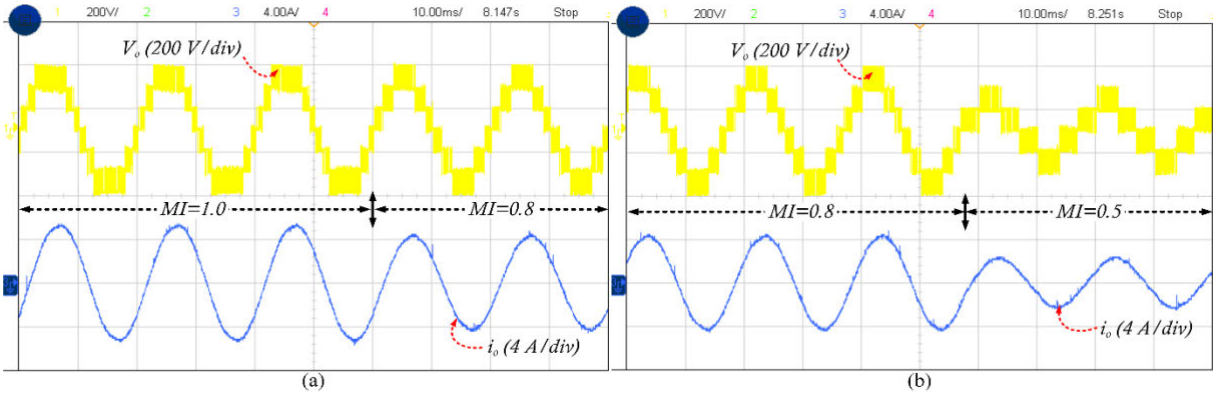


FIGURE 9. 7L operation, (a) Change in modulation index from 1 to 0.8, (d) Change in modulation index from 0.8 to 0.3.

while comparing the proposed topology with the topologies [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [30], [31], [32], [33] of Table 9. The proposed topology uses ten power switches, out of which two switches do not require anti-parallel diodes. It uses the third least number of components in the list. Though the topologies [11], and [13] use a smaller number of switches than the proposed topology, they can provide a voltage gain of 1.5, which is lower than the proposed topology. Even though the topology in [14] can provide a triple voltage boost like the proposed topology, the $MBV_{p.u.}$ of two of their switches is equal to the output voltage, i.e., $3V_{in}$. While the topologies [10], [12], and [31] use the same power component counts with two and one driver less than the proposed topology, they can boost the input voltage to 1.5 times. The topology proposed in [16] can boost the input voltage to three times using ten switches, but their $TSV_{p.u.}$ is higher than the proposed topology. Regarding $MBV_{p.u.}$, the proposed topology is second-least among the topologies under comparison. The $TSV_{p.u.}$ value for the proposed topology is lower than that of all other topologies

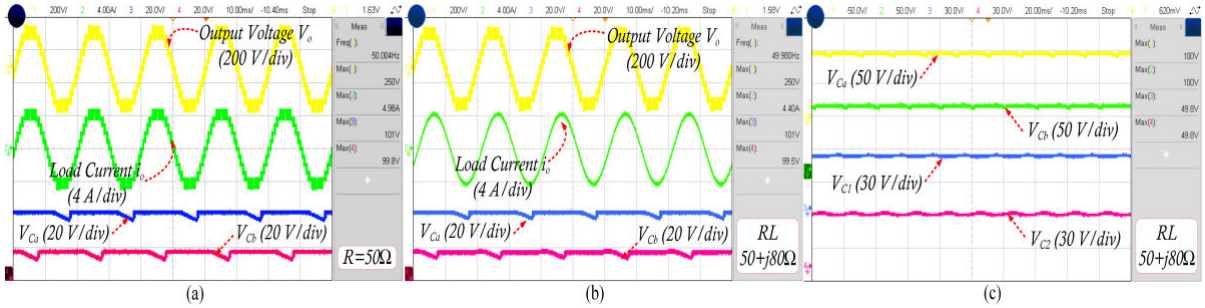


FIGURE 10. 11L operation, (a) R-Load (50 Ω), (b) R-L Load (50+j80) Ω, (c) Capacitor voltages V_{Ca}, V_{Cb}, V_{C1},and V_{C2}.

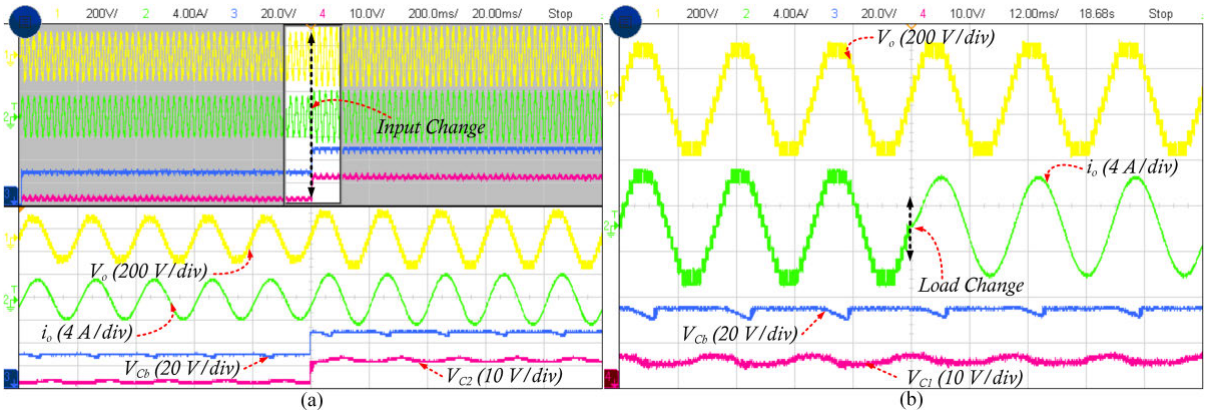


FIGURE 11. 11L operation, (a) Step change in input 80 V to 100 V, (b) Load change from R to R-L Load (50+j80) Ω.

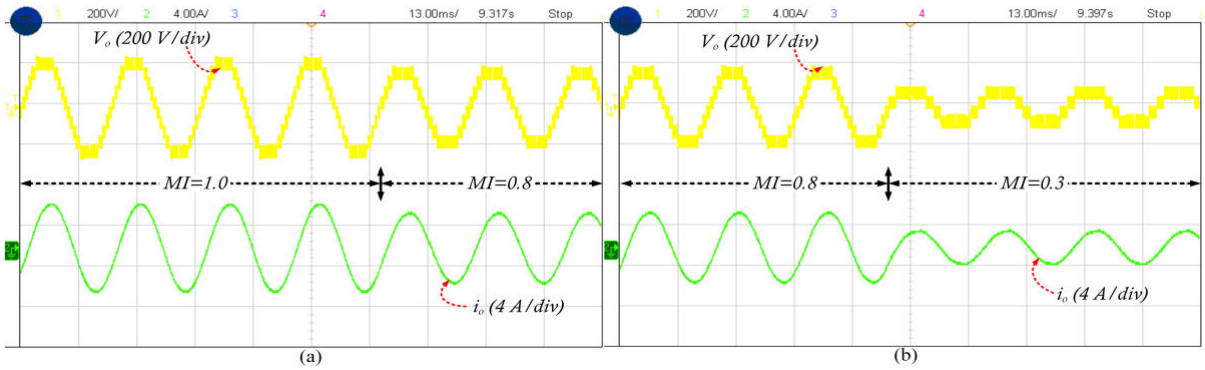


FIGURE 12. 11L operation, (a) Change in modulation index from 1 to 0.8, (d) Change in modulation index from 0.8 to 0.3.

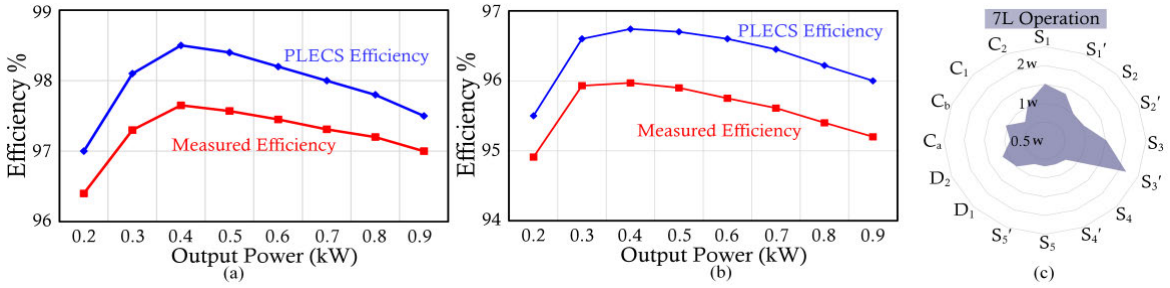


FIGURE 13. Simulation efficiency, (a) 7L operation, (d) 11L operation, (c) PLECS loss distribution during 7L operation with a voltage gain of 3.

except the one presented in [15], which stands at 4.3, slightly better than the 4.6 TSVp.u. value observed in the proposed topology. However, the $MBV_{p.u.}$of [15] is higher than the proposed topology. In Table 9, when considering the ratio

TABLE 9. Comparison with other similar topologies.

Ref	N_L	A	B	C	D	E	F	G	H	I	J	K	L	M					N
														C_1	C_2	C_3	C_4	C_5	
[10]	7L	1	10	8	0	2	0	1.5	1	5.3	0.67	0.8	14	$V_{in}/2$	$V_{in}/2$	V_{in}	-	-	NR
[11]		1	9	9	0	1	0	1.5	1	7	0.67	1	13.3	$V_{in}/2$	-	-	-	-	NR
[12]		1	10	9	0	3	0	1.5	1	5.7	0.67	0.8	15.3	$V_{in}/2$	$V_{in}/2$	V_{in}	-	-	96
[13]		1	8	7	2	4	0	1.5	1	4.7	0.67	0.7	14.7	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	-	97*
[14]		1	12	12	4	2	0	2	2	8	1	1.1	15.5	V_{in}	-	-	-	-	NR
[15]		1	9	9	2	3	0	3	3	4.3	1	0.6	8	V_{in}	V_{in}	V_{in}	-	-	89
[16]		1	10	8	1	2	0	3	3	6.7	1	0.9	7.3	V_{in}	V_{in}	-	-	-	96*
[17]		1	12	11	0	2	0	3	2	5.3	0.67	0.8	8.7	V_{in}	V_{in}	-	-	-	97
[18]		1	14	14	0	2	0	3	2	5.3	0.67	0.8	10.3	V_{in}	V_{in}	-	-	-	92.5
[19]		1	16	10	0	3	0	3	3	16	1	2.3	10	$V_{in}/2$	$V_{in}/2$	V_{in}	-	-	NR
[30]		1	12	11	0	2	1	3	2	5.33	0.67	0.76	9	Vin	Vin	-	-	-	98.7*
[31]		1	10	8	0	2	0	1.5	1	8	0.67	1.14	14	Vin/2	Vin/2	-	-	-	97.6
[32]		1	11	11	3	3	1	3	2	5	0.67	0.71	10	Vin	Vin	Vin	-	-	98*
[33]		1	12	11	4	4	0	1.5	2	9.33	1.33	1.33	21.3	Vin/2	Vin/2	Vin/2	Vin/2	-	96.7
[P]		**1**	**10**	**10**	**2**	**4**	**0**	**3**	**2**	**4.6**	**0.67**	**0.66**	**9**	V_{in}	V_{in}	V_{in}	V_{in}	-	**97.2**
[20]	11L	1	12	7	0	2	0	1.25	2	6.5	1.6	0.6	17.6	$V_{in}/4$	$V_{in}/4$	-	-	-	97.6*
[25]		1	14	6	0	5	0	1	2	4	2	0.4	24	$V_{in}/5$	$V_{in}/5$	$.6V_{in}$	$.4V_{in}$	$.1V_{in}$	NR
[26]		1	11	10	0	2	0	1.25	1	6.2	0.8	0.6	19.2	$V_{in}/4$	$V_{in}/4$	-	-	-	96.4
[27]		2	11	11	0	1	0	1.25	4	5.3	3.2	0.5	20	V_{in}	-	-	-	-	95.2*
[28]		2	8	8	1	1	0	1.67	3	6	1.8	0.5	12	V_{in}	-	-	-	-	96.5*
[29]		1	14	12	2	3	0	2.5	2	6.4	0.8	0.6	12.8	$V_{in}/2$	$V_{in}/2$	V_{in}	-	-	96.75*
[34]		2	8	7	0	2	0	2.5	2.5	4.4	1	0.4	7.6	$V_{in}/2$	$V_{in}/2$	-	-	-	NR
[35]		2	10	9	2	2	0	1.67	1.67	6.2	1	0.56	14.9	V_{in}	V_{in}	-	-	-	96.2*
[P]		**1**	**10**	**10**	**2**	**4**	**0**	**2.5**	**2**	**4.4**	**0.8**	**0.4**	**10.8**	$V_{in}/2$	$V_{in}/2$	V_{in}	V_{in}	-	**96.5**

N_L: Number of Levels, **A:** Source Count, **B:** Switch Count, **C:** Driver Count, **D:** Diode Count, **E:** Capacitor Count, **F:** Inductor Count, **G:** Gain, **H:** $MBV_{p.u.}$, **I:** $TSV_{p.u.}$, **J:** $MBV_{p.u.}$/Gain, **K:** $TSV_{p.u.}/N_L$, **L:** T_C/Gain, **M:** Variety of Capacitors, **N:** Efficiency, **NR:** Not Reported, *: Simulation Efficiency.

$TSV_{p.u.}/N_L$, the proposed topology stands out as having the second lowest value among all the 7L topologies. Furthermore, when comparing the ratio of TC/Gain for the proposed topology, it shows a value of 9, which is slightly higher than the ratios in topologies [16] and [17], which have values of 7.3 and 8.7 respectively. The comparison of the proposed topology when it is operated in 11L mode is done using other recent 11L topologies [20], [25], [26], [27], [28], [29], [34], and [35] as listed in Table 9. Except for the topology [28] and [34], all other topologies use more power components to generate 11L output voltage than the proposed topology. However, the topology in [28] and [34] requires two DC sources to obtain 11L output voltage generation. While considering the boosting ability, the proposed topology and the one in [29] and [34] can boost the input voltage to 2.5 times. The topologies [20], [26], [27], [28], [29], and [35] have a boosting factor lower than the proposed topology. The $MBV_{p.u.}$ of the proposed topology is 2, which is slightly higher than 1.67 of topology [28] and [35], despite the fact that [28] relies on three DC sources and [35] needs two DC sources. The value of $TSV_{p.u.}$ of the proposed topology is 4.4, the second lowest value in Table 9. The topology in [25] has the lowest $TSV_{p.u.}$ value at the cost of a higher number of power switches. Regarding the ratio of T_C/Gain, the proposed topology has the minimum value when compared with all other topologies. In addition, several topologies that use switched capacitors to achieve voltage boost and more output voltage levels 5L [36] and [37], 7L [38], 9L [39], [40], [41], and 13L [42] and [43] have been proposed in recent years. However, each of these topologies has its own advantages, including the ability to boost voltage, a reduced number of devices, and a soft charging method to reduce the inrush current, among others. Compared to the proposed topology, however, the number of switches is high and the voltage boosting versus number of output voltage levels is low.

V. CONCLUSION

A high-step-up switched capacitor multilevel inverter has been proposed. Its capability to deliver 7L and 11L without modifying the circuit structure is analyzed. The aspects like the number of levels, component count, and total standing voltage are compared with the recent topologies. From the comparison, it is established that it is significantly better than the topologies presented in the literature with its reduced component count, voltage stress, current stress and higher number of levels. Regarding the capacitor rating, the topology presented can be operated in both modes without the need to change the capacitor rating. Further, it is observed that the components-to-gain ratio is very minimal when compared to the other topologies synthesizing the same number of levels. The simulation and experimental prototypes are tested under dynamic conditions like sudden load/modulation index, and it is found that the topology smoothly handles the transition between the states. On the basis of performance and suitability for three-phase systems (like CHB three phase

configuration), the proposed topologies are the best option for PV and fuel cell applications requiring high voltage boosting.

ACKNOWLEDGMENT

This research was supported by Princess Nourah bint Abdulrahman University and Researchers Supporting Project number (PNURSP2023R346), Princess Nourah bint Abdulrahman University, Riyadh, Saudi Arabia. The authors would also like to thank the SRM Institute of Science and Technology, India, and Artificial Intelligence Data Analytics Lab. (AIDA), CCCIS, Prince Sultan University, Riyadh, Saudi Arabia, for their support.

REFERENCES

[1] H. Alnuman, Md. R. Hussan, S. Islam, A. Sarwar, E. M. Ahmed, and A. Armghan, "A single-source switched-capacitor 13-level high gain inverter with lower switch stress," *IEEE Access*, vol. 11, pp. 38082–38093, 2023.

[2] J. Sathik, "A nine level ANPC boost type inverter topology with reduced component stress," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, early access, Jul. 14, 2023, doi: 10.1109/TCSII.2023.3305230.

[3] V. Anand, V. Singh, X. Guo, M. A. J. Sathik, Y. P. Siwakoti, S. Mekhilef, and F. Blaabjerg, "Seventeen level switched capacitor inverters with the capability of high voltage gain and low inrush current," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 4, pp. 1138–1150, Oct. 2023.

[4] H. R. Baker and H. L. Bannister, "Electric power converter," U.S. Patent 3 867 643 A. Feb. 18, 1975.

[5] V. Anand, V. Singh, and J. S. M. Ali, "Dual boost five-level switched-capacitor inverter with common ground," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 2, pp. 556–560, Feb. 2023.

[6] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A new nested neutral point-clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec. 2014.

[7] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 256–269, Jan. 2015.

[8] P. K. Pal, K. C. Jana, Y. P. Siwakoti, J. S. M. Ali, and F. Blaabjerg, "A switched-capacitor multilevel inverter with modified pulse-width modulation and active DC-link capacitor voltage balancing," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Jun. 14, 2023, doi: 10.1109/JESTPE.2023.3285690.

[9] M. Tayyab, A. Sarwar, F. I. Bakhsh, A. Al-Durra, and K. M. Siddiqui, "A single-source nine-level inverter with quadratic boost ability for renewable energy applications," *IET Renew. Power Gener.*, vol. 2022, pp. 1–10, Jul. 2022, doi: 10.1049/rpg2.12549.

[10] J. Liu, X. Zhu, and J. Zeng, "A seven-level inverter with self-balancing and low-voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 685–696, Mar. 2020.

[11] M. J. Sathik, K. Bhatnagar, N. Sandeep, and F. Blaabjerg, "An improved seven-level PUC inverter topology with voltage boosting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 1, pp. 127–131, Jan. 2020.

[12] M. J. Sathik, N. Sandeep, and F. Blaabjerg, "High gain active neutral point clamped seven-level self-voltage balancing inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 11, pp. 2567–2571, Nov. 2020.

[13] M. Jagabar Sathik, N. Sandeep, D. Almakhles, K. Bhatnagar, Y. Yang, and F. Blaabjerg, "Seven-level boosting active neutral point clamped inverter using cross-connected switched capacitor cells," *IET Power Electron.*, vol. 13, no. 9, pp. 1919–1924, Jul. 2020.

[14] M. D. Siddique, B. P. Reddy, A. Iqbal, and S. Mekhilef, "Reduced switch count-based n-level boost inverter topology for higher voltage gain," *IET Power Electron.*, vol. 13, no. 15, pp. 3505–3509, Nov. 2020.

[15] T. Roy, M. W. Tesfay, B. Nayak, and C. K. Panigrahi, "A 7-level switched capacitor multilevel inverter with reduced switches and voltage stresses," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 12, pp. 3587–3591, Dec. 2021.

[16] P. S. V. Kishore, N. Jayaram, S. Jakkula, Y. R. Sankar, J. Rajesh, and S. Halder, "A new reduced switch seven-level triple boost switched capacitor based inverter," *IEEE Access*, vol. 10, pp. 73931–73944, 2022.

[17] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, and F. Blaabjerg, "A new switched capacitor 7L inverter with triple voltage gain and low voltage stress," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1294–1298, Jul. 2020.

[18] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A single DC source cascaded seven-level inverter integrating switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7184–7194, Nov. 2016.

[19] S. R. Pulikanti, G. Konstantinou, and V. G. Agelidis, "Hybrid seven-level cascaded active neutral-point-clamped-based multilevel converter under SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4794–4804, Nov. 2013.

[20] M. Ali, M. Tariq, A. Sarwar, and B. Alamri, "A 13-, 11-, and 9-level boosted operation of a single-source asymmetrical inverter with hybrid PWM scheme," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12817–12828, Dec. 2022.

[21] P. Ponnusamy, S. Velliangiri, and J. S. M. Ali, "A hybrid switched capacitor multi-level inverter with high voltage gain and self-voltage balancing ability," *Electr. Power Compon. Syst.*, vol. 48, no. 8, pp. 755–768, Sep. 2020.

[22] P. Prem, J. Sathik, and V. Suresh, "A new generalized cross-connected switched capacitor multilevel inverter topology with the high gain output voltage for single phase solar PV unit," *J. Eng. Res.*, vol. 9, no. 4A, Dec. 2021.

[23] M. H. B. T. Rashid, "Power electronics handbook," in *Dedication*, 3rd ed. Boston, MA, USA: Butterworth-Heinemann, 2011, doi: 10.1016/B978-0-12-382036-5.00052-5.

[24] H. Wang, L. Kou, Y.-F. Liu, and P. C. Sen, "A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5146–5161, Jul. 2017.

[25] N. Panda, B. Das, A. Chakrabarti, P. R. Kasari, A. Bhattacharya, and D. Chatterjee, "A new grid interactive 11-level hybrid inverter topology for medium-voltage application," *IEEE Trans. Ind. Appl.*, vol. 57, no. 1, pp. 869–881, Jan. 2021.

[26] M. Ali, M. Tariq, R. K. Chakrabortty, M. J. Ryan, B. Alamri, and M. A. Bou-Rabee, "11-level operation with voltage-balance control of WE-type inverter using conventional and DE-SHE techniques," *IEEE Access*, vol. 9, pp. 64317–64330, 2021.

[27] M. Rawa, M. D. Siddique, S. Mekhilef, N. Mohamed Shah, H. Bassi, M. Seyedmahmoudian, B. Horan, and A. Stojcevski, "Dual input switched-capacitor-based single-phase hybrid boost multilevel inverter topology with reduced number of components," *IET Power Electron.*, vol. 13, no. 4, pp. 881–891, Jan. 2020.

[28] M. D. Siddique, M. Wasiq, A. Iqbal, S. Mekhilef, A. Wahyudie, and M. Rawa, "11 level boost inverter topology with dual-source configuration," *IET Power Electron.*, vol. 16, pp. 1696–1702, May 2022.

[29] M. R. Hussan, A. Sarwar, I. Khan, M. Tariq, M. Tayyab, and W. Alhosaini, "An eleven-level switched-capacitor inverter with boosting capability," *Electronics*, vol. 10, no. 18, p. 2262, Sep. 2021.

[30] A. K. Singh, R. K. Mandal, and R. Anand, "Quasi-resonant switched-capacitor-based seven-level inverter with reduced capacitor spike current," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 1953–1965, Apr. 2023.

[31] J. Zhao, Y. Chen, J. Zeng, and J. Liu, "Low-voltage stress seven-level inverter based on symmetrical capacitors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 3, pp. 3033–3044, Jun. 2022.

[32] N. P. Gopinath, K. Vijayakumar, J. S. M. Ali, K. Raghupathi, and S. Selvam, "A triple boost seven-level common ground transformerless inverter topology for grid-connected photovoltaic applications," *Energies*, vol. 16, no. 8, p. 3428, Apr. 2023.

[33] S. Kakar, M. S. B. Arif, S. M. Ayob, N. B. M. Nordin, S. Mekhilef, M. Seyedmahmoudian, and A. Stojcevski, "An improved seven-level switched-capacitor-based neutral-point clamped inverter," *Frontiers Energy Res.*, vol. 10, Aug. 2022, Art. no. 957825.

[34] S. Ahmad, M. Tariq, and V. Verma, "Asymmetrical eleven-level multilevel inverter with low switching count and voltage stress," in *Proc. IEEE 3rd Int. Conf. Sustain. Energy Future Electr. Transp. (SEFET)*, Bhubaneswar, India, Aug. 2023, pp. 1–6.

[35] D. Singh and N. Sandeep, "Switched-capacitor-based multi-source multilevel inverter with reduced part count," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 3, pp. 718–724, Jul. 2023.
[36] S. Negi, V. Singh, and V. Anand, "Design and analysis of reduced switch single-stage single-phase common ground type five-level photovoltaics transformerless inverter," *Iranian J. Sci. Technol., Trans. Electr. Eng.*, vol. 46, no. 4, pp. 1111–1127, Jul. 2022.
[37] A. Jakhar and N. Sandeep, "Five-level common-ground-type boosting inverter with lesser capacitor-stored energy," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15121–15125, Dec. 2023, doi: 10.1109/TPEL.2023.3314896.
[38] S. Kumari, N. Sandeep, and A. K. Verma, "T-type seven-level inverter with triple voltage-boosting gain," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 3, pp. 899–906, Jul. 2023.
[39] D. Singh and N. Sandeep, "A novel common-ground multisource inverter," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15142–15146, Dec. 2023, doi: 10.1109/tpel.2023.3316668.
[40] A. Jakhar, N. Sandeep, and A. K. Verma, "A nine-level common-ground-type boost inverter for PV applications," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, early access, Aug. 21, 2023, doi: 10.1109/JESTIE.2023.3307000.
[41] S. Kumari and N. Sandeep, "A self-balancing switched-capacitor-based dual boosting nine-level inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 5, pp. 5311–5320, Oct. 2023.
[42] V. Anand and V. Singh, "A 13-level switched-capacitor multilevel inverter with single DC source," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 1575–1586, Apr. 2022.
[43] S. S. Neti, V. Anand, and V. Singh, "Single-phase generalized switched-capacitor multilevel inverter using reduced number of power semiconductor components with voltage boosting ability," *Arabian J. Sci. Eng.*, vol. 47, no. 3, pp. 2613–2627, Mar. 2022.

JAGABAR SATHIK MOHAMED ALI (Senior Member, IEEE) received the B.Eng. degree in electronics and communication engineering from Madurai Kamaraj University, Madurai, India, in 2002, and the M.Eng. and Ph.D. degrees from the Faculty of Electrical Engineering, Anna University, Chennai, India, in 2004 and 2016, respectively. He was a consultant for various power electronics companies for the design of power electronics converters. He is currently an Associate Professor with the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai. He has authored more than 60 articles and publications in international refereed journals and conference proceedings. His current research interests include multilevel inverters, grid-connected inverters, and power electronics converters and their applications to renewable energy systems. He received the certificate of recognition from the IEEE Madras Section for the paper published, from 2019 to 2021.

AMJAD REHMAN KHAN (Senior Member, IEEE) received the Ph.D. degree in information security using image processing techniques from the Faculty of Computing, University Teknologi Malaysia (UTM), Malaysia, in 2010. He is currently an Associate Professor with the College of Computer and Information Sciences (CCIS), Prince Sultan University, Riyadh, Saudi Arabia. He is a PI in several projects and completed projects funded by MOHE, Malaysia, and Saudi Arabia. His research interests include bioinformatics, the IoT, information security, and pattern recognition. He received the Rector Award for the 2010 Best Student from UTM Malaysia.

GOPINATH NARAYANAN PANDURANGAN was born in Tiruchirappalli, India. He received the B.E. degree in electrical and electronics engineering from the Noorul Islam College of Engineering, Anna University, India, in 2009, and the M.Tech. degree in power electronics and drives from SRM University, India, in 2013, where he is currently pursuing the Ph.D. degree in electrical and electronics engineering with the Faculty of Electrical and Electronics Engineering, SRM Institute of Science and Technology (SRMIST). His main research interests include the design and control of power electronic converters, multilevel voltage source inverters, and photovoltaic transformerless inverters.

PREM PONNUSAMY received the B.E., M.E., and Ph.D. degrees from the Faculty of Electrical Engineering, Anna University, Chennai, in 2006, 2008, and 2018, respectively. He is currently an Associate Professor with the Department of Electrical Engineering, St. Thomas' College of Engineering and Technology, Kolkata. His research interests include power systems and power converters for renewable energy stems.

FATEN S. ALAMRI received the Ph.D. degree in system modeling and analysis in statistics from Virginia Commonwealth University, Richmond, VA, USA, in 2020. Her Ph.D. research included Bayesian dose-response modeling, experimental design, and nonparametric modeling. She is currently an Assistant Professor with the Department of Mathematical Sciences, College of Science, Princess Nourah bint Abdul Rahman University. Her research interests include spatial areas, environmental statistics, and brain imaging.

SAEED ALI BAHAJ received the Ph.D. degree from Pune University, India, in 2006. He is currently an Associate Professor with the Department of Computer Engineering, Hadhramout University, and the Department of Management Information Systems, COBA, Prince Sattam bin Abdulaziz University, Saudi Arabia. His main research interests include information management, forecasting, information engineering, and information security.