IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 14 October 2023, accepted 10 November 2023, date of publication 15 November 2023,
date of current version 29 November 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3332920

RESEARCH ARTICLE

A Seven Level Fault Tolerant Switched Capacitor Boost Inverter With a Single DC Source

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This work was supported by the Princess Nourah bint Abdulrahman University Researchers Supporting Project, Princess Nourah bint Abdulrahman University, Riyadh, Saudi Arabia, under Grant PNURSP2023R79.

ABSTRACT A Fault-Tolerant Multi-Level Inverter (FT-MLI) is essential to ensure power supply continuity for crucial applications. At the same time, the cost and efficiency of MLI is also important for its successful use in the commercial market. The existing seven level FT-MLI topologies demand more than one input DC source, which increases the cost function. This article proposes a single DC source seven level FT-MLI topology with minimum number of switches (IGBT) to reduce the cost function. The proposed FT-MLI topology generates seven level output voltage with 1.5 times voltage boosting. In case of open or short circuit fault on any single or multi switch, the topology continues to operate with five level output voltage using reserved switches. It consists of eight active switches, two diodes, two capacitors, six thermal fuses, and three reserved switches. In comparison to the existing seven level fault tolerant (open circuit and short circuit fault) topologies, the suggested structure requires minimum number of component count. The efficiency and power losses of the proposed structure are analyzed theoretically. The proposed topology has an efficiency of 96 % at an output power of 600 W under healthy condition and 97% at an output power of 272 W under post fault condition. The level shift pulse width modulation approach is used to generate required triggering pulse for the switch during pre-fault and post-fault. The proposed topology is simulated in the MATLAB/Simulink platform and experimentally verified using dSPACE 1104. The response of the output voltage and current during the transition from pre-fault to post-post fault for each switch fault are presented.

INDEX TERMS Fault tolerant multi level inverter (FT-MLI), switched-capacitor multi-level inverter (SC-MLI), open circuit fault (OCF), short circuit fault (SCF).

I. INTRODUCTION

Power electronic equipments play an important role in today's Power conversion system due to increasing interconnectivity and intelligent automation. Power electronic devices are the medium between the processor and real time application. The demand for multi-functional power electronic converters with robust operation is increasing in telecommunication system (power and signal transmission), renewable energy grid interconnection, electric vehicles, biomedical equipment, military, electric aircraft [1], and smart home applications, among other applications.

A. MOTIVATION AND INCITEMENT

The basic two level inverter gives a quasi-square wave output, that consists of lower-and higher-order harmonics. By applying the Pulse Width Modulation (PWM) technique to the conventional two level inverter, the lower order harmonics at the output voltage can be reduced. However, the switching frequency of modulation for the basic two level inverter is in the order of kHz or MHz. Due to this reason, the electromagnetic interference, dV/dt, and switching loss are higher. In case of medium and high power applications, the current

The associate editor coordinating the review of this manuscript and approving it for publication was N. Prabaharan.

carried by the switch is high. So turning ON and OFF of the switch with a high switching frequency results in huge switching losses and heat generation. Therefore, conventional two level inverters with adapted high switching PWM techniques can be preferred only for low power applications but not for medium and high power applications. As well, the conventional two level inverter is not preferred for critical applications (example: electric aircraft, biomedical, etc.) due to huge electromagnetic interference.

Multi-Level Inverters (MLIs) are a preferable choice for medium and high power applications. In MLI, the small voltage sources are combined in series to get a large voltage, with an increasing number of levels such that the output voltage waveform is nearer to sinusoidal. As a result, the power quality will be improved in MLI with lower switching frequency, $\frac{dV}{dt}$ variations, and electromagnetic interference. However, the main drawback of conventional MLI's are its component count. It requires more number of DC sources, switches, diodes, and capacitors based on its structure.

The Single DC Source (SDCS) conventional MLI's are widely used for motor drives, Flexible AC transmission system, and electric vehicle [2], [3], [4], etc. It has the disadvantage of capacitor voltage unbalancing problem, less fault tolerant capacity, and greater requirement of component count. The multi DC source MLI has better fault tolerant capability in comparison to the SDCS-MLI. However, it requires more number of DC sources, which is not convenient for most of the drive applications. In the recent years, researchers have presented many Reduced Device Count MLI (RDC-MLI) topologies. The presented topologies in [5], [6], and [7] are able to generate higher number of voltage levels with reduced component count. However, it losses reliability by loosing the redundancy of switching states for each voltage level. The RDC-MLI's are unable to provide continuity of power supply, if any switch fault occurs. The continuity of power supply is essential for the critical applications, otherwise it leads to an immeasurable economic and life loss. A Fault Tolerant Multi Level Inverter (FT-MLI) with optimal device count is required to ensure the continuity of power supply, low initial cost and higher efficiency [8], [9], [10].

B. LITERATURE REVIEW

SDCS seven-level RDC-MLIs are presented in [11], [12], and [13]. But, these topologies are unable to boost the output voltage. SDCS seven-level RDC-switched capacitor MLI topologies presented in [14] and [15] with voltage boosting capabilty. However, the switched capacitors are not self-balanced. It requires additional voltage sensor to balance the capacitor voltage. SDCS seven-level RDC self-balanced switched capacitor boost MLI's are presented in [16], [17], [18], and [19]. However, the redundancy states in these topologies are almost zero. If any switch fault occurs, inverter will shutdown completely.

The majority of faults in MLI are caused by Open Circuit Fault (OCF) and Short Circuit Fault (SCF) in semiconductor switches. The recently presented single phase FT-MLI topologies are reviwed in [20]. The seven level FT-MLI's are presented in [21], [22], [23], [24], [25], [26], [27], and [28]. The topology presented [21], [22], [23], [24], [25] can provide continuity of power supply with reduced voltage levels in the post fault condition. However, it works only for OCF not for SCF. The topology presented in [26], [27], and [28] can continue to give seven level output voltage in the post fault condition for OCF and SCF. The topologies presented in [21] and [22] requires two DC sources and the topologies mentioned in [23], [24], [25], [26], [27], and [28] requires three DC sources. But, most of the drive applications use SDCS MLI. The SDCS switched capacitor FT-MLI topologies are investigated in [29] and [30]. The topology presented in [29] and [30] are for fifteen level and twenty six level respectively. For higher voltage levels, the device count has become huge. Most of the commercial applications are prefered for five level and sevel level only [6]. A fault tolerant five level flying capacitor MLI is presented in [31] by using extra bidirectional switches to bypass the fault. Similarly a FT three level neutral point clamped MLI is presented in [32] by using resonant legs to handle the fault. But, it requires more number of switches than the conventional MLI. In order to address these problems a novel optimal device count SDCS FT switched capacitor MLI is introduced in this article for providing continuity of power supply even if any OCF or SCF occurs in the semiconductor switch.

The primary issue with SCMLI is its impulse charging current. The switches present in the capacitor charging loop damages, if the surge current exceeds the limit. The impulse current of the capacitor depends on its voltage deterioration. That capacitor draws a very high impulse current, if the voltage reduction is large. For the topologies labelled in [16], [17], [18], [33], [34], [35], and [36], the capacitor discharges at consecutive output voltage values. As a results the capacitor voltage degradation becomes large.

Seven level FT-MLI topologies presented in the literature require more than one DC source. The existing SDCS seven level switched capacitors inverters are not FT-MLI topologies. Therefore, this article proposes a single DC source seven level switched capacitor FT-MLI topology with minimum number of switches.

C. CONTRIBUTION AND PAPER ORGANIZATION

The following are the key features of the proposed topology.

- The proposed FT-MLI requires only single DC source.
- To obtain the seven level output voltage with 1.5 voltage gain, only 8 switches and two diodes are required.
- Three reserved switches are used in addition to the healthy switches to provide continuity of power supply for any OCF and SCF in the semiconductor switch.
- Proposed topology gives five level output voltage under post fault for single and multiple switch fault.
- Only six thermal fuses are used to convert the SCF into an OCF.
- At each voltage level, only three switches are in conduction to carry the load current.

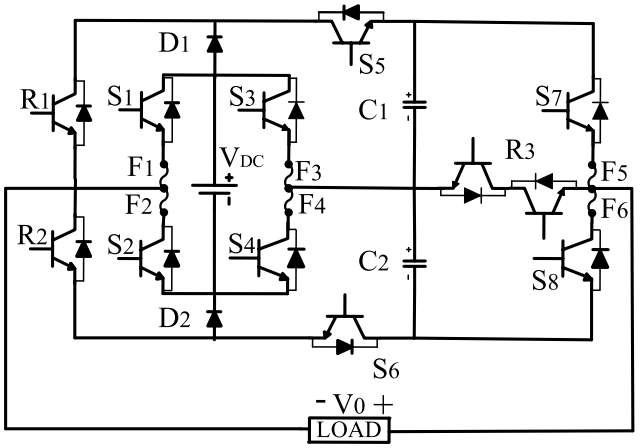

FIGURE 1. Proposed Single DC source 7-Level FT – SCMLI.

TABLE 1. Redundancy for each voltage level.

VOLTAGE LEVEL	SWITCHING REDUNDANCY	TURN ON SWITCHES	STATE OF CAPACITOR	
			C_1	C_2
$0V_{DC}$	Z_{01}	S_1,S_5,S_6,S_7	C	C
	Z_{02}	S_2,S_5,S_6,S_8	C	C
	Z_{03}	S_1,S_3,R_3	NC	NC
	Z_{04}	S_2,S_4,R_3	NC	NC
	Z_{05}	R_1,S_5,S_7	NC	NC
	Z_{06}	R_1,S_5,S_6,S_7	C	C
	Z_{07}	R_2,S_6,S_8	NC	NC
	Z_{08}	R_2,S_5,S_6,S_8	C	C
$+0.5V_{DC}$	P_{11}	S_2,S_4,S_7	D	NC
	P_{12}	S_1,S_3,S_7	D	NC
	P_{13}	R_2,S_6,R_3	NC	D
	P_{14}	R_2,S_6,R_3,S_5	C	C
	P_{15}	S_2,S_3,S_8	NC	C*
$-0.5V_{DC}$	N_{11}	R_1,S_5,R_3	D	NC
	N_{12}	R_1,S_5,S_6,R_3	C	C
	N_{13}	S_1,S_3,S_8	NC	D
	N_{14}	S_2,S_4,S_8	NC	D
	N_{15}	S_1,S_4,S_7	C*	NC
$+V_{DC}$	P_{21}	S_2,S_5,S_6,S_7	C	C
	P_{22}	S_2,S_3,R_3	NC	NC
	P_{23}	S_6,S_7,R_2	D	D
	P_{24}	S_5,S_6,S_7,R_2	C	C
$-V_{DC}$	N_{21}	S_1,S_5,S_6,S_8	C	C
	N_{22}	S_1,S_4,R_3	NC	NC
	N_{23}	R_1,S_5,S_8	D	D
	N_{24}	R_1,S_5,S_6,S_8	C	C
$+1.5V_{DC}$	P_{31}	S_2,S_3,S_7	D	NC
$-1.5V_{DC}$	N_{31}	S_1,S_4,S_8	NC	D

- The proposed topology keeps the capacitor voltage almost constant even for high power loads, which is not possible with similar kind of existing topologies.
- The cost function of proposed FT-MLI is less than the existing similar topologies.

The following is how the paper is organized. Segment II introduces the proposed topology, segment III presents power losses and efficiency, segment IV presents experimental and real time simulation results, segment V presents comparative analysis, segment VI concludes the paper.

II. PROPOSED 7-LEVEL SCMLI

A. PROPOSED TOPOLOGY DESCRIPTION

The proposed single DC source 7-Level FT-SCMLI with a voltage gain of 1.5 is shown in Fig.1. It consists of eight healthy switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8), two diodes, two capacitors, six thermal fuses, and three reserve switches (R_1, R_2, and R_3). The two self-balanced capacitors (C_1 and C_2) are charged to $0.5V_{DC}$ by using an input DC source (V_{DC}), through the switches S_5, S_6, D_1, and D_2. The Switches S_1:S_2, S_3:S_4, and S_7:S_8 are switched in a complementary manner, to protect IGBT leg from shoot-through fault.

Four switches (S_1, S_2, S_3, S_4) have Maximum Blocking Voltage (MBV) of V_{DC}, the five switches (S_5, S_6, S_7, S_8, and R_3(bidirectional switch)) have MBV of $0.5V_{DC}$, and the two switches (R_1, R_2) have MBV of $1.5V_{DC}$. Therefore, the summation of voltage stress acros each switch (Total Standing Voltage (TSV)) is shown in (1)

$$TSV = 8V_{DC} + 6\,(0.5V_{DC}) = 11V_{DC} \tag{1}$$

The current stress of switches S_1, S_2, S_3, S_4, S_7, S_8, R_1, R_2, and R_3 is equal to load current. The current stress of switches S_5 and S_6 is equal to load current plus capacitor charging current. At each voltage level, only three switches are in conduction to carry the load current. The possible switching redundancy for each voltage level are mentioned in the Table-1. Except the $\pm 1.5V_{DC}$ state, all the remaining states are having redundant states to tolerate the fault in any switch. Here, Z_O is zero voltage level, P_1 is the positive $0.5V_{DC}$ level, P_2 is the positive V_{DC} level, P_3 is the positive $1.5V_{DC}$ level, N_1 is the negative $0.5V_{DC}$ level, N_2 is the negative V_{DC} level, N_3 is the negative $1.5V_{DC}$ level, C indicates capacitor charges with the source voltage, C$*$ indicates capacitor charges through the load, D indicates capacitor discharge, and NC means no change.

The proposed topology can generate seven level output voltage under healthy condition. If any OCF or SCF occurs in single or multi switch, the proposed topology operates with a five level output voltage. A thermal fuse is used in series with the IGBT leg as shown in Fig.1 to convert the SCF into an OCF. Thermal fuse is designed in such a way that it isolate the IGBT from the circuit, after crossing prescribed current limit. The proposed topology becomes FT against SCF in each switch with the help of thermal fuses.

In most of the FT topologies the switching pattern is different for each switch fault. In the proposed topology, the control approach is made easier by allocating a set of switching patterns for a group switch faults shown in Table 2. Group-I switching pattern is to generate 7 level output voltage during healthy condition and no reserve switches are in operation. Group-II switching pattern will generate 5–level output voltage, when OCF occur on S_1 or S_2 or S_3 or S_4 or (S_1 and S_2) or (S_3 and S_4) or (S_1, S_2, S_3, and S_4), or SCF occur in S_1 or S_2 or S_3 or S_4 or S_5 or S_6 or (S_1 and S_2) or (S_3 and S_4) or (S_5 and S_6) or (S_1, S_2, S_3, and S_4).

TABLE 2. Possible switching combination during pre fault and post fault condition (single and multi switch fault).

FAULT STATUS	NUMBER OF OUTPUT LEVELS	GROUP	VOLTAGE LEVELS						
			$+1.5V_{DC}$	$+V_{DC}$	$+0.5V_{DC}$	0	$0.5V_{DC}$	$-V_{DC}$	$-1.5V_{DC}$
Healthy condition	7-Level	I	P_{31}	P_{21}	N_{13}	Z_{01}	P_{12}	N_{21}	N_{31}
Open or Short circuit fault in S_1/ S_2/ S_3/ S_4/ S_1,S_2/ S_3,S_4/ and S_1,S_2,S_3,S_4.	5-Level	II	X	P_{24}	P_{14}	Z_{06}	N_{12}	N_{24}	X
Short circuit fault in S_5/ S_6/ S_5,S_6.									
Open circuit fault in S_5/ S_6/ S_5,S_6.	5-Level	III	X	P_{22}	P_{15}	Z_{03}	N_{13}	N_{22}	X
Open or Short circuit fault in S_7/ S_8/ S_7,S_8.	5-Level	IV	X	P_{22}	P_{14}	Z_{03}	N_{12}	N_{22}	X

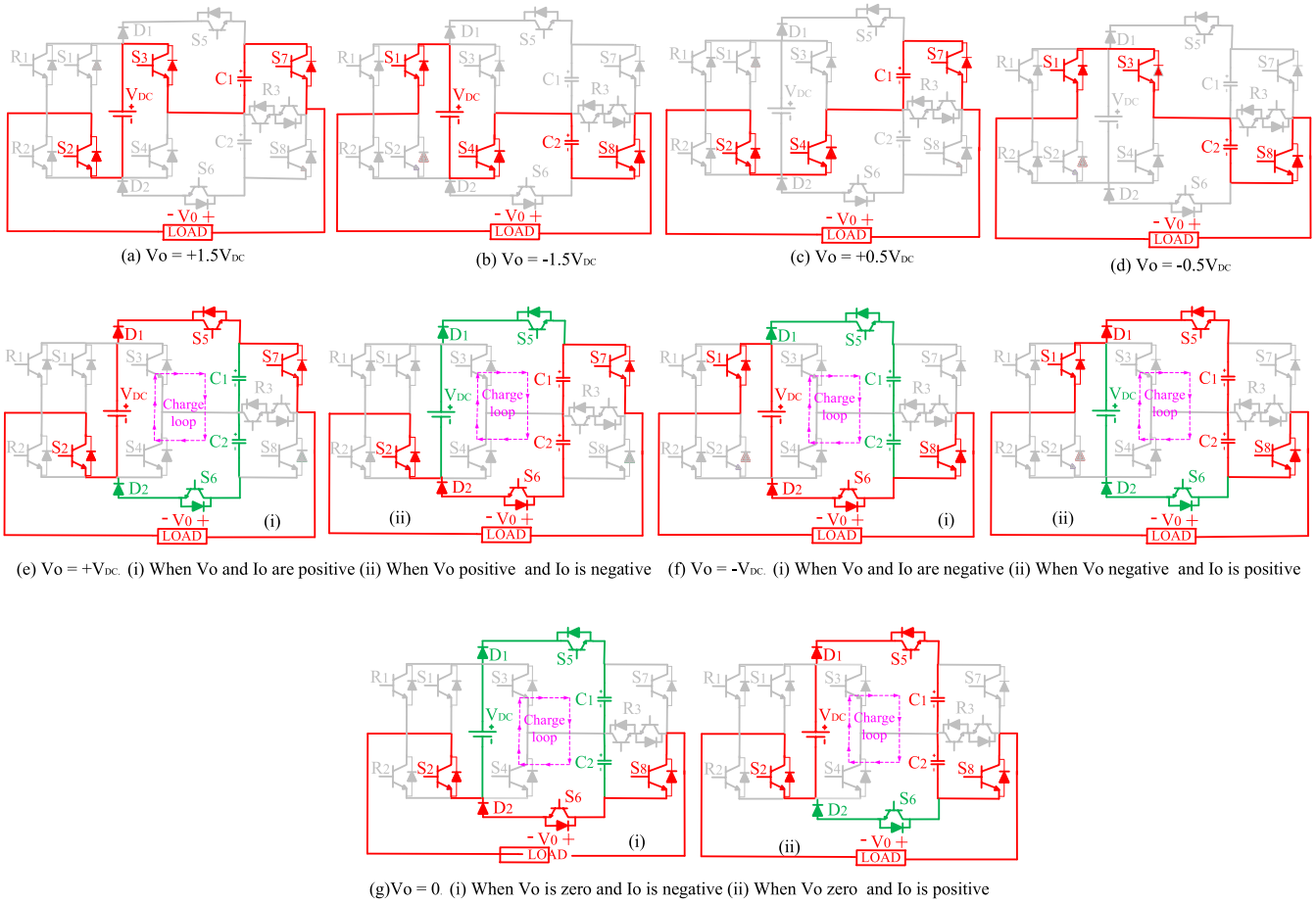

FIGURE 2. The current paths of proposed topology in each voltage level during healthy condition (Group-I).

Group-III switching pattern will generate 5–level output voltage, when OCF occur in S_5 or S_6 or (S_5 and S_6).

Group-IV switching pattern will generate 5-level output voltage, when OCF occur in S_7 or S_8 or (S_7 and S_8). or SCF occur in S_7 or S_8 or (S_7 and S_8). Fig.2 displays the current paths at each voltage level under healthy conditions (Group-I). Similar to this, Group-II, Group-III, and Group-IV for 5-level operation can also be drawn in accordance with the Table-2 switching arrangement. For identifying the fault and detection of faulty switch, researchers are introduced many techniques in the literature [37]. This paper basically provides a solution for the post fault operation. The flow chart shown in Fig.3 gives an implementation of control algorithm during healthy and post fault conditions.

B. SELF-BALANCED CAPACITORS AND THEIR CAPACITANCE CALCULATION

Self-balancing of capacitor is an important feature of SCMLI. In the proposed 7 level SCMLI topology the charging time of each capacitor is independent of load current in the healthy state, since the capacitors are charged by the source voltage. So, the charging time of each capacitor is less than the period of output voltage level. However, the capacitor discharges through the load from its nominal voltage

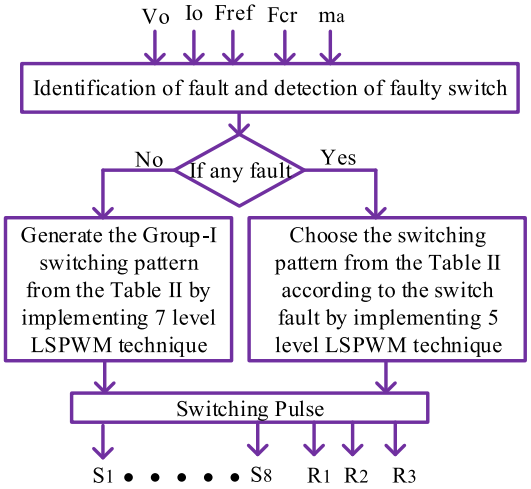

FIGURE 3. Flowchart for selecting the switching pattern based on the fault condition.

until the succeeding charging state. The two capacitors are charged to $0.5V_{DC}$ during the states of ± 0, and $\pm V_{DC}$. The capacitor C_1 discharges during the states of $+0.5V_{DC}$, and $+1.5V_{DC}$. Similarly, capacitor C_2 discharges during the states of $-0.5V_{DC}$, and $-1.5V_{DC}$. Therefore, the capacitors C_1 and C_2 are self-balanced to keep the constant voltage across it, irrespective of output load parameter values. the maximum discharge of the C_1 and C_2 are during the state of $+1.5V_{DC}$ and $-1.5V_{DC}$ respectively. The maximum discharge amount of capacitors C_1 is during the period from θ_3 to π-θ_3 ($+1.5V_{DC}$ level). Similarly, C_2 is during the period from $\pi + \theta_3$ to 2π-θ_3 ($+1.5V_{DC}$ level). So, the maximum discharge amount of capacitors C_1 and C_2 is calculated as follows.

$$\Delta Q_{C1} = \Delta Q_{C2} = \frac{1}{2\pi f} \int_{\theta_3}^{\pi-\theta_3} I_o\,(wt)\,dwt \tag{2}$$

where f is the frequency of output voltage. From the (2) the maximum change in voltage is calculated as follows.

$$\Delta V_{C1} = \Delta V_{C2} = \frac{1}{2\pi f \times C} \int_{\theta_3}^{\pi-\theta_3} I_o(wt)dwt \tag{3}$$

By considering the voltage ripple (ΔV_{cr}) of each capacitor as 10% of the input DC source voltage. The capacitance value of each capacitor is as follows. Where I_o is the the inverter output current and ΔV_{cr} is the ripple voltage of capacitor.

$$C_1 = C_2 = \frac{1}{2\pi f \times 0.1V_{DC}} \int_{\theta_3}^{\pi-\theta_3} I_o(wt)dwt \tag{4}$$

C. PRE CHARGE PROCEDURE AND CHARGE CURRENT

The capacitor's voltage will drop below the desired amount if it is left idle for an extended length of time. Therefore, the capacitor must be pre-charged before the converter operates. The precharge circuit can be difficult in some SCMLI designs, if various capacitors must charge at different voltage levels. The pre charge procedure of proposed SCMLI is easy [38]. Initially, the switches S_5 and S_6 must be turned ON. The series-attached capacitors C_1 and C_2 are connected to the DC source as shown in Fig. 4. The pre charge resistor control the peak of charging current in pre charge operation. The charge resistor is bypassable using the contactor after a set period of time.

The charging current is one of the important specification in SCMLI topology. If the charging current is not with in the limit, it may damage the switches. The average discharge current is equal to the average charge current in the self balanced capacitor. The capacitor charge current is shown in equation (5).

$$I_{ch} = I_{disch} = 2 * f_0 \left\{ \int_{\theta_{\frac{0.5}{w}}}^{\theta_{\frac{1}{w}}} i_o\,(wt) \right\} + f_o \left\{ \int_{\theta_{\frac{1.5}{w}}}^{\pi-\theta_{\frac{1.5}{w}}} i_o\,(wt) \right\} \tag{5}$$

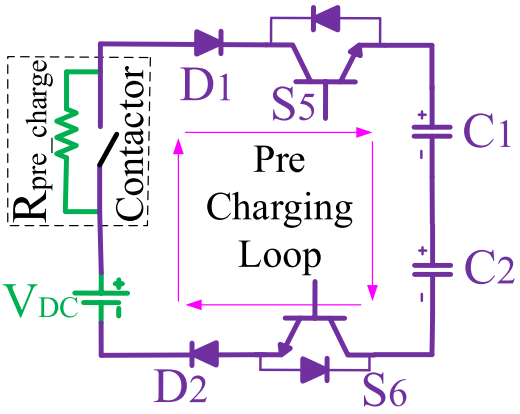

FIGURE 4. Capacitor Pre charging operation.

D. MODULATION STRATEGY

The required gate pulse to the IGBT is generated using the Level Shift Pulse Width Modulation (LSPWM) technique [39]. In this approach, the modulating or reference signal 'V_{ref}' (Sinusoidal) is compared with the carrier signals 'V_c' (Triangular) shown in Fig.5. All the triangular waveforms have the same peak to peak voltage, but their positions are level displaced shown in Fig.5. The logic diagram is implemented to generate required switching pattern based on the selection of switching group from Table-2 shown in Fig.6. The modulation Index (m_i) value is changed according to the variation in the reference signal shown in (6). Where $V_{Max\_carrier}$ is the peak of carrier wave and V_{Max_ref} is the peak of reference waveform. The output voltage will be controlled based on the m_i value. The output voltage levels will be seven only if the m_i value is in between 0.66 to 1.

$$m_i = \frac{V_{Max_{ref}}}{3 * V_{Max_{carrier}}} \tag{6}$$

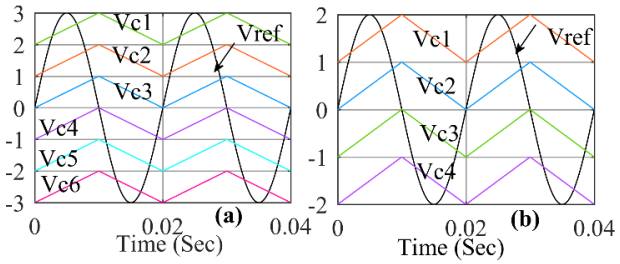

FIGURE 5. LSPWM for (a) 7 level (Group-I) (b) 5 level (Group-II/III/IV).

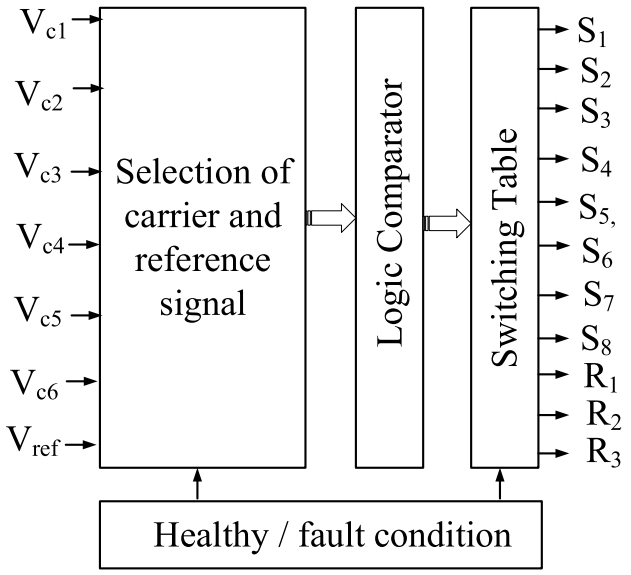

FIGURE 6. LSPWM logic diagram to generate switching pulse in healthy condition.

III. POWER LOSS AND EFFICIENCY

The conduction loss (P_C), switching loss (P_S), and capacitor loss (P_{CA}) are three basic losses in SCMLI. P_S occurs when the switch is switched from ON to OFF or vice versa. P_C occurs during the ON state of the switch. Similarly, P_{CA} occurs due to the capacitor's Equvialent Series Resistance (ESR) and ripple voltage. The conduction, switching, and capacitor losses of the proposed single DC source seven level FT-SCMLI are given in the following sub sections.

A. CONDUCTION LOSS (P_C)

The conduction losses mainly depend on the on state resistance of the switch and diode. It is indicated as R_S and R_D respectively. Each switch's conduction loss is computed using equation (7) [40]. Where $I_{C\_avg}, I^2_{C\_RMS}, and, I_{d\_avg}, I^2_{d\_RMS}$ are the average and RMS currents through the switch and diode, respectively. Similarly, V_s, V_D are the ON state voltages across the switch and diode, respectively.

$$P_{C,S} = \left\{V_S * I_{C_{avg}} + R_S * I^2_{C_{RMS}}\right\} + \left\{V_D * I_{d_{avg}} + R_D * I^2_{d_{RMS}}\right\} \quad (7)$$

B. SWITCHING LOSS (P_S)

The switching loss occurs during the transition of the switch state. The time taken by the switch to change its state from OFF to ON is termed as turn ON time (T_{on}). Similarly, the time taken by the switch to change its state from ON to OFF is termed as turn OFF time (T_{off}). The total switching losses are the sum of T_{on} power losses and T_{on} power losses of all the switches [41]. Where, $I_{on\_final,S}$, $I_{on\_intial,S}$, $V_{b,S}$ are final current after complete turn ON, initial current before turn OFF, blocking voltage across the S^{th} switch, respectively. The switching frequency is f_{sw}. The switching loss of each switch is computed using (8).

$$P_{S,S} = \left\{\frac{1}{6} * f_{sw} * V_b * I_{on\_final} * T_{on}\right\} + \left\{\frac{1}{6} * f_{sw} * V_b * I_{on\_intial} * T_{off}\right\} \quad (8)$$

C. CAPACITOR LOSS (P_{CA})

The internal resistance of a capacitor, which is called Equivalent Series Resistance (ESR), causes ohmic loss in the capacitor. The self balanced series coonected capacitors (C_1 and C_2) are charged by the DC sources. Therefore, the RMS current flow ($I_{C1} = I_{C2}$) and change in voltage ($\Delta V_{C1} = \Delta V_{C2}$) in each of capacitor are the same. The resistive and ripple loss of each capacitor is computed using (9). The total capacitor losses are given in equation (43). Where f_o is the fundamental frequency.

$$P_{CA,C} = ESR * I_c^2 + f_o * C * \Delta V_C^2 \quad (9)$$

Total losses are calculated by adding the conduction, switching, and capacitor losses shown in (10). Therefore, The efficiency can be expressed using (11). Where P_i and P_o are input and output powers, respectively.

$$P_L = P_C + P_S + P_{CA} \quad (10)$$

$$Efficiency = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_L} \quad (11)$$

The theoretical efficiency of the proposed topology is calculated by considering the input voltage, switching frequency, fundamental frequency are 230V, 5KHz, and 50Hz respectively. The SKM75GB12T4 IGBT is used for the switch positions S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, R_1, R_2, and R_3. Similarly, a 10A10 diode is used for the diode positions D_1 and D_2. The required parameters are taken from the data sheets of the IGBT and diode shown in Table-3. The conduction and switching losses of each switch, conduction (ESR) and ripple loss of each capacitor at an output power of 600W are tabulated in Table-4. The conduction, switching, and capacitor losses share in terms of percentage are represented in Fig.7. Similarly, the loss shares of each switch in terms of percentage are represented in Fig.8.

The theoretical efficiency of the proposed topology at different output powers is computed, as shown in Fig.9. The efficiency of the proposed topology during healthy (Group-I) and post fault (Group-II/III/IV) is calculated at a fixed load.

TABLE 3. Specifications of IGBT, diode and capacitor.

IGBT (SKM75GB12T4)	Diode (10A10)	Capacitor (B43464-S5478-M2)
Vs =1.85V, V_d =1.3V	V_t =1V	C = 4700μF
R_s = 0.014Ω. R_d = 0.012Ω	R_D = 0.02Ω	ESR =0.0054 Ω
T_{on} =150ns		
T_{off} =370ns		

TABLE 4. Power losses of each switch, diode and capacitor.

	Conducting Loss (W)	Switching Loss (W)	Capcitor Ripple Loss (W)
S_1	3.53	0.109	-
S_2	3.53	0.109	-
S_3	1.41	0.042	-
S_4	1.41	0.042	-
S_5	2.07	0.054	-
S_6	2.07	0.054	-
S_7	3.53	0.109	-
S_8	3.53	0.109	-
D_1	1.17	-	-
D_2	1.17	-	-
C_1	0.02	-	0.33
C_2	0.02	-	0.33
Total	23.48	0.631	0.66
Total Power Loss = 24.77W			

The efficiency of proposed topology for group-I switching pattern is 96.03% at an output power of 600 W. Similarly, for group-II, group-III, and group-IV switching patterns are 95.16%, 97.14%, and 96.95% respectively, as shown in Fig. 10. The post fault output power is less than the pre fault output power, as the peak of the output voltage decreases.

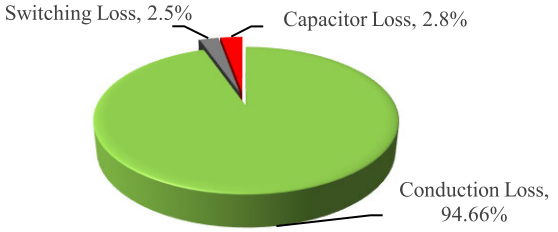

FIGURE 7. Conduction and switching losses share.

IV. EXPERIMENTAL AND REAL TIME SIMULATION RESULTS

The proposed single DC source seven level FT SCMLI is verified using MATLAB/ SIMULINK software. LSPWM control technique is used to generate the required triggering pulse during pre fault (7)-level) and post fault (5)-level) condition. A real time digital controller of dSPACE 1104 is used to generate the trigger pulse of IGBT. Digital controller is interfaced with the MATLAB/Simulink model in the host personal computer. The experimental setup is shown in Fig.11. The apparatus model and ratings are displayed in Table 5.

The performance of proposed topology is verified at m_i one with a low (50Hz) and high (5kHz) carrier frequency. The model is tested using a 230V input source voltage for

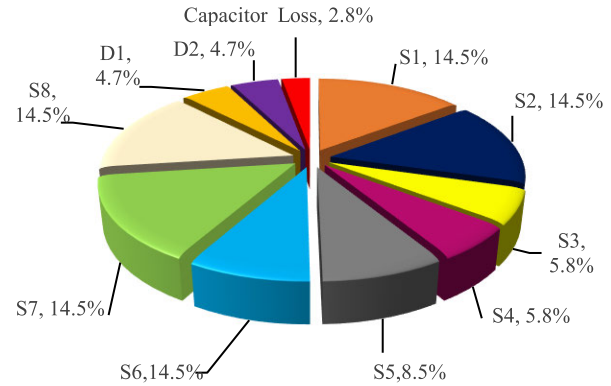

FIGURE 8. Power Loss shared by each switch and capacitors.

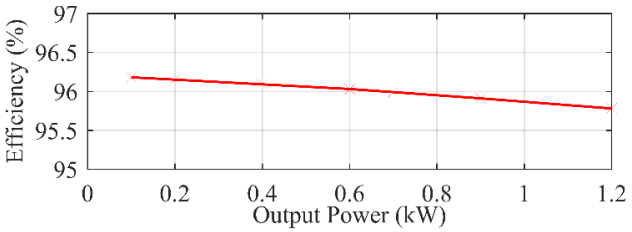

FIGURE 9. Efficiency with respect to output power.

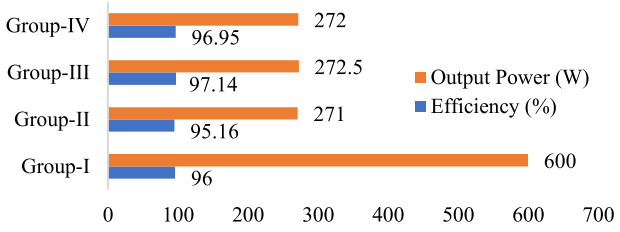

FIGURE 10. Efficiency of each group for a fixed load.

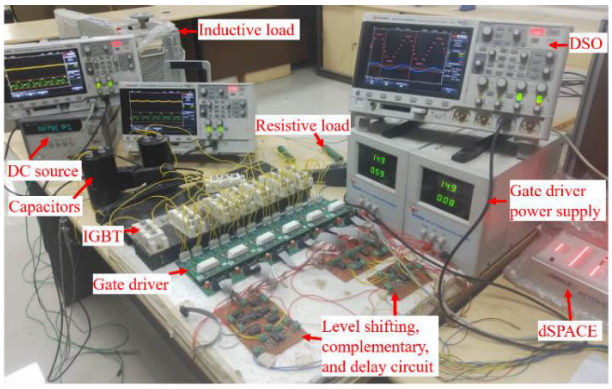

FIGURE 11. Experimental setup.

a resistive (R=100Ω) and inductive (R=100Ω, L=200mH) loads. The voltage and current of FT-MLI in case of seven and five level for resistive load are shown in Fig.12(a) and (b) respectively. By keeping the carrier frequency at 5kHz, the measured RMS voltage and current for the seven level

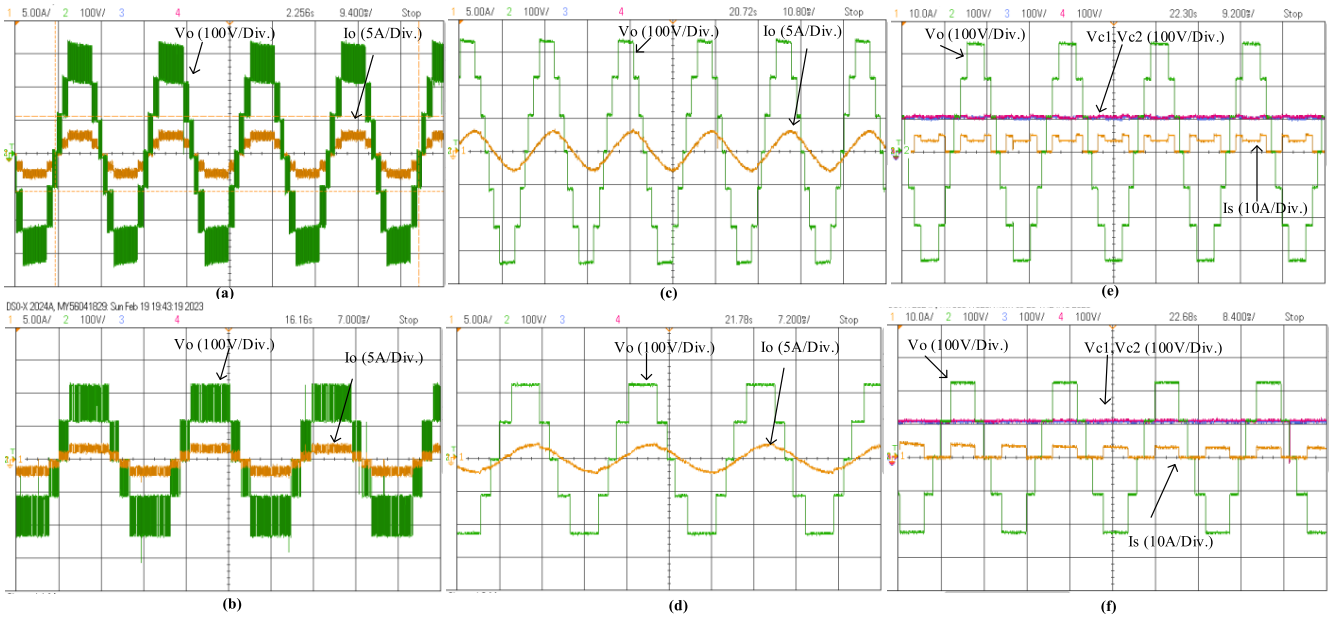

FIGURE 12. Experimental results for R-and RL load (a) 7-level for R load (b) 5-level for R load (c) 7-level for RL load (d) 5-level for RL load (e) Capacitor voltages and source current for 7-level with R load (f)) Capacitor voltages and source current for 5-level with R load.

TABLE 5. Apparatus used in the experimentation.

Apparatus /Model Number	Rating
IGBT (SKM75GB12T4)	1200V/75A
Diode (10A10)	10A
Gate driver (Skyper32R)	+15V
Capacitor (B43464-S5478-M2)	4700μf, 450V
DSO (DSOX3054A).	200MHz
Current Probe (GCP- 100)	140A Peak
dSPACE (1104)	8 Chanel I/O
Resistor	100Ω/ 7A
Reactor	0-200mH/10A
Level shit, complementary and delay ICs	LM339, CD40106, and CD4013

are 227V and 2.3A, respectively, and for the five level are 151V and 1.5A. Similarly, by keeping the carrier frequency at 50Hz, the measured output voltage and current for inductive load in case of seven and five level FT-MLI are shown in Fig.12(c) and (d) respectively. The Fig.12(e) and (f) are evident that the capacitors are not drawing any impulse charging current from the source. The voltage across capacitor C_1 and C_2 are almost constant in both 7-level and 5-level operation shown in Fig.12(e) and (f), respectively.

A pre programmed fault is created in the model for two cycles and it is cleared by rearranging the switching logic according to the Table–2. The FT capability of proposed topology against single and multi switch OCF is tested experimentally. The topology is able to regenerate all the losing voltage levels except the $-1.5V_{DC}$ and $+1.5V_{DC}$. These two states do not have any redundancy. The topology is reconfigured for 5 level output at each switch fault. The experimental analysis for each fault is as follows.

A. OCF ON SWITCH S_1

OCF on switch S_1 causes loss of 0, $-V_{DC}$, $-0.5V_{DC}$ and $-1.5V_{DC}$ voltage levels. In the experimental result shown in Fig.13(a) displays $-0.5V_{DC}$, because of its anti parallel diode. During the post fault, 0, $-0.5V_{DC}$ and $-V_{DC}$ levels are able to reproduce by reconfiguration of circuit with Group-II switching pattern.

B. OCF ON SWITCH S_2

OCF on switch S_2 causes loss of $+0.5V_{DC}$, $+V_{DC}$ and $+1.5V_{DC}$ voltage levels. In the experimental result shown in Fig.13(b) displays $+0.5V_{DC}$, because of its anti parallel diode. During the post fault, the $+V_{DC}$ level is able to reproduce by reconfiguration of circuit with Group-II switching pattern.

C. OCF ON SWITCH S_3

OCF on switch S_3 causes loss of $-0.5V_{DC}$, and $+1.5V_{DC}$ voltage levels. In the experimental result shown in Fig.15(c) displays $-0.5V_{DC}$, because of its anti parallel diode. The circuit is reconfigured with Group-II switching pattern shown in Fig.13(c).

D. OCF ON SWITCH S_4

OCF on switch S_4 causes loss of $+0.5V_{DC}$ and $-1.5V_{DC}$ voltage levels. In the experimental result shown in Fig.13(d) displays $+0.5V_{DC}$, because of its anti parallel diode. The circuit is reconfigured with Group-II switching pattern.

E. OCF ON SWITCH S_5

OCF on switch S_5 causes loss of 0, and $+V_{DC}$ voltage levels shown in Fig.13(e). If fault is not cleared immediately, the

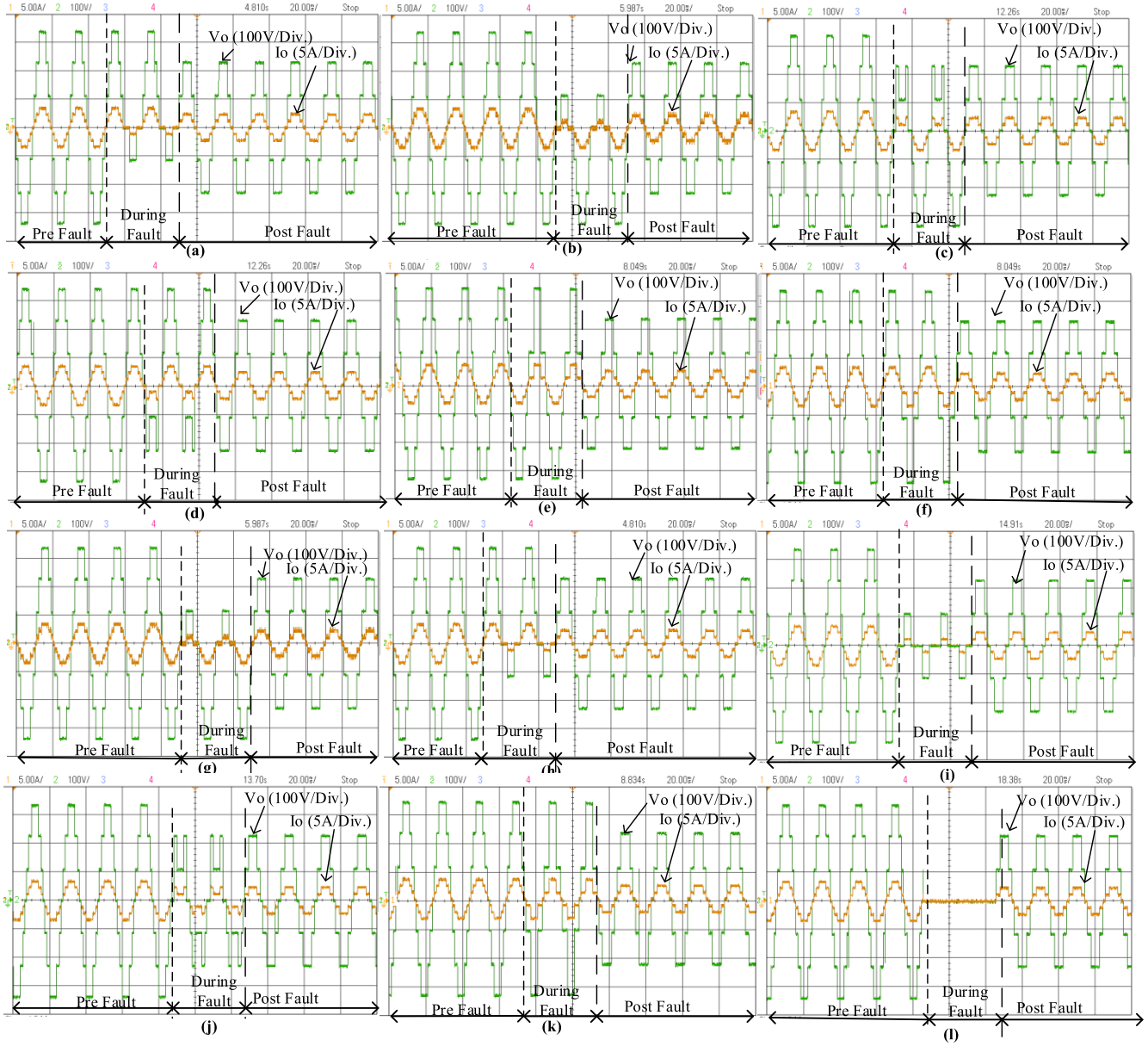

FIGURE 13. Experimental results for single and multiple OCF (a) Fault on S_1 (b) Fault on S_2 (c) Fault on S_3 (d) Fault on S_4 (e) Fault on S_5 (f) Fault on S_6 (g) Fault on S_7 (h) Fault on S_8 (i) Fault on (S_1 and S_2) or (S_7 and S_8) (j) Fault on S_3 and S_4(k) Fault on S_5 and S_6(l) Fault on S_1, S_2, S_3 and S_4.

Capacitor will discharge totally and leads to loss of $\pm 0.5V_{DC}$ voltage level. It is difficult to recharge the capacitor again to $0.5V_{DC}$. The fault is cleared immediately and reconfigured with Group-III switching pattern.

F. OCF ON SWITCH S_6

OCF on switch S_6 causes loss of 0, and -V_{DC} voltage levels shown in Fig.13(f). Similar to the fault on S_5 condition, this fault also needs to clear immediately and reconfigured with Group-III switching pattern.

G. OCF ON SWITCH S_7

OCF on switch S_7 causes loss of 0, $+V_{DC}$ and $+1.5V_{DC}$ voltage levels as shown in Fig.13(g) which is similar to the S_2 fault The circuit is reconfigured with Group-IV switching pattern.

H. OCF ON SWITCH S_8

OCF on switch S_8 causes loss of $-0.5V_{DC}$, $-V_{DC}$ and $-1.5V_{DC}$ voltage levels as shown in Fig.13(h), which is similar to the S_1 fault. The circuit is reconfigurated with Group-IV switching pattern.

I. OCF ON SWITCH S_1 AND S_2

OCF on switch S_1 and S_2 causes loss of 0, $\pm 0.5V_{DC}$, $\pm V_{DC}$, and $\pm 1.5V_{DC}$. The experimental result in Fig.13(i) shows $\pm 0.5V_{DC}$ voltage levels, because of its anti parallel diodes. The circuit is reconfigured with Group-II switching pattern.

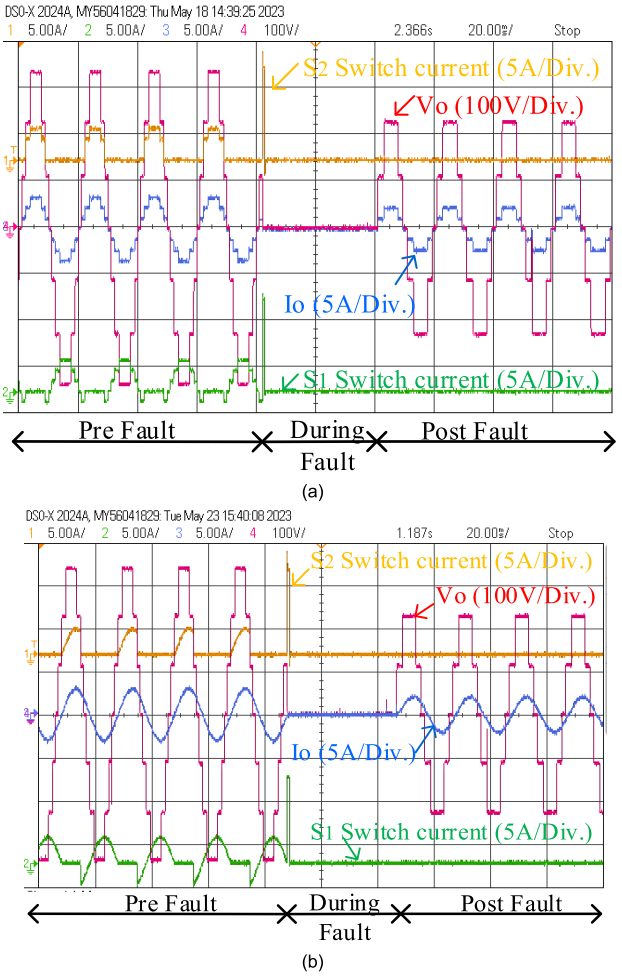

FIGURE 14. Response of the output voltage and current during the transition from pre-fault to post-post fault when SCF occurs at switches S_1 (a) for R load (b) for RL load.

The OCF fault on switch S_7 and S_8 are also similar to this fault.

J. OCF ON SWITCH S_3 AND S_4

OCF on switch S_3 and S_4 causes loss of $\pm 0.5V_{DC}$ and $\pm 1.5V_{DC}$. The experimental result in Fig.13(j) shows $\pm 0.5V_{DC}$ voltage levels, because of its anti parallel diodes. The circuit is reconfigured with Group-II switching pattern.

K. OCF ON SWITCH S_5 AND S_6

OCF on switch S_5 and S_6 causes loss of 0, and $\pm V_{DC}$ as shown in Fig.13(k). This fault is also similar to the fault on S_5 condition. The circuit is reconfigured with Group-III switching pattern

L. OCF ON SWITCH S_1, S_2, S_3 AND S_4

OCF on switch S_1,S_2,S_3, *and* S_4 causes loss of 0, $\pm 0.5V_{DC}$, $\pm V_{DC}$ and $\pm 1.5V_{DC}$ shown in Fig.13(l). During the post fault, the 0, $\pm 0.5V_{DC}$ and $\pm V_{DC}$ levels are able to reproduce by reconfiguration of circuit with Group-II switching pattern.

TABLE 6. Comparison of different 7- level FT-MLI.

	[22]	[23]	[25]	[26]	[28]	CHB	P
N_{DC}	2	3	3	3	3	3	1
N_{SW}	12	12	12	16	12	12	12
N_D	0	0	0	0	0	0	2
N_G	9	9	10	16	12	12	11
N_C	2	0	0	4	0	0	2
Relay or fuses	0	0	0	6	12	12	6
Component count	25	24	25	45	39	39	34
TSV(xV_{DC})	12	18	20	18	12	12	11
TSV_{PU}	8	6	6.6	6	4	4	7.3
CF	13	12.8	13.5	21.8	18.4	17.1	5.4
SSOCF	√	√	√	√	√	√	√
MSOCF	X	X	X	√	√	√	√
SSSCF	X	X	X	√	√	√	√
MSSCF	X	X	X	√	√	√	√
$P_{prefault}$=$P_{postfault}$	No	NO	NO	YES	NO	NO	NO
N_L at Post fault	5	5	5 / 3	7	5	5	5
Voltage gain (β)	1.5	1	1	1	1	1	1.5

P= proposed topology, N_{DC}= DC sources, N_{SW}= Switches, N_D = Diodes, N_G= Gate drivers, N_C = capacitors, N_r= Relay or fuse, TSV =Total Standing Voltage, CF= Cost Function, SSOCF= Single switch OCF, MSOCF=Multi switch OCF, SSSCF= Single switch SCF, MSSCF= Multi Switch SCF, N_L= No. of voltage levels, β= Voltage boosting, MBV= Maximum Blocking Voltage, TCS= Total Conducting Switches, α =weighting factor =1.

M. SCF ON SWITCH S_1 WITH REAL TIME SIMULATION RESULTS

The SCF does greater harm to inverter than the OCF. If SCF arises on any of the complimentary switches, the DC source or capacitor is shorted through the complementary switches (S_1, S_2; S_3, S_4; S_7, S_8). To protect the switch from the SCF, connected a thermal fuse or relay in series with the complementary switches, as shown in Fig.1. When the short circuit current through the switch exceeds the limit, the switch is disconnected from the circuit using a thermal fuse or relay. As a result, the SCF of the IGBT leg is turned into an OCF [42].

To analyze SCF experimentally, a specially designed thermal fuse is required. Besides, the fault identification and isolation are not the scope of this research work. This paper is mainly on the reconfiguration of the proposed topology after the fault is cleared. However, the SCF analysis is implemented in real time simulation with the help of Typhoon HIL (402-01-004). The main objective of this real-time simulation is to determine the loss of voltage levels for the SCF and reproduce possible voltage levels by reconfiguring the topology.

The SCF on S_1 is created in the programmable model for two cycles. So that the DC source is shorted through the switches S_1 and S_2. As a result, an impulse current is drawn by the source through these switches. The switches S_1 and S_2 will be cut off from the circuit by a thermal relay, when the current through these switches exceeds the permitted limit. Then the SCF is converted into OCF. After the fault is cleared, the circuit is reconfigured with the group II switching pattern. The response of the output voltage and current during the

TABLE 7. Comparison of single DC source 7- level 1.5 boost self balanced SCMLI (without reserve switches).

Topology	N_{SW}	N_D	N_G	N_C	Component count	TSV_{PU}	MBV (XV_{DC})	No. Of unequal rating switches	TCS			CF
									$\pm0.5V_{DC}$	$\pm1V_{DC}$	$\pm1.5V_{DC}$	α=1
[38]	7	2	7	2	18	5.0	1.5	3	3	3	3	3.0
[43]	10	0	8	4	22	7.3	2	3	2	3	2	3.8
[16]	10	0	8	4	22	6.0	1	2	3	4	3	3.7
[17]	10	0	9	3	22	6.0	1	2	3	5	5	3.7
[18]	10	0	8	3	21	5.3	1	2	3	4	3	3.5
[33]	9	0	8	3	20	5.0	1	2	4	4	3	3.3
[35]	8	2	7	4	21	6.0	1	2	3	4	3	3.5
[36]	11	0	11	3	24	5.3	1	2	4	4	5	3.9
[34]	10	0	8	2	20	6.0	1	2	3	4	3	3.4
[19]	8	2	6	4	20	5.3	2	4	2	3	2	3.3
P	**8**	**2**	**8**	**2**	**20**	**5.3**	**1**	**2**	**3**	**3**	**3**	**3.3**

transition from pre-fault to post-fault is measured for the SCF on switch S_1, as shown in Fig. 14. Similary, The SCFs on the other legs can also be changed from SCFs to OCFs and then reconfigured with the corresponding group switching pattern.

V. COMPARATIVE ANALYSIS

The proposed FT-MLI is compared with the existing 7-level FT-MLI topologies in terms of component count and performance indexed parameters shown in Table-6.

Most of the drive applications use single DC source MLI. But, the existing seven level FT-MLI requires more than one DC source. Whereas the proposed 7-level FT-MLI requires only single DC source. The CF of MLI mainly depends on component count and its TSV_{PU} shown in equation(12) [44]. These two parameters has to keep at minimum to reduce the CF. The proposed topology requires minimum number of switches and TSV. As a result, the CF of the proposed FT-MLI is lower than that of the comparable existing topologies displayed in Table-6. The topology [22] and proposed (P) one can boost the output voltage by 1.5 times but the remaining topologies do not have boosting capabilty. The topology P and [28] uses only 6 fuses to make the topology FT against single and multiple SCF. The topology [28] use 12 relays.

Apart from maintaining continuous power supply during post-fault conditions, some FT-MLI's can also maintain the same output power and voltage levels in both pre and post-fault conditions. The topology presented in [26] can generate same number of output voltage levels with preserving the output power under post fault. The remaining topologies can provide continuous power but the output power and voltage levels are reduced. However, the component count and TSV of [26] is highest among the existing topologies in Table–6. The topology [26], [28], and P are FT against single and multi switch faults. The topology [22] and P boost the output voltage by 1.5 times.

$$CF = \frac{N_{DC}}{N_L}\left\{N_{SW} + N_D + N_G + N_C + N_r + \frac{\alpha \times TSV_{PU}}{\beta}\right\} \tag{12}$$

The proposed topology (excluding the reserve switches) is compared with existing self balanced 7-level 1.5 times voltage boosting topologies shown in Table –7. The topology [38] requires minimum number of switches among all. However, It uses the switches with a blocking voltage higher than the DC supply voltage. The topology [19], [35], and P uses only eight switches. But, The number of capacitors required in [19] and [35] is twice that of the suggested topology. In the proposed topology, the number of switches with different ratings is kept at a minimum. The CF of topology of [19] and [33], and P are maintained at minimum, except the topology [38]. However, the topology [38] uses three unequal rating switches, which is not preferable for commercial usage.

VI. CONCLUSION

This paper proposed a single DC source fault tolerant seven level 1.5 boost SCMLI. It has a fault tolerant capability against single and multiple switch faults (open circuit and short circuit faults). The following are the conclusion points.

- The proposed FT-MLI is suitable for electric vehicles and biomedical applications, where the continuity of power supply is crucial in case of fault occurred at the inverter.
- It generates the 5-level output voltage during post fault for all single and multiple switch faults.
- It requires only twelve switches (8 working switches and four reserve switches), two diodes, two self-balanced capacitors, six fuses, and a DC source.
- The proposed topology has minimum number of switches and minimum TSV. As a result, the cost function of proposed topology is less than the existing similar kind topologies
- The power loss and efficiency of the proposed topology under pre fault and post fault are analysed theoretically. The efficiency is 96 % at an output power of 600 W under healthy condition and 97% at an output power of 272W under post fault condition.

ACKNOWLEDGMENT

Princess Nourah bint Abdulrahman University Researchers Supporting Project number (PNURSP2023R79), Princess Nourah bint Abdulrahman University, Riyadh, Saudi Arabia.

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