IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 30 September 2023, accepted 10 November 2023, date of publication 14 November 2023,
date of current version 27 November 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3333035

RESEARCH ARTICLE

Injection-Locked Frequency Sixtuplers in 90 nm CMOS by Using the Push-Push Doubler

SHENG-JEN CHENG[1], PI-NENG SHEN[2], CHUNG-HUNG HONG[3], ZHENG-WEI CHEN[4], CHUNG-PING CHEN[1], AND SHENG-LYANG JANG[2], (Senior Member, IEEE)

[1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan
[2]Department of Electronic Engineering, National Taiwan University of Science and Technology, Taipei 106335, Taiwan
[3]Department of Biomedical Engineering, College of Biomedical Engineering, China Medical University, Taichung 404333, Taiwan
[4]Department of Electronic Engineering, National Taipei University of Technology, Taipei 10608, Taiwan

Corresponding authors: Chung-Ping Chen (cpchen@ntu.edu.tw) and Sheng-Lyang Jang (sljjj@mail.ntust.edu.tw)

ABSTRACT This paper designs two single-stage *LC*-tank injection-locked frequency sixtuplers (ILFSs) fabricated in a 90 nm CMOS process and it describes the circuit design, operation principle, and measurement results of the ILFSs. The ILFS circuit with a differential input and single-phase output is made of a first-harmonic injection-locked oscillator (ILO), a frequency tripler, and a push-push doubler. The first ILFS uses an octagonal inductor. For a supply voltage of 0.4 V, the free-running frequency is around 41.52 GHz, DC power consumption is 9.03 mW at the incident power of 0 dBm, and the output locking range at 0 dBm input power is 10.21 %. The second ILFS uses an 8-shaped inductor for low electromagnetic (EM) noise generation. The free-running frequency is around 37.2 GHz, DC power consumption is 7.72 mW at the incident power of 0 dBm, and the output locking range at 0 dBm input power is 17.4 %. The two chips have the same area, 0.7×0.7 mm^2. This paper also provides a further analysis and comparison of the RF performance of on-chip inductors designed. Simulation shows the substrate noise coupling and distance noise coupling between victim and aggressor, the 8-shaped inductor exhibits a significant reduction in coupling. By the measurement results, it is evident that the performance of the 8-shaped inductor ILFS is superior to that of the octagonal inductor ILFS.

INDEX TERMS 5G, millimeter-wave (mm-wave), low power, LC-tank, g_m-boosted, push-push frequency doubler, frequency tripler, 8-shaped inductor, injection-locked frequency sixtupler, locking range, 90nm CMOS, magnetic field coupling noise interference.

I. INTRODUCTION

Fifth Generation (5G) cellular systems are being designed to communicate over both sub-6 GHz bands as well as mm-wave bands driven by the ever-increasing data-rate requirements. The frequency bands for 5G high-frequency band may cover 38.6 GHz to 40 GHz [1]. Owing to the low-quality factor of varactors at mm-wave, as well as flicker noise, the phase noise of the voltage-controlled oscillator (VCO) is very poor and its power consumption is quite high [2]. N-push VCO [3] and injection-locked frequency multipliers (ILFM) [4] following the fundamental VCO are the other mm-wave signal generation options, here the fundamental oscillator often runs at a subharmonic frequency. N-push oscillators consume high power and occupy a large chip area because of the N-stage of active FETs. Injection-locked frequency multipliers (ILFM) are popular in mm-wave signal generation due to their high power efficiency and superior phase-noise performance. Within its locking range, the ILFM phase noise closely tracks the input phase noise operating at a much lower frequency.

This paper designs two multiply-by-6 ($\times$6) ILFMs in a 90nm CMOS process. ILFMs are often used with oscillators or phase-locked loops to relax the signal source design at a low frequency while supplying a high output frequency signal. A previous C-band single-stage $\times$6 ILFM is unsuitable for 5 G application, and it uses an injection-locked oscillator (ILO) with a mixer-type frequency tripler with the aid of

The associate editor coordinating the review of this manuscript and approving it for publication was Feng Lin.

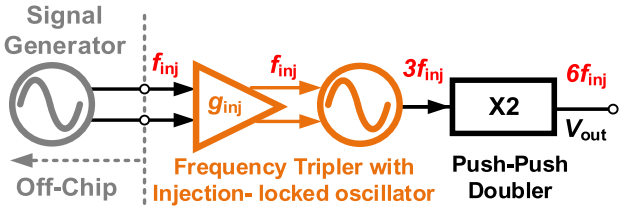

FIGURE 1. Block diagram of the injection-locked frequency sixtupler.

a self-generated frequency doubler signal for enhancing the injection efficiency [5], [6]. The other CMOS two-stage ×6 ILFM [7], [8] utilizes a single-FET acting as a frequency tripler (FT) in front of an ILO and also as a push-push frequency doubler. This ILFM is not fully characterized and it uses an FT loaded with a narrow-band filter. A CMOS three-stage ×6 ILFM [9] utilizes a shunt-injection ×3 ILFM in front of a push-push frequency doubler and an ILO following the doubler. This ×6 ILFM is not fully characterized either. A similar ×6 frequency multiplier (FM) chain is designed [10] by using a frequency tripler followed by a frequency doubler.

Passive inductors are crucial elements in RF circuits such as amplifiers, oscillators, and filters. *LC* voltage-controlled oscillators (VCOs) with inductive load are essential parts of all RF-integrated transceivers and they normally integrate with output buffers for driving other circuits or for measurement purposes. Literature has shown various inductor topologies, which include tapered inductors [11] and 8-shaped inductors [12]. The latter inductor uses one-turn [13], 2-turn [14], or 3-turn [12]. A twisted inductor normally has two lobes with far-field magnetic field generation in opposite directions to offset each other in the location sitting between the symmetric axis of the two lobes. The twisted inductor VCO [15] has a significant advantage in suppressing the interference of integrated transceiver chips.

In this paper, two mm-wave ×6 ILFMs are designed. The first ILFS uses octagonal-shaped inductors and the second ILFS uses 8-shaped inductors, which are notoriously known for suppressing the coupling noise [13], [16], [17]. In the second ILFS, the frequency tripler uses an 8-shaped inductor, the push-push frequency doubler also uses the 8-shaped inductor, and the ILO also uses the 8-shaped inductor as the resonator component. We also propose using electromagnetic (EM) simulation to compare the differences between the 8-shaped inductor and the octagonal inductor regarding signal coupling.

II. CIRCUIT DESIGN

Fig. 1 shows the block diagram of ×6 ILFM, which consists of a frequency tripler, an ILO, and a frequency doubler. Fig. 2 shows the off-chip measurement setup and circuit diagram of ×6 ILFM using an injection-locked frequency tripler and a push-push frequency doubler. A differential injection signal is applied to the gates of M3 and M4. The common node

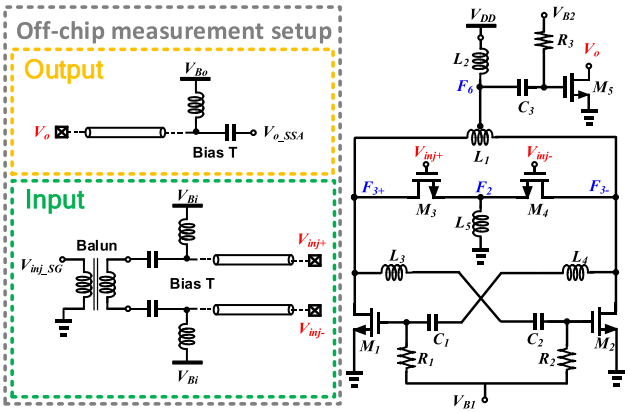

FIGURE 2. The measurement setup and block diagram of the ILFS.

of frequency tripler with L5, M3, and M4 generates a 2nd harmonic of injection signal at the F2 node, and the drains of M3 and M4 as mixers contain a 3rd harmonic of injection signal by mixing the injection signal with the self-generated 2nd harmonic. M1, M2, C1, C2, and R1, R2 act as a negative resistance generator, which forms the ILO with L1, and a parasitic capacitor comprising the resonator. When the output frequency of the frequency tripler falls in the locking range of the ILO, the ILO output tracks the injection signal. Inductors L3 and L4 enable M1 and M2 as g_m boosters [18], [19], which boost the ac-gate voltages of M1 and M2 for lower power operation. Compared with a conventional push-push pair, incorporating a g_m-boosted push-push pair as a full-wave rectifier not only increases second-harmonic swing but also operates at low power consumption. The common mode 2nd harmonic drain current supplied by M1 and M2 generates the 6th harmonic at the F6 node by using the L2 load. M5 is a capacitive coupling output buffer for the sixth harmonic extraction. No buffer is used for the ILO reducing the capacitive load for speed and locking range enhancement. Time domain simulation would illustrate the circuit operation principle. Fig. 3 presents the post-simulated results of the first ILFS, including voltage (a) and current (b) waveforms in the time domain of the whole integrated circuit. The circuit behavior of the first and second ILFS are similar, so just show the first ILFS.

III. COMPARISION OF NOISE SUPPRESSION BETWEEN 8- AND O-SHAPED INDUCTORS

This section compares the performance of a 1-turn 8-shaped inductor and a 1-turn o-shaped inductor for the topologies with and without center-tapped connection.

A. CENTER-TAPPED INDUCTORS

Fig. 4 shows the designed center-tapped inductor layout and simulated *Q*-factor and inductance. For the o-shaped inductor, the internal distance is 107.4 μm× 90 μm. For one lobe of the 8-shaped inductor, the internal distance is 109 μm×42 μm. Fig. 5(a) shows the layout of an o-shaped inductor for interference study with an o-shaped aggressor and o-shaped

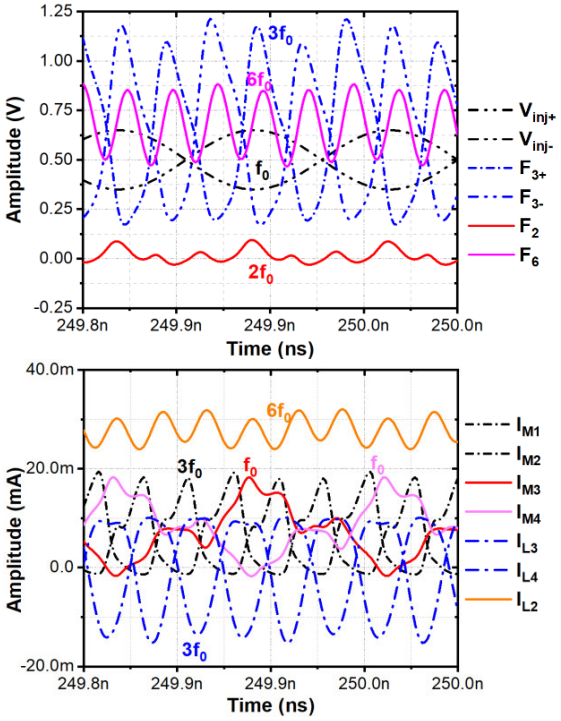

FIGURE 3. Post-simulated voltage and current waveforms of ILFS. V_{DD} = 0.4 V, $V_{B1} = V_{B2}$ = 0.5 V, injection signal of V_{inj+} and V_{inj-} and the frequency is 6.9 GHz, DC bias is 0.5 V. (a) (Top plot) Voltage waveforms of circuit node. Black dotted line: injection signal. Red solid line: node of F_2. Blue dotted line: nodes of F_{3+}/F_{3-}. Pink solid line: node of F_6. (b) (bottom plot) Current waveforms of circuit devices. Red and pink solid lines: the currents of M_3 and M_4. Black dotted lines: the currents of M_1 and M2. Blue dotted lines: the currents of L_3 and L_4. Orange solid line: the current of L_2.

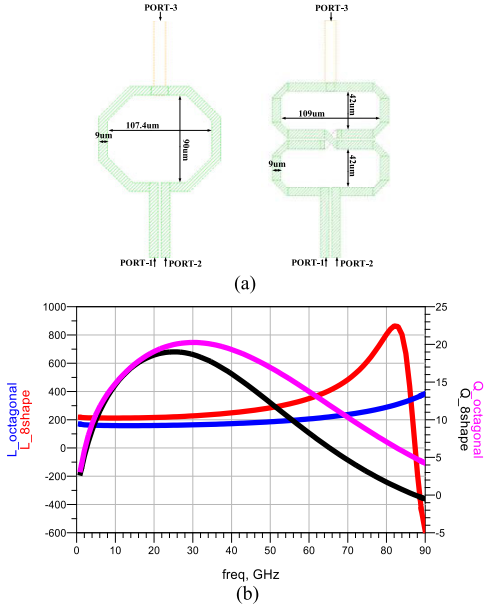

FIGURE 4. (a) Layout of octagonal and 8-shaped inductors. (b) Simulated Q-factor and inductance of octagonal inductor and 8-shaped inductor.

victim by varying the aggressor-victim distance t_d. Increasing t_d yields smaller V_o/V_{in} and coupling factors as shown in Fig. 5(b) and Fig. 5(c), respectively. Fig. 6(a) shows the

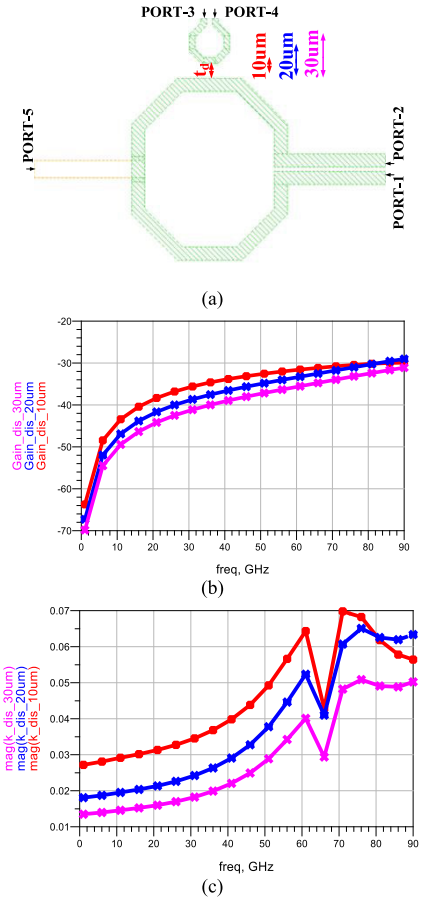

FIGURE 5. (a) Layout for interference study with o-shaped aggressor and o-shaped victim by varying the aggressor-victim distance t_d = 10μm, 20μm, 30μm. (b) Vo/Vin. (c) Coupling factor of o-shaped.

layout of a 1-turn 8-shaped inductor for interference study with the center-tapped 8-shaped aggressor and o-shaped victim by varying the aggressor-victim distance t_d. Increasing t_d yields smaller Vo/Vin and coupling factor as shown in Fig. 6(b) and Fig. 6(c), respectively, and shifts the dip. Fig. 6 shows the coupling noise is smaller than Fig. 5. Fig. 7(a) shows the layout of a 1-turn o-shaped center-tapped inductor for interference study with o-shaped aggressor and o-shaped victim by varying the substrate thickness t_{sub} and fixed distance t_d. Fig. 7(b) and Fig. 7(c) show that increasing substrate thickness t_{sub}increases the substrate noise coupling. Fig. 8(a) shows the layout of a 1-turn 8-shaped center-tapped inductor for interference study with a center-tapped 8-shaped aggressor and o-shaped victim by varying the substrate thickness and fixed distance t_d. Fig. 8(b) and Fig. 8(c) show that increasing substrate thickness t_{sub} increases the substrate noise coupling. Increasing thickness t_{sub} increases coupling noise, but the 8-shaped inductor shows smaller coupling.

B. DIFFERENTIAL INDUCTORS

Fig. 9 shows the designed inductor layout and simulated *Q*-factor and inductance. For one lobe of the o-shaped inductor, the internal distance is 87.4 μm×70 μm. For the 8-shaped inductor, the internal distance is 85 μm× 26 μm.

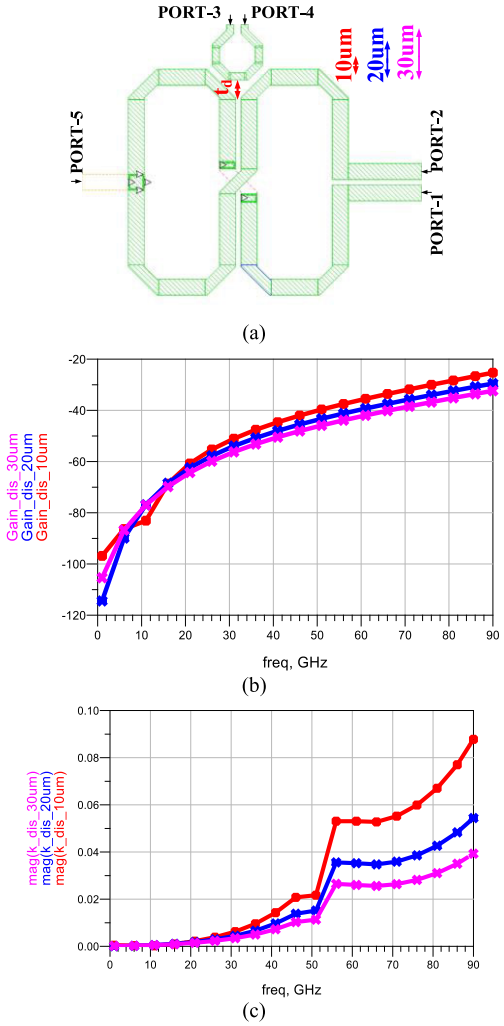

FIGURE 6. (a) Layout for interference study with the 8-shaped aggressor and o-shaped victim by varying the aggressor-victim distance $t_d = 10\mu$m, 20μm, 30μm. (b) Vo/Vin. (c) Coupling factor of 8-shaped.

Fig. 10 to Fig. 13 show the same analysis method as a center-tapped inductor and obtain the same trend.

Simulation shows the substrate noise coupling between victim and aggressor is dominant by the substrate coupling. Shrinking the substrate thickness reduces the noise coupling, and by varying the aggressor-victim distance, the 8-shaped inductor exhibits a significant reduction in coupling. The 8-shaped inductor shows significantly reduced coupling for the victim sitting along the symmetric axis of the two lobes with current flowing in the opposite direction.

Modern RFICs have achieved an impressively high integration level, making cross-coupling effects among different sections of the circuit a potential limit to their functionality. Integrated spiral inductors are a potential source of EM interference. In conventional integrated circuit technologies, a grounded metal guard ring (MGR) is widely used to mitigate the coupling effect between any pair of inductors. Full-wave electromagnetic (EM) simulation results indicate that the guard ring size can significantly affect the inductance

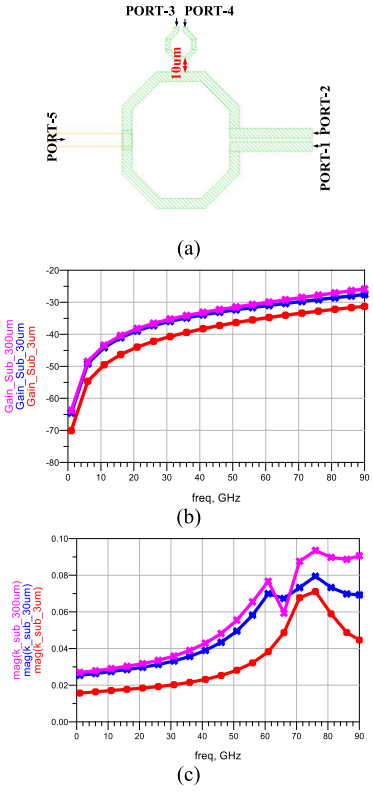

FIGURE 7. (a) Layout for interference study with o-shaped aggressor and o-shaped victim by varying the substrate thickness t_{sub} =3μm, 30μm, 300μm and fixed distance t_d =10μm. (b) V_o/V_{in}. (c) Coupling factor.

value of a single-turn planar inductor. The present analysis shows the 6-shaped inductor reduces the cross-talk level.

IV. SIMULATED SURFACE CURRENT DENSITY

Fig. 14(a) shows simulated surface current density in the center-tapped 8-shaped inductor excited in the differential mode and the common mode. The applied frequency is 0.01 GHz. Fig. 14(b) shows simulated surface current density in the 8-shaped inductor excited in the DM and the CM modes. The applied frequency is 40 GHz. Fig. 14(c) shows simulated surface current density in the 8-shaped inductor excited in the DM and the CM modes. The applied frequency is 81 GHz.

The CM mode shows lower current density. Fig. 15(a) shows simulated surface current density in the o-shaped inductor excited in the differential mode and the common mode. The applied frequency is 0.01 GHz. Fig. 15(b) shows simulated surface current density in the o-shaped inductor excited in the DM the CM modes. The applied frequency is 40 GHz. Fig. 15(c) shows simulated surface current density in the o-shaped inductor excited in the DM the CM modes. The applied frequency is 81 GHz. The CM mode shows lower current density.

Fig. 16(a) shows simulated surface current density in the 8-shaped inductors excited in the differential mode. No CM mode because of no center tap. The applied frequencies are 0.01 GHz, 40 GHz, and 70 GHz. Fig. 16(b) shows simulated

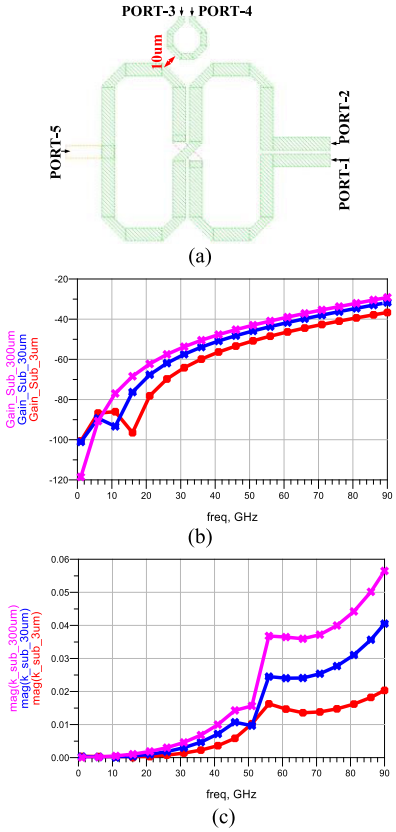

FIGURE 8. (a) Layout for interference study with 8-shaped aggressor and 8-shaped victim by varying the substrate thickness t_{sub} =3μm, 30μm, 300μm and fixed distance t_d =10μm. (b) Vo/Vin. (c) Coupling factor.

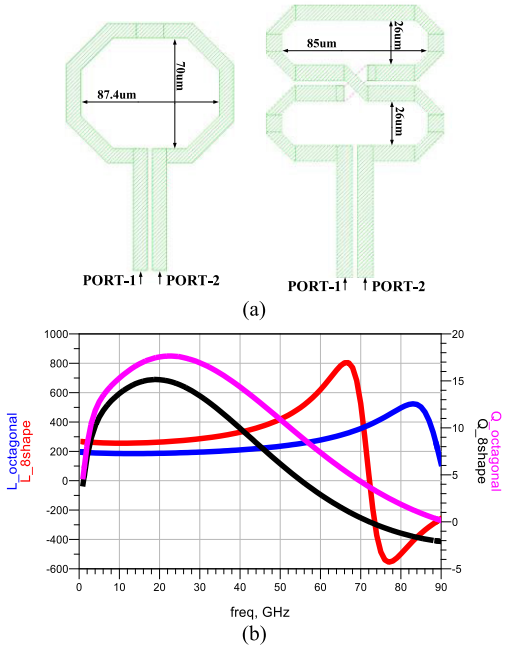

FIGURE 9. (a) Layout of octagonal and 8-shaped inductors. (b) Simulated Q-factor and inductance of octagonal inductor and 8-shaped inductor.

surface current density in the o-shaped inductor excited in the DM mode. The applied frequencies are 0.01 GHz, 40 GHz,

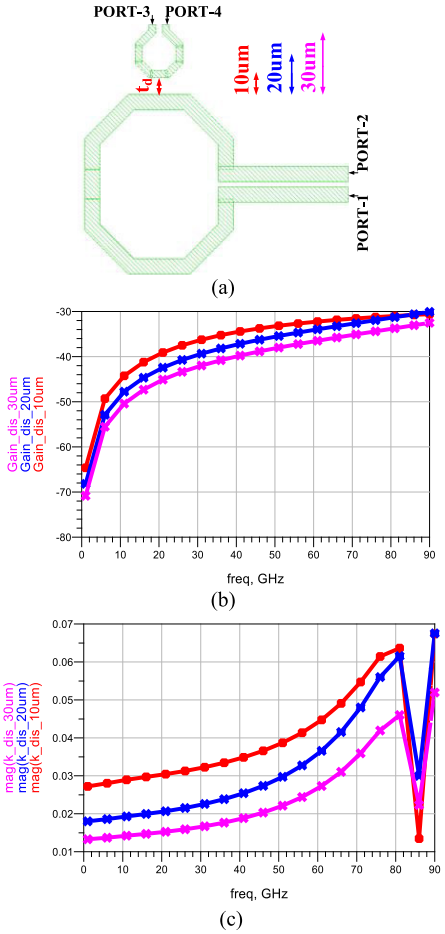

FIGURE 10. (a) Layout for interference study with o-shaped aggressor and o-shaped victim by varying the aggressor-victim distance t_d = 10μm, 20μm, 30μm. (b) V_o/V_{in}. (c) Coupling factor of o-shaped.

and 70 GHz. In the DM mode, the inner edge of the top lobe shows higher current density.

V. MEASUREMENT RESULTS

The photos of two ×6 ILFMs shown in Fig. 17 have been designed and fabricated in the TSMC 90 nm CMOS technology. The die micrographs occupy the same area of 0.7 × 0.7 mm^2.

The two ×6 ILFMs are measured via fully on-wafer probing, PGPPGP for DC signal, and GSGSG for high-frequency signal. A Keysight E8257D signal generator is used to provide the input signal. The output of the ILFM was analyzed using a Keysight E4448A spectrum analyzer. All losses associated with the probe, cable, and connector were embedded in the measurement results. The output path loss is approximately 13.5 dB at 40 GHz.

A. MEASUREMENT OF THE ×6 ILFM USING OCTAGONAL INDUCTOR

Fig. 18 shows measured free-run and locked spectra of ILFS buffer output at V_{DD} = 0.4 V. The output cable loss is 13.5 dB

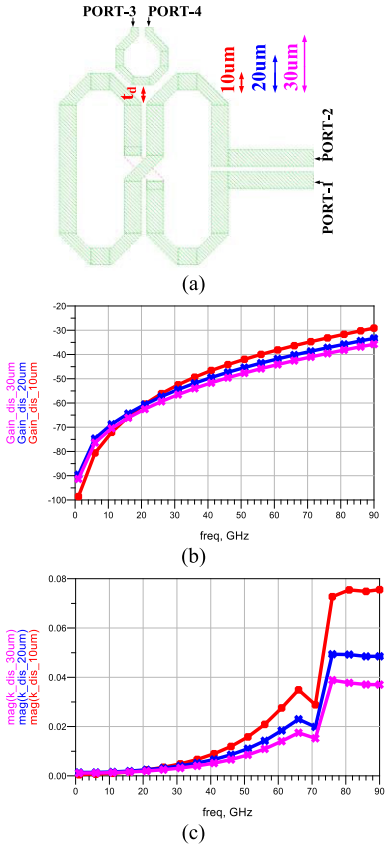

FIGURE 11. (a) Layout for interference study with 8-shaped aggressor and 8-shaped victim by varying the aggressor-victim distance t_d = 10μm, 20μm, 30μm. (b) V_o/V_{in}. (c) Coupling factor.

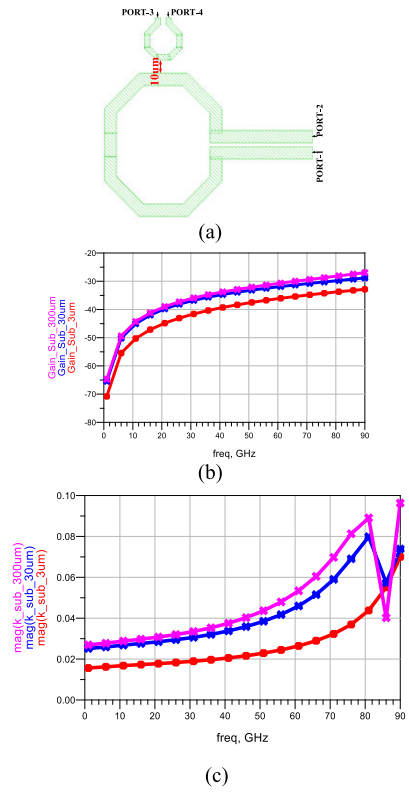

FIGURE 12. (a) Layout for interference study with the o-shaped aggressor and o-shaped victim by varying the substrate thickness t_{sub} =3μm, 30μm, 300μm and fixed distance t_d =10μm. (b) Vo/Vin. (c) Coupling factor.

at 40 GHz. Therefore, the actual output power is approximately -6.5 dBm. The power consumption is 6.9 mW at the free-run frequency and 9.03 mW at the injection frequency of 6.92 GHz. Fig. 19 shows measured phase noises of the locked ILFS of the sixth harmonic and the injection signal from the signal generator. The phase noise at 1 MHz frequency offset from the 41.52 GHz carrier is -118.08 dBc/Hz.

Fig. 20 illustrates the measured locking range at 0 dBm input power. Fig. 21(a) shows measured $\times$6 harmonic output power levels over different input power at the input frequency f_{inj} of 6.8 GHz, the ILFS operates normally irrespective of input power level. It can be observed that the maximum output power is achieved when the input power is -5 dBm. As injection power increases, the injection MOSFET shows larger channel conductance. Fig. 21(b) shows measured $\times$6 harmonic output power over the frequency range of interest with the input power of 0 dBm. It can be observed that the further away from the free-run frequency, the smaller the output power.

Fig. 22(a) shows the measured free-run spectrum of the ILFS output buffer, the carrier is at 41.83 GHz, and its output power is -20.45 dBm. Other harmonics are smaller than the carrier by more than 6.65 dB. Fig. 22(b) shows the measured locked spectrum of ILFS buffer output, it contains more harmonics than those shown in Fig. 22(a) and the harmonics are caused by the leakage of injection signal and mixing products. The sixth harmonic is larger than the 1st harmonic by 6.28dB. Caused by the unbalanced layout or measurement setup, the phase difference of the ILFS inputs may be not exactly 180^o, the injected fundamental is leaked to the ILFS outputs and it induces a doubler frequency signal at the ILFS output. The fundamental leakage is suppressed by the ILFS load filter, and the doubler leakage in the ILFS output is also suppressed. Another unbalanced factor is the measurement setup. From Fig. 2, we can observe that the signal generator has a single-ended output and needs to be converted to a differential output using a balun. Additionally, the balun differential output requires an individual cable path and bias-tee to provide DC bias for the injection MOSFETs and final through the GSGSG differential signal probe. As a consequence, it causes amplitude and phase mismatching, resulting in excessive harmonics.

Unfortunately, correcting high-frequency differential input amplitude and phase mismatching is very challenging because it requires the use of a high-frequency oscilloscope or network analyzer. Even if mismatching is identified, it is challenging to correct it with the existing resources, especially the mismatching caused by the GSGSG probe.

The final reason is that, due to the limited area, the distance between signals is restricted, resulting in coupling between signal lines and causing excessive harmonics. Later, we will mention that the ILFS with the 8-shaped inductor

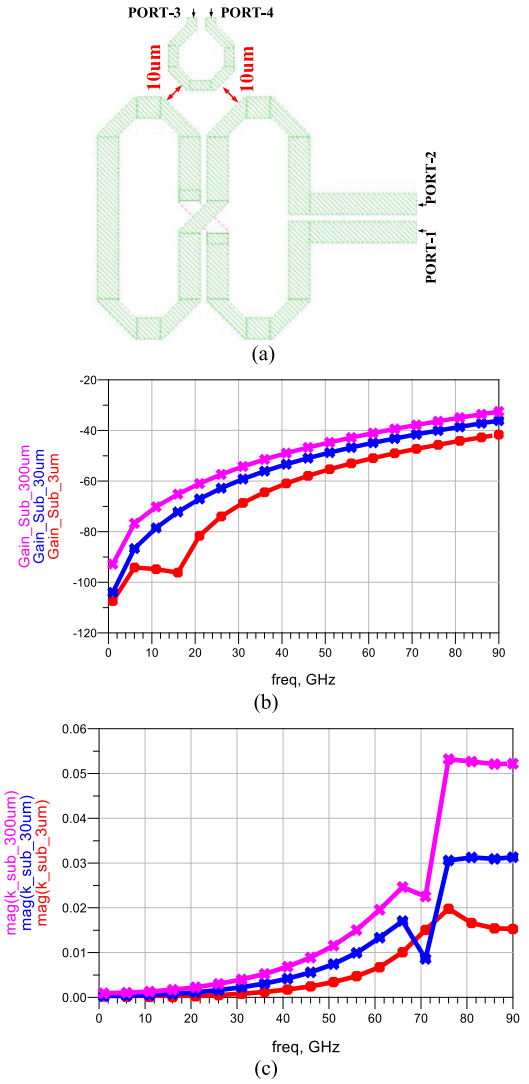

FIGURE 13. (a) Layout for interference study with 8-shaped aggressor and 8-shaped victim by varying the substrate thickness t_{sub} =3μm, 30μm, 300μm and fixed distance t_d =10μm. (b) Vo/Vin. (c) Coupling factor.

significantly improves the coupling between signals, and this has been verified through measurements.

B. MEASUREMENT OF THE ×6 ILFM USING 8-SHAPED INDUCTOR

The measurement items for the 8-shaped inductor ILFS are the same as for the previous octagonal inductor ILFS. Fig. 23 shows measured free-run and locked spectra of ILFS buffer outputs at V_{DD} = 0.4 V. The output cable loss is 13.5 dB at 40 GHz. Therefore, the actual output power is approximately -1 dBm. The power consumption is 5.53 mW at the free-run frequency and 7.72 mW at the injection frequency of 6.2 GHz. Fig. 24 shows measured phase noises of the locked ILFS of the sixth harmonic and the injection signal from the signal generator. The phase noise at 1 MHz frequency offset from 37.2 GHz carrier is -120.7 dBc/Hz. Fig. 25 illustrates the measured locking range at 0 dBm input power for

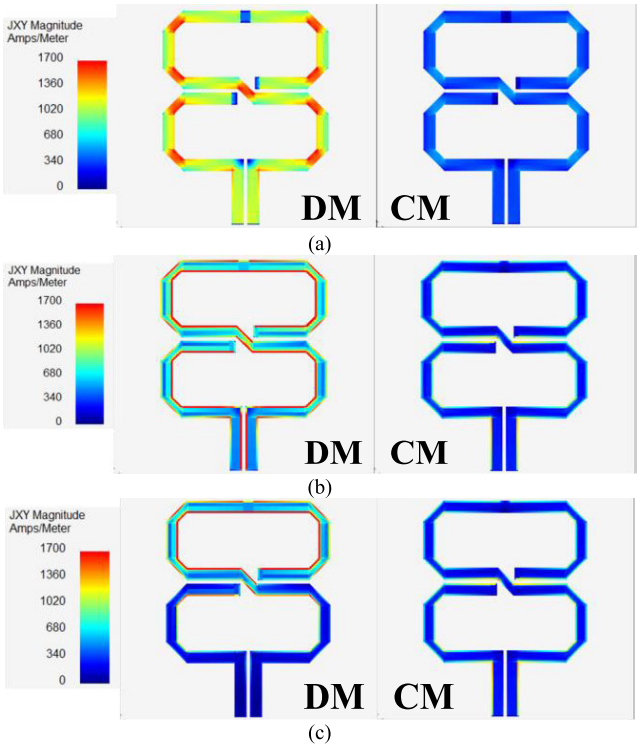

FIGURE 14. The center-tapped 8-shaped inductor. (a) Simulated DM/CM surface current density at 0.01 GHz. (b) Simulated DM/CM surface current density at 40 GHz. (c) Simulated DM/CM surface current density at 81 GHz.

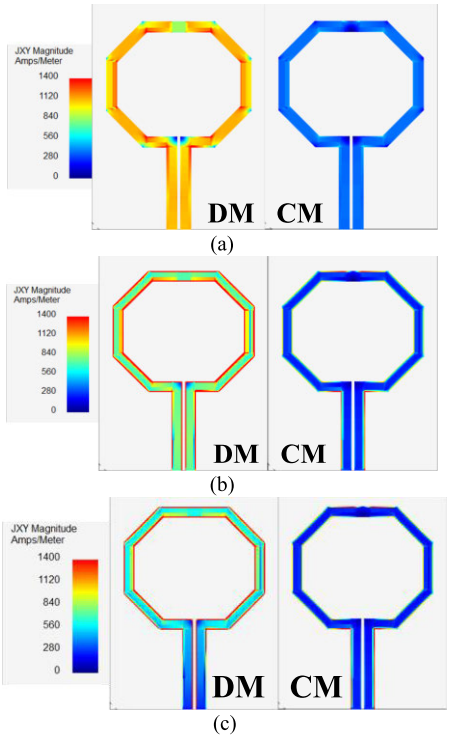

FIGURE 15. The center-tapped o-shaped inductor. (a) Simulated DM/CM surface current density at 0.01 GHz. (b) Simulated DM/CM surface current density at 40 GHz. (c) Simulated DM/CM surface current density at 81 GHz.

various V_{DD} levels. Fig. 26(a) shows measured ×6 harmonic output power levels over different chip input power at the

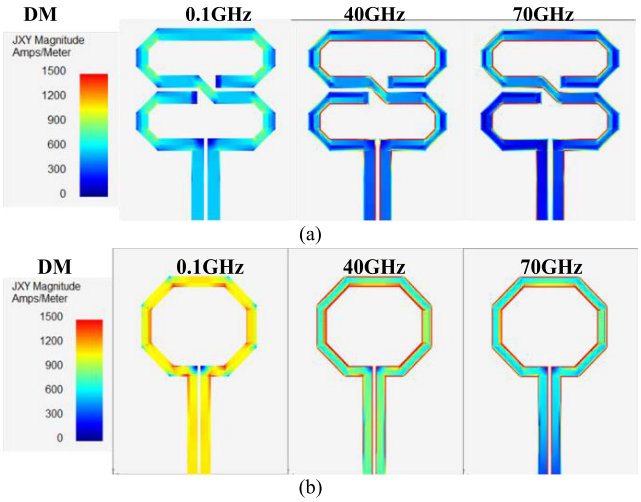

FIGURE 16. The differential inductor. (a) Simulated DM surface current density of 8-shaped inductor at 0.01 GHz,40 GHz, and 70 GHz. (b) Simulated DM surface current density of o-shaped inductor at 0.01 GHz, 40 GHz, and 70 GHz.

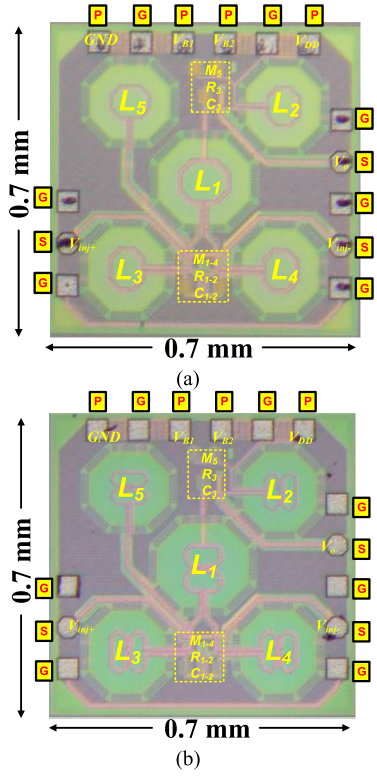

FIGURE 17. Chip micrograph of the ×6 ILFM's. (a) ×6 ILFM using octagonal inductor. (b) ×6 ILFM using 8-shaped inductors.

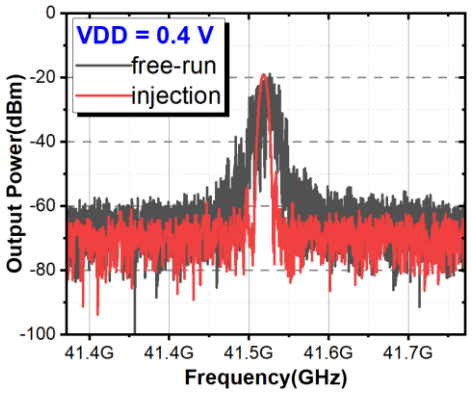

FIGURE 18. Measured ×6 free-run and locked spectra.

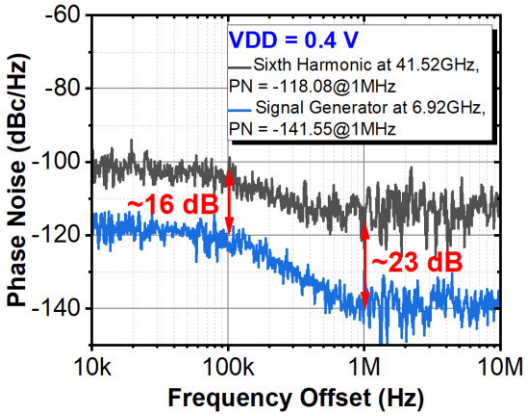

FIGURE 19. Measured phase noises of the locked ILFS of the sixth harmonic and the injection signal from the signal generator.

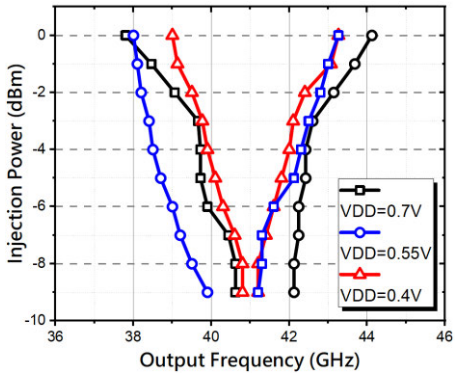

FIGURE 20. Measured ×6 output sensitivity using an octagonal inductor.

input frequency f_{inj} of 6.2 GHz. Fig. 26(b) shows measured ×6 harmonic output power over the frequency range of interest with the input power of 0dBm. The maximum output power is achieved when the input power is -5dBm, it exhibits the same trend as the measurement results of the ×6 ILFM using an octagonal inductor.

Fig. 27(a) shows the measured free-run spectrum of the ILFS output buffer, the carrier is at 37 GHz and its output power is −16.07dBm. Other harmonics are smaller than the carrier by more than 37.03dB. Fig. 27(b) shows the measured locked spectrum of ILFS buffer output, the sixth harmonic is larger than the 1st harmonic by 15.96dB. The harmonic rejection performance is significantly better than ×6 ILFM using an octagonal inductor. The measurement results verify that the 8-shaped inductor ×6 ILFM significantly reduces signal coupling between inductors. These results are the same as the previously mentioned inductor analysis trend.

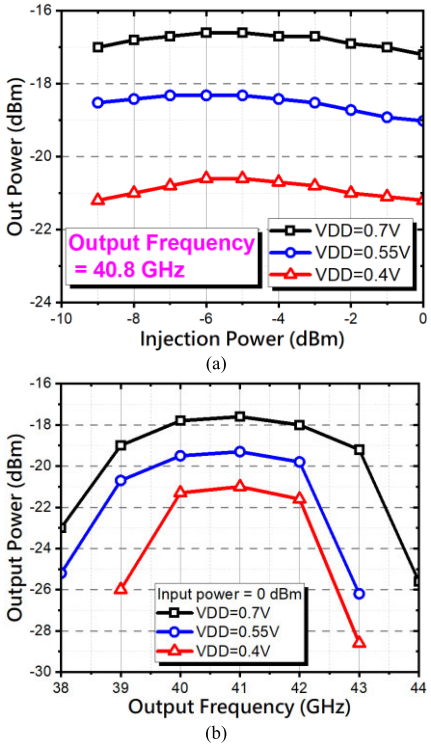

FIGURE 21. Measured ×6 harmonic output power at (a) different input power at the input frequency of f_{inj} of 6.8 GHz, and (b) output power versus the frequency range of interest with the input power of 0 dBm.

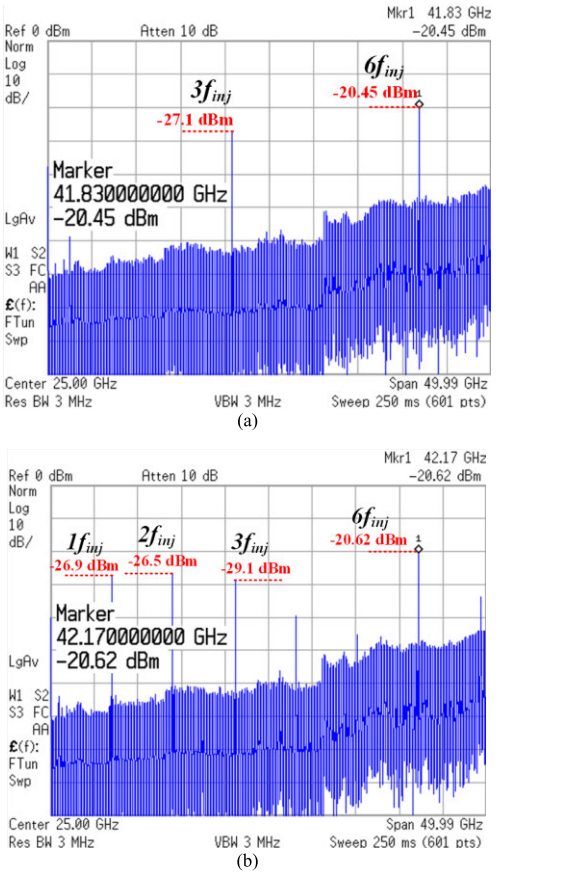

FIGURE 22. Measured output spectra of the ILFS under (a) free-running, (b) injection-locked, covering the full range.

Actually, these two ×6 ILFMs only differ in the inductor type, where the inductor was changed from o-shaped to 8-shaped, while all other component parameters remain unchanged and the layout remains completely unchanged. Therefore, in the pursuit of smaller area system circuits, utilizing 8-shaped inductors to address coupling between signals proves to be a powerful and practical approach. However, we also encountered the same issue as before, the unbalanced layout or measurement setup resulted in the harmonic rejection performance being not as perfect as desired.

Table 1 shows the performance summary and comparison. The performance comparison table clearly demonstrates that the 8-shaped inductor ×6 ILFM outperforms the O-shaped inductor ×6 ILFM by a significant margin. Moreover, when compared to other literature, it maintains a highly competitive edge.

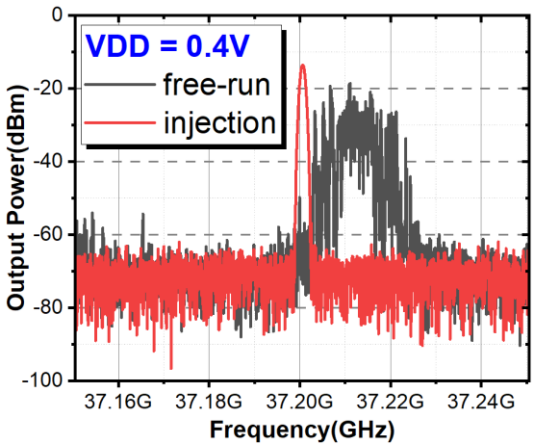

FIGURE 23. Measured ×6 free-run and locked spectrum for the 8-shaped ILFS.

VI. DISCUSSION

With the aggressive scaling of CMOS technologies in recent years and due to the fast-growing emerging applications in ultra-high-speed wireless/wireline communications, high-resolution imaging, and sensing systems, more and more integrated circuits are designed and implemented for signal generation at millimeter-wave (mm-wave), automotive radar system and terahertz (THz) frequencies [7], [23]. Frequency multipliers are widely used in the aforementioned scenarios. In addition to the integration with the frequency synthesizer to offer a local frequency source, the ILFS can simplify the circuit architecture in the frequency multiplier chain for driving mixers above 200 GHz transceivers [23]. The sixtuplers reduce the stages of frequency multipliers and hence the die area, design complexity, and power consumption reduce too.

In extremely high-frequency applications, frequency multipliers also offer significant advantages in terms of high

TABLE 1. Performance summary and comparison.

	[5]	[8]	[20]	[21]	[22]	O-Shaped Inductor	8-Shaped Inductor
Process	180nm CMOS	65nm CMOS	65nm CMOS	130nm CMOS	55nm CMOS	90nm CMOS	90nm CMOS
Input-Output	Diff-Sing	Sing-Sing	Diff-Diff	Diff-Quad	Sing-Sing	Diff-Single	Diff-Single
Supply Voltage(V)	1	1	1	1.3	1.8	0.4	0.4
Frequency (GHz)	5.62-6.23	74.7-82.2	22.2	24	30.8-40	39 - 43.2	33.6 - 40
Locking Range(%)	10.29	9.6	21.6	3.3	26	10.21	17.39
Muliple Number	x6	x6	x3	x3	x4	x6	x6
Pin(dBm)	0	0	0	0	0	0	0
DC Power(mW)	20.8	6.3#	8.16	10.4	39	9.03	7.72
Peak Output Power(dBm)	N/A	4▼	N/A	-17	Min: -10 Max: -7.1	-6.5@ 41.52GHz☼	-1@ 37.2GHz☼
Chip Size(mm^2)	1.368*	1.19▼	0.32*	0.125**	0.67*	0.49*	0.49*

* Overall area (including pads). # Only core chip. ▼ Overall LO-chain (including pads). ** Core area only (without pads). ■ BW_{-3dB}.
☼ Without Cable loss is 13.5 dB at 40 GHz.

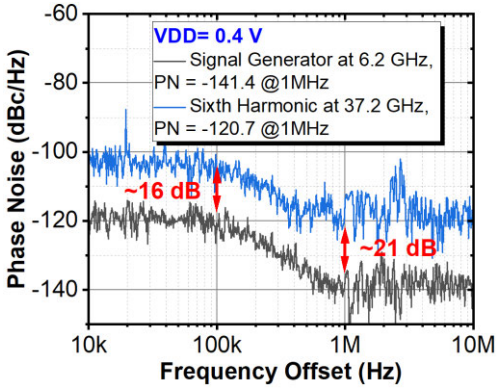

FIGURE 24. Measured phase noises of the locked ILFS of sixth harmonic and the injection signal from signal generator.

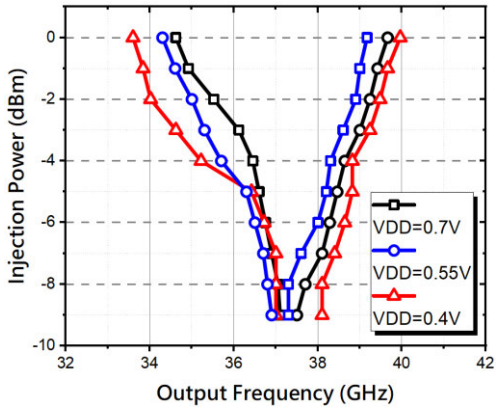

FIGURE 25. Measured ×6 output sensitivity using octagonal inductor.

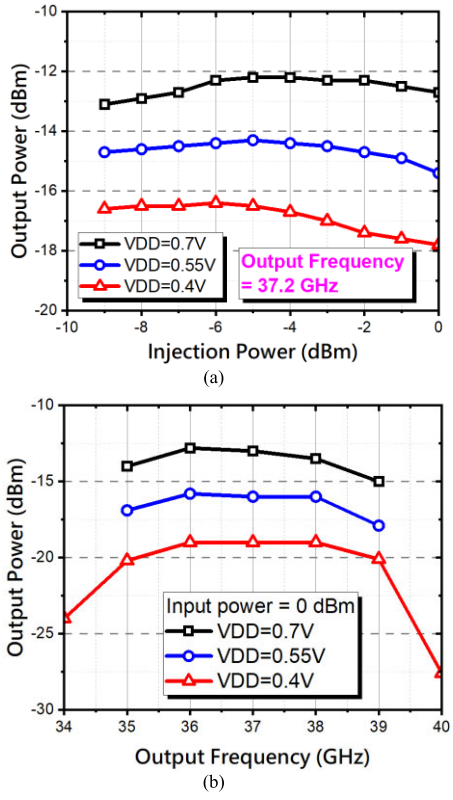

FIGURE 26. Measured ×6 harmonic output power at (a) different input power at the input frequency of f_{inj} of 6.2 GHz, and (b) output power versus the frequency range of interest with the input power of 0 dBm.

integration and scalability. The proposed ILFS with simple structure, it is easy to operate at another frequency band by tuning the size of the 8-shaped inductors or connecting the switched capacitor array. Integrated with the input and output buffers it is also easy to integrate with other RF components to form a larger RF system without significant modifications of the ILFSs. One transceiver architecture application example is shown in Fig. 28, the ILFS provides the local signal to the mixer to up- or down-convert the signal while lowering the operation frequency of the PLL for performance enhancement of the PLL and the overall system.

Due to the impact of Process-Voltage-Temperature (PVT) variation, flexibility and adjustability are essential in the system. A post-layout simulation for PVT analysis is used to ensure the correct circuit operation. Following the concept of the multi-mode oscillator design [20], [24], multi-mode and multi-band ILFSs can be designed by modifying the resonator

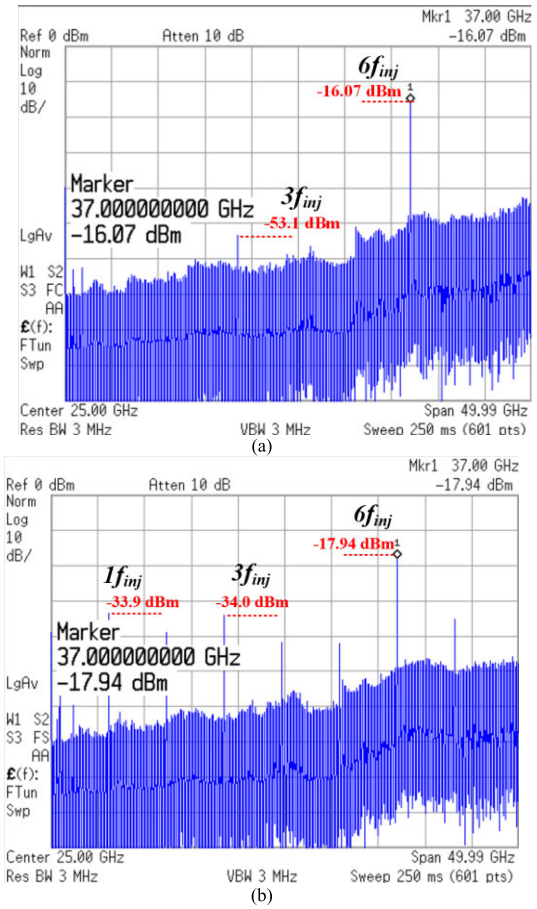

FIGURE 27. Measured output spectra of the ILFS under (a) free-running, and (b) injection-locked, covering the full range.

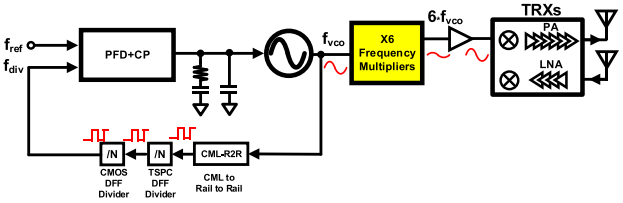

FIGURE 28. The architecture of integrated X6 Frequency Multipliers with PLL and TRXs.

with L_1 from Fig. 2 or connecting a switchable capacitor bank. The inductor and capacitor dimension is tuned in iteration to fit the application specification.

A circuit [25] composed of a power amplifier and a frequency divider with a multi-turn twisted inductor shows magnetic coupling reduction experimentally. The proposed sixtupler under interference from other RF components will show a similar reduction of coupling because injection-locked frequency divider and frequency multiplier belong to the same class of injection-locked oscillators.

VII. CONCLUSION

This paper presents two mm-wave single-stage fully integrated n-core CMOS *LC*-tank injection-locked frequency sixtuplers that combine an injection-locked frequency tripler and a push-push frequency doubler. The two successfully implemented ILFSs in 90nm CMOS show good locking range and phase noise performance. The simulation results confirm that the 8-shaped inductor ×6 ILFM significantly reduces signal coupling, leading to improved harmonic suppression performance. To our knowledge, this is the first reported ILFM employing the 8-shaped inductors for frequency doubler, frequency tripler, and the first-harmonic ILO for high EMI performance.

ACKNOWLEDGMENT

The authors would like to thank the Staff of the Taiwan Semiconductor Research Institute (TSRI) for their help.

REFERENCES

[1] R. T. Prabu, M. Benisha, V. T. Bai, and V. Yokesh, "Millimeter wave for 5G mobile communication application," in *Proc. 2nd Int. Conf. Adv. Electr., Electron., Inf., Commun. Bio-Inform. (AEEICB)*, Chennai, India, Feb. 2016, pp. 236–240, doi: 10.1109/AEEICB.2016.7538280.

[2] K.-H. Nam, N.-P. Hong, and J.-S. Park, "A 16-times frequency multiplier for 5G synthesizer," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 11, pp. 4961–4976, Nov. 2021, doi: 10.1109/TMTT.2021.3103203.

[3] B. Catli and M. M. Hella, "Triple-push operation for combined oscillation/divison functionality in millimeter-wave frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1575–1589, Aug. 2010.

[4] X. Liu and H. C. Luong, "A 170-GHz 23.7% tuning-range CMOS injection-locked LO generator with third-harmonic enhancement," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2668–2678, Jul. 2020, doi: 10.1109/TMTT.2020.2986757.

[5] S.-L. Jang, W.-C. Lai, and R.-H. Lu, "Single-stage injection-locked frequency sixtupler in CMOS process," *IEEE Access*, vol. 10, pp. 40316–40323, 2022.

[6] S.-L. Jang, W.-C. Lai, Y.-J. Chang, D.-L. Wang, and M.-H. Juang, "CMOS injection-locked frequency quadrupler/quintupler," *IEEE Access*, vol. 10, pp. 78168–78175, 2022.

[7] Y.-H. Hsiao, Y.-C. Chang, C.-H. Tsai, T.-Y. Huang, S. Aloui, D.-J. Huang, Y.-H. Chen, P.-H. Tsai, J.-C. Kao, Y.-H. Lin, B.-Y. Chen, J.-H. Cheng, T.-W. Huang, H.-C. Lu, K.-Y. Lin, R.-B. Wu, S.-J. Chung, and H. Wang, "A 77-GHz 2T6R transceiver with injection-lock frequency sextupler using 65-nm CMOS for automotive radar system application," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 10, pp. 3031–3048, Oct. 2016.

[8] Y.-C. Chang, Y.-H. Hsiao, Y.-H. Lin, and H. Wang, "A W-band LO-chain with injection-locked frequency sextupler and medium power amplifier using 65-nm CMOS technology for automotive radar applications," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, vol. 1. Nanjing, China, Dec. 2015, pp. 1–3.

[9] X. Liu and H. C. Luong, "A fully integrated 0.27-THz injection-locked frequency synthesizer with frequency-tracking loop in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1051–1063, Apr. 2020, doi: 10.1109/JSSC.2019.2954232.

[10] A. Kankuppe, S. Park, P. T. Renukaswamy, P. Wambacq, and J. Craninckx, "A wideband 62-mW 60-GHz FMCW radar in 28-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 6, pp. 2921–2935, Jun. 2021, doi: 10.1109/TMTT.2021.3075437.

[11] V. N. R. Vanukuru, "High-*Q* inductors utilizing thick metals and dense-tapered spirals," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3095–3099, Sep. 2015, doi: 10.1109/TED.2015.2458772.

[12] H.-C. Lee, S.-L. Jang, H.-W. Liu, and L. Y. Chen, "Divide-by-2 injection-locked frequency divider exploiting an 8-shaped inductor," *Microw Opt. Technol. Lett.*, vol. 63, no. 4, pp. 1024-1028, Apr. 2021.

[13] A. Poon, A. Chang, H. Samavati, and S. S. Wong, "Reduction of inductive crosstalk using quadrupole inductors," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1756–1764, Jun. 2009, doi: 10.1109/JSSC.2009.2020525.

[14] A. Mahmoud, L. Fanori, T. Mattsson, P. Caputa, and P. Andreani, "A 2.8-to-5.8 GHz harmonic VCO based on an 8-shaped inductor in a 28 nm UTBB FD-SOI CMOS process," *Anal. Integr. Circuits Signal Process.*, vol. 88, no. 3, pp. 391–399, Sep. 2016, doi: 10.1007/s10470-016-0759-4.

[15] N. Itoh, S.-I. Fukase, K.-I. Hirashiki, and M. Nagata, "Twisted Inductor VCO for suppressing on-chip interferences," in *Proc. Asia–Pacific Microw. Conf.*, Dec. 2007, pp. 1–4, doi: 10.1109/APMC.2007.4554539.

[16] P.-Y. Wang, T.-L. Wu, M.-Y. Chen, Y.-C. Shen, Y.-C. Chang, D.-C. Chang, and S. S. H. Hsu, "A low phase-noise class-C VCO using novel 8-shaped transformer," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 886–889.

[17] P. Andreani, K. Kozmin, P. Sandrup, M. Nilsson, and T. Mattsson, "A TX VCO for WCDMA/EDGE in 90 nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1618–1626, Jul. 2011.

[18] S.-W. Chu and C.-K. Wang, "An 80 GHz wide tuning range push-push VCO with g_m-boosted full-wave rectification technique in 90 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 4, pp. 203–205, Apr. 2012.

[19] L. Li, P. Reynaert, and M. S. J. Steyaert, "A 60-GHz CMOS VCO using capacitance-splitting and gate–drain impedance-balancing techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 406–413, Feb. 2011.

[20] C. Wan, L. Wu, H. Zhu, T. Xu, and Q. Xue, "A 22.2-GHz injection-locked frequency tripler featuring dual injection and 39.4% locking range," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 7, pp. 3548–3556, Jul. 2022.

[21] D. Shin and K.-J. Koh, "24-GHz injection-locked frequency tripler with third-harmonic quadrature phase generator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 2898–2906, Aug. 2019.

[22] Y. Yu, P. Tang, K. Yi, C. Zhao, H. Liu, Y. Wu, W.-Y. Yin, and K. Kang, "A wideband CMOS frequency quadrupler with transformer-based tail feedback loop," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 4, pp. 1153–1157, Apr. 2021.

[23] M. H. Eissa, A. Malignaggi, R. Wang, M. Elkhouly, K. Schmalz, A. C. Ulusoy, and D. Kissinger, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Sep. 2018, doi: 10.1109/JSSC.2018.2839037.

[24] W. Jung, H. Kim, Y. Song, K.-H. Lee, and D.-K. Jeong, "A 0.99μs FFT-based fast-locking, 0.82GHz-to-4.1GHz DPLL-based input-jitter-filtering clock driver with wide-range mode-switching 8-shaped LC oscillator for DRAM interfaces," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Antonio, TX, USA, Apr. 2023, pp. 1–2, doi: 10.1109/CICC57935.2023.10121322.

[25] P. Martin, R. Horn, and K. Ben Atar, "A multi-turn twisted inductor for on-chip cross-talk reduction," in *Proc. IEEE Int. Conf. Sci. Electr. Eng. (ICSEE)*, Nov. 2016, pp. 1–5, doi: 10.1109/ICSEE.2016.7806138.

SHENG-JEN CHENG is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

He is a member of the SoC VLSI-EDA Laboratory, Graduate Institute of Electronics Engineering, National Taiwan University. His research interests include SerDes and RFIC.

PI-NENG SHEN is currently pursuing the M.S. degree in electrical engineering with the National Taiwan University of Science and Technology, Taipei, Taiwan.

His current research interests include RF and analog integrated circuits.

CHUNG-HUNG HONG was born in Kaohsiung, Taiwan. He received the Ph.D. degree from National Taiwan University, Taipei. He is currently an Assistant Professor with the Department of Biomedical Engineering, College of Biomedical Engineering, China Medical University, Taichung, Taiwan.

ZHENG-WEI CHEN is currently pursuing the bachelor's degree in electronic engineering with the National Taipei University of Technology, Taiwan.

He specializes in researching virtual reality joint rehabilitation assistive devices, phase-frequency-locked, buck converter, and low-EMI buck converter.

CHUNG-PING CHEN received the B.S. degree in computer science and information engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1990, and the M.S. and Ph.D. degrees in computer science from The University of Texas at Austin, in 1996 and 1998, respectively. From 1996 to 1999, he was with Strategic CAD Labs, Intel Corporation, as a Senior CAD Engineer. Since 1999, he has been an Assistant Professor with the Electrical and Computer Engineering Department, University of Wisconsin–Madison. Since 2003, he has been an Associate Professor with the Department of Electrical Engineering (EE), National Taiwan University, Taipei. He is currently a Professor with the GIEE, BIO, and the EE Department, National Taiwan University. His research interests include EDA and BIO topics, including computer-aided design and microprocessor circuit design with an emphasis on interconnect and circuit optimization, circuit simulation, statistical design, and signal/power/thermal integrity analysis and optimization. He served as a Program Committee Member and/or an Organizer for the DAC, ICCAD, DATE, ISPD, ASPDAC, ISQED, SASIMI, VLSI/CAD Symposium, and ITRS. He received the D2000 Award from Intel Corporation and the National Sciences Foundation Faculty Early Career Development Award (CAREER), from 1999 to 2001. He received the 2002 SIGDA/ACM Outstanding Young Faculty Award and the 2002 IBM Peter Schneider Faculty Development Award.

SHENG-LYANG JANG (Senior Member, IEEE) was born in Taiwan, in 1959. He received the B.S. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1981, the M.S. degree from National Taiwan University, Taipei, in 1983, and the Ph.D. degree from the University of Florida, Gainesville, FL, USA, in 1989. He joined the Noise Research Laboratory, University of Florida, in 1986. In 1989, he joined the Department of Electronics, National Taiwan University of Science and Technology, Taipei, and became a Full Professor, in 1993. He has coauthored more than 300 SCI journal articles in the MOSFET devices and circuits. He also holds 17 U.S. patents.