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RESEARCH ARTICLE

# Quantum Mode Series Resonant Converter Utilized as Active Voltage Regulator of a Split DC Bus Capacitor

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**ABSTRACT** Certain modern power electronics systems require active regulation of the split DC bus capacitor voltages. The series resonant converter is suitable to be utilized as an active voltage regulator, due to its ability to operate with soft switching, and hence, with high efficiency. In discontinuous conduction mode, the series resonant converter operates with a constant unity voltage gain, thus achieving balancing of the DC link. However, discontinuous conduction mode does not provide means for achieving a different voltage distribution, which is important in many scenarios. On the other hand, by operating in quantum mode (i.e. type 2 discontinuous conduction mode), the voltages across DC bus capacitor can be regulated. Therefore, the modeling of the quantum mode series resonant converter connected across split DC bus is presented in this paper. The steady-state operation as well as transient behavior are discussed and experimentally verified on a laboratory prototype.

**INDEX TERMS** Active voltage balancing, partial power rated converters, quantum mode series resonant converter, soft switching, switched capacitor converter, zero current switching.

## I. INTRODUCTION

The efficiency and power density are one of the most important requirements of power converters today. Partial Power Rated Converters (PPRC) are one of possible solutions to improve those features. By processing part, instead of full power, PPRC are able to reduce power losses, and consequently the volume of the converter [1], [2], [3]. However, depending on the type of PPRC, they have different drawbacks. On one hand the Input-Parallel Output-Series (IPOS) and Input-Series Output-Parallel (ISOP) PPRC topologies require isolation within the DC to DC converter, while not providing input to output galvanic isolation [4], [5]. On the other hand, the Input-Series Output-Series (ISOS) PPRC requires active voltage regulation across split DC bus [3]. In some cases of a split DC bus capacitor, such as neural-point-clamped three-level inverter or three-level DC to DC converter, the converter interfacing the split DC bus has the ability to regulate the DC bus voltages [6], [7], [8], [9], [10]. While the main benefit of this approach is the avoidance of an additional converter solely for the purpose of regulating the split DC bus voltages, in both cases the voltage balancing has limits depending on the duty-cycle or modulation index [10]. Also, considering the cases of PV inverters, some publications proposed the operation without the regulation of a split DC bus voltages [11], [12]. On the other hand, in applications in which the DC bus voltages have to be regulated externally, such as in the case of ISOS PPRC, the auxiliary converter has to be used to regulate the DC bus voltages. One option is to utilize the buck/boost based DC to DC converter as an Active Voltage Regulator (AVR) [13], [14], [15], [16]. However, these types of AVRs significantly decrease the efficiency of the converter, undermining the motivation for utilizing the PPRC in the first place [17], [18]. Another possibility is to utilize the Dual-Active-Bridge (DAB) DC to DC converter [19], or

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Resonant Switched-Capacitor Converter (RSCC) [20], in which case the voltages of the split DC bus can be regulated with the phase-shift control. While, in both cases, i.e. DAB and RSCC, the converters can operate with the Zero Voltage Switching (ZVS), in light load conditions the ZVS cannot be ensured, which consequently reduces the system efficiency. On the other hand, the Series Resonant Converter (SRC) used as an AVR can operate with Zero Current Switching (ZCS) on all load conditions, and, hence, with negligible switching losses [21], [22], [23]. The ZCS is achieved by operating at the resonant frequency [24], [25] or in Discontinuous Conduction Mode (DCM), in which case, the voltage gain is constant and equal to one [26], [27], [28], [29]. While vast majority of applications require voltages across upper and lower DC bus capacitor to be equal, such as bipolar DC grids [30], [31], the ratio between those voltages limits the voltage gain in case of ISOS PPRC [3]. Namely, the voltage gain of ISOS boost PPRC is limited between 1 and $(1 + k)$, where $k$ is the ratio between upper and lower DC bus capacitor voltages. Therefore, regulating the ratio of these voltages can expand the gain of the ISOS boost PPRC, as well as allow for a more efficient operation.

Having that the voltage gain of the SRC operating in DCM is constant and equal to 1 (i.e. cannot be controlled), this paper explores the possibility of using SRC in quantum mode (i.e. in type 2 discontinuous conduction mode (DCM2)) [32], [33], in order to achieve an arbitrary voltage regulation across the DC bus capacitors. By operating in DCM2, the ZCS is still ensured in all load conditions, and hence, the highly efficient operation is maintained. Summarizing, the main contributions and novelties of this manuscript are the analysis of the steady-state operation, derivation of the linearized average model and the transient behavior, as well as, the closed-loop control of the SRC operating in DCM2, and utilized as an active voltage regulator of a split DC bus capacitor.

The rest of the paper is organized as follows. In section II the stability of the steady-state operation of quantum mode series resonant converter utilized as active voltage balancing device is analyzed. In section III the linearized average model of the SRC operating in DCM2 is presented, together with the transfer functions of interest. Lastly, in section IV, the prototype example is presented, with the experimental verification of the discussed steady-state operation and transient behavior of the SRC operating in DCM2.

## II. STEADY-STATE OPERATION

The SRC, presented in Figure 1, has been utilized as an Active Votlage Balancing Device (AVBD) [21], [22]. By operating in DCM, the constant voltage gain 1 is ensured [26], i.e. the voltages across upper and lower DC bus capacitors are equal. On the other hand, in case the voltages across DC bus capacitors need to be regulated on different levels, the SRC can be operated in DCM2 [32], [33]. Therefore, in this

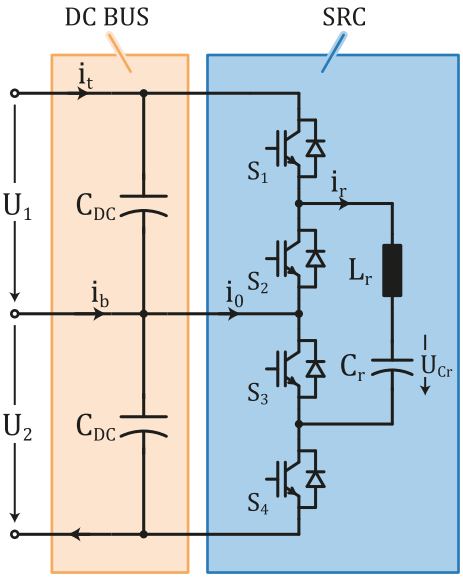


**FIGURE 1.** Series resonant converter topology connected across split DC bus capacitors.

section, the stability of the SRC operation in DCM2 is discussed, as well as the steady-state operation in ideal and non-ideal case.

### A. STABILITY OF THE STEADY-STATE OPERATION

The DCM2 operation is achieved in case the switching frequency of the SRC is at least two times lower than the resonant frequency [32], [33], i.e.

$$f_s \leq \frac{f_0}{2} \tag{1}$$

In this case, the gain is not constant and equal to 1, but dependent on the switching frequency [32], [33]. Also, contrary to the DCM operation of the SRC, the DCM2 operation contains six different switching states (four of which are the conduction states, while the remaining two are the idle states), as shown in Fig. 2.

Without losing generality, let us start the analysis by assuming that the voltage across the lower DC bus capacitor is higher than the voltage across the upper DC bus capacitor (i.e. $U_2 > U_1$). In this case the modulation is such that only the switch $S_4$ is on during $t \in \left(0, \frac{T_0}{2}\right)$, and only the switch $S_3$ is on during $t \in \left(\frac{T_s}{2}, \frac{T_s}{2} + \frac{T_0}{2}\right)$. On the other hand, the switches $S_1$ and $S_2$ are used in case the voltage across the upper DC bus capacitor is higher than the voltage across the lower DC bus capacitor, enabling the bidirectional operation of the SRC. Therefore, with the assumption, which will be justified later in this section, that the voltage at the beginning of the period $i$ is positive and satisfies the inequality

$$U_{C_{r_0}} < U_2 - U_1, \tag{2}$$

the steady-state operation can be analysed through switching states represented in Fig. 2 as follows:

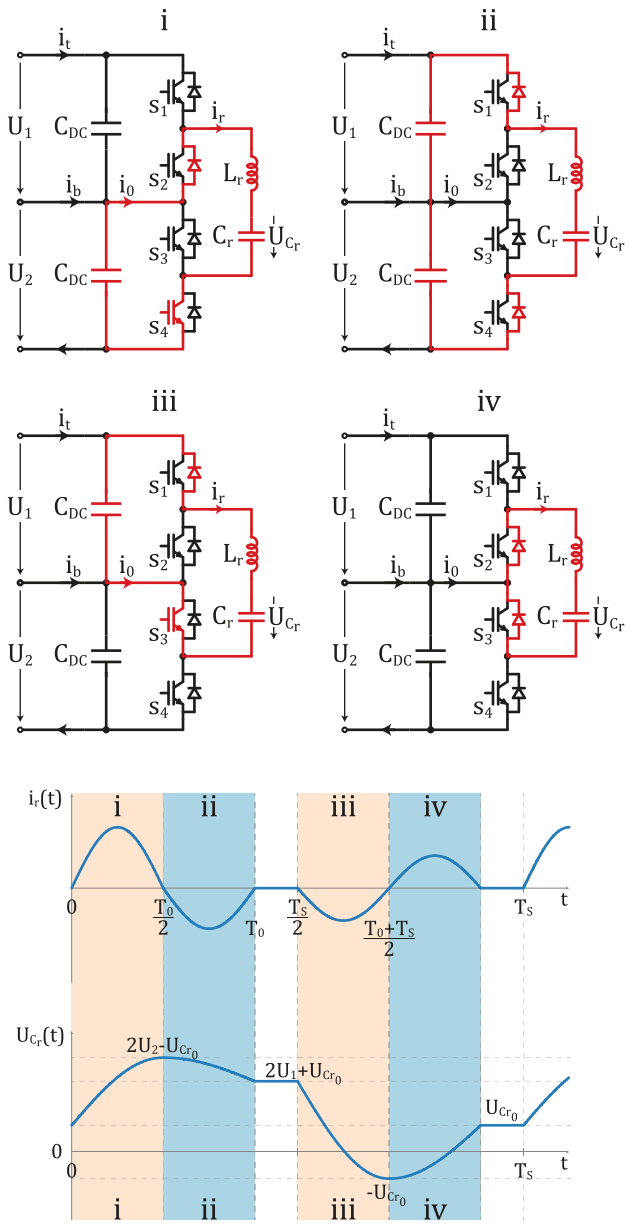


**FIGURE 2.** Switching states of the SRC operating in DCM2, in case $U_2 > U_1$, and respective resonant current, $i_r$, and resonant capacitor voltage, $U_{Cr}$, waveforms.

i. Switch $S_4$ and diode $D_2$ are conducting: $t \in \left(0, \frac{T_0}{2}\right)$.
During this period, the resonant capacitor is being charged by the lower DC bus capacitor. This period ends when the resonant current falls back to zero and at this moment, the voltage across resonant capacitor can be expressed as

$$U_{C_r}\left(t = \frac{T_0}{2}\right) = 2U_2 - U_{C_{r0}} \tag{3}$$

Having the assumption given in (2), the voltage $U_{C_r}\left(t = \frac{T_0}{2}\right)$ is higher than $U_1 + U_2$, and hence, the diodes $D_1$ and $D_4$ are forward biased and can start conducting.

ii. Diodes $D_1$ and $D_4$ are conducting: $t \in \left(\frac{T_0}{2}, T_0\right)$.
During this period, the resonant capacitor voltage is discharged through full DC bus. This period ends when the resonant current falls back to zero and at this moment the voltage across the resonant capacitor can be expressed as

$$U_{C_r}\,(t = T_0) = 2U_1 + U_{C_{r0}} \tag{4}$$

Since the voltage $U_{C_r}\,(t = T_0)$ is lower than $U_1 + U_2$, all four diodes are reverse polarized and the resonant tank is idle until the next switching action.

iii. Switch $S_3$ and diode $D_1$ are conducting: $t \in \left(\frac{T_s}{2}, \frac{T_s}{2} + \frac{T_0}{2}\right)$.
This period starts by turning-on the switch $S_3$ and since the voltage $U_{C_r}\,(t = T_0)$ is higher than the voltage $U_1$, the resonant capacitor is being discharged through the upper DC bus capacitor. The voltage across the resonant capacitor at the end of this period can be expressed as

$$U_{C_r}\left(t = \frac{T_s}{2} + \frac{T_0}{2}\right) = -U_{C_{r0}} \tag{5}$$

Having that the voltage $U_{C_r}\left(t = \frac{T_s}{2} + \frac{T_0}{2}\right)$ is negative, the diodes $D_2$ and $D_3$ are forward biased and can start conducting.

iv. Diodes $D_2$ and $D_3$ are conducting: $t \in \left(\frac{T_s}{2} + \frac{T_0}{2}, \frac{T_s}{2} + T_0\right)$.
During this period the resonant tank is being short-circuited. At the end of this period the voltage across the resonant capacitor is

$$U_{C_r}\left(t = \frac{T_s}{2} + T_0\right) = U_{C_{r0}} \tag{6}$$

At the end of this period, the resonant tank is idle again until the next switching period. The resonant current remains equal to zero, and the resonant capacitor voltage, expressed in (6), is constant. Hence, the resonant capacitor voltage at the end of the switching period is equal to the resonant capacitor voltage at the beginning of the switching period, meaning that the SRC is in steady-state.

The above analysis assumed the inequality (2). To justify this assumption, let's assume that this inequality is not satisfied, i.e.

$$U_{C_{r0}} \geqslant U_2 - U_1 \tag{7}$$

From the equation (3), the voltage at the end of period $i$ is

$$U_{C_r}\left(t = \frac{T_0}{2}\right) = 2U_2 - U_{C_{r0}} \tag{8}$$

Combined with the inequality (7), the voltage across the resonant capacitor at the end of the period $i$ is lower than total DC bus voltage, i.e.

$$U_{C_r}\left(t = \frac{T_0}{2}\right) \leqslant U_1 + U_2 \tag{9}$$

Therefore, all diodes are reverse polarized and the resonant tank is idle until the next switching action (i.e. until the period *iii*). Furthermore, at the end of the period *iii* the voltage across the resonant capacitor can be expressed as

$$U_{C_r}\left(t=\frac{T_s}{2}+\frac{T_0}{2}\right)=-2(U_2-U_1)+U_{C_{r_0}} \tag{10}$$

From the equation (10) and considering the inequality (7), two possible cases are distinguishable:

- Case1: $U_{C_{r_0}} > 2(U_2-U_1)$
  In this case, the voltage at the end of the period *iii* is higher than zero, all diodes are reverse polarized and the resonant tank remains idle until the next switching period. Additionally, the voltage at the beginning of the next switching period is lower than $U_{C_{r_0}}$ by $(U_2-U_1)$. Hence, this case is repeated until the condition $U_{C_{r_0}} > 2(U_2-U_1)$ is not satisfied anymore, and either inequality (2) or the second case condition is satisfied.
- Case2: $U_2-U_1 < U_{C_{r_0}} < 2(U_2-U_1)$
  In this case, the voltage at the end of the period *iii* is negative, the diodes $D_2$ and $D_3$ are forward biased and can start conducting (i.e. the period *iv* occurs). Therefore, the voltage at the end of the period *iv* is

  $$U_{C_r}\left(t=\frac{T_s}{2}+T_0\right)=2(U_2-U_1)-U_{C_{r_0}} \tag{11}$$

  Combining the equation (11) and the given condition in this case, i.e. $U_2-U_1 < U_{C_{r_0}} < 2(U_2-U_1)$, the voltage across the resonant capacitor at the end of the period *iv* and hence at the beginning of the next switching period is

  $$U_{C_r}(t=T_s) \in (0, U_2-U_1) \tag{12}$$

Hence, from the equation (12) it can be concluded that either assumed inequality (2) is satisfied, or it will be satisfied after certain number of switching periods, without any control action, ensuring convergence towards the steady-state operation.

### B. IDEAL OPERATION

In the steady-state the average current extracted from the midpoint of the DC bus, $I_0$, has to compensate the average current injected in the midpoint of the DC bus, $I_b$. Considering the Fig. 2, the SRC extracts the current from the DC bus midpoint during intervals *i* and *iii*. Hence, during interval *i*, the voltage $U_2$ is applied across resonant tank and the differential equation describing the resonant circuit during this interval can be expressed as

$$U_2 = u_{C_{r_1}} + L_r\frac{di_{r_1}}{dt} \tag{13}$$

Together with the initial conditions (the initial resonant current is zero and initial voltage across resonant capacitor is $U_{C_{r_0}}$), the resonant capacitor voltage and the resonant current can be expressed as

$$u_{C_{r_1}}(t) = U_{C_{r_0}}cos(\omega_0 t) + U_2(1-cos(\omega_0 t)) \tag{14a}$$

$$i_{r_1}(t) = \omega_0 C_r(U_2 - U_{C_{r_0}})sin(\omega_0 t) \tag{14b}$$

Furthermore, the average current extracted from the DC bus midpoint regarding the period *i*, $I_{r1}$, is calculated as

$$I_{r1} = \frac{1}{T_s}\int_0^{\frac{T_0}{2}} i_{r_1}(t)\,dt = 2f_sC_r(U_2 - U_{C_{r_0}}) \tag{15}$$

Considering the period *iii*, the voltage applied across resonant tank is $U_1$ and the differential equation describing the resonant circuit during this period can be expressed as

$$U_1 = u_{C_{r_3}} + L_r\frac{di_{r_3}}{dt} \tag{16}$$

By solving the equation (16) and considering the initial conditions (the initial resonant current is zero and initial voltage across resonant capacitor is given in the equation (4)), the resonant capacitor voltage and the resonant current during this period can be expressed as

$$u_{C_{r_3}}(t) = U_{C_{r_0}}cos(\omega_0 t) + U_1(1+cos(\omega_0 t)) \tag{17a}$$

$$i_{r_3}(t) = -\omega_0 C_r(U_1 + U_{C_{r_0}})sin(\omega_0 t) \tag{17b}$$

Hence, the average current extracted from the DC bus midpoint during interval *iii*, $I_{r3}$, is calculated as

$$I_{r3} = \frac{1}{T_s}\int_0^{\frac{T_0}{2}} -i_{r_3}(t)\,dt = 2f_sC_r(U_1 + U_{C_{r_0}}) \tag{18}$$

Combining the equations (15) and (18) the total average current extracted from the DC bus midpoint by SRC, $I_0$, can be expressed as

$$I_0 = 2f_sC_r(U_1+U_2) \tag{19}$$

In addition to the resonant current expressed in (14b) and (17b), for periods *i* and *iii* the current waveforms during periods *ii* and *iv*, $i_{r_2}$ and $i_{r_4}$ respectively, can be expressed as

$$i_{r_2} = \omega_0 C_r(U_1 - U_2 + U_{C_{r_0}})sin(\omega_0 t) \tag{20a}$$

$$i_{r_4} = \omega_0 C_r U_{C_{r_0}} sin(\omega_0 t) \tag{20b}$$

Hence, considering the equations (14), (17) and (20), the average currents, injected by the SRC, in the top and bottom nodes of the DC bus, $I_{rt}$ and $I_{rb}$, can be expressed as

$$I_{rt} = \frac{1}{T_s}2C_rU_2 \tag{21a}$$

$$I_{rb} = \frac{1}{T_s}2C_rU_1 \tag{21b}$$

Furthermore, considering that in the steady-state, those currents have to match the external average currents injected in the top and extracted from the bottom nodes of the DC bus, shown in Fig. 2, i.e. $I_{rt} = -I_t$ and $I_{rb} = I_t + I_b$, the voltages across DC bus capacitors can be expressed as

$$U_1 = \frac{I_t + I_b}{2f_sC_r} \tag{22a}$$

$$U_2 = \frac{-I_t}{2f_sC_r} \tag{22b}$$

Therefore, by considering that the switching frequency, $f_s$, is the control variable and based on the external current injected in the midpoint of the DC bus, $I_b$, the DC bus voltage $U_{DC}$ can be controlled as expressed in the equation (19), and based on the external currents injected/extracted from the top, bottom and midpoint of the DC bus capacitor, the voltages across top and bottom DC bus capacitor, $U_1$ and $U_2$ can be calculated as shown in (22).

Theoretically, in the ideal case, the initial resonant capacitor voltage at the beginning of the switching period, $U_{C_{r_0}}$, can have any value between 0 and $U_2 - U_1$. Hence, from Fig. 2, the resonant capacitor voltage changes in a range from $-U_{C_{r_0}}$ to $2U_2 - U_{C_{r_0}}$, which combined with $U_{C_{r_0}} \in (0, U_2 - U_1)$ yields

$$u_{C_r} \in (-(U_2 - U_1), 2U_2) \tag{23}$$

Therefore, the voltage across the resonant capacitor varies significantly, and hence it should be taken into account when designing the resonant capacitor, i.e. the capacitance of the resonant capacitor should not be strongly dependent on its voltage.

### C. NON-IDEAL OPERATION

Without neglecting the parasitic components, such as parasitic series resistances of the resonant inductor, $r_L$, switch on-resistance, $r_{ce}$, diode on-resistance, $r_{d_{on}}$ and resonant capacitor equivalent series resistance, $ESR$, and switch and diode forward voltages, $U_{F_s}$ and $U_{F_d}$, are not neglected, the differential equations describing each conductive time period (i.e. $i$, $ii$, $iii$ and $iv$ shown in Fig. 2) can be expressed as

$$E_x = R_{par_x} i_r + L_r \frac{di_r}{dt} + u_{C_r} \tag{24a}$$

$$i_r = C_r \frac{du_{C_r}}{dt} \tag{24b}$$

where $E_x$ is the voltage applied across the resonant tank in different time periods, i.e.

$$E_i = U_2 - U_{F_s} - U_{F_d} \tag{25a}$$

$$E_{ii} = U_1 + U_2 + 2U_{F_d} \tag{25b}$$

$$E_{iii} = U_1 + U_{F_s} + U_{F_d} \tag{25c}$$

$$E_{iv} = -2U_{F_d} \tag{25d}$$

Also, $R_{par_x}$ represents the total parasitic resistance in different time periods, depending whether transistor and diode, or two diodes are conducting, i.e.

$$R_{par_i} = R_{par_{iii}} = r_{L_r} + ESR + r_{ce} + r_{d_{on}} \tag{26a}$$

$$R_{par_{ii}} = R_{par_{iv}} = r_{L_r} + ESR + 2r_{d_{on}} \tag{26b}$$

Similarly to the ideal case, by solving the differential equations given in (24), the average values of the resonant current in each time interval $i$,$ii$,$iii$ and $iv$ can be expressed as

$$I_{r_x} = f_s C_r \left(1 + e^{-\frac{\pi}{2}\frac{R_{par_x}}{2\omega_x L_r}}\right) A_x \tag{27}$$

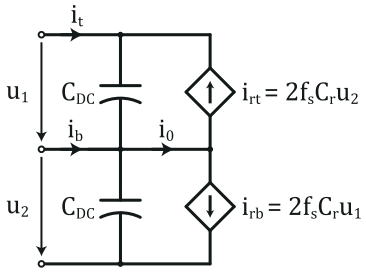


**FIGURE 3.** Linearized average model of the SRC connected across split DC bus and operating in DCM2.

where $x$ denotes the time interval (i.e. $x = i|ii|iii|iv$), and constants $A_x$ can be calculated as

$$A_i = U_2 - U_{C_{r_0}} - U_{F_s} - U_{F_d} \tag{28a}$$

$$A_{ii} = U_1 + U_{F_s} + 3U_{F_d} - A_i e^{-\frac{\pi}{2}\frac{R_{par_i}}{\omega_i L_r}} \tag{28b}$$

$$A_{iii} = -U_2 - U_{F_d} + U_{F_s} - A_{ii} e^{-\frac{\pi}{2}\frac{R_{par_{ii}}}{\omega_{ii} L_r}} \tag{28c}$$

$$A_{iv} = -U_1 - U_{F_s} - 3U_{F_d} - A_{iii} e^{-\frac{\pi}{2}\frac{R_{par_i}}{\omega_i L_r}} \tag{28d}$$

Also, the angular frequencies $\omega_i$ and $\omega_{ii}$ are calculated as

$$\omega_i = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_{par_i}}{2L_r}\right)^2} \tag{29a}$$

$$\omega_{ii} = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_{par_{ii}}}{2L_r}\right)^2} \tag{29b}$$

Furthermore, the average values of the current extracted from the midpoint of the DC bus, $I_0$, and of the current injected in the top and bottom of the DC bus, $I_{rt}$ and $I_{rb}$, can be calculated from the equations (27) and (28) as

$$I_0 = I_{r_i} - I_{r_{iii}} \tag{30a}$$

$$I_{rt} = -I_{r_{ii}} - I_{r_{iii}} \tag{30b}$$

$$I_{rb} = I_{r_i} + I_{r_{ii}} \tag{30c}$$

Lastly, the residual voltage across the resonant capacitor $U_{C_{r_0}}$ can be expressed as

$$U_{C_{r_0}} = \left(1 + e^{-a_i} e^{-a_{ii}}\right)^{-1} \left[U_2 e^{-a_i} e^{-a_{ii}} - U_1 e^{-a_{ii}} - \left(U_{F_s} + U_{F_d}\right) e^{-a_{ii}} \left(1 + e^{-a_i}\right) - 2U_{F_d} \left(1 + e^{-a_{ii}}\right)\right] \tag{31}$$

where $a_i$ and $a_{ii}$ can be calculated as

$$a_i = \frac{\pi}{2} \frac{R_{par_i}}{\omega_i L_r} \tag{32a}$$

$$a_{ii} = \frac{\pi}{2} \frac{R_{par_{ii}}}{\omega_{ii} L_r} \tag{32b}$$

## III. LINEARIZED AVERAGE MODEL AND TRANSIENT BEHAVIOR

In previous section, the steady-state operation of the SRC operating in DCM2 is described. For the purpose of the control design, it is useful to now derive a linearzied average

model. Therefore, in this section, the linearized average model of the SRC is presented, and from it, all transfer functions of interest are derived, together with the control-to-output transfer functions in two examples.

From the analysis given in the previous sections, the linearized average model of the SRC operating in DCM2 can be derived using the equivalent circuit shown in Fig. 3. The currents injected in top and bottom nodes of the DC bus, $i_{rt}$ and $i_{rb}$, respectively, and the current extracted from the midpoint of the DC bus, $i_0$, can be expressed as

$$i_{rt} = 2 f_s C_r u_2 \tag{33a}$$
$$i_{rb} = 2 f_s C_r u_1 \tag{33b}$$
$$i_0 = 2 f_s C_r \left(u_1 + u_2\right) \tag{33c}$$

On the other hand, the currents $i_b$ and $i_t$ are dependent on the external circuit and can be considered as disturbances. From the linearized average model given in Fig. 3, the two state equations can be written as

$$C_{DC} \frac{du_1(t)}{dt} = i_t(t) + i_{rt}(t) \tag{34a}$$
$$C_{DC} \frac{du_2(t)}{dt} = i_b(t) + i_t(t) - i_{rb}(t) \tag{34b}$$

Considering the small-signal approximation, i.e. by exchanging each variable $a(t)$ with its DC value and a small perturbation, i.e. $a(t) = A + \tilde{a}(t)$, the DC values of voltages $U_1$ and $U_2$ can be expressed from the equations (33) and (34) as

$$U_1 = \frac{I_b + I_t}{2F_s C_r} \tag{35a}$$
$$U_2 = -\frac{I_t}{2F_s C_r} \tag{35b}$$

Additionally, the AC system of equations can be written in Laplace domain as

$$sC_{DC}U_1(s) = I_t(s) + 2F_s C_r U_2(s) + 2C_r U_2 f_s(s) \tag{36a}$$
$$sC_{DC}U_2(s) = I_b(s) + I_t(s) - 2F_s C_r U_1(s) - 2C_r U_1 f_s(s) \tag{36b}$$

From the system of equations given in (36), the transfer functions describing the response of voltages $u_1$ and $u_2$ on the changes in switching frequency $f_s$ (i.e. control variable) can be expressed as

$$H_{f1}(s) = \frac{U_1(s)}{f_s(s)} = 2\frac{C_r}{C_{DC}} U_2 \frac{s - 2F_s \frac{C_r}{C_{DC}} \frac{U_1}{U_2}}{s^2 + \left(2F_s \frac{C_r}{C_{DC}}\right)^2} \tag{37a}$$

$$H_{f2}(s) = \frac{U_2(s)}{f_s(s)} = -2\frac{C_r}{C_{DC}} U_1 \frac{s + 2F_s \frac{C_r}{C_{DC}} \frac{U_2}{U_1}}{s^2 + \left(2F_s \frac{C_r}{C_{DC}}\right)^2} \tag{37b}$$

Furthermore, the transfer functions describing the response of the voltages $u_1$ and $u_2$ on the disturbances (i.e. currents $i_t$ and $i_b$) can be expressed as

$$H_{I_{t_1}} = \frac{U_1(s)}{I_t(s)} = \frac{1}{C_{DC}} \frac{s + 2F_s \frac{C_r}{C_{DC}}}{s^2 + \left(2F_s \frac{C_r}{C_{DC}}\right)^2} \tag{38a}$$

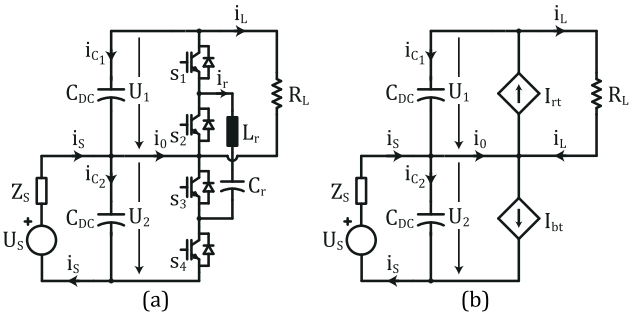


**FIGURE 4.** The SRC connected across split DC bus capacitor with stable voltage, $U_S$, connected across lower DC bus capacitor, and load resistor, $R_L$, connected across upper DC bus capacitor: (a) circuit diagram, (b) linearized average model.

$$H_{I_{t_2}} = \frac{U_2(s)}{I_t(s)} = \frac{1}{C_{DC}} \frac{s - 2F_s \frac{C_r}{C_{DC}}}{s^2 + \left(2F_s \frac{C_r}{C_{DC}}\right)^2} \tag{38b}$$

$$H_{I_{b_1}} = \frac{U_1(s)}{I_b(s)} = 2F_s \frac{C_r}{C_{DC}^2} \frac{1}{s^2 + \left(2F_s \frac{C_r}{C_{DC}}\right)^2} \tag{38c}$$

$$H_{I_{b_2}} = \frac{U_2(s)}{I_b(s)} = \frac{1}{C_{DC}} \frac{s}{s^2 + \left(2F_s \frac{C_r}{C_{DC}}\right)^2} \tag{38d}$$

Therefore, from the given transfer functions in (37) and (38), and depending on the system level requirements, the control algorithms can be developed.

The transfer functions given in (37) and (38) can be used in general, where the external circuit defines the disturbance currents $i_t$ and $i_b$, while with the switching frequency $f_s$, the voltage $u_1$, $u_2$, or their sum $u_1 + u_2$, are controlled, depending on the system requirements. However, to analyze the dynamic behavior of the SRC operating in DCM2, two examples of the external circuit are given in the following subsections.

### A. EXAMPLE A

Considering the case where the stable voltage (i.e. DC voltage source or large external capacitance) is connected across the lower DC bus capacitor, and load resistance is connected across the upper DC bus capacitor, as shown in Fig. 4(a), the transfer function describing the response of the voltage across the upper DC bus capacitor, $u_1$, on the changes in switching frequency, $f_s$, can be derived.

The linearized average model in the given case is presented in Fig. 4(b), in which the currents $I_{rt}$ and $I_{rb}$ are expressed in the equation (21). Also, since the voltage across lower DC bus capacitance is constant, i.e. $U_2 = U_S$, the differential equation describing the voltage across the upper DC bus capacitor can be written as

$$C_{DC} \frac{du_1(t)}{dt} = i_{rt}(t) - i_L(t) = 2C_r U_2 f_s(t) - \frac{u_1(t)}{R_L} \tag{39}$$

By considering that the voltage $u_1(t)$ and switching frequency $f_s(t)$ are composed of DC component and a small disturbance, i.e. $u_1(t) = U_1 + \tilde{u}_1(t)$ and $f_s(t) = F_s + \tilde{f}_s(t)$, the DC value

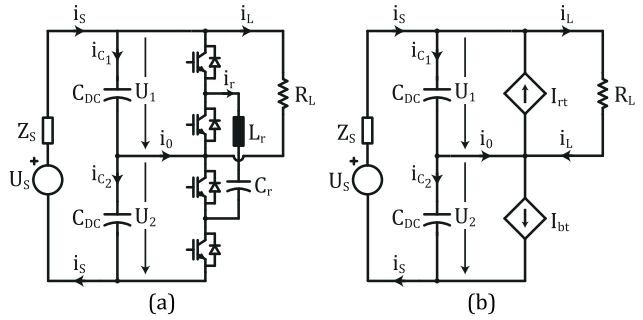


**FIGURE 5.** The SRC connected across split DC bus capacitor with stable voltage, $U_S$, connected across DC bus, and load resistor, $R_L$, connected across upper DC bus capacitor: (a) circuit diagram, (b) linearized average model.

of the voltage across the upper DC bus capacitance can be calculated from the differential equation (39) as

$$U_1 = 2F_s C_r R_L U_2 \tag{40}$$

Additionally, the transfer function describing the response of the voltage $U_1(s)$ on the changes in switching frequency $f_s(s)$ can be expressed as

$$H_1(s) = \frac{U_1(s)}{f_s(s)} = 2\frac{C_r}{C_{DC}} U_2 \frac{1}{s + \frac{1}{R_L C_{DC}}} \tag{41}$$

The same result can be obtained from the equations (36) and by considering conditions of this example, i.e. $U_2 = const.$ and $i_t\,(t) = \frac{u_1(t)}{R_L}$.

As it can be seen from (41), the transfer function $H_1(s)$ has a single pole, real and negative, i.e. $s_p = -\frac{1}{R_L C_{DC}}$, and hence, the response of the voltage $u_1$ on the step change in the switching frequency, $f_s$, is exponential, with the time constant $\tau = R_L C_{DC}$.

### B. EXAMPLE B

Similarly to the previous case, the case where the stable voltage (i.e. DC voltage source, or large external DC bus capacitance) is connected across full DC bus, $U_{DC} = U_S$, and the load resistance is connected across the upper DC bus capacitor, presented in Fig. 5(a), the two transfer functions describing the responses of the voltages $u_1$ and $u_2$ on the changes in switching frequency $f_s$ can be derived.

The linearized average model in this case is presented in Fig. 5(b), in which the currents $I_{rt}$ and $I_{rb}$ are expressed in (21). Hence, from the linearized average model given in Fig. 5(b) and (21), the state equations in this case can be expressed as

$$C_{DC}\frac{du_1(t)}{dt} = i_s(t) + 2C_r f_s(t) u_2(t) - \frac{u_1(t)}{R_L} \tag{42a}$$

$$C_{DC}\frac{du_2(t)}{dt} = i_s(t) - 2C_r f_s(t) u_1(t) \tag{42b}$$

Furthermore, by considering that the voltage $u_1(t)$ and the switching frequency $f_s(t)$ are composed of the DC component and a small disturbance, i.e. $u_1(t) = U_1 + \tilde{u}_1(t)$ and $f_s(t) = F_s + \tilde{f}_s(t)$, and since the voltage $u_2(t)$ can be expressed as

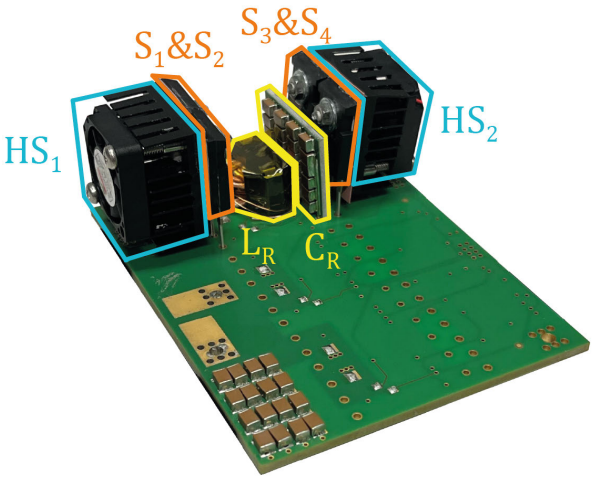


**FIGURE 6.** The Series Resonant Balancing Converter prototype: resonant inductor $L_r$; resonant capacitor $C_r$; switches $S_{1,2,3,4}$; and heat sinks $HS_{1,2}$.

$u_2(t) = U_{DC} - u_1(t)$, the DC values of the voltages $u_1$ and $u_2$ can be expressed from the (42) as

$$U_1 = 2F_s C_r R_L U_{DC} \tag{43a}$$

$$U_2 = U_{DC} - U_1 \tag{43b}$$

Additionally, the transfer functions describing the response of the voltages $U_1(s)$ and $U_2(s)$ on the changes in switching frequency $f_s(s)$ can be expressed as

$$H_1(s) = \frac{U_1(s)}{f_s(s)} = \frac{C_r}{C_{DC}} U_{DC} \frac{1}{s + \frac{1}{2R_L C_{DC}}} \tag{44a}$$

$$H_2(s) = \frac{U_2(s)}{f_s(s)} = -\frac{C_r}{C_{DC}} U_{DC} \frac{1}{s + \frac{1}{2R_L C_{DC}}} \tag{44b}$$

The results obtained in (44) can be obtained from the equations (36) by considering the conditions of this example, i.e. $U_1 + U_2 = const.$ and $i_t\,(t) = -\frac{u_1(t)}{R_L}$.

Both transfer functions given in (44) have a single pole, real and negative, i.e. $s_p = -\frac{1}{2R_L C_{DC}}$, and hence, the response of voltages $u_1$ and $u_2$ on the step change in switching frequency, $f_s$, is exponential, with the time constant $\tau = 2R_L C_{DC}$.

## IV. EXPERIMENTAL RESULTS

This section shows expermiental verifications performed on the developed prototype of SRC operating in DCM2. Besides the steady-state verifications, the proposed dynamic model is verified in transient conditions using the two configurations presented in Fig. 4 and Fig. 5.

### A. PROTOTYPE

The prototype is shown in Fig. 6, and the prototype components, together with the laboratory equipment used during testing are given in TABLE 1. Additionally, the laboratory test setup is shown in Fig. 7.

The core of the resonant inductor is RM7 ferrite core from TDK (part number: B65819J0000R087), and the resonant

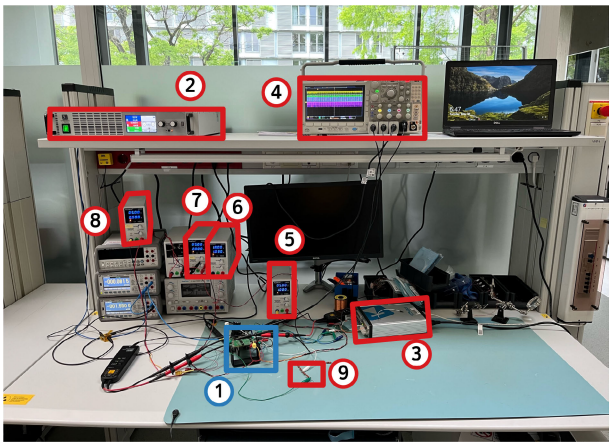


**FIGURE 7.** Laboratory setup: 1 - prototype; 2 - DC source; 3 - RT Box; 4 - oscilloscope; 5,6,7,8 - auxiliary supplies; 9 - load resistor.

**TABLE 1.** SRC components and laboratory equipment.

| Designator | Component | Part number |
|---|---|---|
| $L_r$ | Resonant inductor | / |
| $C_r$ | Resonant capacitors | CGA8N4X7T2W474K |
| $C_{DC}$ | DC bus capacitors | EKXL451ELL330MK25S |
| $S_{1,2,3,4}$ | IGBTs | IKW50N65H5 |
| HS1, HS2 | Heat sinks | ATS-61290K-C1-R0 |
| / | Fans | MA2506H05C-RSR |
| 2 | DC source | EA-PSI 9750-06 2U |
| 3 | Plexim RT Box CE | / |
| 4 | Oscilloscope | Tektronix MDO3104 |
| 5, 6, 7 | Auxiliary power supplies | PeakTech 6226 |
| 8 | Load resistors | RR03J3R0TB |

inductor winding is made of Litz wire (135x0.071 *mm*), with 3 turns and 4 parallel windings. The resonant capacitor consists of 2 ceramic capacitors in parallel and the capacitance of the DC bus capacitors is $C_{DC} = 33\ \mu$F. The *RTBox* is used as a PWM generator and to initiate the transient by step changing the switching frequency.

### B. EXPERIMENTAL VERIFICATION OF THE STEADY-STATE OPERATION

The circuit used to verify the steady-state operation of the SRC operating in DCM2 is shown in Fig. 5(a). The source is connected across lower DC bus capacitance, and its voltage is 30 V. The voltage across the upper DC bus capacitance is around 6 V and the total DC bus voltage is around 36 V. The obtained waveforms are shown in Fig. 8. The cyan and blue colored waveforms are voltages across upper and lower DC bus capacitance, respectively. The full DC bus voltage is in green, while the resonant current is depicted in magenta.

As it can be seen on Fig. 8, the SRC is operating in DCM2, with much smaller conducting periods compared to the switching frequency. Additionally, since the conductive periods are short compared to the switching period, the resonant current has relatively high spikes, causing non-negligible voltage ripples across DC bus capacitors. In case the system

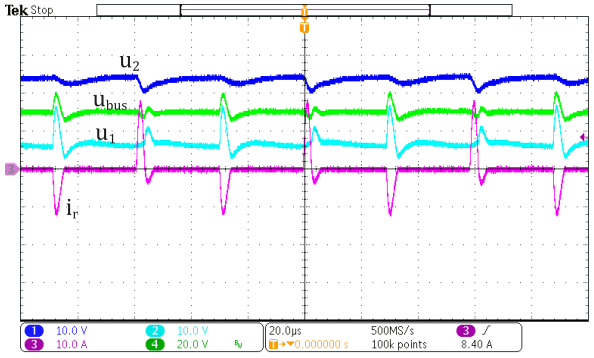


**FIGURE 8.** Waveforms of the resonant current, $i_r$, upper and lower DC bus voltages $u_1$ and $u_2$, and total DC bus voltage, $u_{bus}$, during the steady-state operation of the SRC in DCM2.

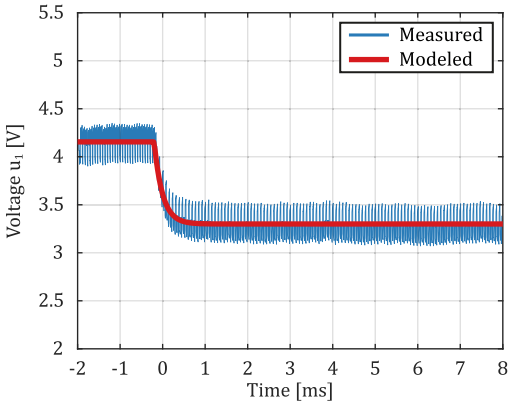


**FIGURE 9.** Comparison between modeled and measured response of the upper DC bus voltage, $u_1$, on the step change in switching frequency, $f_s$, in example A, presented in Fig. 4(a).

requirements are not allowing large voltage ripples, the higher values of DC bus capacitance can be chosen.

### C. EXPERIMENTAL VERIFICATION OF THE TRANSIENT BEHAVIOR

Considering the examples A and B, given in section III, the transient behaviour of the SRC operating in DCM2 is experimentally verified. The test circuits are shown in Fig. 4(a) regarding example A, and in Fig. 5(a) regarding the example B, and the test parameters in both cases are:

- Source voltage: $U_S = 30\ V$
- Load resistance: $R_L = 6\ \Omega$
- Resonant inductor: $L_r = 1\ \mu H$
- Resonant capacitor: $C_r = 0.94\ \mu F$

The transient is imposed by step change of the switching frequency $f_s$, from 17 kHz to 13 kHz.

Considering the example A, in Fig. 9 the modeled transient response of the voltage across the upper DC bus capacitor, $u_1$, based on the equation (41), is compared against the measured voltage response. It can be seen that the two traces overlap, verifying the proposed model.

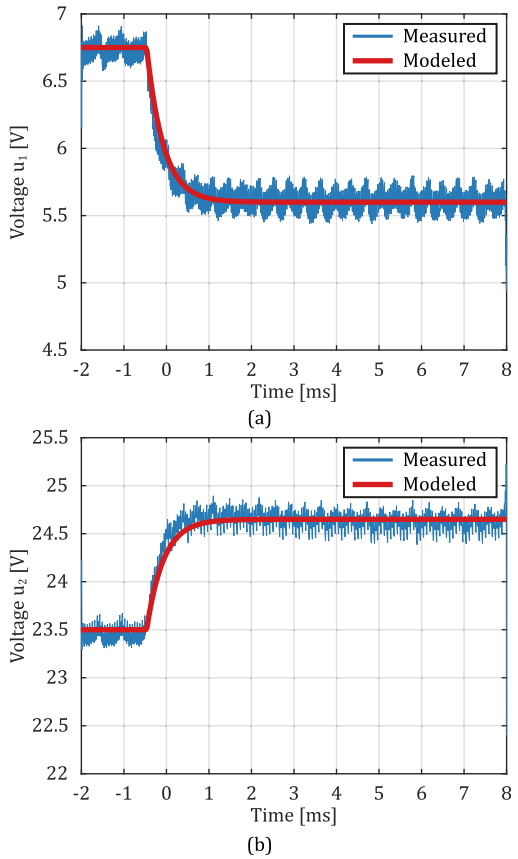


**FIGURE 10.** Comparison between modeled and measured response of the: (a) upper DC bus voltage, $u_1$, (b) lower DC bus voltage, $u_2$; on the step change in switching frequency, $f_s$, in example B, presented in Fig. 5(a).

Considering the example B, in Fig. 10 the modeled transient responses of the voltages across upper and lower DC bus capacitors, $u_1$ and $u_2$, based on the equation (44), are compared to the measured voltage responses. It can be seen that two traces overlap in both Fig. 10(a) and Fig. 10(b), verifying the proposed model.

As it can be seen on Fig. 9 and Fig. 10, the modeled transients responses match with the measured ones.

### D. EXPERIMENTAL VERIFICATION OF THE CLOSED-LOOP OPERATION

Considering the example A given in Fig. 4(a), i.e. with stable voltage $u_2$, and based on the transfer function derived in (41), the voltage $u_1$ can be controlled with the switching frequency. The control loop is closed with the PI regulator, as shown in Fig. 11. The target bandwidth of the closed-loop system is around 10 $Hz$, and hence, all delays of the digital system are neglected since the bandwidth is significantly lower than the sampling rate. From the Fig. 11, the closed-loop transfer function, $H_{CL}(s)$, can be expressed as

$$H_{CL}(s) = \frac{H_1(s)\left(K_p + \frac{K_i}{s}\right)}{1 + H_1(s)\left(K_p + \frac{K_i}{s}\right)} \tag{45}$$

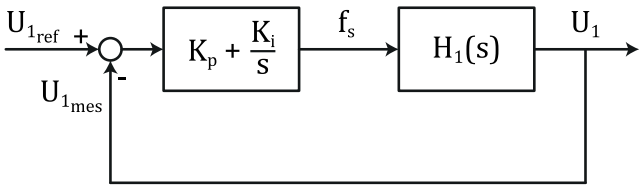


**FIGURE 11.** Diagram of the implemented closed-loop control with PI regulator and the plant $H_1(s)$, expressed in (41). Constants $K_p$ and $K_i$ are the proportional and integral gains of the PI regulator, and $U_{1_{ref}}$ and $U_{1_{mes}}$ are the upper DC bus voltage reference and measured values, respectively.

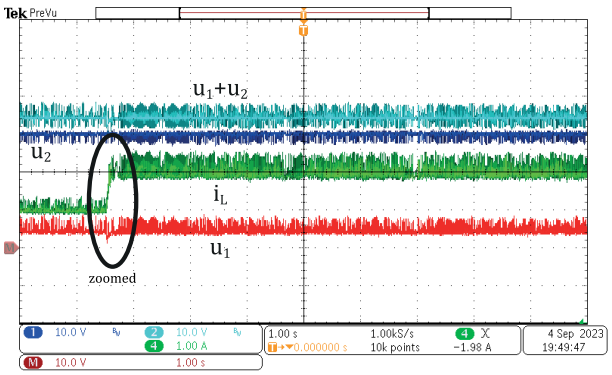


**FIGURE 12.** Waveforms of the full DC bus voltage, $u_1 + u_2$, upper and lower DC bus voltages, $u_1$ and $u_2$, and the load current, $i_L$, during the transient imposed by step changing the load resistance from $R_L = 4\ \Omega$ to $R_L = 2\ \Omega$.

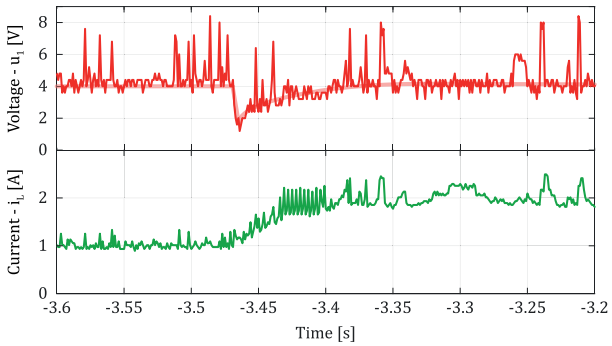


**FIGURE 13.** Zoomed waveforms of the upper DC bus voltage, $u_1$, and the load current, $i_L$, as indicated in Fig. 12.

Furthermore, the PI regulator proportional and integral gains, $K_p$ and $K_i$, respectively, are designed to obtain the bandwidth of the closed-loop control around 10 $Hz$. Hence, from (41) and (45), and having that the test parameters are:

- Source voltage: $U_S = U_2 = 30\ V$
- Resonant inductor: $L_r = 1\ \mu H$
- Resonant capacitor: $C_r = 0.94\ \mu F$
- DC bus capacitor: $C_{DC} = 220\ \mu F$

the gains of the PI regulator are $K_p = 50\ \frac{Hz}{V}$ and $K_i = 250000\ \frac{Hz}{Vs}$. Plexim RT Box CE is used to implement the PI regulator, while the closed-loop control is tested for constant voltage reference, i.e. $U_{1_{ref}} = 4\ V$, and by step changing

the load $R_L$ from 4 Ω to 2 Ω. In Fig. 12 are given obtained waveforms of the voltages $u_2$ and $(u_1 + u_2)$ in blue and cyan colors, respectively, and the load current, $i_L$, in green. In addition, in red is given the waveform of the voltage $u_1$, which is obtained with oscilloscope math function by subtracting the total bus voltage, $(u_1 + u_2)$ with the voltage $u_2$. To better observe the transient behavior, as indicated in Fig. 12, the zoomed waveforms of the voltage $u_1$ and the load current $i_L$ are given in Fig. 13. As it can be seen, the voltage $u_1$ drops approximatelly 50% on the step change of the load resistance and the disturbance is eliminated in around 100 *ms*. Comparing to the other methods of the split DC bus voltages regulation [13], [14], [15], [16], [19], [20], the frequency controlled SRC operating in DCM2 has the ability to operate with soft-switching (i.e. ZCS) irrespective of the load conditions.

## V. CONCLUSION

In this paper, the Series Resonant Converter (SRC), used as an active voltage regulator (AVR) by operating in DCM2, is analysed. The stability of the steady-state operation is presented, together with the modeling of the steady-state operations in ideal and non-ideal cases. These models are experimentaly verified on the developed prototype.

Furthermore, the linearized average model of the SRC operating in DCM2 is presented and used to derive the transfer functions describing the responses of the upper and lower DC bus voltages on the changes in switching frequency. Application examples are presented, for which the transient behavior is experimentally verified. Additionally, the transfer functions describing the responses of DC bus voltages on disturbances, i.e. changes in currents injected in top and midpoint of the DC bus are presented and discussed.

Lastly, the example of a closed-loop control with the PI regulator is presented and experimentally verified in case of a load step-change.

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