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RESEARCH ARTICLE

GaN Monolithic PWM Generator With Dynamic Offset Compensation

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ABSTRACT The first fully integrated GaN pulse width modulation (PWM) generator for power conversion applications is presented in this paper. The solution is implemented in a 0.5-μm technology, avoiding additional pins and external capacitors for sawtooth signal generation while providing high accuracy. Indeed, the large GaN process spreads are addressed through an innovative dynamic offset compensation approach whose clock signal takes advantage of the PWM signal itself. The proposed PWM generator adopts a 6-V power supply and includes a 2^5 digital divider to set the PWM frequency at 500 kHz and the minimum and maximum duty cycles at 6% and 94%, respectively. Experimental results on integrated prototypes validated the correct circuit functionality over the temperature range from –40°C to 120°C. As a main achievement, this work demonstrates effective all-GaN integration of complex mixed analog and digital circuits, thus representing a significant advancement in the approaches to overcome the main limitations of GaN devices and enable fully integrated signal processing implementation.

INDEX TERMS GaN Pulse width modulation generator, GaN ICs, GaN power converters, GaN control circuit, GaN technology.

I. INTRODUCTION

Gallium nitride (GaN) technology is becoming very popular in the power electronics community because it allows for increasing both efficiency and performance while reducing system dimensions [1], [2], [3]. GaN, as a wide bandgap material, can withstand higher voltages with lower area occupation than silicon counterpart. In addition, the GaN/AlGaN heterojunction results in the formation of the two-dimensional electron gas inside the GaN layer, which has high mobility and allows high-frequency operation [4]. For this reason, GaN high electron mobility transistors are naturally on (depletion-mode or D-HEMTs), and only subsequently normally-off or enhancement-mode transistors (E-HEMTs) have been devised for power consumption and reliability reasons. To this end, the most common approach uses a p-GaN gate over a normally-on structure [5].

The promising GaN HEMT properties, especially for RF and power applications, have pushed up the development of low-power GaN devices along with GaN high-power technology to enable the fabrication of all-GaN integrated circuits (ICs) that include both control circuitry and power section. This is required to further reduce parasitics and losses and to increase operating frequency. Several experimental studies have been conducted to validate the possibility of GaN monolithic integration, incorporating functionalities such as driver, overcurrent protection, galvanic isolation, soft start-up, and PWM control [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. Among these functions, PWM generation is one of the most important. It provides a pulse width

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modulated signal, V_{PWM}, whose duty cycle is related to the voltage, V_{RECT}, which is the dc-dc converter output. The goal of duty cycle modulation is to keep V_{RECT} constant regardless of process, voltage, and temperature (PVT) variations.

State-of-the-art PWM generators in GaN technology invariantly use external components to provide a sawtooth wave. This approach is expensive both in terms of area and power consumption and increased manufacturing costs. Moreover, it requires a GaN IC with a high drive capability, and offset compensation is not pursued, which is highly desirable to overcome the typical limitations of the GaN technology [16], [17], [18].

This study focuses on the design and validation of an on-chip high-accuracy GaN PWM generator, which offers advantages in terms of area occupation and cost because no external components are required and solves the problem of process parameter spread using an innovative dynamic offset compensation approach. The circuit was designed to be embedded in a fully integrated GaN galvanic isolation interface, shown in Fig. 1, which consists of two chips and exploits planar micro-antennas for data communication [19]. The PWM generator, which is only briefly described in [19], is a complex mixed-signal circuit employing several building blocks that are accurately specified and analyzed in this paper. Specifically, Sec. II describes the proposed solution and its operating principle. Details of the analog and digital subsections are discussed in Sec. III, highlighting design trade-offs and the main simulation results. Sec. IV presents the experimental measurements validating the proposed approach. Finally, conclusions are drawn in Sec. V.

II. THE PROPOSED SOLUTION

It is well known that the duty cycle of a PWM generator is related to its input voltage level. Specifically, it must decrease (increase) if the converter output voltage exceeds (falls below) the desired value.

PWM generators conventionally exploit an integrator to provide a triangle-wave signal and a comparator with a variable threshold to generate a square wave with a variable duty cycle. In this framework, the main obstacle to fully monolithic GaN implementation is the large HEMT threshold voltage mismatch, which is responsible for a high offset voltage that is compensated via a switched-capacitor (SC) approach as described below.

A. CIRCUIT DESCRIPTION

A simplified schematic of the proposed PWM generator is shown in Fig. 2. It is based on a mixed analog/digital solution, in which SC offset compensation in analog circuits and dynamic biasing in interface digital circuits were adopted to guarantee accuracy against process mismatches.

We begin the description from the digital section, at the bottom of Fig. 2. It includes a 2^5 divider, a D-Flip Flop, a disoverlap circuit, two NOR gates, $NOR_{1,2}$, and two NOT gates, $NOT_{1,2}$, dynamically biased using storage capacitor C_{H3}. Two clock phases, ϕ_1 and ϕ_2, are required for the offset compensation and dynamic biasing, which are generated by the disoverlap circuit exploiting the PWM signal, V_{PWM_C}, as the reference clock to guarantee synchronous operation. All digital gates are implemented in direct coupling FET logic (DCFL), whose pull-down network uses E-HEMTs whereas the pull-up current generator is a D-HEMT, as discussed in Sec. III.

The analog section in Fig. 2 includes an integrator, a comparator, and a resistive divider R_1-R_2. The integrator is composed of an operational transconductance amplifier (OTA_1) whose feedback network, composed of resistor R_{INT} and capacitor C_{INT}, sets the integrator time constant. The storage capacitor C_{H1} with associated switches and an additional filtering capacitor C_1 perform the offset compensation. The integrator input signal, V_{IN}, is derived from V_{RECT} with a voltage partition. The comparator is made up of OTA_2, C_{H2}, and associated switches. OTA_1 and OTA_2 share the same topology.

B. OPERATING PRINCIPLE

During phase ϕ_1, which corresponds to V_{PWM_C} low, offset compensation and reset of the integration capacitor are performed, whereas integration and comparison operations are carried out during phase ϕ_2, with V_{PWM_C} high. The digital section sets the frequency and maximum (minimum) duty

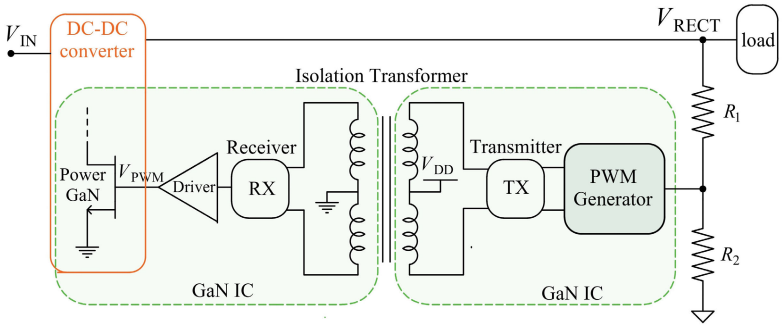

FIGURE 1. Galvanic isolation interface embedding the PWM generator [19].

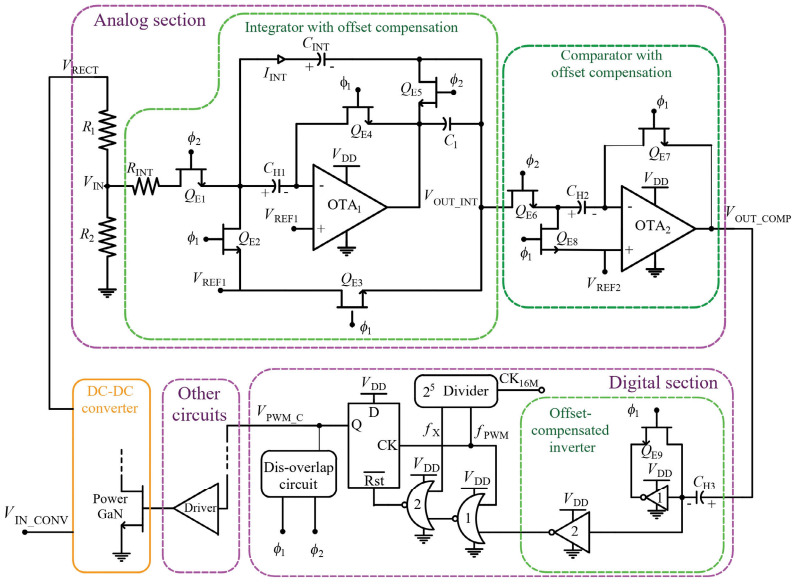

FIGURE 2. Analog and digital sections of the PWM generator.

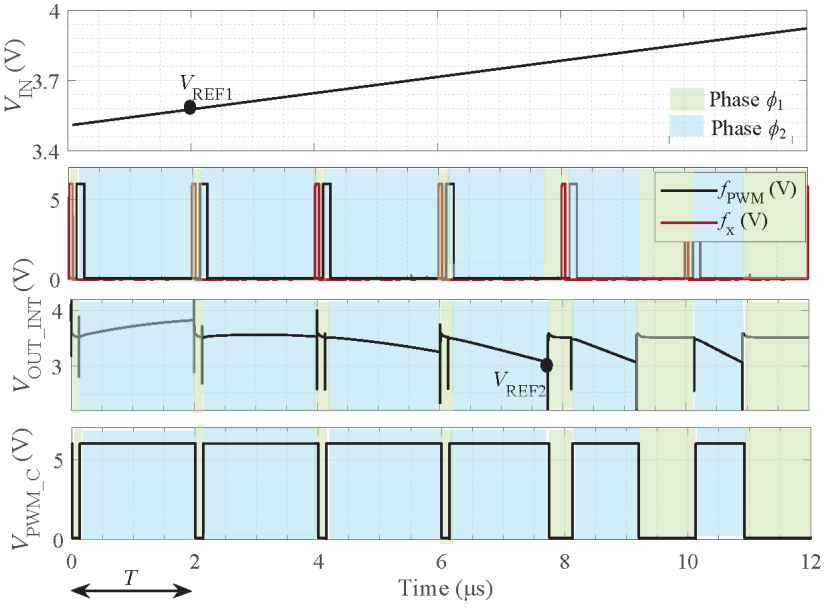

FIGURE 3. Example of circuit operation.

cycles for V_{PWM_C} at 0.5 MHz and 94% (6%), through signals f_{PWM} and f_x, respectively.

Fig. 3, obtained from measurements, illustrates the circuit operating principle. During phase ϕ_1, capacitors C_{H1} and C_{H2} are charged to the offset voltages, V_{OxS1} and V_{OS2} of OTA_1 and OTA_2, through switches Q_{E2}, Q_{E4} and Q_{E7},Q_{E8}, respectively. Moreover, C_{H3} stores the bias voltage of $NOT_{1,2}$ thanks to Q_{E9} that shorts NOT_1 input and output terminals.

Therefore, the current of the pull-down transistor of NOT_1 is mirrored in the pull-down transistor of NOT_2, whose output goes high since the current in its pull-up network was set higher than the pull-down one, as a design constraint, and switching low the output of NOR_1. When the rising edge of clock f_{PWM} arrives, D-Flip Flop output V_{PWM_C} becomes high and phase ϕ_2 starts.

During ϕ_2, current I_{INT} flowing through R_{INT}-C_{INT} is

$$I_{INT} = \frac{V_{REF1} - V_{IN}}{R_{INT}} \tag{1}$$

Assuming negligible V_{IN} variations within the V_{PWM_C} period, T, current I_{INT} is almost constant and then linearly

charges C_{INT} generating a voltage ramp at the integrator output

$$V_{OUT\_INT} = -\frac{I_{INT}}{C_{INT}} \cdot t + V_{REF1} = \frac{V_{REF1} - V_{IN}}{R_{INT}C_{INT}} \cdot t + V_{REF1} \tag{2}$$

During phase ϕ_2, the NOT_2 input follows the comparator output variations and switches accordingly.

In the following, the duty cycle expression is obtained by assuming $V_{REF2} > V_{REF1}$, as a design constraint. If V_{OUT_INT} decreases and reaches V_{REF2} at time, t^*, the comparator output, V_{OUT_COMP}, switches from low to high and NOT_2 output goes low. Consequently, the NOR_1 output goes high because f_{PWM} is low, resetting the D-Flip Flop output through NOR_2 that goes low, thus switching low V_{PWM_C}. A new phase ϕ_1 pulse was also started. The D-Flip Flop reset determines the V_{PWM_C} duty cycle, D, as follows

$$D = \frac{t*}{T} \approx \frac{1}{T}\left(V_{REF2} - V_{REF1}\right)\frac{R_{INT}C_{INT}}{V_{REF1} - V_{IN}} \tag{3}$$

where t* has been derived from (2).

Owing to the positive time slot of f_{PWM}, the reset terminal is disabled for 6% of the PWM period, thus setting the minimum duty cycle value. In addition to satisfying the power transistor switching requirements, a minimum duty cycle is also important to make the circuit insensitive to undesired switching of the comparator at the beginning of phase ϕ_2, which could erroneously determine the duty cycle value.

The output f_X of the divider resets the D-Flip Flop to 94% of T when V_{RECT} is too low and V_{OUT_INT} cannot reach V_{REF2} within a PWM period. This sets the maximum duty cycle for V_{PWM_C} and meets another power switching requirement.

III. DETAILS OF ANALOG AND DIGITAL BUILDING BLOCKS

A. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The schematic of the OTA employed for both the comparator and the integrator is shown in Fig. 4.

TABLE 1. OTA main simulated parameters versus corners.

Corners	TT	FF	SS
V_{DD}-V_{REF} (V)	6-3.5	6-3.5	6-3.5
Standby current (µA)	200	288	98
DC Gain (dB)	70	62	55
Phase margin (deg)	70°	56°	90°
GBW (MHz)	380	640	97
CMRR @ DC (dB)	42	27	34
PSRR @ DC (dB)	67	52	54

It implements a two-stage OTA that is made up of an input differential pair, $Q_{E1,2}$, with the load resistors, $R_{1,2}$, two source followers, Q_{E3}, Q_{E4}, and an output differential pair, $Q_{E5,6}$, with a depletion load, Q_{D5}, and a diode-connected E-mode device, Q_{E7}. The first and second stages provide a gain of approximately 10 and 60 dB, respectively. The source followers act as level shifters to set the correct input bias voltage for pair $Q_{E5,6}$. Because a differential to single-ended conversion is not feasible owing to the lack of p-channel devices, the use of Q_{E7} provides a certain improvement in the symmetry of the second stage.

Bias currents and active loads are performed by the depletion transistors, Q_{D1-5}, using degeneration resistors, R_{4-8}. The bias current values were superimposed on the circuit branches, as shown in Fig. 4. Traditional biasing with E/E current mirrors was avoided since the expected mismatch between transistors is so high that bias current would not be adequately controlled.

Finally, capacitor C_C implements dominant-pole frequency compensation that is needed in both the integrator and comparator during the offset compensation phase (ϕ_1). C_C is removed during the integration phase (ϕ_2) thanks to switch Q_{E8}, thus avoiding overcompensation for the integrator and speed reduction for the comparator.

The aspect ratios of transistors Q_{E1-4}, $Q_{E5,6}$, and Q_{D1-5} were set to 10/1, 20/1, and 5/1 (μm/μm), respectively. Degeneration resistors R_4 and R_8 were set to 12 kΩ, R_5 and R_7 to

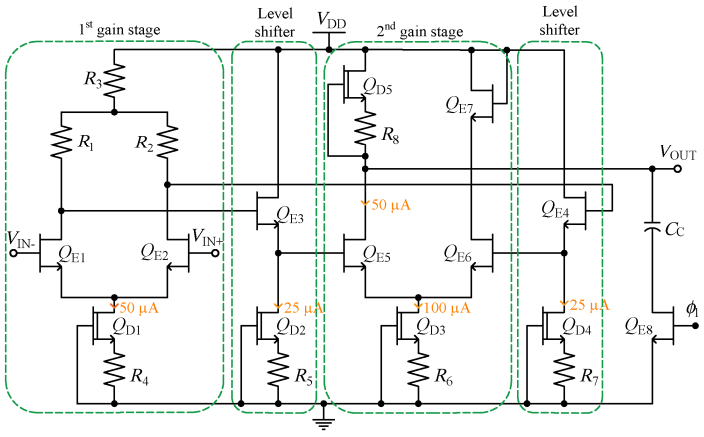

FIGURE 4. OTA schematic diagram.

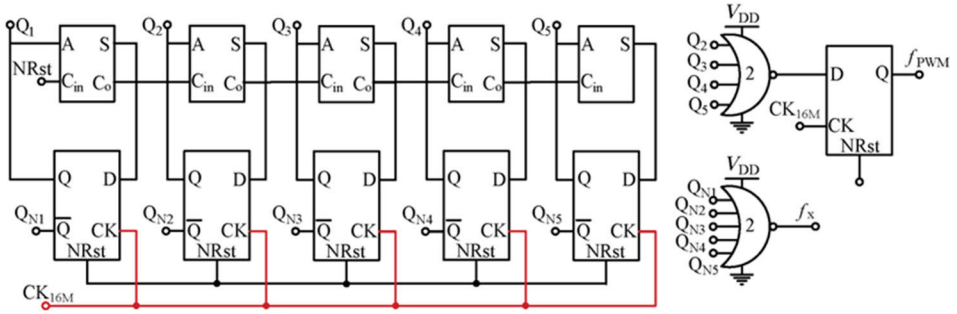

FIGURE 5. Simplified schematic of the frequency divider.

15 kΩ, R_6 to 5 kΩ, and R_1 and R_2 to 30 kΩ. C_C was set to 1 pF.

The simulated DC and small signal parameters for the different process corners (FF, SS, and TT) are summarized in Table 1. The DC gain and gain-bandwidth product (GBW) are higher than 55 dB and 97 MHz, respectively.

B. FREQUENCY DIVIDER

The frequency divider, as shown in Fig. 5, consists of five 1-bit half adders, six master-slave D-flip flops, and two NOR gates. It receives a 16-MHz signal, CK_{16M}, and a reset signal, NRst, as inputs and generates signals f_{PWM} and f_x at 0.5-MHz. The purpose of signal f_x is to set the maximum duty cycle. Signal f_{PWM} is used to set both the frequency and the minimum duty cycle for V_{PWM_C}.

The 1-bit half adder, shown in Fig 6(a), adds two 1-bit digits, C_{IN} and A, and produces two bits, S (sum) and C_{OUT} (carry out). S and C_{OUT} were obtained with an AND gate and XOR gate, respectively. Finally, Fig. 6(b) shows the adopted master-slave D-flip flop which comprises two XOR gates, two NOT gates, and one NAND gate.

The time simulation of the divider is illustrated in Fig. 7. After the reset pulse, signals Q_{1-5} are generated whose frequencies are scaled two, four, eight, sixteen, and thirty-two times compared to that of the clock signal CK_{16M}. Signals Q_2-Q_5 produce in turn signal f_{PWM} owing to NOR_1 and a D-flip flop, whereas Q_{N1}-Q_{N5} produce signal f_x passing through NOR_2 as shown in Fig. 2.

C. LOGIC GATES, DISOVERLAP AND NOT OFFSET COMPENSATION

As already stated, the NOT, NOR, and NAND gates were designed using DCFL logic with degeneration resistors [11].

The phase generator, shown in Fig. 8(a), includes four NOT gates and two NAND gates. It performs two complementary clock phases that are never high at the same time, thus avoiding the simultaneous occurrence of offset compensation and integration phases.

The dynamically biased inverter in Fig 8(b), is made up of two inverters, NOT_1 and NOT_2, a switch, Q_{E9}, and a capacitor, C_{H3}. Because Q_{E2} has the same dimensions as Q_{E1},

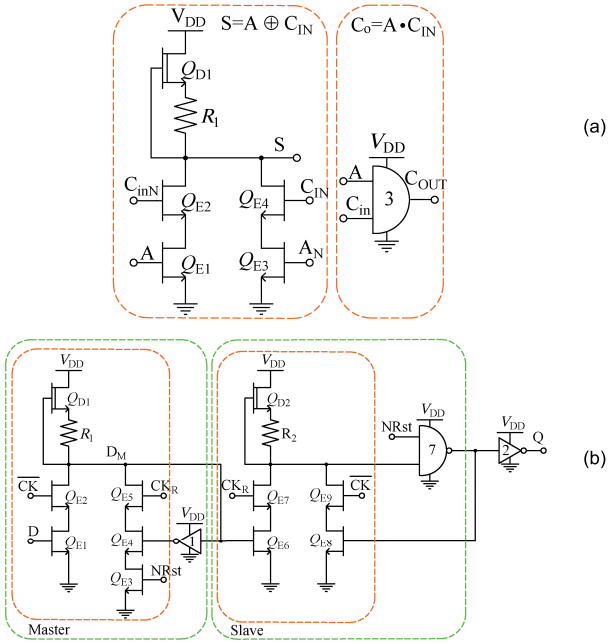

FIGURE 6. Schematic diagrams of: a) 1-bit adder and (b) D-Flip Flop circuit.

it mirrors the same current during phase ϕ_1. Moreover, each current generator in NOT_2, Q_{D2-4} with degeneration resistors R_{2-4}, is a replica of Q_{D1}-R_1, so that the overall pull-up current is three times higher than that of Q_{D1}-R_1 regardless of the process corner. Therefore, during the compensation phase when the storage capacitor C_{H3} is charged to the bias voltage, NOT_2 output switches high, thus maintaining the flip flop in Fig. 2 under reset conditions.

The aspect ratios of all depletion and enhancement transistors of the DCFL gates, divider, D-flip flop, and disoverlap circuit were set to 5/1 (μm/μm), whereas all degeneration resistors in DCFL gates were set to 20 kΩ.

IV. EXPERIMENTAL RESULTS

The circuit was designed and fabricated using a commercial 0.5-μm GaN-on-Si technology. Switches Q_{E1-9} in Fig. 2 were sized with an aspect ratio of 20/1 (μm/μm) and

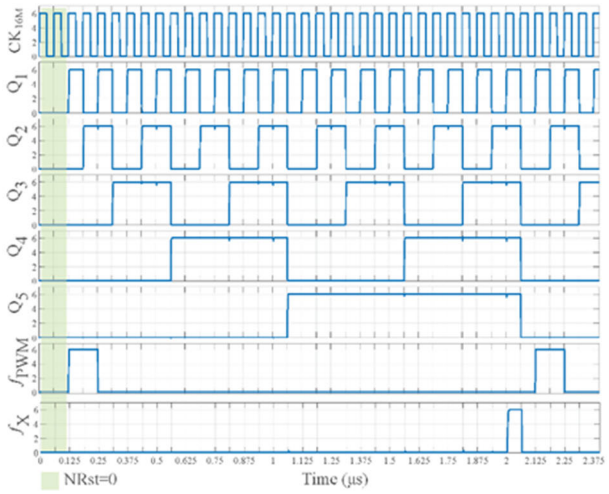

FIGURE 7. Frequency divider timing diagram.

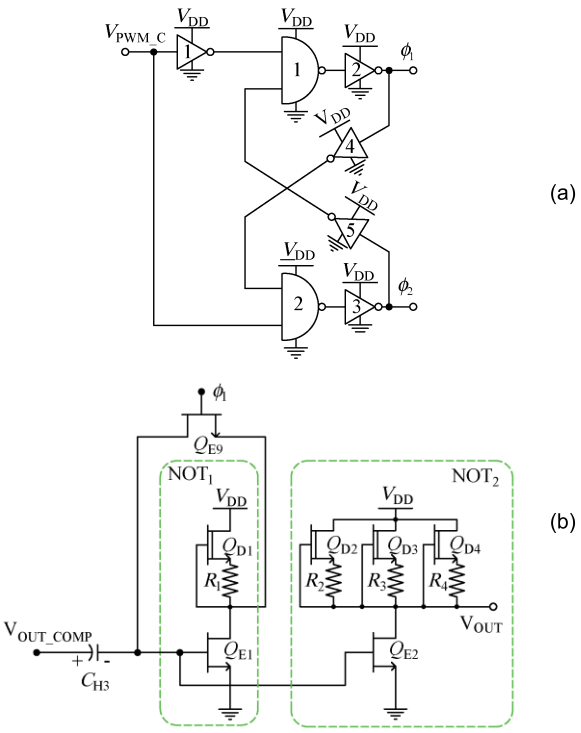

FIGURE 8. Schematic diagrams of: (a) Phase generator and (b) inverter with dynamic biasing.

capacitors C_{H1-3} and C_{INT} were set to 800 fF and 1.5 pF, respectively. The die micrograph is shown in Fig. 9 which is a detail of the entire system [19]. The area occupation is 800 μm $\times$ 750 μm. The circuit was supplied at 6 V and the reference voltages, V_{REF1} and V_{REF2}, were set to 3.5 V and 3 V, respectively. A 16-MHz clock signal was also applied to the divider circuit.

The circuit was tested to verify the correct operation and to evaluate the effect of parameter variations in the -40°C to 120°C temperature range, allowed by the measurement

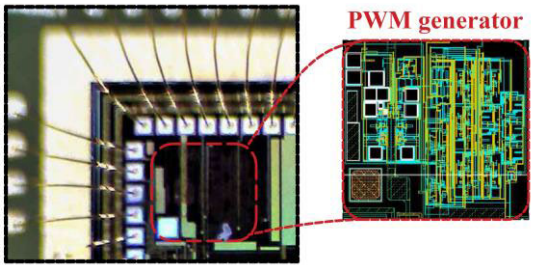

FIGURE 9. Chip photograph detail and layout of the PWM generator.

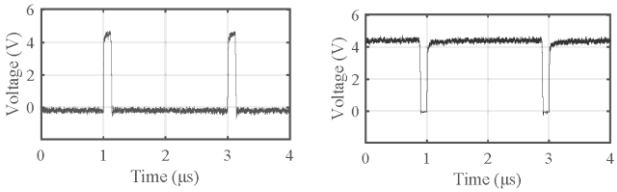

FIGURE 10. 500-kHz V_{PWM_C} signal with (a) minimum (6%) and (b) maximum (94%) duty cycle.

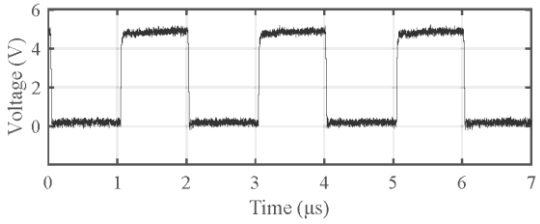

FIGURE 11. 500-kHz VPWM_C signal with 50% duty cycle.

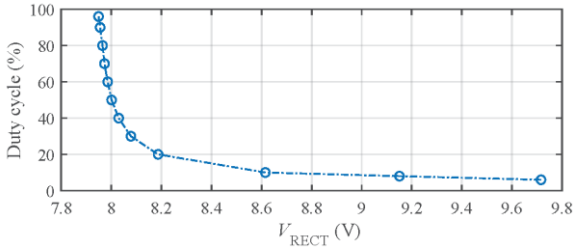

FIGURE 12. 500-kHz VPWM_C signal with 50% duty cycle.

equipment. Specifically, when V_{RECT} is greater than approximately 9.7 V, the minimum duty cycle of 6% for V_{PWM_C} was achieved, as shown in Fig. 10(a), whereas the maximum duty cycle of 94%, was achieved for V_{RECT} lower than approximately 7.95 V, as shown in Fig. 10(b). A 50% duty cycle for the nominal value of V_{RECT} of 8 V was found as shown in Fig. 11. Fig. 12 shows the dependence of the duty cycle on the voltage V_{RECT}.

As can be seen, V_{RECT} is kept constant over temperature thanks to the offset compensation, which also compensates for the temperature offset drift.

Finally, Fig. 14 shows the average current consumption versus the temperature. It decreases, as temperature increases, from 2.7 mA at -40°C to 0.9 mA at 120°C. The current reduction is mainly due to the increase in the degeneration resistances of the D-HEMT current sources.

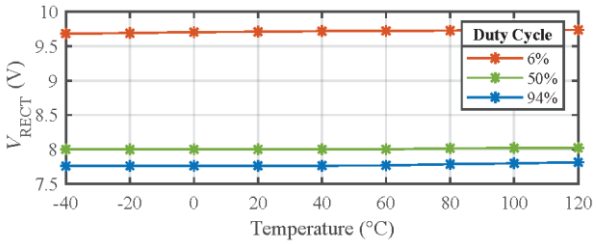

FIGURE 13. Measured rectified voltage versus temperature.

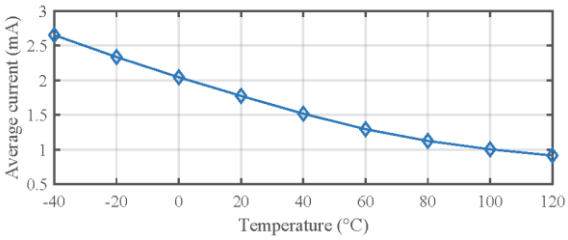

FIGURE 14. Measured overall average current consumption versus temperature, at 50% duty cycle for V_{PWM_C}.

V. CONCLUSION

A fully integrated PWM generator fabricated in a 0.5-μm GaN technology has been presented and experimentally demonstrated. It avoids the use of large external capacitors and compensates for technology limitations owing to an innovative dynamic offset compensation, making the circuit robust against global process tolerances, which are the main causes of failure in GaN monolithic implementations.

The proposed PWM generator is powered from 6 V and includes a 25 digital divider to set the 500-kHz PWM frequency with minimum and maximum duty cycle equal to 6% and 94%, respectively. Functionality was tested at temperatures ranging from −40°C to 120°C. This work is a significant step toward full-GaN system integration and demonstrates the feasibility of complex digital integration.

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