RESEARCH ARTICLE

A Novel Methodology to Improve Efficiency and Extend Dynamic Range of Shunt-Diode Class-F Rectifier for Wireless Power Transfer

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ABSTRACT This paper presents a novel methodology to enhance power conversion efficiency (PCE) and extend dynamic range for class-F shunt-diode rectifier design based on increasing the number of diodes connected in parallel. The prototypes employ class-F harmonic termination which can eliminate almost loss due to harmonic generation and instead of one diode, using more diodes connected in parallel will reduce losses on the diode due to built-in potential voltage (V_{bi}) and breakdown voltage (V_{br}). The proposed methodology mechanism is analyzed and demonstrated by closed-form equations where the variation of the losses is clarified in the comparison. Furthermore, based on Schottky diode HSMS2850, two prototypes in two cases: a single diode and two parallel-connected diodes are designed at 0.915 GHz, and measured to compare the efficiency for methodology verification. The implementation results show that the PCE of two parallel-connected diode case is higher than the one of a single diode case when the highest PCEs of two parallel connected diodes are 78.3% in simulation and 73.2% in measurement while the corresponding PCEs of single diode case are only 75.3% and 70.7%. Moreover, the dynamic range of the two-diode prototype is also improved by about 2 dB. These experimental results have good agreement with theory and clarify the advantages of the proposed methodology.

INDEX TERMS Class-F harmonic termination, efficiency improvement, shunt-diode rectifiers, wide dynamic range, wireless power transfer.

I. INTRODUCTION

Microwave wireless power transfer (WPT) technology has attracted attention in the development of electronic devices wireless-charging where wire-based charging is unavailable or difficult to apply [1], [2], [3]. In microwave WPT systems, the total power transfer efficiency depends a lot on the power conversion efficiency (PCE) of the rectifier which is a dispensable component [4]. Therefore, PCE improvement in rectifier design has always been a priority and interest. In additions, dynamic range is a factor that

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always accompanies PCE and it also is prioritized for improvement.

In microwave applications, diode-based rectifiers are common and widely applied where the diode loss accounts for most of the total losses. The general diode efficiency and diode losses can be exhibited by a graph as shown in Fig. 1 where the diode loss includes loss due to built-in potential voltage (V_{bi}), loss due to breakdown voltage (V_{br}), and loss due to harmonic generation. In recent years, there are many published reports about improving the PCE of rectifiers by harmonic termination techniques such as class-C [5], [6], class-E [7], [8], class-F [9], [10], inverse class-F [11], [12] or power recycling [13], [14]. However, harmonic termination
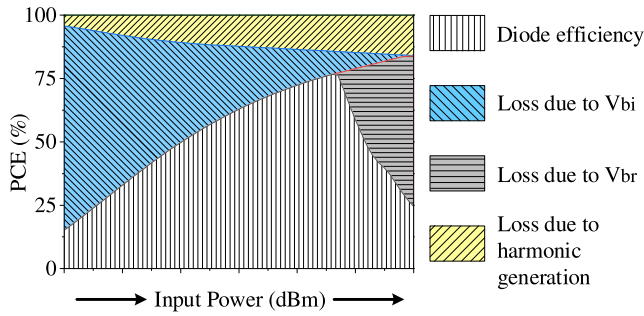
FIGURE 1. The general distribution of diode losses and diode efficiency.
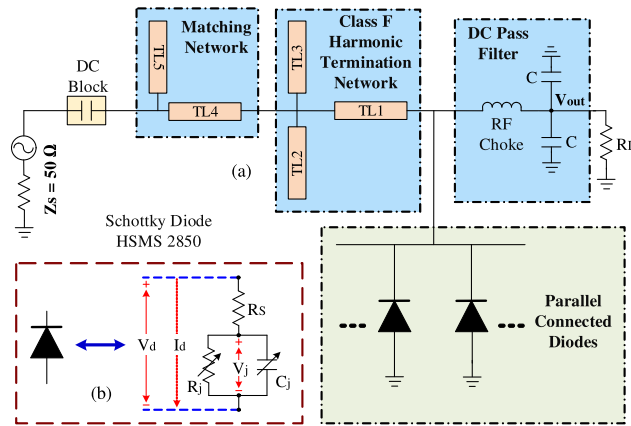
FIGURE 2. a) Detailed structure of the proposed rectifier and b) Equivalent model of the diode.

FIGURE 3. Reshaped waveforms of voltage and current across the diode by class-F harmonic termination in the time domain without effect of breakdown voltage (V_{br}).

FIGURE 4. Reshaped waveforms of voltage and current across the diode by class-F harmonic termination in the time domain when breakdown voltage (V_{br}) begin to have influence.

techniques only can reduce loss due to harmonic generation of the diode while losses due to V_{bi} and V_{br} still do not decrease by a not small percentage.

In this research, a PCE enhancement methodology is proposed for class-F rectifier design by reducing the loss due to V_{bi} and V_{br} on the diodes. Instead of using a single diode as almost published rectifiers, using more diodes connected in parallel will reduce total power consumption on series resistor R_S of the diode which is demonstrated by closed-form equations based on losses theory analysis of class-F rectifier. In addition, two rectifier cases: single diode and two parallel-connected diodes are designed and measured showing that by two diodes connected in parallel, the PCE can be improved around 3% and dynamic range of higher 50% PCE can be extended 2 dB in comparison with the PCE of single diode case in both simulation and measurement. Moreover, the measured PCE and dynamic range of the two-parallel-connected diode prototype are higher than almost all one of the published rectifiers which are based on similar diode model. Remarkably, the measured results show a superior frequency-weighted efficiency (FE) in comparison with those published works with FE is employed for evaluating PCE and frequency (FE = PCE $\times f^{0.25}$) [11]. Based on theoretical analysis and experiment results, it can be confirmed that the proposed methodology can improve the PCE and dynamic range in rectifier design.
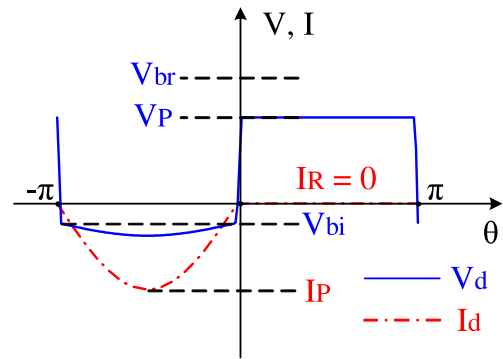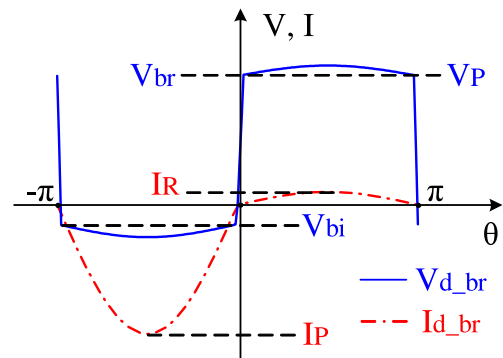
II. ANALYSIS OF EFFICIENCY IMPROVEMENT METHODOLOGY AND RECTIFIER DESIGN

Fig. 2a shows the detailed structure of the proposed rectifier where the loss due to harmonic generation can be minimized by Class-F harmonic termination which is based on three transmission lines (TLINs). Then, instead of using one diode, adding more diodes connected in parallel will improve the rectifier PCE when it is matched to the source of 50Ω by matching network constructed by two TLINs as shown in Fig. 2a. These five TLINs have corresponding characteristic impedance (Z_i) and electrical length (θ_i^f) at operating frequency (f) with $i = 1, 2, \ldots, 5$ and. In addition, DC block and DC pass filter are indispensable parts of shunt-diode configuration rectifier the DC block is a capacitor and the DC pass filter consists of a high-inductance inductor connected in series with two parallel capacitor.

A. DESIGN OF CLASS-F HARMONIC TERMINATION NETWORK

Class-F harmonic termination is applied for reshaping diode-across current and voltage when square waveform in voltage and half-sinusoidal waveform in current are results. To achieve these results, the class-F harmonic termination will be designed with the targets of impedance satisfied

TABLE 1. Extracted TLIN parameters of two designed rectifiers.

		TL$_1$	TL$_2$	TL$_3$	TL$_4$	TL$_5$
Single diode	$Z_i(\Omega)$	70	70	70	70	79
	$\theta_i(°)$	90	45	30	10.4	76
Two diodes	$Z_i(\Omega)$	70	70	70	70	70
	$\theta_i(°)$	90	45	30	8	70.8

electrical lengths $\theta_i(°)$ at the frequency of 0.915 GHz.

FIGURE 5. Photograph of fabricated rectifiers: a) single diode and b) two parallel connected diodes.

FIGURE 6. Measurement setup of fabricated rectifiers for verification.

zero impedance at even harmonics and infinite impedance at odd harmonics. By ensuing analysis and design in [15], the electrical length of TLINs (TL_1 - TL_3) which organize class-F harmonic termination network can be extracted as follows:

$$\theta_1^f = \lambda/4, \tag{1}$$

$$\theta_2^{2f} = \lambda/4, \tag{2}$$

$$\theta_3^{3f} = \lambda/4, \tag{3}$$

where the electrical lengths are defined at the frequency indicated by the notion superscripts. With these values, the impedance at the diode cathode will be zero at second harmonic and infinite at third harmonic and these impedances is not affected by increasing number of diode, thus ensuring the efficiency of the class-F harmonic termination network.

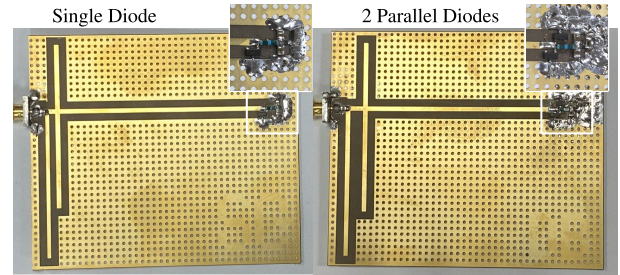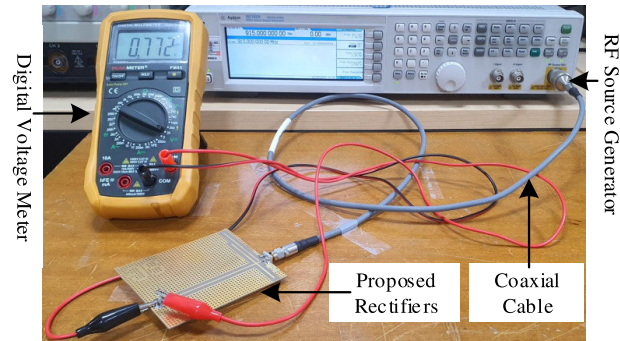## B. ANALYSIS OF EFFICIENCY IMPROVEMENT METHODOLOGY BASED ON PARALLEL CONNECTED DIODES

The equivalent model of the diode is presented in Fig. 2b, it consists of a series resistor (R_S), a nonlinear capacitor (C_j) and a nonlinear resistor (R_j). In the diode loss, the power dissipation on the resistor R_S due to V_{bi} and V_{br} accounts significant proportion that leads to if this power dissipation can be reduced, the diode efficiency will be improved. By employing class-F harmonic termination, the diode-across current was reshaped to half-sinusoidal waveform and the diode-across voltage was reshaped to square waveform are shown in Fig. 3 and Fig. 4, then it can be extracted by equations as follows:

$$V_d = \begin{cases} -V_{bi} + I_P R_S \sin(\theta)), & -\pi < \theta < 0 \\ V_P + I_R R_S \sin(\theta)), & 0 < \theta < \pi \end{cases} \tag{4}$$

and

$$I_d = \begin{cases} I_P \sin(\theta)), & -\pi < \theta < 0 \\ I_R \sin(\theta)), & 0 < \theta < \pi \end{cases} \tag{5}$$

where I_P is the diode-across current peak during the diode ON-period, V_P is the highest level of diode voltage during the diode OFF-period, and I_R is the peak of diode reverse current. When breakdown voltage (V_{br}) has no influence, V_P increase corresponding to augment of the input power level and $I_R = 0$ as shown in Fig. 3. When breakdown voltage (V_{br})

begins to have influence, V_P is limited equal to V_{br}, and if the input power level continues to increase, I_R will start to grow from 0 and be linear with the input power as shown in Fig. 4. Then the diode loss on R_S due to V_{bi} and V_{br} of single-diode case can be calculated by analysis in [16] as follows:

$$L_{R_S, V_{bi}} = \frac{1}{2\pi} \int_{-\pi}^{\pi} V_d I_d d\theta = \frac{I_P^2 \pi R_S + 4I_P V_{bi}}{4\pi}, \tag{6}$$

$$L_{R_S, V_{br}} = \frac{1}{2\pi} \int_{-\pi}^{\pi} V_{d\_br} I_{d\_br} d\theta$$

$$= \frac{I_P^2 \pi R_S + I_R^2 \pi R_S + 4I_P V_{bi} + 4I_R V_{br}}{4\pi}. \tag{7}$$

However, if replacing the single diode by n parallel-connected diodes (n is number of used diodes), V_{bi} and V_{br} remain unchanged, I_P and I_R per diode will decrease n times respectively and it can be written as follows:

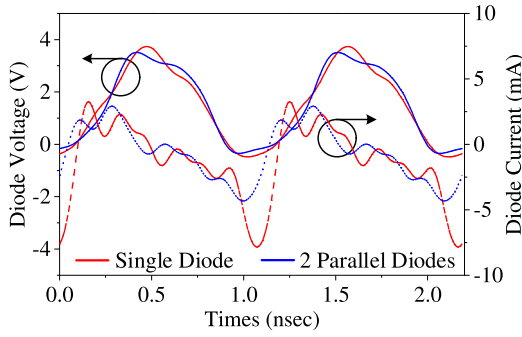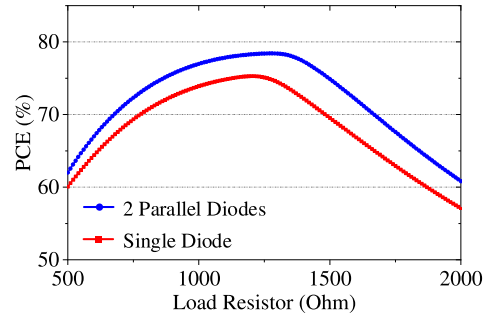$$I_{Pn} = \frac{I_P}{n}, \tag{8}$$

$$I_{Rn} = \frac{I_R}{n}. \tag{9}$$

Then, total loss on R_S due to V_{bi} and V_{br} of n parallel connected diodes will be calculated by below equations (10) and (11):

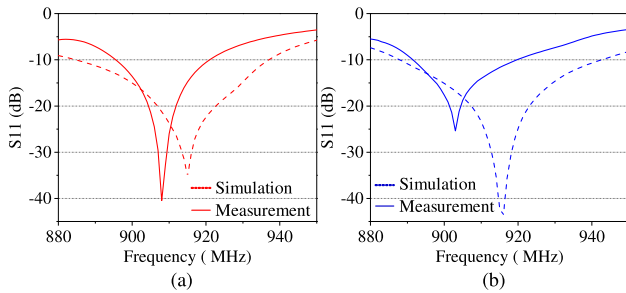$$L_{nR_S, V_{bi}} = n\frac{I_{Pn}^2 \pi R_S + 4I_{Pn} V_{bi}}{4\pi}, \tag{10}$$

$$L_{nR_S, V_{br}} = n\frac{I_{Pn}^2 \pi R_S + I_{Rn}^2 \pi R_S + 4I_{Pn} V_{bi} + 4I_{Rn} V_{br}}{4\pi}. \tag{11}$$

FIGURE 7. Voltage and current waveform of each diode of two cases: single diode and two parallel-connect diodes in simulation.

FIGURE 9. Simulated results of the PCE versus load resistor at 0.915 GHz with the input power level of 4 dBm in two cases: single diode and two parallel-connected diodes.

FIGURE 8. The reflection coefficients S_{11} for both simulation and measurement at the input power of 4 dBm of two cases: a) single diode and b) two parallel-connected diodes.
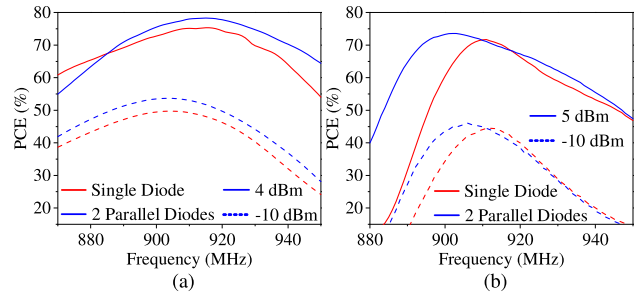
FIGURE 10. The PCE versus frequencies at two input power levels of two cases for both simulation and measurement: a) simulation and b) measurement.

Substituting corresponding diode current I_{Pn} in (8) into (10) and I_{Rn} in (9) into (11) and solving leads to total loss on R_S can be extracted as follows:

$$L_{nR_S, V_{bi}} = \frac{\frac{I_P^2 \pi R_S}{n} + 4I_P V_{bi}}{4\pi}, \quad (12)$$

$$L_{nR_S, V_{br}} = \frac{\frac{I_P^2 \pi R_S}{n} + \frac{I_R^2 \pi R_S}{n} + 4I_P V_{bi} + 4I_R V_{br}}{4\pi}. \quad (13)$$

Assuming that under ideal conditions of space and connection, n can grow to a rather large value, then $L_{nR_S, V_{bi}}$ and $L_{nR_S, V_{br}}$ will decrease to only:

$$L_{nR_S, V_{bi}} \approx \frac{I_P V_{bi}}{\pi}, \quad (14)$$

$$L_{nR_S, V_{br}} \approx \frac{I_P V_{bi} + I_R V_{br}}{\pi}. \quad (15)$$

In comparison between losses on R_S due to V_{bi} and V_{br} of two cases: single diode and n parallel connected diodes, it is clear that $L_{nR_S, V_{bi}}$ in (14) is lower than $L_{R_S, V_{bi}}$ in (6) and $L_{nR_S, V_{br}}$ in (15) is lower than $L_{R_S, V_{br}}$ in (7) which leads to the conclusion that increasing the number (n) of the parallel connected diodes will reduce the loss of the diode and the PCE of the rectifier can be improved. However, due to the limitation of realistic fabrication, the number of parallel-connected diodes can hardly be increased much, the value of n equal to 2 or 3 is optimal when it is suitable for fabrication while still being to improve the PCE significantly.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

To clarify the presented analysis of the proposed methodology, Schottky diode HSMS2850-based rectifier prototypes in two cases: single diode and two parallel-connected diodes were designed and measured for comparison (Schottky diode HSMS2850 by Avago parameters: $V_{bi} = 0.15V$, $V_{br} = 3.8V$, $R_S = 25\Omega$, $C_{j0} = 0.18\,pF$, $I_S = \mu A$). The nonlinear simulation is based on *Harmonic Balance Simulaation* in *Advanced Design System* software with the following setup: Harmonic order is 15, a single power tone is used as input excitation. the diode model used in simulation is the model given by the manufacturer Avago. In both the simulation and measurement, the output voltage at the load resistor is probed and extracted, then the DC component of output voltage is used to calculate PCE. The characteristics and electrical lengths of TLINs in two designed rectifiers are extracted in Table. 1. For a fair comparison, it can be seen that two cases have same the class-F harmonic termination network, two matching networks have similar structures while TLIN parameters of matching networks are a little adjusted to match source impedance with corresponding input impedances. Two rectifier prototypes are implemented on the substrate Taconic TLY-5 ($\epsilon_r = 2.2$, $\tan(\delta) = 0.0009$, 0.8 mm thickness). Moreover, two cases of rectifiers have the same DC pass-filter structure which is constructed by two series-connected inductors of 390 nH and two parallel-connected capacitors of 2400 pF, the DC blocks are also formed by this capacitor. The photographs of two fabricated rectifiers are shown in

TABLE 2. Comparison of the proposed rectifier in this work with the published reports based on similar diode models.

Ref.	Year	Frequency (GHz)	Harmonic Termination	Maximum PCE (%)	Maximum FE (%)	Input Power (dBm)	Schottky Diode	Dynamic Range of > 50% PCE
[17]	2017	0.9	No	63.1	61.5	0	HSMS 285C	12.5 dB (−5 <> 7.5)
[18]	2023	0.425	Class F^{-1}	72.8	58.8	5	HSMS 2850	22.5 dB (−7.5 <> 15)
[19]	2019	0.433	No	64.4	52.2	5	HSMS2850	18.9 dB (−6.8 <> 12.1)
[20]	2021	0.433	No	71.6	58.1	5	HSMS2850	22 dB (−8 <> 14)
[21]	2020	0.9	No	50.2	48.9	2	HSMS2850	1 dB (1.5 <> 2.5)
[22]	2014	0.94	No	63.5	62.5	2	SMS7630	16 dB (−9 <> 7)
This work	2023	0.902	Class F	73.2	71.3	5	HSMS 2850	24.5 dB (−10 <> 14.5)

Evaluate power conversion efficiency with frequency: FE = PCE $\times f^{0.25}$
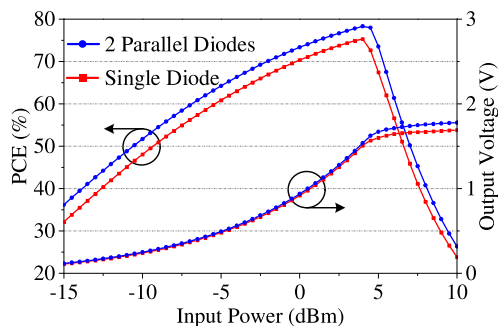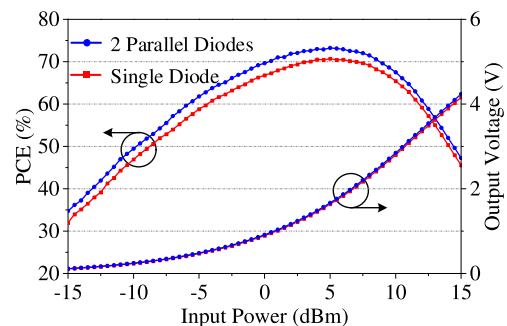

FIGURE 11. Simulation results of the PCE versus input power levels at 0.915 GHz in two cases: single diode and two parallel-connected diodes.

FIGURE 12. Measurement results of the PCE versus input power levels in two cases: single diode at 0.908 GHz and two parallel-connected diodes at 0.902 GHz.

Fig. 5 with a slight difference and the lowest distance between two stubs is 1.5 mm so there is almost no influence of electromagnetic coupling. These rectifiers were measured by setup as shown in Fig.6.

The voltage and current waveforms of each diode in simulation with 4 dBm input power of two cases: single diode and two paralled-connected diodes are presented in Fig. 7. In comparison with the calculated waveforms in Fig. 3 and Fig. 4, it can be seen that these waveforms have similar shapes with some ripples because the employed Class-F harmonic termination only control to third harmonic while the waveforms in Fig. 3 and Fig. 4 are results of idea Class-F harmonic termination with all harmonic terminated. Fig. 8 depicts the reflection coefficients S_{11} at the input power of 4 dBm in both simulation and measurement of two rectifier cases. As observed, in simulations, the S_{11} of both rectifier cases are lowest at the frequency of 0.915 GHz with lower than −30 dBm values. However, in measurement, due to diode model accuracy and influence of fabrication tolerance, the lowest S_{11} frequencies are down-shifted in comparison with the simulated S_{11} when the lowest measured S_{11} of the single diode case is recorded at 0.908 GHz while the one of two-diode case is recorded at 0.902 GHz. The lowest measured S_{11} of both cases are lower than −20 dB which

indicates the mismatch loss is minimized to almost zero. The PCE versus frequencies at 4 dBm and −10 dBm input power levels of two rectifiers are plotted in Fig. 8 that indicates a good agreement between S_{11} and PCE versus frequencies. In simulation, the highest PCE of two cases can be achieved at 0.915 GHz while in the measurement, the PCE of single diode prototype peaks at 0.908 GHz, and the highest PCE of two diode prototype is recorded at 0.902 GHz. By sweeping load resistor in simulation at the input power of 4 dBm with the results depicted in Fig. 9, the resistor around 1200Ω is determined to be the optimal load resistor for the highest PCE of two rectifier cases, so 1200Ω resistor is used to measure output DC voltage and calculated PCE. Fig. 11 shows the output voltages and the PCEs versus input power levels of two rectifiers in simulation at the frequency of 0.915 GHz where the highest PCE at 4 dBm of two parallel-connected diodes is 78.3% which is higher than the one of a single diode prototype with 75.3%. In measurement, at 0.902 GHz frequency, the peak PCE of two parallel-connected diode prototype is 73.2% at 5 dBm while at 0.908 GHz frequency, the highest PCE of single diode rectifier is lower, only 70.7% at 5 dBm with measured results are shown in Fig. 12. The different considering about input power between simulation

and measurement can be explained due to the breakdown voltage of the diode model in measurement is usually higher than in simulation that leads to measured PCE has a higher saturation point than simulated PCE.

Moreover, the 50% PCE dynamic range of two parallel-connected diodes is wider 2 dB than the one of single diode when the dynamic ranges of two-diode prototype are 17.5 dB (-10.5 dBm to 7 dBm) in simulation and 24.5 dB (-10 dBm to 14.5 dBm) in measurement while the corresponding dynamic range of single-diode prototype are only 15.5 dB (-9 dBm to 6.5 dBm) and 22.5 dB (-8.5 dBm to 14 dBm), respectively. From these results, it is clear that by increasing the number of diodes connected in parallel, the PCE will be improved at all input power levels, which also leads to extending the dynamic range of over 50% PCE. The advantages of the proposed methodology for PCE and dynamic range improvement are more clarify by when the measurement results of the two-parallel-connected diode prototype are compared with the published rectifiers in recent years which use the same or similar diode models. This comparison are presented in Table 2, it can be seen that the proposed rectifier has the highest PCE and the largest over 50% PCE dynamic range, furthermore, the frequency-weight (FE) of the proposed rectifier is superior to the ones of articles published in recent years.

IV. CONCLUSION

In this paper, a novel methodology was proposed for the PCE enhancement and dynamic range extension in class-F rectifier design with shunt-diodes configuration. Instead of using one diode, by connecting multiple diodes in parallel (adjacent diodes), the PCE will be boosted which was successfully demonstrated in theory analysis by closed-form equations. Furthermore, the methodology also was verified by the implementation of two rectifiers: single diode prototype, and two parallel-connected diode prototype which indicates a good consistency between theory and experiment results. These prototypes were designed with the same class-F harmonic termination and differ only slightly in the matching network for comparison. The measured results show that with two parallel-connected diodes, the PCE was improved by 3 % and the dynamic range was extended by 2 dB in comparison with the ones of the single diode prototype. In addition, another comparison between measurement results of the two-diode prototype and published work in recent years that use the same or similar diode models indicates the PCE and the dynamic range has been greatly improved when the frequency-weight efficiency factor is used to evaluate.

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