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SURVEY

A Comparative Study of Ring VCO and LC-VCO: Design, Performance Analysis, and Future Trends

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ABSTRACT Voltage-controlled Oscillator (VCO) is a prominent part that has been used to generate a stable frequency for the high-frequency transceiver system. This survey encompasses a comparative analysis of two commonly used VCO architectures: the Ring VCO and LC-VCO. The Ring VCO has been constructed with the collection of ring delay cells. Moreover, the LC-VCO utilizes inductors, capacitors, fine-tuning circuits, coarse-tuning circuits to generate frequency. Furthermore, this study investigates an in-depth exploration of VCO structures, operational principles, advantages, limitations, and performance metrics. In addition, it evaluates performance parameters, including operating frequency range, phase noise, figure of merit, and tuning techniques. This research suggests that based on the application and its requirements, the VCO performance parameters need to be varied. This survey employs diverse types of VCO, and its design methods. Implications for future research and study of VCO design and integration are discussed.

INDEX TERMS Current starved delay cell based VCO, differential delay cell based VCO, FOM, LCVCO, maximum operating frequency, ring VCO, sensitivity, oscillator, phase noise, tuning range.

I. INTRODUCTION

The need for precise and low-power features in wireless personal digital assistance devices has grown in recent years, which emphasizes the need for RF designers to work within the ultimate limits of technology [1], [2], [3], [4]. It is identified that in recent years, voltage-controlled oscillators (VCO) have been extensively designed, as it was the most prominent building block in the Phase-Locked Loop (PLL) system, which could generate a stable frequency [5], [6], [7], [8], [9]. The VCO designers have addressed parameters like good phase noise, low power, tuning range, smaller area, lower Figure of Merit (FOM), and cost [9], [10]. The VCOs have been employed in various kinds of applications such as optical transmission, clock generation, frequency synthesizers, function generators, and Radio Frequency Integrated Circuits (RFIC) [11], [12], [13], [14], [15] etc. The most predominantly used VCOs in PLL have been categorized into different types, as shown in Fig. 1, which are: 1. Ring oscillator VCO; 2. Inductance-capacitance VCO (LC-VCO) [16], [17], [18], [19]. The selection of a required VCO architecture is to design a PLL depending on numerous factors, including the desired frequency range, phase noise performance, tuning range, power consumption, and integration complexity [20], [21], [22], [23]. In the last few years, high-performance VCOs have been in demand to have high-speed wireless applications [24], [25], [26], [27].

In the last two to three decades, most of the communications were in the radio frequency range; hence, a current-starved VCO was the best choice to have a high tuning range and less power dissipation [28]. These current-starved VCOs (CS-VCO) could provide a better tuning range and lower power dissipation at the expense of more extensive phase noise [29]. Nevertheless, the problem with the CS-VCO was that it could provide frequency around 4.5 GHz. However, during the past few last decades, communication technology was in the transition stage from Radio Frequency (RF) range to the millimetre-wave range [30], [31], [32]. Consequently, the researcher needed a VCO that would contribute high frequency with better phase noise [33], [34], [35], [36]. Subsequently, the researchers came up with an LC-VCO, which would offer higher frequency with transcendent phase

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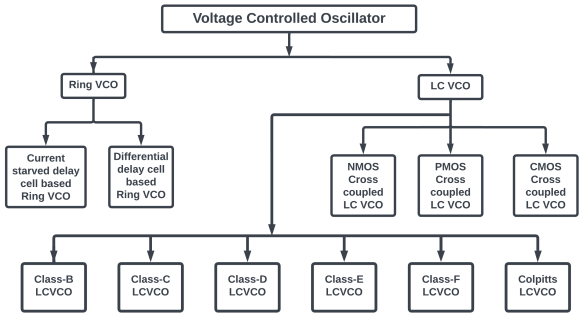

FIGURE 1. Types of VCO architectures.

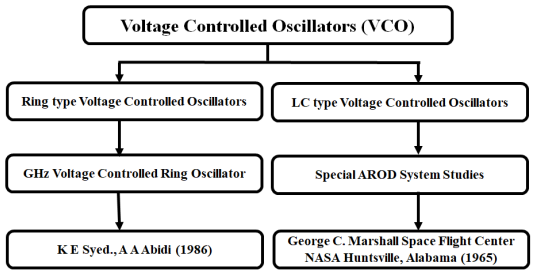

FIGURE 2. Basic VCO taxonomy diagram.

noise when compared to the CSVCO [37], [38]. Henceforth, this study seeks to present a comprehensive comparison between the Ring VCO and LC-VCO architectures. It is suggested that the designer choose the appropriate VCO for their requirements based on specific applications.

It is stated by Syed et al. [39] and George et al. [40] that the basic VCO diagram represents the pioneer research articles in the field of Ring VCO and LC-VCO (As shown in Fig. 2). Thus, during the analysis of the VCOs performance parameters like tuning range, FOM, operating frequency, phase noise, and the power consumption of the reported VCOs would be very helpful for the researchers.

II. RING VCO

The ring VCO Taxonomy diagrams are shown in Fig. 3, Fig. 4 and Fig. 5. The taxonomy diagram represents the researcher's efforts to develop and enhance the ring oscillator circuit throughout the period from 1983 to 2023.

Ring oscillators constructed with an odd number of inverting gates or delay cells are incorporated like a ring and impart an oscillation between the two different voltage ranges. The inverting gates or delay cells have connected with feedback from the last gate to the first one [20], [60], [71], [72], [168]. The ring oscillator's performance highly depends on the parasitic capacitance placed in the active NMOS transistor chip. Thereby, a number of tighter layouts with more delay cells can improve considerable performance [41], [49]. The core building block of a ring VCO is a group of delay cells interconnected in a positive or regenerative feedback loop to create a fundamental ring oscillator [45], [73]. Janet [42] constructed a ring oscillator with ten inverters, output buffers, and a NAND gate in 1984. The NAND gate can be used to reject the multiple oscillations from the ring oscillator. The capacitive loading problem can be reduced by doubling the channel widths in each successive stage, as shown in Fig. 6 [42].

Calzolari et al. [43] have summed up with a mathematical equation for the propagation delay τ_d that can be calculated from the period of oscillation (T) given in equation (1), [68], [74],

$$\tau_d = \frac{T}{2N} \tag{1}$$

where N = number of inverters. Luca Ravezzi [54] has concluded in 2021 that ring oscillators with capacitive loads are used for frequency tuning. However, the researcher has formulated unsustainable and stable oscillations depending on the capacitor's size along with an equivalent value of the severe resistance. Ring oscillators with capacitive loads are frequently used in the industry simply because of their compact size, wide frequency range, and easy operation. However, the ring oscillator may not be able to sustain stable oscillations due to the unavoidable significant resistance of the capacitive load [3], [17], [44], [75]. In 1997, Behzad Razavi [45] stated that ring circuits should develop a phase shift 2π and unity voltage gain at the oscillation frequency in order to attain the oscillation. Stephen Docking et al. [76] have discussed that the phase shift is required for each and every delay stage of $\frac{\pi}{N}$, Where N represents the total delay stages in the ring. The remaining phase shift π of the single-stage ring oscillator is offered by the dc inversion. The single-stage ring oscillator provides the dc inversion done by the odd number of oscillator stages depicted in Fig. 7. When the ring oscillator is designed with an even number of stages, and the output feed-backs are swapped and connected to the input [74], [76] depicted in Fig. 8 [76].

Assume the ring oscillator in each stage produces the delay of T_d. The signal must flow through every N delay stage for the first time, the first 180^0 phase shift in the time of $N * t_d$, and the signal must go through every N delay stage for the second time of the remaining 180^0 phase shift. The resulting total time phase shift can be obtained at $2N * t_d$. The oscillating frequency can be calculated as equation (2) [11], [20], [21], [47], [76], [77],

$$f = \frac{1}{2N.t_d} \tag{2}$$

The negative skewed delay element is connected with one input of CMOS (Complementary Metal Oxide Semiconductor) inverter [47], [61] depicted in Fig. 9 [47]. The PMOS is coupled to the delay element; this PMOS input signal receiving is a little delayed compared to NMOS. If a transition between logic low and high occurs, this delay element will turn on the PMOS before the due time. When the output transitions occur from high to low, the PMOS skewed delay sickens prior to the NMOS turning on, and it accelerates

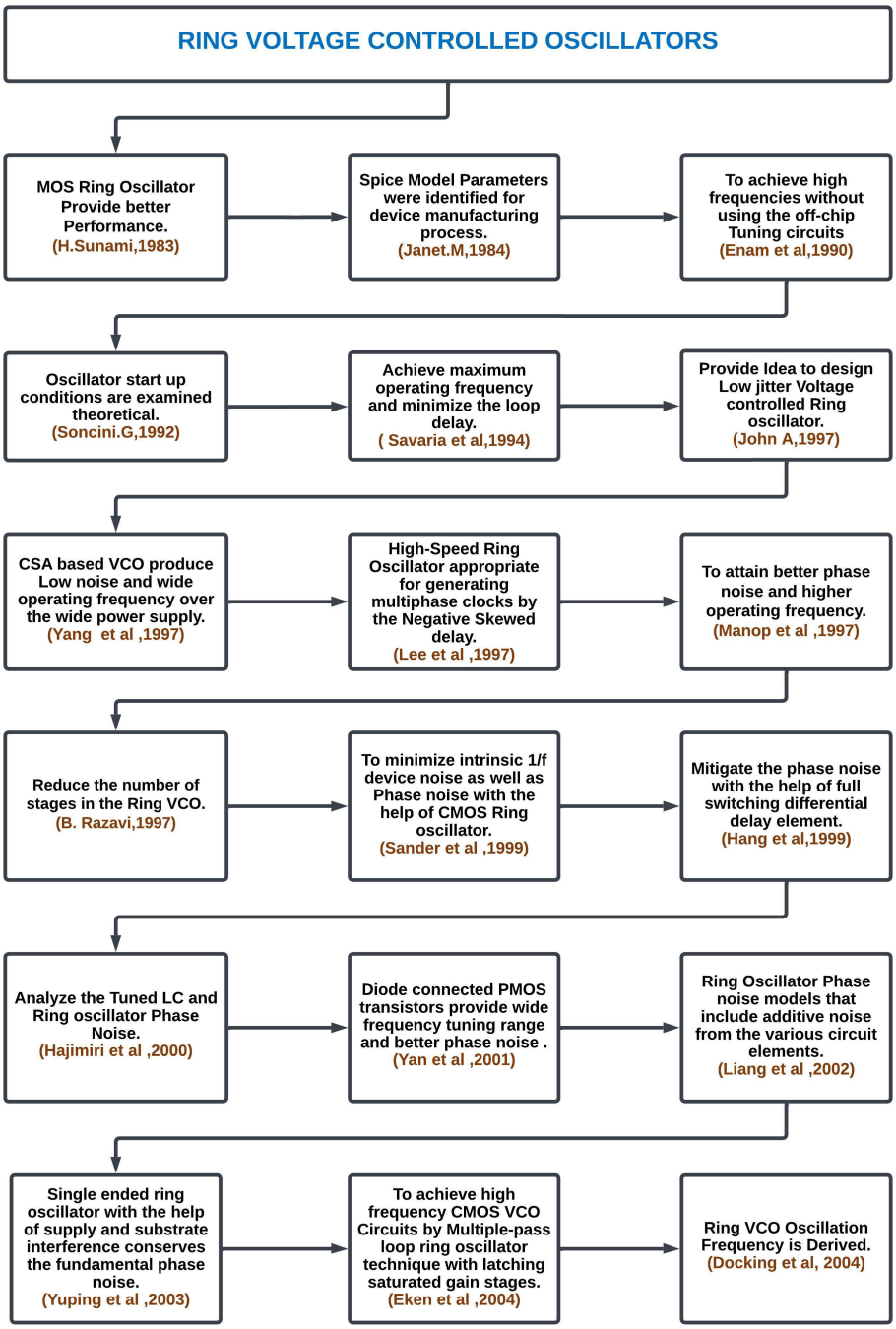

FIGURE 3. Taxonomy diagram of ring VCO Part-I.

the transition. The negative skewed delay element achieved oscillation frequency is maximum. The Negative Skew raises the performance and power consumption; otherwise, performance and power consumption also decrease because the maximum current flows to the ground. The negative skew delay element improves the performance, but it uses more power when both transistors are turned on. This problem is sorted out by the PMOS inputs being connected with outputs distributed from the chain of adjacent cells. The five-stage ring oscillator of the chain of inverters in every PMOS and NMOS derives from the different input signals from its different nodes [47] depicted in Fig. 10. The Oscillation of the VCO can be obtained by an inverter switching at each inverter stage.

In CMOS PLL design, the ring-based VCOs are commonly used, and they are current starved delay cell-based VCOs and differential delay cell-based VCO [48]. Yang et al. in 1997 [48] proposed an inverter-based ring oscillator

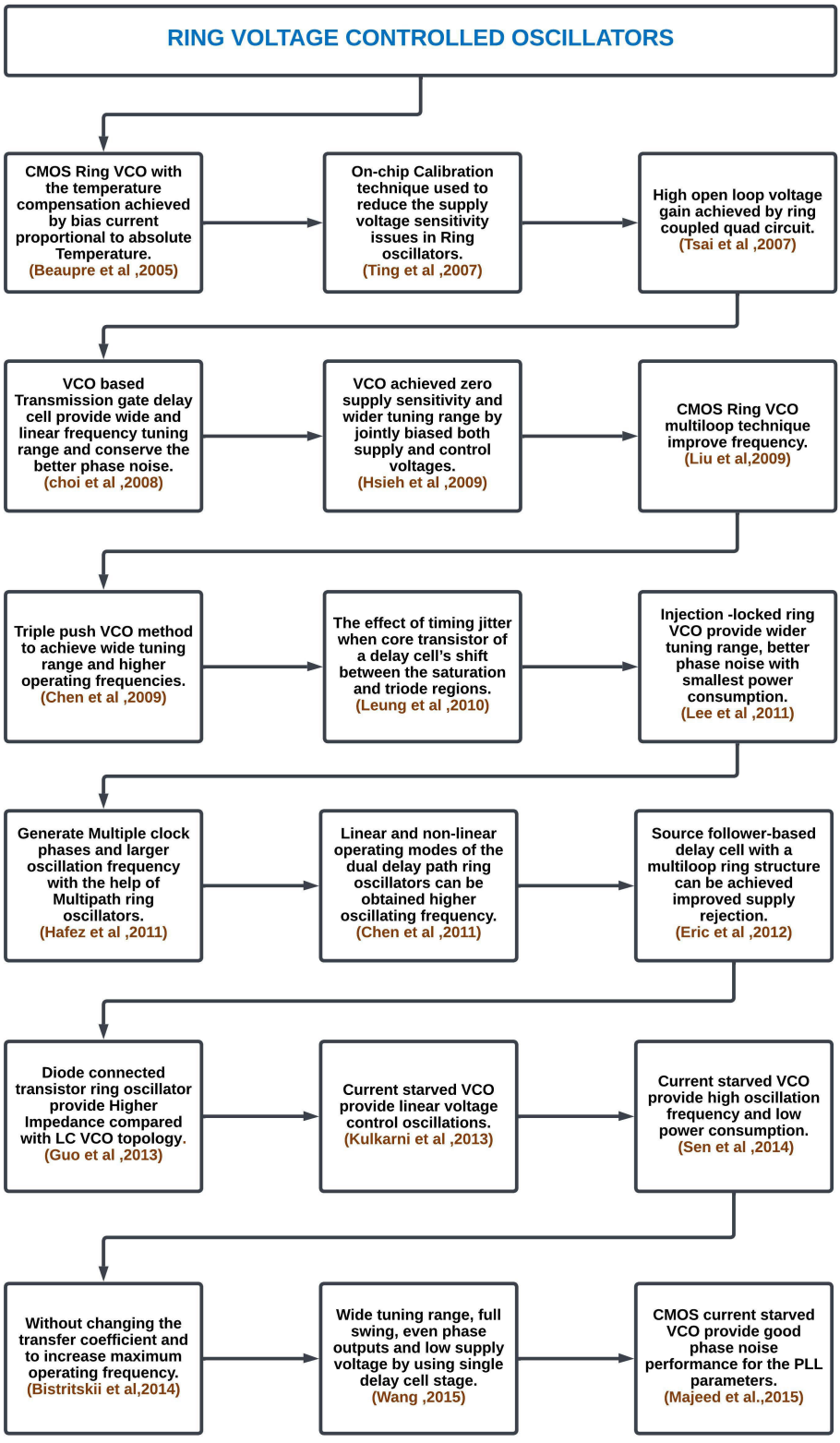

FIGURE 4. Taxonomy diagram of ring VCO Part-II.

VCO design that consists of a voltage-to-current converter (VCC), a current-controlled ring-type oscillator, and a band-gap reference circuit [48]. The current-controlled oscillator (CCO) control input is used to tuneup the particular

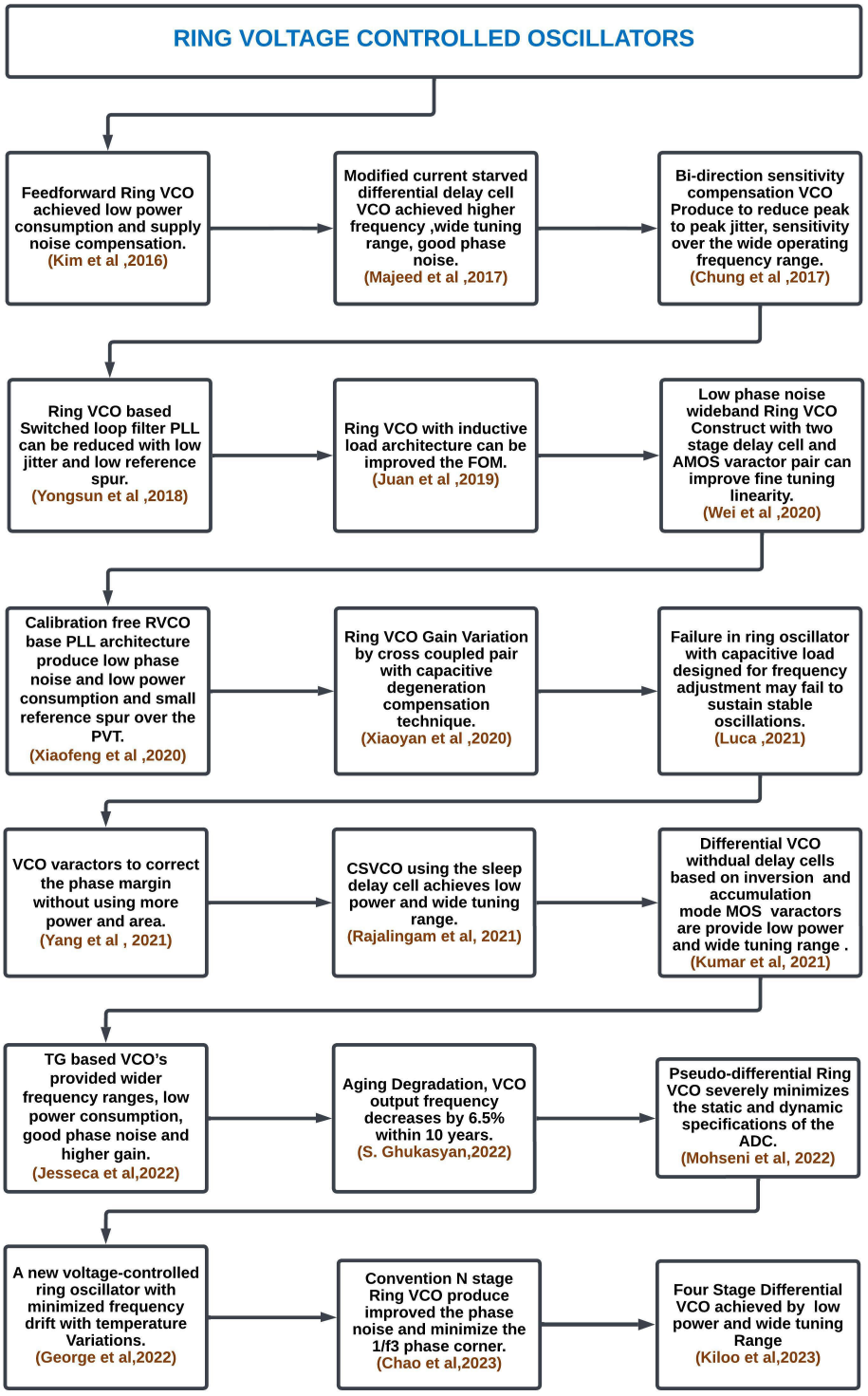

FIGURE 5. Taxonomy diagram of ring VCO Part-III.

frequency range. By using this internal band-gap reference, the supply sensitivities and temperature sensitivities of this system are enhanced [4], [63]. On-chip Voltage regulator circuits are used to minimize the supply sensitivity noise [48], [60], [78].

The Replica feedback biasing circuit, which dynamically controls the oscillator bias current and voltage swing, is shown in Fig. 11 [13], [79], [172]. The bias current is adjusted by a feedback amplifier, such as the voltage drop across the symmetric load.

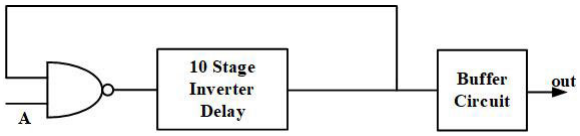

FIGURE 6. 10 stage inverter based ring oscillator.

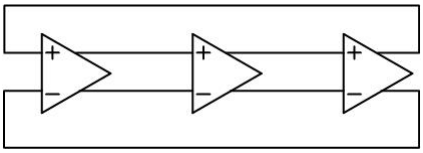

FIGURE 7. Three stage ring oscillator (odd number of oscillator stages).

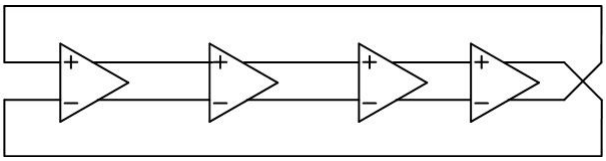

FIGURE 8. Differential ring oscillator (Even number of stages).

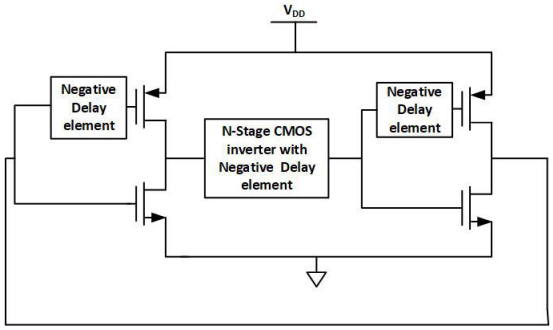

FIGURE 9. Skewed negative delay cell scheme.

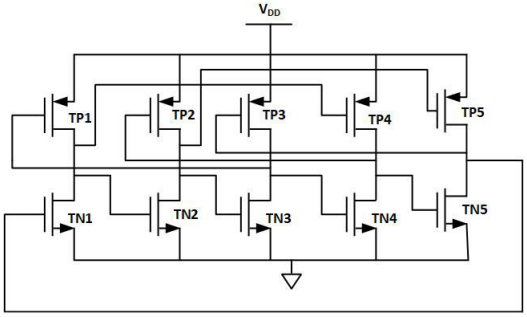

FIGURE 10. Modified negative delay scheme.

The VCO buffer's Voltage swing can be calculated as in the equation (3),

$$V_{swing} = V_{DD} - V_{cntr} \tag{3}$$

The translation from I_{bias} to V_{swing}, is performed by the half buffer replica in the bias generator through the diode-connected MOS device, whose output resistance can

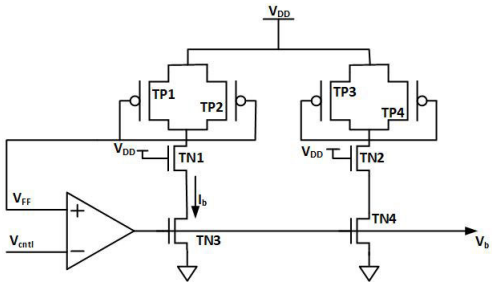

FIGURE 11. Replica feedback biasing.

be made to mimic that of the symmetric load at its full swing [79], [172]. The relationship is dynamically maintained through the replica-feedback bias, which is obtained as equation (4),

$$V_{DD} - V_{cntl} = V_{DD} - V_{swing} = I_{bias} - R_{symm} \tag{4}$$

Voltage swing and control voltage are related to the maximum supply rail V_{DD} and its potential difference with the V_{dd} can be written as equations (5) and (6),

$$\overline{V_{cntl}} = V_{DD} - V_{cntl} \tag{5}$$

and

$$\overline{V_{swing}} = V_{DD} - V_{swing} \tag{6}$$

Jaeha et al. in 2003 [79] propounded that VCO contains a bias generator, which functions essentially as a linear voltage regulator to control the VCO supply, which is made up of CMOS inverters, and it controls the VCO supply to modify the frequency and rejects undesired noise from the external supply, as shown in Fig. 12. The wide voltage swings and abrupt transitions of an inverter-based VCO are useful for lowering jitter [80]. However, an inverter is a single-ended buffer by nature and hence cannot filter out common-mode noise [78].

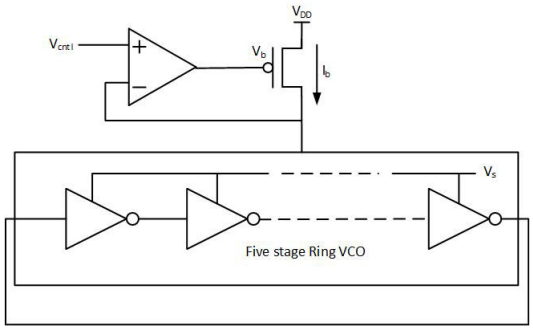

FIGURE 12. The inverter-based VCO.

Since the device speed is interconnected with the maximum oscillation frequency in the reported VCO by Manop Thamsirianunt et al. in 1997 [49], the layout of the MOS oscillator is to be designed in such a way to enhance their speed. The pseudo-three-stage ring oscillator architecture is

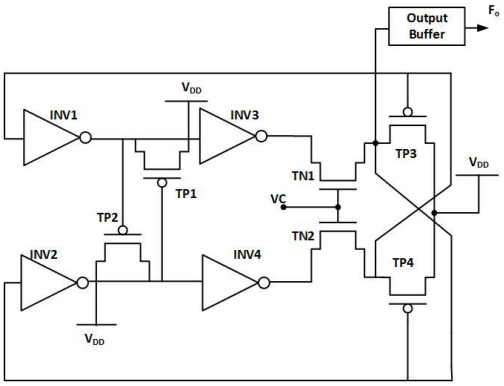

FIGURE 13. Pseudo three stage ring oscillator.

shaped with the two pairs of inverters, and the third pair of the inverter ring is replaced by the TP3 and TP4 PMOS transistor pairs, and TN1 and TN2 act as D-Latch in Fig. 13. When the control voltage V_{cont} is high, the TN1 and TN2 act as D-latch, passing the output signal to the input of PMOS. This circuit starts oscillating when the control voltage V_{cont} becomes high [49].

A. CURRENT STARVED DELAY-BASED VCO.

The ring oscillator is controlled by the gate capacitance of each stage MOS (Metal Oxide Semiconductor) transistor. The time required to charge and discharge the gate capacitance increases to the peak as the charging current decreases [81]. When compared to LC-VCO, the ring oscillator possesses many benefits: easy design with CMOS or BICMOS (Bipolar-CMOS) technologies, better oscillation with less tuning voltage, the high-frequency oscillation with low power dissipation and also the quadrature phase and multi-phase output could be obtained. The top of the PMOS and bottom of the NMOS are operated like the current source, and the middle NAND gate connection can be forced to starve from the current sources shown in Fig. 14 [6].

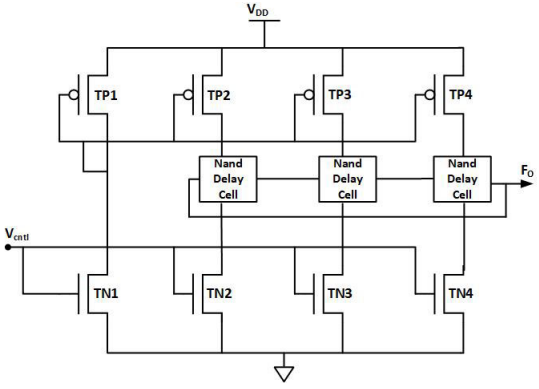

FIGURE 14. Current starved NAND based VCO.

The current sources could be limited, considering that the propagation delay has an opposite relationship with the charging and discharging currents, and the frequency of

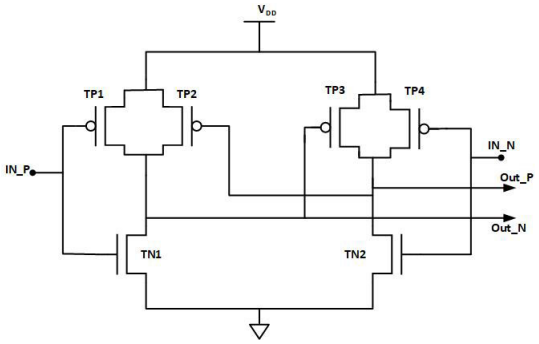

FIGURE 15. Current starved VCO1 delay cell.

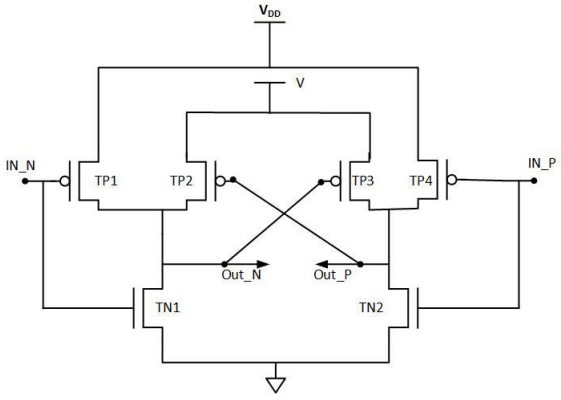

FIGURE 16. Modified current starved VCO2 delay cell.

oscillation might be efficiently controlled [68], [75]. The Modified current-starved VCO1 delay cell can be constructed with the pair of differential NMOS transistors and the cross-coupled connection of four PMOS transistors depicted in Fig. 15 [6]. The input Pair of PMOS transistors acts as the current source, and the output-connected PMOS pair acts as the load. Reported Modified current starved VCO2 delay cell Fig. 16 [50] imparts a higher frequency than the current starved VCO1 delay cell, Fig. 15 [50], [75]. MOSFETs (Metal Oxide Silicon Field Effect Transistors) are used in Pass-Transistor Logic (PTL), not as inverters as they are in CMOS, but as switches. The PTL has the drawback of the threshold voltage drop, which is overcome by using transmission gate logic. The transmission gate inverter (TG-I) VCO Output frequency relies on the propagation delay, and every inverter stage frequency could be inversely proportional to its propagation delay, as depicted in Fig. 17 [51]. It increases the control voltages, and it could increase the output frequency and also decrease the propagation delay. Transmission gate NAND (TG-N) VCO using comparison to the transmission gate inverter(TG-I) shown in Fig. 18 [51], which is provided, when the control voltage is raised, the higher current flow results in a shorter propagation delay and a higher oscillation frequency [51].

The dual threshold CMOS (DTCMOS)-based current starved VCO design method is very efficient to

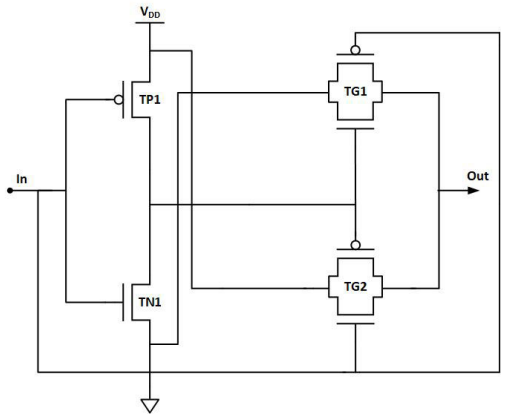

FIGURE 17. Transmission gate inverter(TGI) delay cell.

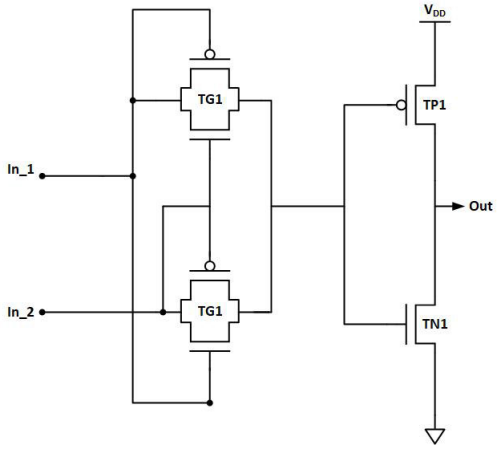

FIGURE 18. Transmission gate NAND (TGN) delay cell.

minimize the limitations of Multiple Threshold CMOS devices(MTCMOS). Also, DTCMOS techniques are operated and provided as the same output of the MTCMOS Fig. 19 [82]. The dual-threshold CMOS device gate terminal is connected to the body terminal. DTCMOS-CSVCO is constructed with five stages, and the delay stage inverter is also made as same as the DTCMOS device. Based on the biasing, the devices act as critical and non-critical paths. If it is in the critical path when the body is coupled with a gate terminal, the NMOS body terminal is tied at the higher potential, whereas the PMOS body terminal is tied at the lower potential, resulting in a decrease in the cut in voltage of both NMOS and PMOS transistors. If the opposite operation is performed in the non-critical path of the DTCMOS, then the DTCMOS- CSVCO can improve performance in the ON state and minimize leakage current in the OFF state [82]. As a result of ageing, the threshold voltage and saturation current of transistors deviate from their starting values, which can have severe consequences [52], [53], [83]. If threshold voltage increases, then the delay of the transistor also increases. The ageing can corrupt the output frequency of the VCO [52], [53].

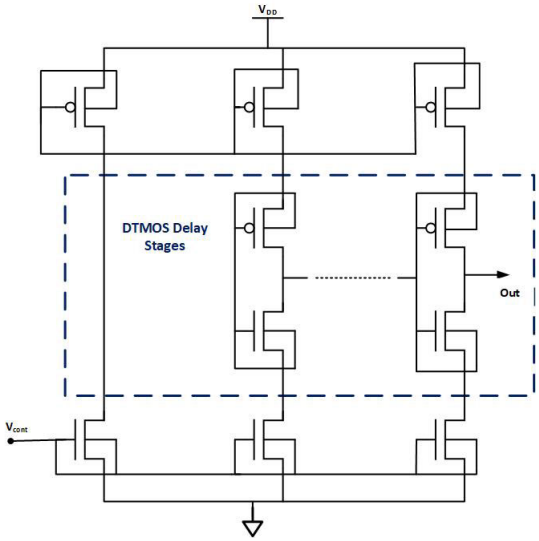

FIGURE 19. N stage DTCMOS-based CSVCO.

A ring oscillator design with decreased frequency drift above the temperature has been proposed by George et al. in 2022 [52]. As a method to eradicate frequency drift, the oscillator's output frequency is compensated with a PTAT (Proportionally To the Absolute Temperature) current. The VCO design consists of ring oscillator configurations and frequency-controlling circuits. The frequency is controlled by two circuit components: the voltage-to-current converter circuit and the PTAT current-generating circuit. The ring oscillator configuration was combined with the nine delay cells, and each delay cell contained the three cascading inverters, and these delay cells produced an equal number of the output phase/frequency. So that the ring oscillator oscillates at the required frequency, the number of inverters within the delay cells has been selected. The PTAT current can be generated by a simple beta multiplier circuit, but it cannot be provided by accurate results. Because of its excellent simplicity and low power consumption, it could be used to generate a PTAT current when accuracy is not essential [52], [59], [84].

B. DIFFERENTIAL DELAY CELL-BASED VCO

A differential ring oscillator type VCO is a type of CS-VCO in which the differential delay cells are used as the delay cells. Delay cell architectures decrease power consumption by eradicating the conventional ring VCOs cross-coupled latch Fig. 20 [85]. Instead of a latch, the inverters of the delay cell generate negative conductance through the addition of an RC network, which enhances the VCO's start-up performance. The Phase noise can also be improved by delay cell architecture. In modified differential cell Fig. 21 architecture, which is replaced the PMOS transistor with the RC network of the Capacitance C_L and resistance R_s. This RC network can Produce negative conductance and eradicate the power dissipation from the latch circuit [85]. The post-layout simulation results demonstrate that a differential ring

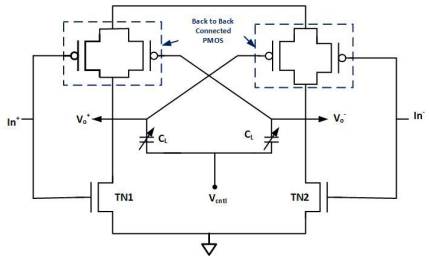

FIGURE 20. Conventional differential delay cell.

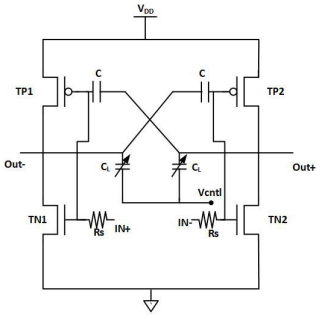

FIGURE 21. Modified differential delay cell.

with a positive feedback architecture based on active CMOS transistors and a polysilicon resistor contributes acceptable performance in terms of the oscillation tuning range, power consumption, and phase noise [58], [74]. The substrate noise can be reduced by the differential mode ring oscillators. Positive feedback has been introduced by a fully differential CMOS amplifier in order to decrease delay time and increase the operation speed, and at the same time, negative feedback increases the speed [74]. The differential logic delay cell can be divided into two categories, which are fully differential and pseudo-differential. As with a fully differential VCO, the presence of a tail bias current makes the VCO simple to oscillate by supplying a constant current to the delay cell. In addition, fully-differential logic can reduce the working voltage swing and the switching time between the various logic levels, allowing for high speed [46], [77], [86].

Typically, the tail current source will have the worst phase noise. In order to ensure known pseudo-differential VCO oscillates deferentially, as opposed to fully differential logic, a cross-coupled circuit is typically used, which results in a slower oscillation speed but improved phase noise. The capacitive circuit tuning will reduce the frequency of oscillation. Due to its higher oscillating frequency, superior tuning linearity, and moderate swing variation, the resistance tuning technique has been employed in this instance [77]. The number of delay cells inside the loop ascertains the frequency of operation. The capacitor and resistor tied to the output terminal are determined by the Quiescent regions of delay-stage transistors. This kind of sized transistors is in accordance with the $\frac{g_m}{I_D}$ method, and it explores the design of the space using the relation between the $\frac{g_m}{I_D}$ ratio and the normalised discharge current $\frac{I_D}{(width/length)}$ as the fundamental design relationship [99]. A quick and enhanced differential VCO is built using symbolic techniques and multi-objective software algorithms to enhance the resolution of an ADC(Analog to Digital Converter).

The differential VCO is then optimized using Multi-Objective Particle Swarm Optimization (MOPSO) and Infeasibility-Driven Evolutionary Algorithm (IDEA) algorithms, which optimize phase noise and power dissipation [87]. The differential ring topology for VCOs can be utilized for rejecting common mode noise and avoiding bypass coupling capacitors with excellent stability and a high frequency. The burden of a differential ring oscillator has both active and passive components. The differential ring oscillator is required to have a broad tuning range, constant voltage output swings, low power consumption, and very low noise [88]. The differential VCO configuration can reduce the substrate noise. Tuning voltage (V_{tune}) is connected to the gate of PMOS transistors, which controls the output frequency of the structure. Positive feedback increases speed, whereas negative feedback requires more resistance for the same speed. The three-stage differential ring is preferred to enhance the oscillation frequency and reduce the power consumption [89].

C. PERFORMANCE PARAMETERS OF THE RING VCO

1) JITTERS AND PHASE NOISE IN RING VCO

The critical analysis of the phase noise of saturated ring oscillators derives from the truth that these types of oscillators are occasionally time-varying systems and the noise sources are modulated, which means they are no longer stationary but cyclo-stationary [80], [81], [90], [91].Typically, Jitter refers to the deviation from the ideal timing of an occurrence. Jitters occur in various system components of the digital system. Each circuit element that generates, transmits, or receives signals may introduce a Jitter. Jitter is commonly known as a time domain behaviour [92], [93]. Jitter can be measured from the eye diagram of the PLL system [94].

The Jitter is also classified into two, which are deterministic Jitter and absolute Jitter. The deterministic Jitter is determined by periodic frequency modulation. Absolute Jitter is the disparity in phase between the noisy oscillator and the noiseless oscillator operating at the analogous standard frequency [71], [92]. In order to describe the phase noise accurately, one must take into account the fact that any oscillator is a frequently time-varying system. The time-variant approach involved here is capable of accurately assessing the impacts on the phase noise of stationary and cyclostationary noise sources, in contrast to phase noise systems that consider linearity and time-invariance [95]. The general noise source of the circuit can be categorized into two, which are interference and device noise. The device noise may be categorised into two types, which are active and passive device noise. Commonly available noise sources in the circuit are thermal noise, shot noise, flicker noise and substrate noise [81], [84], [91], [96], [97]. The active

device $-G_m$ and resistors combined noise is accounted for by an excess noise coefficient F [55].

The Voltage source connected series with the resistance, and it's spectrum is referred to as white, and the noise voltage can be obtained as an equation (7) [71], [81],

$$S(f) = \bar{V}_n^2 = 4kTR \quad V^2/Hz \tag{7}$$

where K=Boltzmann constant $=1.38\times10^{-}23\ JK^{-}1$ and T represent the absolute temperature. If the voltage source is tied series with the resistance and its spectrum is written as equation (8),

$$S(f) = \bar{I}_n{}^2 = \frac{4KT}{R} \quad A^2/Hz \tag{8}$$

The CMOS transistors can generate the flicker noise $\frac{1}{f}$ and thermal noise. The calculation of flicker noise is given as equation (9),

$$S_{\frac{1}{f}}(f) = \frac{K}{\omega LC_{ox}}\frac{1}{f} \tag{9}$$

For computing thermal noise of the saturated is depicted as equation (10),

$$\bar{V_n}^2 = 4KT\gamma g_m \quad A^2/Hz \tag{10}$$

Phase noise performance is methodically inferior compared to devices with high-Quality factor(Q-factor) resonant components. A direct trade-off between power consumption and phase noise performance exists [57], [62], [71], [80], [98].

2) SUPPLY SENSITIVITY OF VARIOUS RING OSCILLATOR TOPOLOGIES

Supply sensitivity is defined as the degree to which a system, device, or circuit is affected or influenced by changes in its power supply voltage. Supply sensitivity is a crucial factor to consider in electrical and electronic engineering, especially while constructing and analyzing circuits, due to its impact on the reliability, efficiency, and functionality of electronic devices. The delay cells in the ring VCO, which are sensitive to supply noise, are effectively mitigated when confronted with significant digital switching noise, and it is achieved through the implementation of a fully differential supply-regulated tuning mechanism [173].

Fully differential and current-starved cells necessitate extra headroom, and voltage regulation introduces power consumption and complicates loop dynamics due to its poles. Furthermore, compensation schemes for delay cells require calibration circuitry since the inherent delay cell sensitivity to supply voltage remains. A low-voltage-operating delay cell that inherently mitigates supply requirements without requiring calibration or additional regulation. In order to address supply sensitivity and incorporate a source-follower structure, it has been effectively isolating the supply appreciations to its saturation output resistance. The source terminal is directly connected to the V_{DD}, so the conventional structure lacks inherent supply isolation, resulting in a static supply sensitivity close to unity [14]. VCO with inherent zero-supply sensitivity would be obtained across a broad frequency range through joint supply and control voltage biasing. Design guidelines facilitate the adjustment of supply sensitivity, positive or negative, as needed. For systems with positive supply sensitivity, the VCO can be configured with negative supply sensitivity for compensation. Employing adaptive feedback, the design optimally determines the bias point to minimize output jitter [60].

A technique to reduce supply sensitivity in the Current Mode Logic (CML) oscillators, established and confirmed through measurements, involves connecting capacitively degenerated cross-coupled pairs in parallel with each delay stage. The CML approach employs negative transconductance near the operating frequency to counter-supply noise-induced frequency variations while also preventing excessive close in-phase noise through high impedance at low frequencies and suppressing sinusoidal jitter [174]. A switched resistor array has been suggested to diminish the tuning sensitivity of the ring VCO does not compromise its tuning range [175]. An oscillator-based PLL utilizing a ring oscillator, coupled with a current source compensation technique, effectively reduces supply sensitivity. This compensation method achieves nearly zero supply sensitivity when optimally calibrated. Especially, it circumvents stability concerns and can be applied to various types of delay cells [176].

From Table 1, the researcher can analyze that the supply sensitivity of a ring oscillator is affected by its topology. CMOS ring oscillators are among the most sensitive devices due to the direct influence of supply voltage on transistor thresholds. When compared to CML, LC tank, and delay-cell ring oscillators, the differential ring oscillators offer greater supply sensitivity. Designers select the optimal topology based on application requirements, taking into account supply noise immunity, frequency stability, and power consumption. In low-power applications, supply sensitivity reduction is crucial. Future designs may prioritise low-power strategies such as Dynamic Voltage Scaling (DVS) or subthreshold operation, which can be combined with adaptive circuitry to maintain oscillator performance while minimising supply variations. Combining various oscillator topologies, such as CMOS and LC tank oscillators, in a hybrid design can provide a balanced solution between supply sensitivity and performance, especially for high-frequency applications.

3) COMPACT SIZE OF RING VCO

The compact size of Ring Oscillators is one of the major reasons for being used in modern integrated circuits (ICs) present in Table 2. Comparing its compactness form factor to other oscillator types is valuable because it offers numerous benefits: 1. In comparison to other oscillator designs, ring oscillators are easier to implement since they require only transistors. 2. They dissipate less power because the circuit design utilized only transistors. 3. Ring oscillators are

TABLE 1. Supply sensitivity comparison table of ring oscillator topologies.

Ring Oscillator Topologies	CMOS Ring Oscillator	Differential Ring Oscillator	Current-Mode Logic (CML) Ring Oscillator	LC Tank Ring Oscillator	Delay-Cell Ring Oscillator
Supply sensitivity in Ring Oscillator	Moderate to High	Moderate	Low	Low to Moderate	Low
Merits	Widely used because of their simplicity and good frequency stability	Provide better supply noise rejection compared to single-ended CMOS ring oscillators.	Less sensitive to supply voltage variations because the delay elements depend more on the tail current.	Less sensitive to supply voltage variations compared to CMOS oscillators.	Less sensitive to supply voltage variations because the delay cells are designed to be relatively immune to changes in supply voltage.

comprehended to include in a variety of IC designs, and they can be positioned adjacent to other functional blocks to improve signal routing and reduce parasitic effects. 4. Ring oscillators are appropriate for applications that need fast clock signals because they can operate at high frequencies.5. Ring oscillators offer the flexibility to tune their output frequency by adjusting the number of stages. 6. Ring Oscillator provides moderate phase noise, but other types of oscillators may offer superior frequency stability and phase noise.

TABLE 2. Comparison of compact size ring VCO and LC-VCO.

Ref	VCO Type	Area (mm^2)	Ref	VCO Type	Area (mm^2)
22	Current Starved	0.047	106	LC-NMOS	0.88
23	Current Starved	0.003	111	LC-NMOS	0.807
63	Current Starved	0.0075	118	LC-NMOS	0.74
64	Current Starved	0.023	142	LC-CMOS	0.7
94	Current Starved	0.244	143	LC-CMOS	0.9

In comparison with LC types of oscillators, often, quite large and complex circuits will consume more power because inductors and capacitors are used. LC types of oscillators also render high frequencies, but tuning circuits are quite complex.

III. LC-VOLTAGE CONTROLLED OSCILLATOR

Generally, Phase lock loops are implemented using two different VCO architectures: the Ring oscillator VCO and the LC oscillator VCO. The CS-VCO based PLL causes higher phase noise and a lower operating frequency, and hence it is not generally used for high-frequency applications [38], [56], [100]. LC-VCO comprises a cross-coupled pair of transistors, Inductors, and variable capacitors, as shown in Fig. 22 [101]. The cross-coupled transistors can generate negative resistance ($-R_p$), and this negative resistance needs to be overcome by introducing parallel resistance ($-R_p$) [101], [102], as shown in Fig. 22 [101].

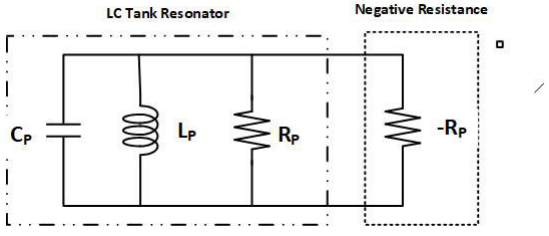

FIGURE 22. Negative resistance model.

The generic LC-VCO circuit contains the LC resonator with negative resistance in Fig. 22. This Circuit shows that the C_p, L_p, and R_p are equivalent circuit resistance, capacitance, and inductance, and ($-R_p$) projects the negative resistance produced by the active transistors. If R_p is equal to ($-R_p$) ($R_p = -R_p$), sustained oscillation occurs, or if R_p is less than the $-R_p$ ($R_p < -R_p$), the oscillation decays exponentially; if R_p is greater than ($-R_p$) ($R_p > -R_p$) the oscillation grows in nature. The latter's presence results in continual energy loss in the resonant cavity. In order to prevent this loss, energy from an outside source must be continuously pumped into the system to ensure stable and continuous oscillation [97]. The LC-VCO is commonly used to construct the three architectures, which are 1) N-MOS Cross coupled LC Oscillator, 2) P- MOS Cross-coupled LC Oscillator, and 3) complementary cross-coupled LC Oscillator.

A. NMOS CROSS-COUPLED LC OSCILLATOR

Fig. 23 shows the NMOS cross-coupled LC Oscillator architecture [101]. The circuit consists of two NMOS tail current-connected current sources, two varactors, and two inductors.

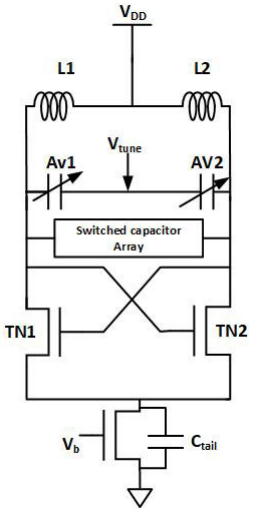

FIGURE 23. NMOS cross-coupled LC oscillator.

The NMOS LC-VCO Taxonomy diagram is highlighted in Fig. 24. The taxonomy diagram represents the researchers

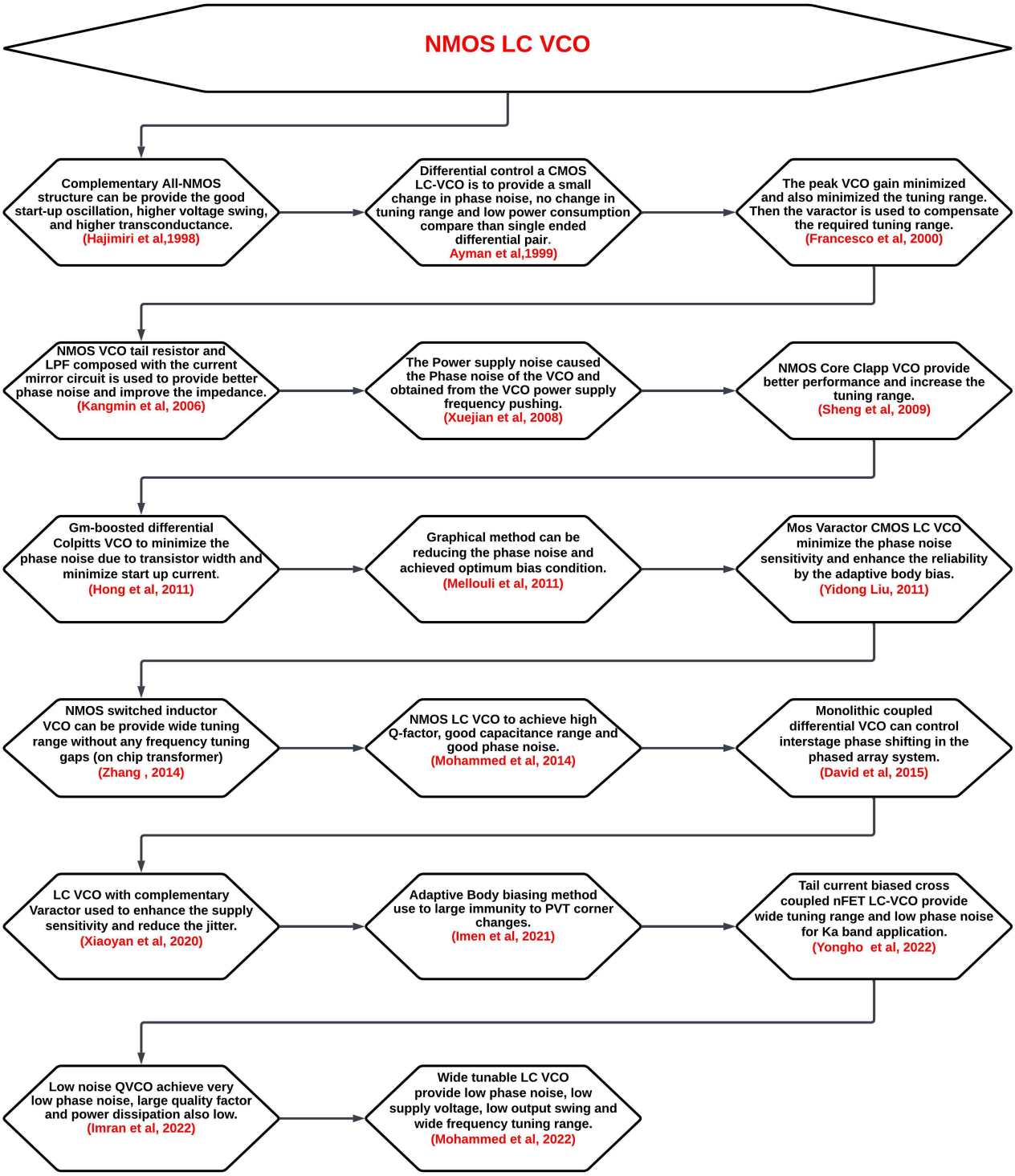

FIGURE 24. NMOS LC-VCO taxonomy diagram.

who developed and enhanced the NMOS LC-VCO circuit throughout the period from 1998 to 2022. The varactor pair is used to tune the frequency and boost the varactor quality factor, which can improve the generation of harmonic power [103]. Injection-locked VCO: VCO oscillating frequency could be obtained by the input of the injected frequency. Tail-connected inductor achieved acceptable phase noise [104], [127]. Inductive transformer feedback method-based PN-VCO architecture achieved low phase noise and improved the Q factor and negative conductance [105], [128].

Reduce the quadrature error and phase noise by modifying the self(automatic) injection-based QVCO (Quadrature- VCO) [106], [129]. A perfect selection of coupling coefficient (k) and common mode resonance is used to attain the largest oscillation frequency for the flicker noise suppression method [96]. A Dual-band VCO structure is implemented with a bandpass filter and Injection amplifier [107]. The bandpass filter selects the second harmonic output signal, which the injection amplifier stage then amplifies. Symmetrically split inductors have improved the frequency of oscillation and power consumption. The tuning range is increased by using a larger size of varactors [107].

A pair of sandwich-type connected MOS capacitors employed as varactors can be utilized to create a tuning range [108]. If varactors are connected in the middle, the phase noise will be degraded, or else, in parallel with an NMOS device, it does not suffer the phase noise [108]. The back-to-back connected varactors can increase the tuning range and reject the required decoupling capacitors. Face-to-face Connected varactors with decoupling resistors can be connected and decoupled with the RF output terminals, decreasing the VCO loading effect. In this case, resistance should be large [109]. Phase noise can highly depend on the quality factor of the varactor [109]. With a selection of voltages, the MOS varactor can be provided with a broad tuning range. The greater phase noise issue can be overcome by the fixed value capacitor cascade connection with the varactor [110].

NMOS VCO is supplied by the PMOS current source, which induces noise in the VCO output, that increases the power supply rejection ratio and fixes the constant current. This noise problem can also be solved by the low pass filter. Tail-connecting resistors can increase source-connected NMOS pair impedance and prevent quality factor degradation [111]. One more cross-coupled transistor has connected with NMOS VCO circuits, this pair wants to generate negative resistance and rejects the resistance loss in the LC tank circuit. The impedance circuit can be split into two parts: the negative resistance device and capacitance. The negative resistance and tank loss can wipe each other out. Increasing the oscillation frequency decreases the negative resistance value [111], [112]. The cross-coupled NMOS transistor operating under a subthreshold region and its tank loss and transconductance g_m can be expressed as an equation (11),

$$g_{active} = -\frac{g_{m_{nmos}}}{2} \tag{11}$$

The width of the transistor should be selected to offer the least amount of transconductance while increasing the Number of transistor Fingers(NF) [120], [122]. The adaptive body biasing technique enhances startup constraints and PVT (Process Voltage Temperature) variations [122]. An adaptive rectifier reduces the equilibrium threshold voltage, and a bias resistor allows for the coupling of the dynamic body voltage to the drain voltage and voltage of the bonding wire. This bonding can be used to enhance the overall circuit performance [113], [122]. The dynamic body bias method is used on the VCO core transistors to enable faster-switching transitions, which concurrently reduces conduction time and, in turn, results in lower power consumption and provides improved noise performance [170]. Differential Colpitts VCO architecture with a new method of drain-to-source feedback-based boosting that improves oscillation amplitude and startup conditions, and it demonstrates decreased optimal phase noise by maintaining the transistor in the saturation region at the most significant oscillation amplitude [114], [130]. Conventional NMOS LC-VCO is modified, which connected tail current with a current source. This tail capacitance can minimize the tail current high-frequency portion and tail node voltage fluctuations [95], [115].

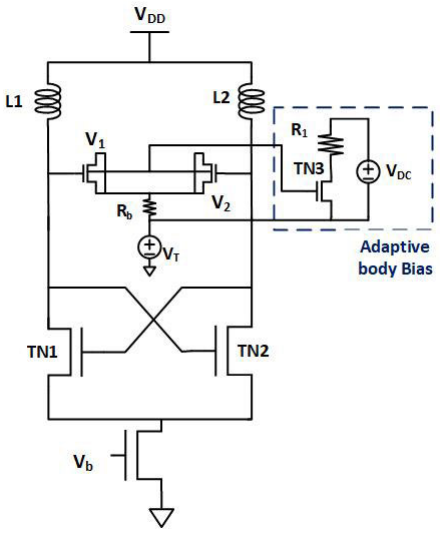

FIGURE 25. Adaptive body biasing technique.

The resultant tank deteriorates the centre frequency and phase noise of VCO change, resulting in stress-induced threshold voltage shift of the MOS varactor. The threshold voltage change can affect the VCO Performance. So, the Adaptive body biasing technique minimizes the phase noise sensitivity and enhances the VCO reliability, Performance [116] depicted in Fig. 25. The compromise between operating frequency, tuning frequency, and capacitors are required to maintain the oscillation frequency of operation, which will increase the area of the capacitance in the LC tank circuit that can be determined the operating frequency. The number of inductors can be calculated by the desired tuning frequency ratio $\frac{f_{max}}{f_{min}}$ and capacitance ratio of the maximum tank to the minimum tank. The desired inductance can be calculated for its adjacent bands. $\frac{L_n}{L_{n+1}}$ is given by equation (12) [117],

$$\frac{C_{tank_{max}}}{C_{tank_{min}}} \geq \left(\frac{f_{max}}{f_{min}}\right)^{\frac{2}{n}} = \frac{L_n}{L_{n+1}} \tag{12}$$

If switched capacitor banks are increased in the VCO design, tuning frequency will also be increased [118], [131], [132], [133]. The transconductance can be modified for the tank circuit by adjusting the bias currents. This VCO works in the triple mode of operation, and this circuit works under transformer-based dual coupled triple mode LC-VCO [118]. A transformer-based millimeter-wave VCO architecture has been used to extend the tuning range while maintaining minimal phase noise degradation. In order to mitigate the effect of OFF-state parasitic capacitance, differential switches were working in the secondary and tertiary coils. The enhancement not only improved the effective quality factor seen by the primary coil but also advanced the TR in comparison to a single-ended implementation. Besides, a 3-D implementation of the transformer, with each coil placed out in a separate metal layer, enhanced the mutual coupling factors between coupling coils. Consequently, this led to reduced effective ON-state resistance (due to the switches) at the primary coil [171]. However, the researcher has a great challenge while designing the high-speed LC-VCO, 1. Varactor/Capacitor banks need to provide a wide tuning range, 2. Tank loss wants to be significantly less, 3. Better phase noise, 4. Proper biasing current biasing source, 5. The quality factor ought to be as high as possible, 6. Parasitic capacitance should be as low as possible, 7. The designer must avoid high power supply resilience and the largest up-conversion in the flicker noise [31], [67], [102], [119], [134]. The Compensation technique minimizes supply sensitivity in the single-ended VCO and achieves low phase noise, a higher operating frequency, low power, tuning range, and a higher supply rejection speed. The periodic jitter performance can be degraded by the primary factors, which are the two varactors and switched capacitors. The Periodic jitter is obtained from the ratio of the fundamental power to the first sideband power, and the jitter is expressed as equation (13) [48], [84], [121],

$$\hat{J}_{p\_p} = \frac{2}{\pi * \sqrt{\frac{P_0}{P_1}}} \tag{13}$$

An RC low pass filter at the tail Field Effect Transistor (FET) gate node enhances the output resistance over a wide range of V_{ds}, as well as suppresses the output noise of the tail FET [123]. It consequently fosters the phase noise when combined with an LC tail filter. An inter-stage LC filter at the VCO buffer interface boosts the swing at the buffer input to avoid unwanted phase noise degradation. Consequently, when used with an LC tail filter, it reduces phase noise. One more LC filter is used in between the stages, and this will improve the input swing in the buffer and avoid the undesired phase noise reduction [123]. By incorporating a substantial tail capacitance in the common source node of the differential pair and a bias network to ensure that the transistors work outside of the deep triode region, it is possible to accomplish two significant advantages simultaneously. First, we convert the DC bias current into class-C current waveforms with a high conversion efficiency. Second, minimize the undesirable noise generation, thereby optimizing phase noise performance. In addition, the capacitance of the tail effectively filters out high-frequency noise caused by the bias current [230]. The QVCO configuration is better to provide negative conductance and also relatively low power consumption because the drain terminal provides the current, and this current could be reused by the back gate method [5], [124] as shown in Fig. 26 [124].

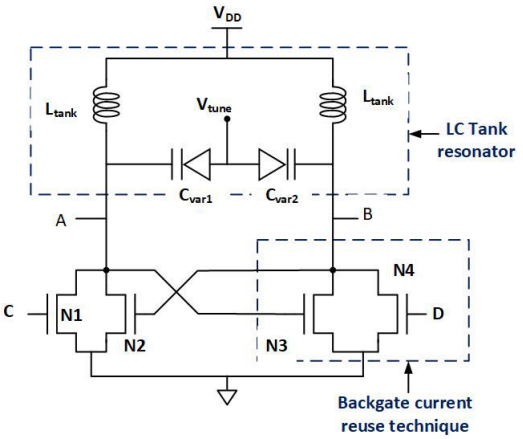

FIGURE 26. Back-gate technology.

In the tail current, two varactors can control the frequency tuning, and the oscillator can develop a wide frequency range [125]. Oscillator tail current can suffer from the characterization of an active inductor. So, the tail current requirement and the parallel resistance value cannot be obtained each of these independently. The desired frequencies and the parallel resistance value are obtained and verified; this value does not surpass the dynamic frequency range of the inductor [125]. The oscillation frequency can be expressed as (14),

$$f = \frac{1}{2\pi * \sqrt{L_1 C_1}} \tag{14}$$

By lowering the power supply voltage to obtain a low threshold voltage, the cross-coupled NMOS pair can be supplied in a subthreshold regime. According to the oscillation frequency, on-chip inductors, varactors, and active transistor sizes have to be fixed [76], [125], [135].

B. PMOS CROSS-COUPLED LC OSCILLATOR

Fig. 27 shows that the PMOS Cross-Coupled LC Oscillator architecture [136], [145]. The circuit consists of two PMOS tail current-connected current sources, two capacitors, and two inductors. The PMOS LC-VCO Taxonomy diagram is shown in Fig. 28. The taxonomy diagram represents the researchers who developed and enhanced the PMOS LC-VCO circuit throughout the period from 2005 to 2023. The tail capacitor is used to reduce voltage variations in the tail node and attenuate the high-frequency noise components

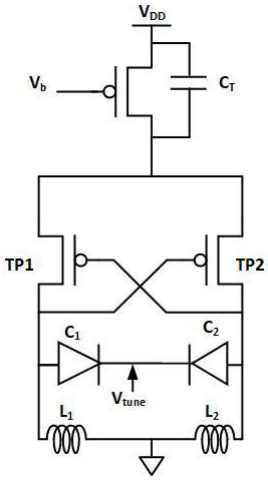

FIGURE 27. Basic PMOS cross-coupled LC oscillator.

of the tail current [136]. Cross-coupled VCO with a capacitive feedback method will impart high symmetric wave-forms and minimum harmonic distortion in the output of the VCO. PMOS transistors achieve lower 1/f noise than NMOS transistors by using the PMOS tail current source. Persistently decrease flicker noise, which will substantially minimize near the phase noise by increasing the PMOS tail transistor's width and length. VCO achieves the best performance of the circuit, specifically for the higher frequencies, by using the capacitive feedback of the PMOS cross-coupled pair [137], [145]. Capacitive feedback of the PMOS cross-coupled design also enhances output swing and phase noise [137], [145].

To fulfil the Barkhausen criterion for sustaining oscillation, ensure both the oscillation frequency and the unity loop gain condition are given as (15) [137],

$$f = \sqrt{\frac{C_1 + C_2}{C_1 C_2 L_D}} \tag{15}$$

Small-size PMOS transistors cannot produce the required transconductance for oscillation start-up. Additionally, larger transistors can generate a large capacitance, which will minimize the frequency tuning range(FTR) [138]. The back gate methodology reduces the transistor threshold voltage; thus, the method is to have opted for the low voltage applications. The LC tank introduces the fine-tuning and coarse-tuning methods [139]. The fine-tuning technique consists of two varactors: likewise, the coarse-tuning method consists capacitor array. Tuning circuit design is very simple and enhances the performance of the VCO. The cross-coupled PMOS VCO design minimizes phase noise and less flicker noise compared to the NMOS. CMOS-based LC tank VCO topology linearizes the tuning range with PMOS varactors [140]. With PMOs varactors that stay in the inversion zone for a wide range of the control voltage, where the VCO tuning range is linearized. Tuning is accomplished by designing the output nodes for the VCO's quiescent operating region to get a value to the supply rails, allowing the varactors to behave almost linearly within the range of achievable VCO tuning. Increasing the frequency range of the varactor requires a high ratio of $\frac{C_{max}}{C_{min}}$ corresponding with a large Q-factor [141], [146].

The transistors in the PMOS pair are able to carry a small amount of current for a small portion of the cycle if the capacitor is sufficiently large. This effect is essential because it diminishes the noise injection from the drain current during the tank differential voltages zero crossing. The system incorporates a dual loop control, consisting of analog components, to adjust finely and broadly tune the VCO [142]. Switched resonator design enables effective noise cancellation through a low VCO gain while still maintaining a wide range of tuning capabilities. The VCO coarse input is controlled through an analog circuit that continuously modifies the gain. The dual-band of the VCO design is used with a switched resonator [143], [144]. Switched resonators can achieve the same levels of phase noise and power consumption. To enhance the performance of the switched resonator of the VCO, when the control switch is also activated, it is essential to minimize the mutual inductance of the inductor coil and optimize the size of the transistor switch [143].

C. CMOS CROSS-COUPLED LC OSCILLATOR

The Fig. 29 shows the Complementary-CMOS LC-VCO architecture [149]. This Circuit is constructed with two PMOS transistors, two NMOS transistors, two inductances, and two variable capacitors.

The CMOS LC-VCO Taxonomy diagram is shown in Fig. 30. The taxonomy diagram represents the researchers who developed and enhanced the CMOS LC-VCO circuit during the period from 2005 to 2023.

The CMOS transistors, including NMOS and PMOS transistors, play a vital role in the CMOS LC-VCO circuit [147], [160]. The researchers are associated in a cross-coupled configuration, creating a positive feedback loop that sustains the oscillation. The NMOS transistors have their source terminals connected to the ground, whereas the PMOS transistors have their source terminals linked to the supply voltage. The Resistance is generated by the cross-coupled NMOS transistors TN1 and TN2 to eliminate the losses caused by the Parallel LC tank in the resonance. The PMOS transistors, TP1 and TP2, in the cross-coupled configuration of the CMOS LC-VCO circuit, have a width that is double of the NMOS transistors, and it is deliberate sizing asymmetry to enhance the loop gain, improving circuit performance. Moreover, using PMOS devices enables better symmetry at each resonant node by balancing the positive and negative drive strengths. Phase noise is reduced in large part by this emphasis on symmetry in both the full circuit and each half circuit. The topology of the CMOS LC-VCO, combined with careful attention to symmetry, plays a pivotal role in reducing phase noise. One immediate impact of this characteristic is that when the bias current is doubled in the CMOS

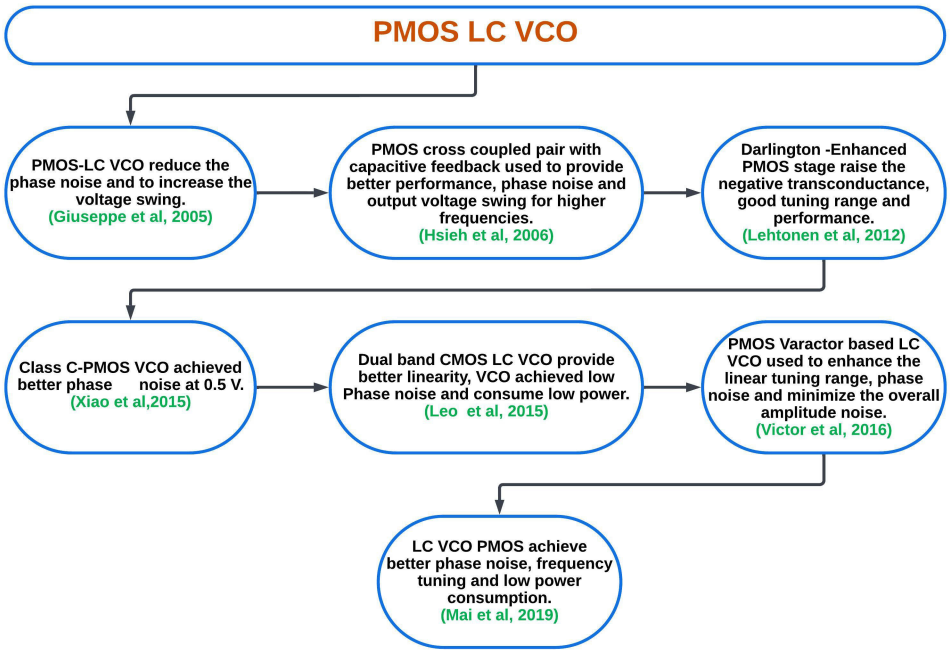

FIGURE 28. PMOS LC-VCO taxonomy diagram.

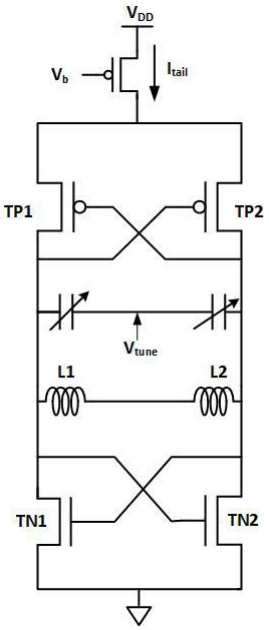

FIGURE 29. Basic CMOS LC-VCO.

LC-VCO, it never reshapes the noise prompted by the oscillator core [148].

However, doubling the bias current results in oscillation amplitude also doubled. As a result, the phase noise is improved. When parasitic capacitances exist among the tank outputs and ground in a CMOS LC-VCO, the ideal symmetry among the PMOS and NMOS transistors pair is compromised. This occurs since the PMOS sources are no longer floating, allowing PMOS noise to discover a path through the tank to the ground. Meanwhile, the NMOS noise is still effectively ignored due to cascading from tail source bias, assuming that parasitic capacitance at NMOS sources is negligible. The utilization of a cascade pair of tail current sources effectively mitigates 1/f noise without introducing any additional area consumption overhead. By employing a PMOS current source with an extended gate length and implementing bias filtering techniques, the achievement of low phase noise has been made possible [149], [162].

Moreover, to minimize flicker noise upconversion without compromising thermal noise, both the tail current source and mirror in the VCO are maintained at a large size. Bias filters are employed within the VCO circuit to effectively reduce reference current noise and mitigate dynamic switching causes on the bias line. In this subthreshold regime, the MOS drain current is primarily governed by the diffusion mechanism [125], [135]. Phase noise is reduced as a result of the large transconductance-to-drain current ratio that is produced. Consequently, low power consumption and low phase noise particularities can be attained without the need for non-conventional high Q passive components. The dynamic common mode feedback design is employed to dynamically adjust the common-mode (CM) voltage of the differential varactor tuning signals with the VCO CM voltage [150].

In contrast, with replica biassing and other widely used methods, this strategy doesn't require any more power [151]. Besides, it precisely trails the VCOs output common-mode voltage during oscillations. By utilizing a differential control scheme, this technique enables a significantly wide tuning

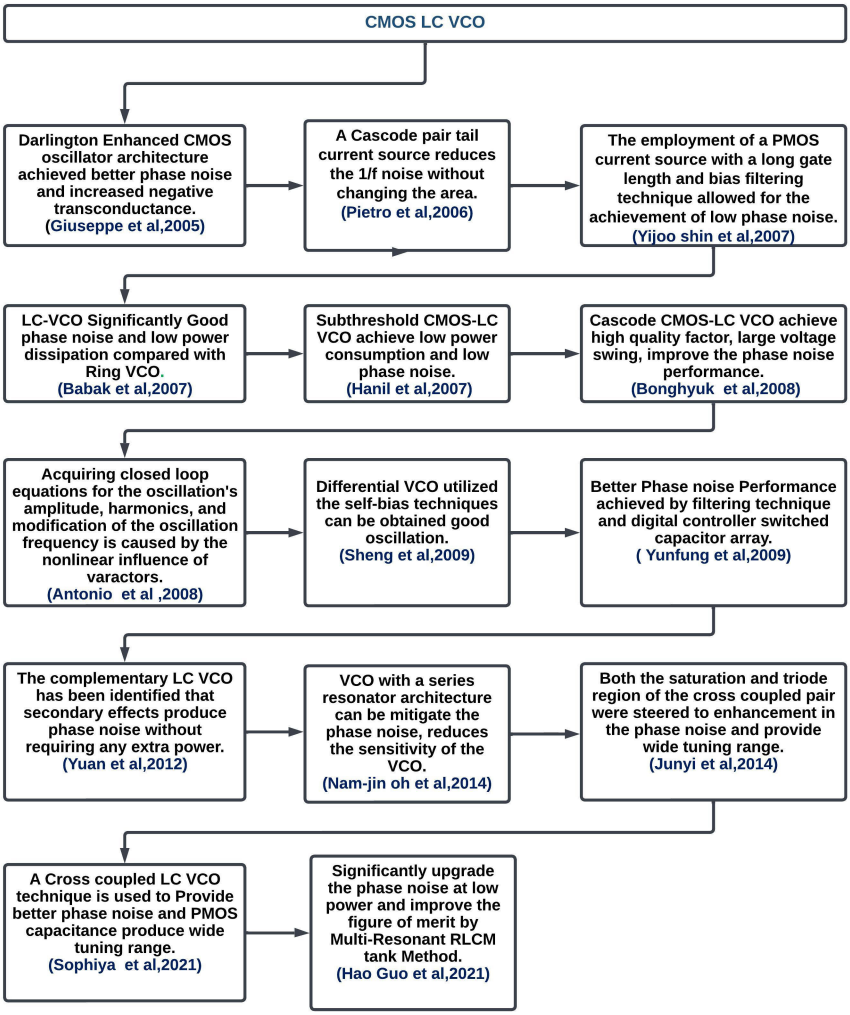

FIGURE 30. CMOS LC-VCO taxonomy diagram.

range. Introducing negative conductance can effectively minimize the overall output conductance of a VCO, leading to an increased output swing and an improved quality factor. This enhancement in performance results in enhanced phase noise characteristics for the VCO. The shape of the oscillation and its frequency are influenced not only by the nonlinearity of devices, as typically observed in LC-tuned oscillators, but also by the nonlinearity of varactors [152]. Therefore, the frequency tuning curve deviates from the anticipated curve based on the capacitance-voltage characteristics of the varactors. The aforementioned difficulties are frequently solved by making the assumption of constant capacitance. The circuit model is simplified to a single second-order differential equation as a result. The differential VCO circuit consists of two single-ended half-circuit Colpitts oscillators combined into a single differential configuration [153]. A configuration consisting of NMOS and PMOS transistors is used to provide the necessary negative conductance in order to enable oscillation start-up. In this study, the proposed differential VCO incorporates self-bias techniques for both the VCO core and buffer interface, resulting in improved oscillation performance when compared to alternative topologies. By utilizing a long-channel NMOS tail current source, achieving the perfect common mode, which parallels the VCO and the divide-by-two circuit, becomes easier, eliminating the need for an additional DC-level shifting circuit [154].

The LC tank uses switched capacitor bank arrays along with a small varactor to achieve a wide frequency range with a relatively low tuning sensitivity. The desired frequency range is divided into 16 sub-bands using a 4-bit binary-weighted array of switched metal-insulator-metal (MIM) capacitors. The coarse tuning will be done by the varactors. Simultaneous achievement of a broad tuning range and low phase noise performance is accomplished in the VCO by incorporating a switched capacitor array and noise filtering technique. The CMOS LC QVCO features a unique capability to automatically change its NMOS from a

strong inversion region to an accumulation region, thereby effectively reducing flicker noise [155]. The Researcher provides a unique quadrature coupling method (QCM) that enables this seamless and automated switching. The unique quadrature coupling method involves dividing the tail by biasing the current source and injecting the connecting signal directly into the current source's gate. A phase error results when there is a mismatch between the two VCO cores. The utilization of a composite CMOS transistor structure enhances the gain of the negative-transconductance stage, ensuring a dependable initiation, and also enhances device reliability by incorporating high-voltage transistors [156].

The square of the resultant swing, whose expansion most likely instantly results in higher supply, determines the phase noise in an inverse proportion [157]. The tail bias current source and the differential pair of negative g_m switches are the major noise inputs of the up-conversion. In order to further enhance the noise performance, the current source, which adds a significant amount of noise to its output, is eliminated by the series resonator VCO [158]. In the series-connected node containing the inductor and capacitor, the series resonator increases the fundamental frequency while attenuating the noise and harmonic components.The Self-Adaptive Active Resistor (SAAR) will automatically adjust itself to a higher resistance level in order to maintain the quality factor of the LC tank and mitigate the detrimental impacts of the tiny conducting resistor in the cross-coupled transistor entering the triode area [159], [163].

This adjustment prevents any degradation in the quality factor caused by the cross-coupled transistor's conduction resistance. The SAAR fulfils the criteria for achieving the ideal $1/f^3$ phase noise characteristic. The inductor in the Resistor-Inductor-Capacitor-Mutual inductance tank uses a metal resistor approach to remove any mode-ambiguity issue that might arise during the VCO's starting. With this method, the mode-ambiguity problem is completely avoided. By employing a rich harmonics approach in the RLCM tank, the Intermodulation Suppression Filter (ISF) is effectively shaped to mitigate the conversion of transistor noise to phase noise across both the $1/f^3$ and $1/f^2$ frequency regions. Phase noise is significantly reduced as a result of this improvement, especially at low power levels [161].

D. CLASS-B, C, D, E, F AND COLPITTS LCVCO

1) CLASS-B LCVCO

In Class-B LC-VCO, two active CMOS transistors are in a push-pull configuration, where one transistor conducts during the positive half of the signal cycle, and the other conducts during the negative half. By comparison with Class-A VCOs, this helps increase efficiency, frequency, tuning range, and lower power consumption. Class-B Cross-Coupled CMOS oscillator can be utilized in the open loop structure to optimize the low phase noise and low power [178]. VCO employs Class-B biasing with optimized switching amplitudes for tail current sources to enhance phase noise performance and employs a G_m-boosted structure to minimize parasitic effects within the LC tank, thereby achieving a larger tuning range [187].

Capacitive coupled with enhanced G_m boosting method also provides and increase in the output amplitude and lower phase noise [188]. Hybrid Class AB/class-B VCO also achieved lower supply, better tuning range, and high performance [189]. The best power efficiency and, thus, the optimum phase-noise-versus-power trade-off are obtained by CMOS oscillators that contain two tail resonators [190]. In order to isolate the LC-tank resonator from internal and external loads and to produce greater negative resistance, the push-pull complementary class-B oscillator is used in the VCO and allows for a large frequency tuning range [191]. Inductive source degeneration is used for the tail current source in a novel Class-B VCO operating in the K-band. As a result, the VCO's core size is decreased, and a compact, low-Q tail filtering inductor can be used at millimeter-wave frequencies [192].

2) CLASS-C LCVCO

The compromise between startup conditions and oscillation amplitude in class-C LC-VCOs reduces the advantages of this topology in comparison to traditional class-B operations. There are two VCOs in the dynamic bias scheme. The first VCO makes use of an active current tail generator, whereas the second VCO uses a passive resistive tail and enables an increasing in oscillation amplitude while maintaining all the advantages of the class-C design. It improves phase noise performance as a result of a given current consumption [179]. By naturally transitioning from class-B to class-C, the class-B oscillator overcomes early design limitations. Startup problems are solved with a low-frequency feedback loop, which also ensures reliable operation and ideal oscillation without sacrificing efficiency [177], [193]. Class-B/C hybrid current-reuse voltage-controlled oscillator (VCO) with strong starting, improved phase noise, and differential balancing at low area and power [194]. A class-B and class-C connected oscillator is used to achieve low phase noise, low power consumption, fast startup, switchable transformers to increase the tuning range, and the push-push approach to produce the W-band oscillation [195].

A class-C core for the main portion and a class-B cross-coupled pair for the secondary portion were constructed for an adaptively biased class-C VCO. The use of the class-B auxiliary pair solves the intrinsic startup problem of the class-C VCOs. When the VCO reaches a steady state, it uses an adaptive bias method to switch itself off. It only operates during startup [196]. A class-C architecture constructed with Capacitive Source Degeneration (CSD) principles and optimizing current efficiency through the segmentation of the PMOS tail current source operating in the subthreshold region. In addition to reducing flicker noise up-conversion in the tail current source, this segmentation increases current efficiency [197]. The phase noise in class-C VCOs is

improved by the introduction of both the Darlington-pair and the noise shifting approaches. A straightforward technique of two cascaded stages in the VCO core is employed to utilise balanced and differential topologies to absorb the strength of both the Colpitts and class-C VCO topology, elevating the VCO driving capabilities without reducing power efficiency [198]. Class-C push-push topology as the VCO core improves phase noise, minimises parasitic capacitance, and improves second-harmonic content to improve mixing efficiency [199].

3) CLASS-D LCVCO

Class-D which combines lower phase noise, lower supply voltage, and higher efficiency by simply expanding the cross-coupled MOS switches of the conventional class-B VCO and eliminating the current control circuitry at the same time. The oscillation amplitude reaches maximum peak voltage up to $3V_{dd}$, and it enhances the power efficiency above 90%. The class-D architecture is appropriate for very low-voltage applications due to the relatively very large oscillation amplitude, which benefits phase noise [200]. In contrast to the time-invariant tank of the Class-B oscillator and its tank losses can be combined into an equivalent parallel tank resistance for efficient analysis of power consumption and phase noise, such simplification is unattainable in the Class-D oscillator. This is primarily due to the time-variant nature of its tank. The enhanced output swing leads to a better phase noise performance. Moreover, with the gate and drain bias voltages being independent, the VCO introduced can oscillate at a reduced supply voltage compared to standard VCOs. This feature preserves valuable chip footprint [181].

An oscillator, fundamentally a feedback-connected amplifier, can be achieved efficient power conversion by using MOSFETs in class D, E, or F modes within a dedicated class of switching amplifiers. Low-voltage class-D differential and QVCOs increase the carrier power through swing growth, which lowers output phase noise. At the lowest supply voltage, this VCO may deliver the greatest FOM to date [201]. A class-D VCO can efficiently use the triode region and improve phase noise performance by using the second harmonic to restore the gain [202]. Low-power class-D VCO that has a resistor to lower power requirements and enhance phase noise [203]. The complementary inverse class-D switching process ensures that the voltage and current waveforms don't cross over, which results in high energy efficiency. The transistor's CDS capacitance is absorbed into the parallel resonant tank, minimizing power loss due to drain parasitic discharge [204].

4) CLASS-E LCVCO

In an effort to diminish chip size, a comparatively modest DC-feed impedance is working, and there's no supplementary harmonic filtering at the output [205]. Class-E oscillators can perform better in all of the factors, which are noise factor, second harmonics, Q-factor of the tank at the fundamental and power efficiency is that directly impact FOM [206]. Theoretically, a class-E amplifier has a straightforward design and a high efficiency of up to 100%. Typically, a transistor serves as the switching mechanism [182], [207].

5) CLASS-F LCVCO

In Class-F VCO, while eliminating the drawbacks of the die size penalty associated with the noise-filtering technique and the voltage swing limits encountered in class-C VCO and the class-F oscillator has achieved excellent phase noise performance and outstanding power efficiency at a low supply voltage [183]. While retaining the oscillator voltage efficiency, the tail current transistor's phase noise contribution is successfully decreased [208]. Transformer feedback is used in the Class-$F_{2,3}$ arrangement to achieve resonant impedance management at two times and three times the VCO fundamental frequency ($f_V CO$). A noise-circulating technique is also used to successfully reduce the noise contribution coming from the tail current transistor [209]. Utilising CM resonance transformers in a CMOS arrangement, a coupled-line-based design is used to construct a scalable multicore Class-F VCO. With this design, tiny inductors have a higher quality factor (Q), and the CMOS setup enables operation at a nominal supply voltage [210].

The parasitic components of the resonator become more prominent as the operating frequency of VCO increases, which lowers the Q-factor. As a result, phase noise degrades and the frequency tuning range (TR) narrow. The FOM for the VCOs is also constrained by this circumstance. A novel graphical Q-optimization technique is used to optimise the Q-factor of the multi-LC resonator using a transformer for Class-F operation. By tweaking the 2nd and 3rd harmonics of the impulse sensitivity function (ISF), it is possible to improve phase noise [211]. Utilizing the class-F VCO and adiabatic switching techniques, a resonant multi-harmonic drive is generated for an N-path-based mixer-first receiver. It is significantly reduces power consumption while upholding a favorable mixer noise figure (NF). Coupled inductors are used to minimize the area of the VCO architecture [212]. The design uses a small quad-core class-F VCO with inductor sharing and a square-geometry transformer tank to minimise chip area. It increases impedance at harmonics and improves phase noise performance Without adding more chip surface [213].

6) COLPITTS LCVCO

Low DC and RMS values for Impulse sensitivity function (ISF) are guaranteed by the PMOS differential Colpitts oscillator pair and switching pair in the VCO core. With this configuration, energy transfer efficiency is maximised, phase noise performance is improved, and a wider output voltage swing is possible [214]. The enhanced Colpitts VCO design to raises the negative resistance and diminishes interference from outside noise, and feedback capacitors are inserted between two transistors [215]. The Colpitts oscillator may

be utilised over a large frequency range, has great frequency stability, and is simple to tune. Due to their excellent phase noise properties, single-ended Colpitts oscillators are frequently utilised [185]. Additionally, under identical circumstances, the output Power Spectral Density (PSD) at the source is substantially smaller than at the drain in NMOS and PMOS. This shows that a bottom-biased PMOS current source performs better than a top-biased PMOS current source for reduced phase noise. Furthermore, by controlling the duty cycle of the current sources in saturation, using a bottom PMOS current source in a cross-coupled system efficiently reduces the close-in phase noise of the VCO [216].

Comparing the Colpitts oscillator to a cross-coupled oscillator, the start-up requirements are often higher. The Colpitts oscillator uses more DC power as a result than its cross-coupled equivalent. Cross-coupled oscillator inherently lower start-up conditions and diminishes parasitic effects, it is a better choice for low-power, high-frequency applications. However, it performs poorly in terms of noise [217]. Differential Colpitts VCO operation lowers common-mode noise in silicon circuits while improving phase noise with a Q factor boost from a symmetric inductor. By using parasitic cancellation, the tank inductor can be made larger [218]. A tunable phase shifter is used by a wideband Colpitts VCO at the input of a common collector Colpitts oscillator to adjust the frequency. A feedback capacitor and an inductor are connected in series to eliminate undesirable harmonic frequencies [219]. A voltage-to-current positive-feedback network is used in low-power Colpitts VCOs to lower the starting transconductance need and reduce DC power. This VCO design also makes use of an improved Q-factor varactor to reduce phase noise [220]. A divide-by-two circuit with a current-reused VCO produces a quadrature output frequency. Phase noise performance and power consumption are balanced by stacking the divide-by-two circuit onto a g_m-boosted Colpitts VCO with gate-to-source feedback and using parasitic capacitance neutralisation [221].

The energy transfer efficiency of the Colpitts VCO has been enhanced by the use of a transformer-coupled tank and an additional inductor in the feedback loop, leading to better phase noise sensitivity [222]. A novel quadrature VCO with low phase noise and power consumption couples two identical current-switching differential Colpitts VCO without the use of additional coupling components that might potentially increase phase noise and power consumption [223]. A dynamic body bias technique-based differential Colpitts VCO with low voltage and high swing. Enhancing switching modes and removing common-mode nodes from the transistors, this is done to provide a significant output swing and reduce phase noise. A low-voltage, high-swing bulk-coupled quadrature-VCO (QVCO) without additional coupling components can also be made using this method [224].

However, by eliminating the tail current source and adding more transconductance, the usage of a Cascode configuration in a Colpitts VCO improves phase noise

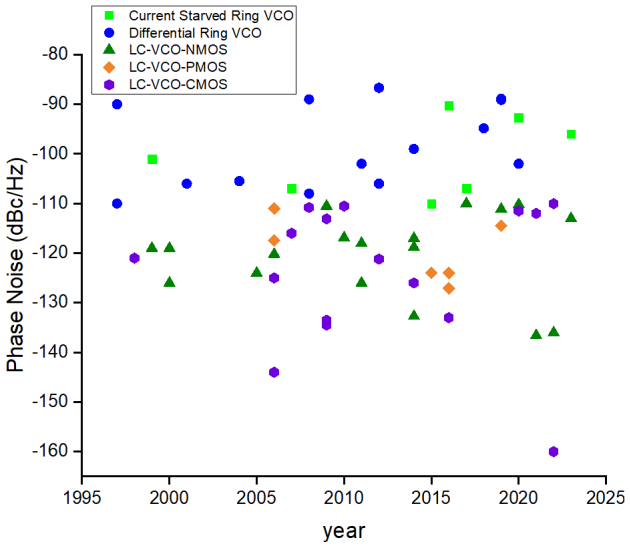

FIGURE 31. Phase noise comparative analysis of the ring VCO and LCVCO at 1MHz offset frequency.

performance while relaxing the VCO's initial oscillation condition [225]. The differential Colpitts VCO achieves a broad tuning range and low phase noise by implementing inductive emitter degeneration and resistive tail bias [226]. The VCO uses an inductor for g_m boosting at the emitter of a hetero-junction bipolar transistor to hasten oscillation starting. Additionally, by lowering the transformer ratio and improving phase noise, a Collector-Emitter cross-coupling capacitor is used to increase the loaded quality factor and oscillation amplitude [227]. The VCO ensures a reliable oscillation startup by using collector-emitter cross-coupled capacitors in a Colpitts structure. Phase noise is improved through a noise-shifting method that raises the loaded Q-factor of the tank. Furthermore, three-bit switches, utilising enhancement-mode high-electron mobility transistors (E-HEMTs), improve the tuning range and reconfigurability of this VCO [228].

IV. LITERATURE RESULT ANALYSIS

The researchers identified through the literature survey that phase noise, maximum operating frequency, FOM, and Frequency Tuning Range (FTR) are the most predominant parameters of the ring VCOs and LC-VCOs.

A. PHASE NOISE ANALYSIS OF THE REPORTED VCOs

Phase noise can be expressed as the proportion of noise within a 1-Hz bandwidth at a given frequency offset (fm), relative to the amplitude of the oscillator signal at the frequency (fo). Fig. 31 depicts a comparison between the phase noise of the ring VCO and the LC-VCO, as stated in the reported work. As a consequence of the literature survey, the phase noise of the Ring VCOs varied between −86.13 dBc/Hz and −110 dBc/Hz, and for the LC-VCO is between −110.5 to −136.57 dBc/Hz. Therefore, it is concluded that to have a better phase noise, LC-VCO would be the better option

TABLE 3. Comparative analysis of the ring VCO and LC-VCO with its performance parameters.

REF NO	Year	Technology	vco Type	Power Supply (V)	Power Consumption (mW)	Phase Noise (dBc/Hz)	Offset Frequency	FOM (dBc/Hz)	Frequency (GHz)	Tuning Range (%)
6	2015	180nm	Current Starved	1.8	6.76	-126	1 MHz	-184.54	2.2	97.00
22	2018	65nm	Current Starved	1	4.6	-121	1 MHz	-183	3	-
29	2021	90nm	Current Starved	1.2	0.000812	-115	1 MHz	-174.5	1	87
51	2022	180nm	Current Starved	1.8	1.4	-127.29	1 MHz	-181.45	4.28	1.76
82	2022	90nm	Current Starved	1.2	1.6	-90.26	1 MHz	-155.8	2.4	96.26
17	2020	180nm	Differential	1.8	17.4	-102	1 MHz	-165	1.9	-
37	2014	180nm	Differential	1.8	7.3	-99	1 MHz	-154.5	2	-
58	1999	60nm	Differential	3	10	-117	600KHz	-173	1.2	50.00
77	2022	0.18m	Differential	1.8	8.1	-86.7	1 MHz	-149.7	5.4	34.00
85	2018	65n	Differential	0.6	45	-94.84	1 MHz	-162.1	0.49	25.20
89	2019	90nm	Differential	1	-	-89.13	1 MHz	-153.35	2.45	150.50
9	2021	65nm	LC-NMOS	1.2	-	-136.57	10 MHz	-188.25	14	26.00
25	2019	65nm	LC-NMOS	1.2	11.2	-116.3	10 MHz	-183.5	62.25	26.20
27	2021	60nm	LC-NMOS	0.9	1.2	-110.6	10 MHz	-171.4	90.4	3.30
27	2021	60nm	LC-NMOS	0.9	1.08	-106.4	10 MHz	-178.2	86.5	11.00
35	2016	65nm	LC-NMOS	1.2	8.8	-112	10 MHz	-180.4	70.2	22.30
105	2022	65nm	LC-NMOS	1.2	7.7	-115.35	1 MHz	-183	7.4	29.9
111	2006	180nm	LC-NMOS	1.8	4	-120	3 MHz	-175.5	4.8	15.7
117	2014	65nm	LC-NMOS	1.2	6	-117	10 MHz	-191.7	27.5	43.3
118	2014	130nm	LC-NMOS	1.2	5.6	-118.8	1 MHz	-176	5.24	8.9
119	2014	130nm	LC-NMOS	1.2	2.2	-132	1 MHz	-201	5.72	37.68
121	2020	180nm	LC-NMOS	1.8	0.9	-111	1 MHz	-185	4.8	10.99
146	2011	65nm	LC-NMOS	1.5	14.3	-108.4	10 MHz	-174.5	76.5	15.80
163	2020	22nm	LC-NMOS	0.8	21.4	-99	10 MHz	-176.2	133	6.54
163	2021	22nm	LC-NMOS	0.8	17.1	-101	10 MHz	-176.53	129	5.40
136	2005	350nm	LC-PMOS	2.7	13.5	-117	1 MHz	-180	5.6	19.36
137	2006	180nm	LC-PMOS	1.8	32	-111	1 MHz	-182	20	-
138	2015	180nm	LC-PMOS	0.5	-	-117.4	1 MHz	-181	2.25	22.13
140	2016	350nm	LC-PMOS	3.3	79	-124	600KHz	-170	1.55	8.05
141	2019	28nm	LC-PMOS	0.9	9	-114.5	1MHz	-188	15.8	25.00
144	2016	180nm	LC-PMOS	1.8	3.33	-127.1	1MHz	-194.7	7.02	10.00
70	2010	65nm	LC-CMOS	2.1	18.5	-110.5	100KHz	-182.7	3.37	19.10
143	2006	180nm	LC-CMOS	1.8	16	-125	600KHz	-176	1.8	22.22
147	1997	500nm	LC-CMOS	2	0.5	-95	100KHz	-179.08	1.6	8.70
148	2006	350nm	LC-CMOS	2.5	-	-144	3 MHz	-191.5	2.3	17.02
149	2007	180nm	LC-CMOS	1.8	3.17	-116	1 MHz	-183.1	5.3	-
150	2007	90nm	LC-CMOS	1.6	14	-115.2	3 MHz	-172	5.63	45.00
151	2008	180nm	LC-CMOS	1.8	4.5	-110.8	1 MHz	-183	12	-
153	2009	130nm	LC-CMOS	1.2	6.24	-113.08	1 MHz	-191.49	20.78	4.80
154	2014	180nm	LC-CMOS	3.3	2.5	-130	1 MHz	-192.12	2.02	40.00
155	2009	180nm	LC-CMOS	1.8	20	-134.5	1 MHz	-185	2.2	17.00
156	2012	130nm	LC-CMOS	2.8	25	-121.2	1 MHz	-181.7	5.3	55.00
158	2014	65nm	LC-CMOS	1	5.6	-137	3 MHz	-201	3.56	8.00
159	2016	65nm	LC-CMOS	2	10	-133	1 MHz	-141.6	5.71	22.40
161	2022	65nm	LC-CMOS	1	11.1	-110.03	1 MHz	-189.3	28.66	15.20

as compared to Ring-based VCO circuits [19]. Fig. 32 shows the comparison between the phase noises reported by Class-B to Class-F and Colpitts oscillators in harmony with the reported work and the results. Therefore, researchers summarize the evidence that the colpitts oscillator brings superior PN [185] upto −140 dBc/Hz, class-C [183] and Class-D [183]: similarly Class- C up to -135 and others can provide moderate phase noise.

B. OPERATING FREQUENCY ANALYSIS OF THE REPORTED VCOS

A VCO's maximum operational frequency is the highest frequency, where it can consistently and accurately produce an output signal. Fig.33 demonstrates the maximum operating frequency ranges of ring-based VCO, Fig. 34 represents the maximum operating frequency ranges of LC-based VCO, Fig. 35 shows the comparison between the maximum operating frequency ranges of Ring- based VCO as well as LC-based VCO and Fig. 36 indicates the maximum operating frequency ranges of Class-B to class-F LC-VCO and Colpitts LC-VCO respectively. Consequently, it is identified from the literature survey that the ring based VCO can opt for radio frequency ranges from 0.4 GHz to 4.3 GHz. Similarly, the LC-VCO can be selected for both radio frequency as well as millimeter wave range frequencies ranging from 1.5 GHz to 105.2 GHz

TABLE 4. Comparative analysis of the Class-B, Class-C, Class-D, Class-E, Class-F and colpitts LC-VCO with its performance parameters.

Ref No	Year	Technology	VCO Type	Power Supply (V)	Power Consumption (mw)	Frequency (GHz)	Phase Noise (dBc/Hz)	offset Frequency	FOM (dBc/Hz)	FTR (%)
178	2012	130nm	Class-B	1	1.3	10	-110	1MHz	-183	-
187	2014	65nm	Class-B	0.5	0.0033	2.93	-121.6	1MHz	-194.4	35.5
189	2014	180nm	Class-AB/ Class-B	0.75	2.4	13.15	-101.4	1MHz	-180	25.63
188	2014	65nm	Class-B	1.2	3.6	6.2	-119.2	1MHz	-188.7	16.1
190	2016	65nm	Class-B	1.2	4.5	3.6	-159	20MHz	-197.2	21.8
191	2018	40nm	Class-B	1.8	20	40.8	-93.5	1MHz	-198	24.8
192	2022	22nm	Class-B	1	14.4	23.8	-96.6	1MHz	-178.3	5
179	2011	65nm	Class-C	1.2	11	7.2	-126	1MHz	-191	33
193	2020	130nm	Class-C	1	0.35	3.07	-119.3	1MHz	-192	28.2
194	2015	65nm	Class-C	1.2	2.2	11.2	-107.73	1MHz	-185	9.6
195	2015	90nm	Class-B/ Class-C	0.7	12	42.5	-101.8	1MHz	-185	13.8
196	2016	65nm	Class-C	1.2	5	2.46	-132.41	1MHz	-192.45	2.79
197	2019	180nm	Class-C	1.2	1.73	2.45	-120	1MHz	-185.4	28.6
198	2020	GaAs	Class-C	5	47.5	2.8	-138.6	1MHz	-191.2	5.63
180	2022	130nm	Class-B/ Class-C	1.4	3.08	18.1	-119.9	1MHz	-193.4	25.5
181	2013	65nm	Class-D	3.2	5	3.3	-144	5MHz	-190	27
200	2013	65nm	Class-D	0.4	10	4.8	-143.5	10MHz	-191	46
201	2015	65nm	Class-D	0.35	2.1	5	-137.1	3MHz	-198.3	5
202	2018	65nm	Class-D	0.8	48	60.83	-132.4	1MHz	-148.6	13
203	2020	65nm	Class-D	0.55	0.55	0.96	-108.7	1MHz	-171	27.35
204	2023	28nm	Class-D	0.56	0.054	7.13	-93.77	1MHZ	-189.6	14.18
204	2023	28nm	Class-D	0.58	0.67	9.38	-98.58	1MHz	-186.97	18.14
206	2022	180nm	Class-E	0.7	4.9	4	-115.3	100KHz	-187.6	10.6
183	2013	65nm	Class-F	1.25	12	7.6	-136	3MHz	-192	34.07
208	2015	65nm	Class-F	1.3	38	8.7	-139	3MHZ	-191	19
209	2021	40nm	Class-F	1.1	13.23	12	-120.2	1MHz	-190.5	7.3
210	2022	65nm	Class-F	1	16	34.51	-108.6	1MHz	-191.3	20.5
210	2023	65nm	Class-F	1	32	34.56	-111.8	1MHz	-191.1	20.4
184	2023	40nm	Class-F	1.2	9.8	9.48	-131	1MHz	-185	25
211	2022	65nm	Class-F	1	7	21.6	-112.2	1MHz	-196.2	25
214	2006	180nm	Colpitts	1.8	12.6	16.5	-115	1MHz	-188.4	6
215	2007	GaAs	Colpitts	5	12.5	1.52	-128.08	100KHz	-194.7	-
186	2008	180nm	Colpitts	1.8	27	29.9	-110	1MHz	-185	0.6
216	2009	180nm	Colpitts	1.8	6.4	5.46	-100.3	100KHz	-187	10.6
218	2009	350nm	Colpitts	2.8	16.8	30.4	-97.5	1MHz	-174.7	4.5
220	2011	180nm	Colpitts	1.35	3.3	18.95	-110.82	1MHz	-191.2	3.58
221	2011	180nm	Colpitts	1.8	4	2.45	-126	1MHz	-188	7
222	2012	250nm	Colpitts	1.2	48	13.08	-101	100KHz	-183	6
223	2013	180nm	Colpitts	1.8	8	5.35	-128.7	1MHz	-194.2	18
225	2013	180nm	Colpitts	1.5	13.2	25	-103.1	1MHz	-180	2.4
224	2017	180nm	Colpitts	0.6	4.71	3.76	-127.66	1MHz	-192.4	17
226	2018	130nm	Colpitts	3.3	99	27.6	-109.1	1MHz	-182.8	17.3
227	2020	90nm	Colpitts	5	45	3.55	-130.77	1MHz	-185	5
227	2021	90nm	Colpitts	5	45	3.4	-137.44	1MHz	-192	4.5
228	2020	20nm	Colpitts	5	9	3.27	-139.46	1MHz	-192.26	21
229	2018	65nm	Colpitts	1	4.3	27.8	-115.7	10MHz	-178.3	34.5

C. FOM ANALYSIS OF THE REPORTED VCOs

The FOM is a numerical expression representing the efficiency of a given system. The FOM can be calculated as SSB noise at the offset Δf from its carrier frequency with the log of the ratio of the different carrier frequencies to its offsets frequencies, which is normalized with the square, and it's multiplied with the VCO core power dissipation [98], [131], [165], [166], [167]. Fig. 37,

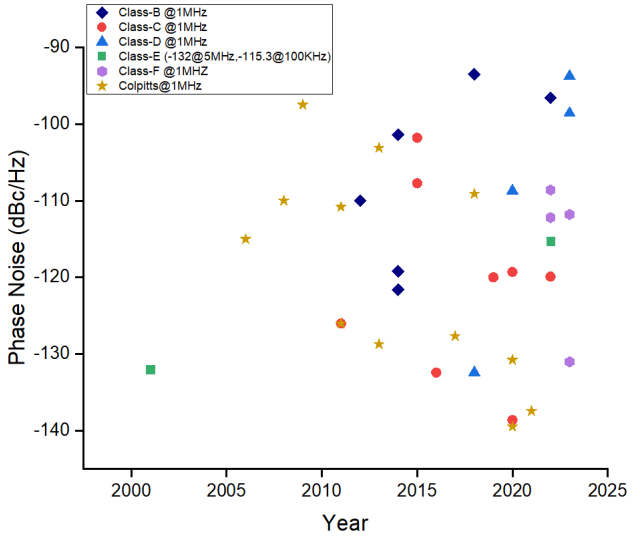

FIGURE 32. Phase noise comparative analysis of the Class-B, Class-C, CLass-D,Class-E, Class-F LCVCO and colpitts LCVCO.

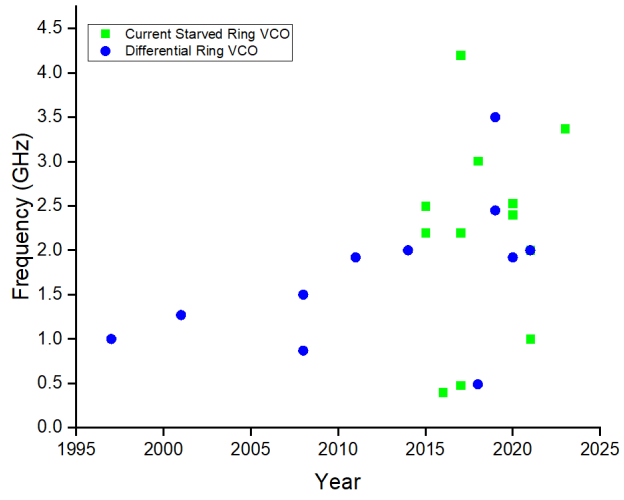

FIGURE 33. Operating frequency analysis of the ring VCO.

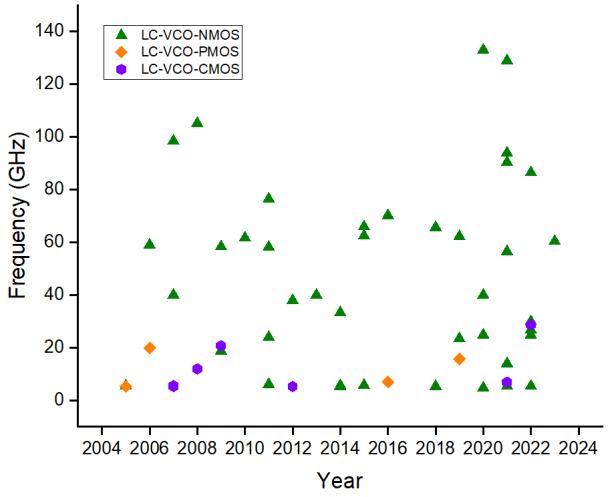

FIGURE 34. Operating frequency analysis of the LC-VCO.

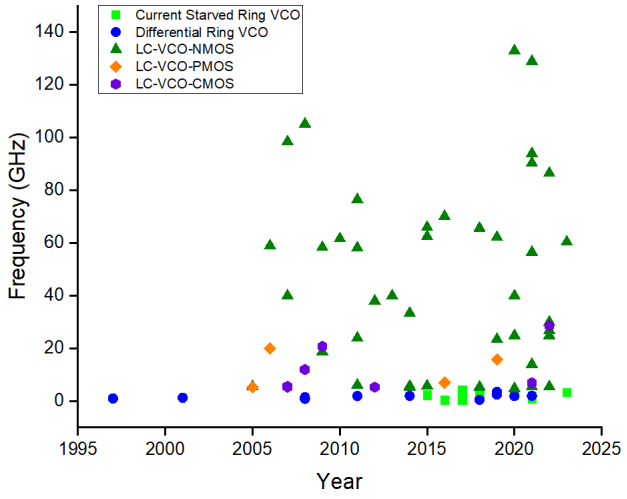

FIGURE 35. Operating frequency comparative analysis of the ring and LC-VCO.

Fig. 38, Fig. 39, Fig. 40 shows the FOM of all the surveyed VCOs.

The FoM can be calculated as per the equation given in (16) [29].

$$FOM = \$(f_o, \Delta f) + 10log\left[\left(\frac{\Delta f}{f_0}\right)^2 * \left(\frac{P_{supply}}{mW}\right)\right] \quad (16)$$

where $\$(f_o, \Delta f)$ is the phase noise at Δf offset frequency from the carrier f_o. FOM formulae has been used to assess the efficiency of VCO. With a greater negative value or a larger absolute value of the FOM, the performance of the VCO is better [167]. According to the FOM observations of the VCOs, the LC-VCO can deliver better phase noise and a higher operating frequency when compared to the ring VCO, which is adequate for high-frequency mm-wave range applications.

D. FTR ANALYSIS OF THE REPORTED VCOS

Fig. 41, Fig. 42 depict the FTR of reported VCOs. The frequency tuning range percentage is stated as the ratio of the variability between the maximum and minimum frequencies to the center frequency(fo) and delivered as a percentage (118). The formula is used to calculate the FTR in terms of percentage for a VCO is given in the equation (17):

$$FTR\ (\%) = \frac{(f_{max} - f_{min})}{f_o} \times 100 \quad (17)$$

where f_{max} is the maximum frequency that the VCO can produce, and f_{min} denotes the minimum frequency that the VCO can generate. It is observed from Fig. 41, Fig. 42, and Table 3, Table 4 that, FTR of the Ring based VCO suggestively offers a wider frequency tuning range than LC-VCO. Table 3, and Table 4 demonstrate the comparative analysis of the Ring VCO and LC-VCO with their performance parameters, Table 4 shows the comparative analysis of the Class B to F and

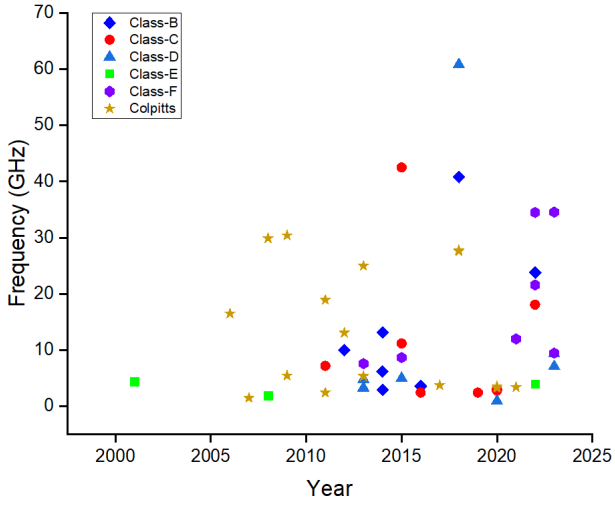

FIGURE 36. Operating frequency comparative analysis of the Class-B, Class-C, CLass-D,Class-E, Class-F LCVCO and Colpitts LCVCO.

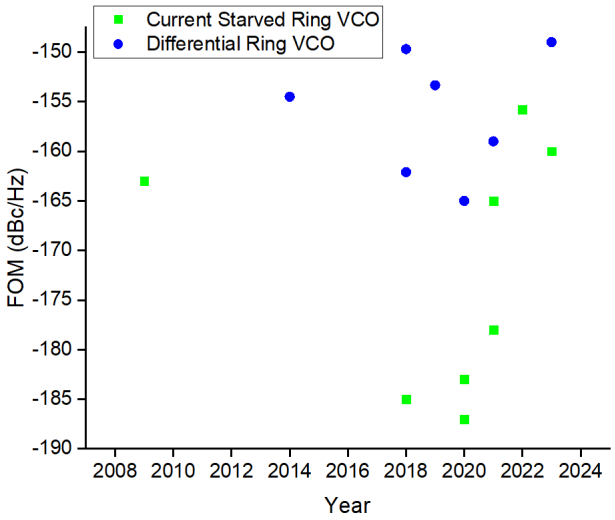

FIGURE 37. FOM analysis of the ring VCO at 1MHz offset frequency.

Colpitts oscillator with their performance parameters. The following advancement has been observed by the researchers from the Ring VCO and LC-VCOs Survey. It is determined that each VCO type has different features and is suitable for distinctive applications. The designers used to select disparate VCOs, necessitating the application requirements like frequency range, power consumption, phase noise, and integration complexity. Furthermore, the decision is also influenced by the particular characteristics of the technology process and the performance metrics sought for the intended application.

1. Future designs may concentrate on attaining wideband and multi-band operation to meet the requirements of contemporary communication systems that facilitate multiple frequency bands and standards.

2. This kind of VCOs may be integrated into compact form factor, and innovative packaging techniques can be explored for improved integration within complex electronic systems.

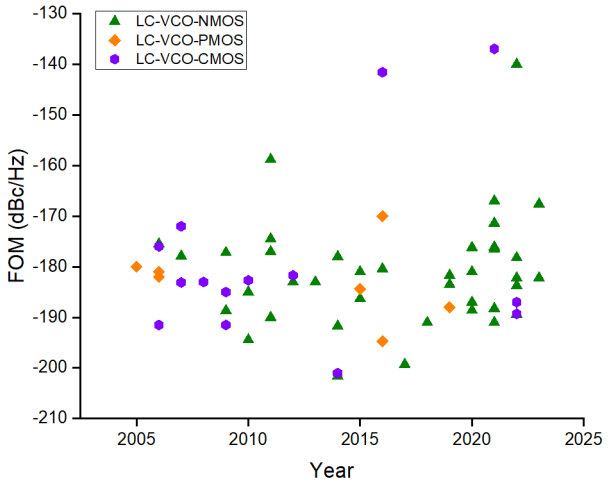

FIGURE 38. FOM analysis of the LC-VCO at 1MHz offset frequency.

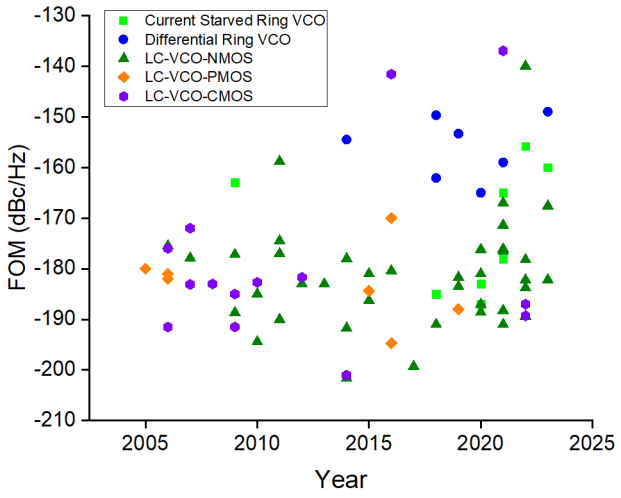

FIGURE 39. FOM comparative analysis of the ring and LC-VCO at 1MHz offset frequency.

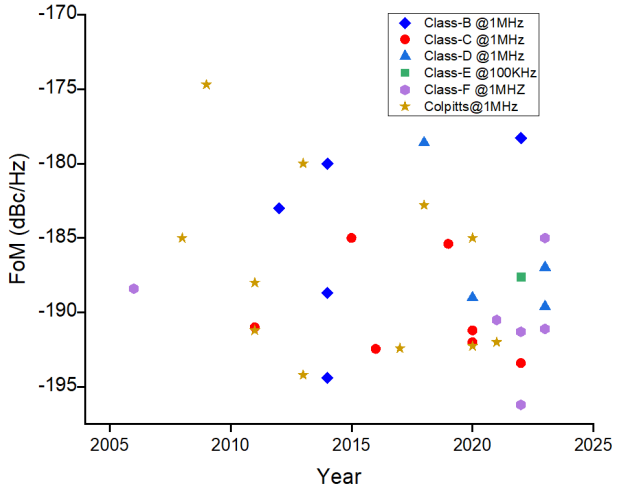

FIGURE 40. FOM comparative analysis of the Class-B, Class-C, CLass-D,Class-E, Class-F LC-VCO and colpitts LC-VCO.

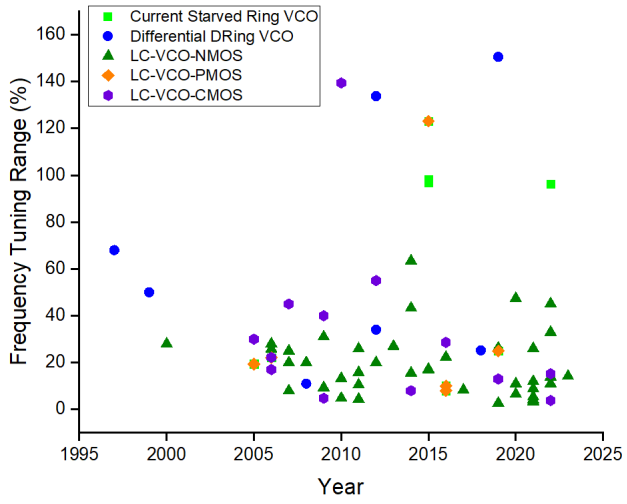

FIGURE 41. Frequency tuning range comparative analysis of the ring VCO and LCVCO.

FIGURE 42. Frequency tuning range comparative analysis of the Class-B, Class-C, CLass-D,Class-E, Class-F LCVCO and Colpitts LCVCO.

3. Exploring new materials and advanced semi- conductor technologies (e.g., FinFET, GaN) are used to improve the VCOs' performance, power efficiency, and frequency range.

4. To meet the demands of high-performance communication systems, continuous efforts must be made to design VCOs with lower power consumption and phase Noise.

5. Achieving precise frequency tuning, modulation, and dig- ital communication interfaces by incorporating digital and mixed-signal control techniques.

6. Designing and optimizing the above-mentioned VCOs for specific applications, specifically 5G, IoT, radar, and space communication.

V. CONCLUSION

This survey has provided a comprehensive analysis on comparison between the Ring and LC-VCOs architectures. Furthermore, both VCO designs propose unique advantages and trade-offs, making them suitable for different applications. Moreover, the Ring VCO has the advantage of a simpler design in its circuit implementation, and it is suitable for low-power and low-frequency applications. Therefore, the LC-VCO imparts an extraordinary phase noise performance and higher output frequency at the cost of a low tuning range. Also, LC-VCO generally requires more complex circuitry and may suffer FOM large chip area and fabrication costs also high. According to the study, using an LC-VCO, one could acquire a millimeter wave range frequency. Therefore, future research directions may concentrate on implementing high-tuning range LC-VCOs for reducing the complexity of the circuits, area, and power consumption.

DECLARATION

COMPETING INTERESTS

The authors declare no competing interests.

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