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RESEARCH ARTICLE

Extended Dynamic-Range and High-Efficiency Rectifier Based on Adaptive Power Distribution and Synthesized Low-Pass Matching Network

DANG-AN NGUYEN, (Graduate Student Member, IEEE), GIA THANG BUI, (Graduate Student Member, IEEE), HYUNGSEOK NAM, (Graduate Student Member, IEEE), AND CHULHUN SEO, (Senior Member, IEEE)
Department of Information and Communication Convergence, Soongsil University, Seoul 06978, South Korea
Corresponding author: Chulhun Seo (chulhun@ssu.ac.kr)

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ABSTRACT This paper presents a novel methodology for designing a rectifier with high efficiency and wide dynamic range (DR). Specifically, the proposed structure employs a combination of two diodes which are optimized for operation at distinct power levels. These diodes are switched automatically according to input power level during rectifying process based on a simple adaptive power distribution (APD) mechanism, which is intimately related to the diode's input impedance and is mathematically analyzed, for DR extension. In addition, a low-pass two-stage matching network is implemented instead of the conventional matching network for simultaneous fundamental matching and multi-harmonic suppression, enabling an efficient power recycling operation which, as a result, further enhances power conversion efficiency (PCE). A rectifier using two types of the Schottky diode (HSMS2850&HSMS2860) is designed, simulated and measured at 915 MHz for verification. The measured results shows peak PCE of 75.5% at an input power of 9.5 dBm and an enhanced DR of 21.5 dB for PCE> 50% while having a compact size, indicating a superior performance, as compared to other designs.

INDEX TERMS Adaptive power distribution, harmonic suppression, low-pass matching networks, power recycling, wide dynamic-range rectifiers.

I. INTRODUCTION

Wireless power transfer (WPT) and energy harvesting (EH) have been emerging as a promising technology for remotely charging electronic devices where wired methods are inconvenient or difficult to be deployed [1]. Fig.1 shows the architecture of a WPT or EH system, including commonly implemented components of the RF front-end. Specifically, the power from ambient sources such as 4G, 5G, Wifi, Satellite, et. al, or dedicated RF power sources operating at the Industrial, Science, and Medical (ISM) bands are received through an antenna and then transformed to dc power by rectifiers which can be used for energizing battery/energy storage, resistor-equivalent circuits, indicators, and low-power consumption internet-of-things (IoT) devices such as sensors, implant medical devices. Rectifiers are the only component in the power chain which is capable of converting RF power to dc power. The rectifying power conversion efficiency (PCE) is one of the important performance matrices which mostly decides the total efficiency of the WPT or EH systems and must be as high as possible [2], [3], [4]. In addition, dynamic range (DR), which represents an efficient input power range that the rectifier can operate in a specific PCE condition, i.e., typically PCE> 50%, is also a crucial aspect in the rectifier design for optimal operation due to fluctuation of the input power level. For instance,

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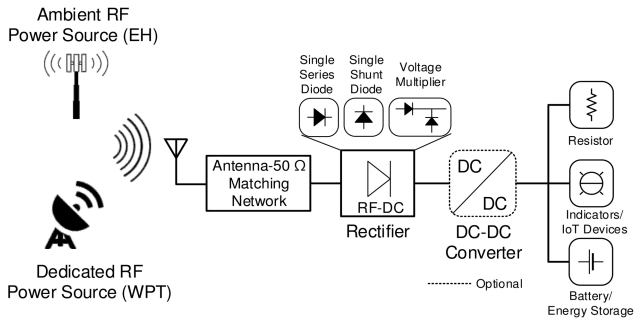

FIGURE 1. Architecture of WPT and EH systems, showing the power sources, types of load and rectifier.

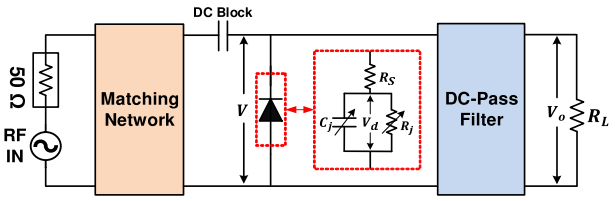

FIGURE 2. Conventional rectifier structure and its equivalent circuit model.

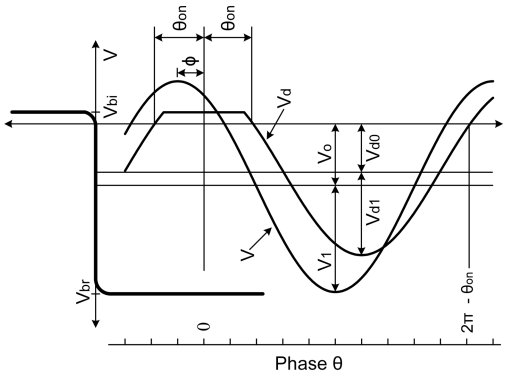

FIGURE 3. Idealized voltage waveforms of the diode and the diode junction.

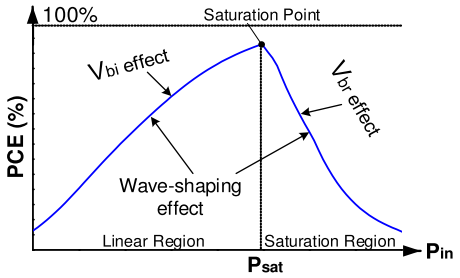

FIGURE 4. Typical PCE curve with main effects at each power region.

in near-field WPT systems, the unstable coupling factor between the transmitter and receiver strongly influences to the received power [5]. In far-field WPT or EH systems, signal attenuation is highly depended on the day time and location, leading to variation of the available signal power at the rectifier input [6]. Besides, compactness is also considered as a priority for easy integration. In general, high PCE, wide DR and compactness are always expected in the rectifier designs.

The rectifier PCE is mainly restricted by the diode loss, the impedance mismatch loss, and the insertion loss of the implemented components. The two latter losses can be minimized by utilizing advanced matching techniques or low-loss components (high quality-factor elements or low-loss substrates), respectively. Meanwhile, the diode loss dominates among all the losses; and depends on the diode characteristic such as the threshold (built-in) and breakdown voltages. Therefore, a low threshold-voltage and high breakdown-voltage diode is often preferred for realizing high-PCE rectifiers [7], [8]. In practical, the diode's non-linearity behavior produces harmonics which reshape the diode-across current and voltage waveforms, resulting in more PCE degradation at the fundamental frequency. This phenomenon is referred as the wave-shaping effect of the rectifier [7]. The loss due to the wave-shaping effect can be minimized with the harmonics-tuned techniques such as class-C [9], [10], class-F [7], [11], inverse class-F [12], [13] or power-recycling [14], [15] techniques. All these techniques enforce the harmonics with the infinite or zero impedance so that the harmonic power is diminished or recycled for more rectification at the fundamental one. Specifically, a class-C microwave rectifier with short-circuit second- and third-harmonic termination was presented in [9] and an improved version was designed in [10]. Both two cases demonstrates a high peak PCE of 72.8% and 82.5%, respectively. Class-F rectifiers had been analyzed and designed in [7] where second and third harmonics are manipulated with short- and open-circuit impedance, respectively. Following the same principle, authors in [11] had extended the class-F harmonic termination beyond the third order to obtain a PCE gain with a recorded peak of 82.2%. In [12] and [13], by enforcing the second harmonic with the infinite impedance, and the third harmonic with the zero impedance, the authors had provided the efficient inverse class-F rectifiers on implementation of transmission lines and lumped elements, respectively. Based on the power-recycling mechanism in rectification process, a design concept with open-circuit harmonics termination had been introduced in [14] and [15], showing a peak PCE of over 80% at 2.45 GHz.

Although the harmonic-tuned techniques can improve PCE over the input power range which, as a result, also leads to DR enhancement, the high PCE gain is mostly achieved at the peak PCE-around region and the DR limitation due to the diode characteristic, in essence, is not solved. Thus, DR gain, i.e, DR is commonly considered as the PCE$>$ 50% input power range, is negligible and is still limited by the diode's inherent built-in and breakdown voltages. Several efforts have been made to improve DR of a rectifier. For example, in [16], [17], and [18], the authors proposed adaptive reconfigurable rectifier topologies which use transistor-based RF switches to alter the RF signal path according to the input power. The higher breakdown voltage of the transistor remains the increase of PCE at higher input power level, yielding a wider DR. However, the nonidealities of the switches

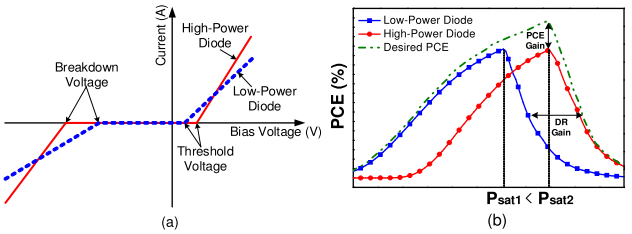

FIGURE 5. a) Typical I-V curves of the low-power and high-power diodes and b) corresponding PCE performance.

in terms of conduction loss and threshold voltage at high frequencies leads to performance degradation. Moreover, the non-linear input impedance of transistors makes input matching difficult within a wide input power range, and then the mismatch loss is not minimized. As another approach, the authors in [19] and [20] employed multiple rectifier branches with identical diodes according to operation of resistance compression networks (RCNs) in order to reduce the input impedance variation for minimizing mismatch loss caused by the non-linearity of the devices. Nevertheless, with such an deployment, the dependence of PCE on input power is not addressed. Another method is proposed in [21] and [22] where an adaptive power distribution (APD) mechanism is embedded to a rectifier array using different-type diodes. In this work, matching networks are designed so that input conduction variation of each rectifier branch is automatically adjusted to deliver power to each rectifier path assigned according to input power level. Although this approach is efficient to some certain extent in the DR improvement, the implemented structure lacks a harmonic-tuned mechanism for high peak PCE achievement and is complicated leading to high insertion loss as well as bulky circuit. In [23], the authors introduced a dual power band rectifier accompanied by a frequency switching mechanism. However, this implementation is inefficient in case of available single-frequency signal and the DR limitation still exists.

Herein, a novel methodology based on passive elements is presented for designing a high-PCE and wide DR rectifier. The proposed structure employs multi-diode configuration with a simple APD mechanism and a low-order ($n = 4$) low-pass circuit topology for both fundamental and harmonic matchings. The multi-diode configuration consists of two diodes operating optimally at different power regions and their input impedance is properly manipulated by only a transmission line so that the increasing proportion of the RF input power is automatically distributed to the high-power diode with the increase of input power, and vice versa for broadening the operating DR. The APD principle is mathematically analyzed and demonstrated by simulation. In addition, the low-pass circuit is synthesized step-by-step based on lumped elements. Optimal fundamental matching and high-level multi-harmonic suppression are provided at the operating frequency, which enables an efficient power recycling behavior resulting in high PCE, especially at the saturation point. With this design concept, a prototype rectifier is tested using two packaged Schottky diodes (HSMS2850&HSMS2860) showing a state-of-the-art performance in terms of peak PCE, dynamic range for PCE > 50%, and electrical size as compared to the recently published results.

II. RECTIFIER OPERATION AND DESIGN APPROACH

A. OVERVIEW OF THE CLASSIC SHUNT-DIODE RECTIFIER

The operation structure of the conventional shunt-diode rectifiers is shown in Fig. 2, which mainly consists of a diode, a load resistor R_L, a dc-pass filter and a matching network. The equivalent circuit of the diode has a series resistor R_S, a non-linear junction resistance R_j which can be described by the diode dc I-V curve, and a non-linear junction capacitance C_j. During a signal cycle, R_j is assumed to be zero in forward bias and infinite otherwise. With assumption of either infinite or zero harmonics impedance seen by the diode, idealized RF voltage waveforms (V and V_d) across the diode and the diode junction are shown in Fig. 3 where V and V_d can be expressed by following equations [3]

$$V = -V_o + V_1 \cos(\omega t), \tag{1}$$

$$V_d = \begin{cases} -V_{do} + V_{d1} cos(\omega t - \phi) & \text{OFF} \\ V_{bi} & \text{ON}, \end{cases} \tag{2}$$

where V_o is the output dc voltage across the load resistor, V_1 is the amplitude of the incident signal, V_{d0} and V_{d1} are the dc component and the amplitude of the fundamental frequency of the diode junction voltage, and V_{bi} is the built-in or threshold voltage in the diode forward bias. Also, V and V_d are in phase difference of ϕ and θ_{on} is referred as the forward-bias conduction angle of V_d as illustrated in Fig. 3 with $0 < \theta_{on} < \pi/2$. The typical PCE curve is shown in Fig. 4 where PCE is as a function of the input power level. The rectification PCE increases with the increase of the input power until reaching the saturation point. Beyond the saturation point, PCE starts to decrease. Based on the Kirchoff's voltage law, the RF-dc PCE can be predicted in two regions as follows [3], [17]

1) Linear region (before reaching the saturation point)

$$\text{PCE} = \frac{P_{dc}}{P_{in}} = \frac{V_o^2}{R_L P_{in}} = \frac{1}{1 + A + B + C}, \tag{3}$$

where

$$A = \frac{R_L}{\pi R_S} \left(1 + \frac{V_{bi}}{V_o}\right)^2 \left[\theta_{on} \left(1 + \frac{1}{2\cos^2\theta_{on}}\right) - \frac{3}{2}\tan\theta_{on}\right] \tag{4}$$

$$B = \frac{R_S R_L C_j^2 \omega^2}{2\pi} \left(1 + \frac{V_{bi}}{V_o}\right) \left(\frac{\pi - \theta_{on}}{\cos^2\theta_{on}} + \tan\theta_{on}\right) \tag{5}$$

$$C = \frac{R_L}{\pi R_S} \left(1 + \frac{V_{bi}}{V_o}\right) \frac{V_{bi}}{V_o} \left(\tan\theta_{on} - \theta_{on}\right), \tag{6}$$

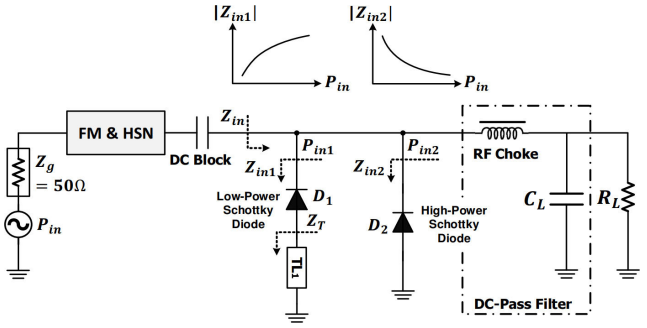

FIGURE 6. Proposed rectifier structure with APD and HS mechanisms.

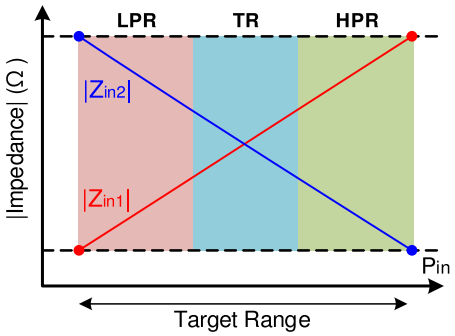

FIGURE 7. Desired variation of impedance magnitude at each diode branch versus input power.

where $\omega = 2\pi f$ is the angular frequency, and θ_{on} can be defined as

$$\tan\theta_{on} - \theta_{on} = \frac{\pi R_S}{R_L(1 + \frac{V_{bi}}{V_o})}. \tag{7}$$

2) Saturation region (after reaching the saturation point)

$$\text{PCE} = \frac{P_{dc}}{P_{in}} = \frac{V_o^2}{R_L P_{in}} = \frac{V_{br}^2}{4R_L P_{in}}, \tag{8}$$

where V_{br} is the break-down voltage of the diode. The diode's input impedance Z_D is also derived as follows

$$Z_D = \frac{\pi R_S}{(\theta_{on} - \cos\theta_{on}\sin\theta_{on}) + j\omega R_S C_j(\frac{\pi - \theta_{on}}{\cos\theta_{on}} + \sin\theta_{on})}, \tag{9}$$

It can be seen from (3)-(8) that PCE is subject to the built-in voltage V_{bi} in the linear region and the break-down voltage V_{br} in the saturation region. PCE across the overall input power range can be improved with lower V_{bi} and higher V_{br} diodes. In practical, the diodes are non-linear components and therefore harmonics are generated during the signal rectifying process, which occupy power portions leading to PCE degradation at the fundamental frequency. In other words, the present of the harmonics reshapes the diode's current and voltage waveforms with more overlap which can be referred as the wave-shaping effect. This effect influences PCE in both the linear and saturation regions, as indicated in Fig. 4.

B. DESIGN APPROACH FOR WIDE DR AND HIGH-EFFICIENCY RECTIFIER

As aforementioned, the rectifying operation can be divided into two different regions. Assuming a well-matched rectifier implemented on a low-loss substrate, the rectifying performance is mainly restricted by diode losses due to the following effects: the built-in voltage V_{bi} effect and the wave-shaping effect during the linear region; and the break-down voltage V_{br} effect and the wave-shaping effect during the saturation region.

The loss due to the wave-shaping effect can be minimized by the harmonic-tuned techniques as presented in [9], [10], [11], [12], [13], [14], and [15]. In addition, a diode with low built-in voltage and high break-down voltage should be selected to minimize the losses induced by the V_{bi} effect and the V_{br} effect; respectively. However, in practical, a diode exhibiting low built-in voltage commonly has a low break-down voltage and vice versa, which makes their optimal operating region different [16]. Specifically, low V_{bi} diodes known as low-power diodes have lower optimal input power region than high-power diodes with high V_{bi}. The I-V curves of these different diode types and the corresponding PCE graphs are illustrated in Fig. 5. As an efficient approach, if there is a rectifier structure that can automatically switch the rectification between the low-power and high-power diodes at low and high input power levels, respectively, together with an optimal wave-shaping mechanism, a wide-DR and high-PCE rectifier can be realized. As a result, it is required to deploy a proper power distribution and an accurate harmonic termination in the implemented structure. In this paper, a simple APD scheme without any external circuits and a multi-harmonic suppression (infinite harmonic impedance) mechanism for power recycling are implemented in the proposed topology which not only provides high performance, but a compact rectifier size. The desired PCE curve is sketched in Fig. 5b which presents two performance gains, i.e., DR gain thanks to the APD operation and PCE gain thanks to the multi-harmonic suppression.

III. PROPOSED STRUCTURE AND ANALYSIS

The proposed structure is shown in Fig. 6 which comprises two different-type Schottky diodes, i.e., a low power diode D_1 and a high power diode D_2, for the rectifying process. At the anode of D_1, a shunt transmission line TL_1 is manipulated so that a proper APD according to the input power is generated for wide DR operation. In addition, a fundamental matching and harmonic suppression network (FM&HSN) is implemented at the input side which can provide accurate fundamental matching for lossless power delivery from the source of 50Ω to the diodes and high-level harmonic suppression for loss minimization due to the wave-shaping effect. The DC-pass filter at the load side is formulated by a L-type cascade of an RF choke and a high-capacitance capacitor for blocking ac signal and flattening dc output voltage.

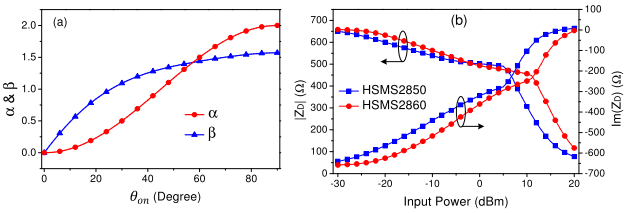

FIGURE 8. a) Variation of α and β as θ_{on} increases from 0 to $\pi/2$, and b) Simulated magnitude and imaginary parts of the diode's input impedance Z_D versus input power.

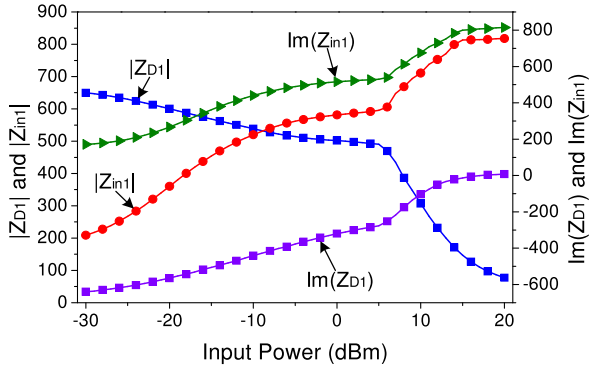

FIGURE 9. Simulated impedance respose versus input power of D_1 diode branch at 915 MHz (D_1: HSMS-2850).

A. POWER DELIVERY BASED ON APD

It is expected that most of RF power is delivered to D_1 branch at the low input power level while D_2 will process high percentage of RF power at the high input power level. Assuming well-matched fundamental impedance or $P_{in} = P_{in1} + P_{in2}$, the power ratio of P_{in1}/P_{in2} can be determined as follows [21]

$$\frac{P_{in1}}{P_{in2}} = \frac{|Z_{in2}|}{|Z_{in1}|}, \tag{10}$$

where $|A|$ denotes the magnitude of A. The power distribution is intimately linked to the impedance variation. The desired impedance magnitude versus input power can be illustrated in Fig. 7. For efficient power allocation, $|Z_{in1}|$ must exhibits positive slope according to input power while $|Z_{in2}|$ is a power-dependent decreasing function. Throughout a target input power range, the rectifying operation can be recognized in three phases:

1) Low power region (LPR): at this region, a large portion of input power is focused for the rectifying process of D_1. The D_2 branch is mostly isolated and PCE is dominated by the rectifying efficiency of D_1.
2) Transition region (TR): at this region, impedance magnitudes of each branch are not much different. Although power is quasi-equally divided into each diode path, but both two diodes contribute to the dc output power. As a result, achievable PCE can be approximated to that of the single diode D_1-based case.
3) High power region (HPR): most of power is delivered to D_2 which rectifies RF signal with higher PCE than D_1 at a high input power level. The D_1 path is ideally isolated in this region.

TABLE 1. Information on the selected diode models.

Models	$V_{br}(V)$	C_{j0}(pF)	$I_S(nA)$	$R_S(\Omega)$	$V_{bi}(V)$
HSMS-2850	3.8	0.18	3000	25	0.15
HSMS-2860	7	0.18	50	5	0.25

TABLE 2. Information on the chip components of the low-pass network.

Elements	Values	Part Numbers	Self-Resonant Frequency
L_1	15 nH	LQW18AN15NG00	6 GHz
C_1	2.2 pF	GJM0335C1H2R2BB01	$>$ 3 GHz
L_2	51 nH	LQW18AN51NG00	3 GHz
C_2	0.6 pF	GJM0335C1HR60WB01	$>$ 3 GHz

As pointed in (9), Z_D is the diode complex impedance, and θ_{on} is half of the conduction angle with $0 < \theta_{on} < \pi/2$ as presented in [3]. Moreover, as seen in (7), θ_{on} is a dynamic variable increasingly-dependent on the output power which rises with the increase of the diode's input power. Therefore, θ_{on} is also an increasing function of the diode's input power. In order to evaluate impedance variation of Z_D with input power, the admittance Y_D is defined as

$$Y_D = 1/Z_D = \mathrm{Re}(Y_D) + j\mathrm{Im}(Y_D); \tag{11}$$

where

$$\mathrm{Re}(Y_D) = \frac{\theta_{on} - \cos\theta_{on}\sin\theta_{on}}{\pi R_S} \tag{12}$$

$$\mathrm{Im}(Y_D) = \frac{\omega R_S C_j(\frac{\pi - \theta_{on}}{\cos\theta_{on}} + \sin\theta_{on})}{\pi R_S} \tag{13}$$

As seen in (13), the susceptance of the diode input admittance Y_D is positive, and hence Z_D is capacitive. Taking derivative of real and imaginary parts of Y_D with respect to θ_{on}, we have

$$\frac{d\mathrm{Re}(Y_D)}{d\theta_{on}} = \frac{1 - \cos 2\theta_{on}}{\pi R_S} \tag{14}$$

$$\frac{d\mathrm{Im}(Y_D)}{d\theta_{on}} = \frac{\omega C_j}{\pi}\frac{(\pi - \theta_{on})\sin\theta_{on} + \cos^3\theta_{on} - \cos\theta_{on}}{\cos^2\theta_{on}} \tag{15}$$

Let $\alpha = 1 - \cos 2\theta_{on}$ and $\beta = (\pi - \theta_{on})\sin\theta_{on} + \cos^3\theta_{on} - \cos\theta_{on}$, the sign of (14) and (15) is determined by the sign of α and β, respectively with condition of $0 < \theta_{on} < \pi/2$. Based on characteristic of the trigonometric functions, α and β is always positive as θ_{on} varies within the range of 0 and $\pi/2$, which can be illustrated in Fig. 8a. In other words, the real and imaginary parts of Y_D increases with θ_{on} as well as the input power. As a result, the diode's capacitive input impedance Z_D exhibits a decreasing variation in magnitude of both its real and imaginary parts which, therefore, lead to the decrease of $|Z_D|$ with the input power. For verification, two different diode models (HSMS2850 and HSMS2860) are selected and simulated at 915 MHz using the Keysight Advanced Design System (ADS). The diodes's parameters are listed in Table 1. Each diode is excited with an input power source P_{in}. Perfect matching is assumed between the source and diode at each power level. As observed in Fig. 8b, the magnitude of Z_D in both two cases is a decreasing function of input power P_{in},

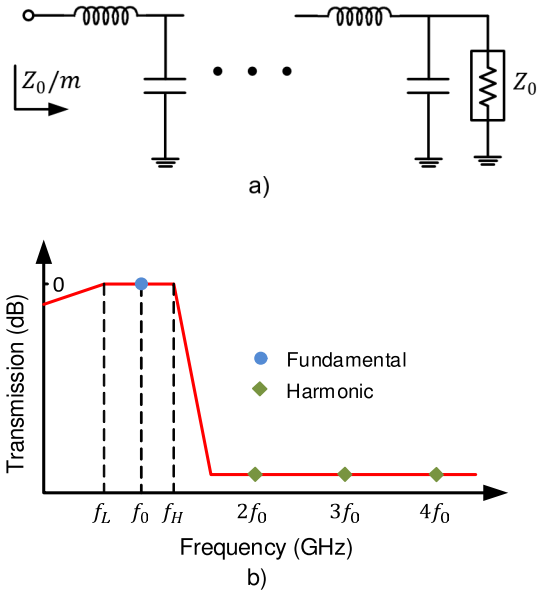

FIGURE 10. a) Generic multistage low-pass ladder network and b) typical frequency response.

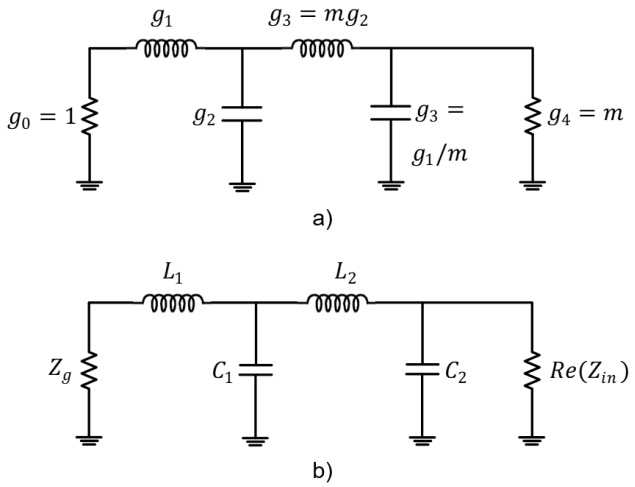

FIGURE 11. Two-stage low-pass matching network a) prototype with g elements, and b) scaled network at the 50-Ohm system and f_0 center frequency.

which confirms the variation of $|Z_D|$ as analyzed above. Also, the imaginary part of Z_D is negative and rises as the input power increases. This characteristic is utilized to formulate a simple APD mechanism in this paper.

For the desired APD operation, $|Z_{in1}|$ is required to exhibit an increasing change of impedance magnitude with input power while $|Z_{in2}|$ descends as illustrated in Fig. 7. With insertion of TL_1, Z_{in1} and Z_{in2} can be expressed based on the transmission line theory as follows

$$Z_{in1} = Z_{D1} + Z_T = Z_{D1} + jZ_1\tan\theta_1 \quad (16)$$

$$Z_{in2} = Z_{D2} \quad (17)$$

where Z_1 and θ_1 represent the characteristic impedance and electrical length of TL_1, respectively. From (16), Z_{in1} can be

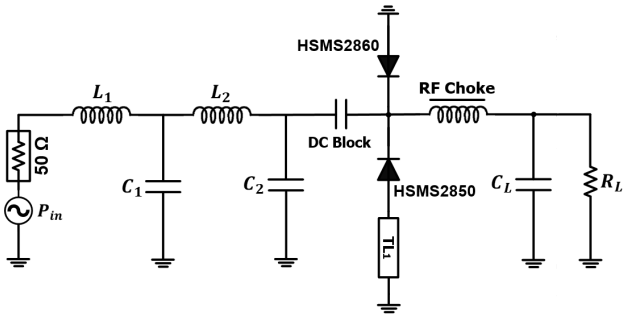

FIGURE 12. Final circuit schematic of the proposed rectifier.

decayed to real and imaginary parts as

$$Z_{in1} = \mathrm{Re}(Z_{D1}) + j\,(\mathrm{Im}(Z_{D1}) + Z_1\tan\theta_1) \quad (18)$$

Due to the power-versus decreasing response of $|\mathrm{Im}(Z_{D1})|$ as demonstrated before, by choosing properly the TL_1 parameters with $0 < \theta_1 < \pi/2$, Z_T is inductive and the imaginary part of Z_{in1}, i.e., $\mathrm{Im}(Z_{D1}) + Z_1\tan\theta_1$, can be converted into positive value with an increasing variation in magnitude during the input power range, which can compensate for the decrease of the real part $\mathrm{Re}(Z_{in1})$ and then makes $|Z_{in1}|$ increase. For example, the diode model HSMS2850 is used as D_1. With parameters of TL_1: $Z_1 = 100\Omega$ and $\theta_1 = 83^o$ at 915 MHz, the impedance response of Z_{in1} according to input power is shown in Fig. 9, in comparison with the diode impedance Z_{D1}. It can be seen that the imaginary part of Z_{in1} is inverted to positive value with a rising fluctuation in magnitude. As a result, the behavior of $|Z_{in1}|$ is a desired positive-slope function of input power which can be combined with power-dependent negative-slope characteristic of Z_{in2} to formulate an efficient ADP mechanism in the proposed rectifier.

B. FM&HS NETWORK DESIGN

Apart from a APD, the rectifier needs an efficient impedance matching to transform the impedance Z_{in}, i.e., $Z_{in} = Z_{in1}||Z_{in2}$, to the source impedance of 50Ω at the fundamental frequency for delivering power to the diodes without mismatch loss. Also, it has been demonstrated that high-level suppression at the harmonics can improve PCE to some certain extent as a result of power-recycling process in the rectification. The harmonic suppression technique is typically implemented at the diode anode side with a $\lambda/8$ transmission line [14], [15] or a LC resonator [24] for the second-harmonic suppression. However, such the deployment deteriorates the APD operation and endures a limitation on the number of terminated harmonics. Therefore, in this research, the fundamental matching network and harmonic filter are co-designed at the location as shown in Fig. 6 which can reduce circuit complexity and provide multi-harmonic destruction for more efficient PCE improvement [8].

Multi-stage low-pass matching networks have been widely utilized for designing broandband high-efficiency power

amplifiers [25], [26], broadband rectifiers [27] thanks to their capability of performing simultaneous fundamental and harmonic matchings with the pass-band and stop-band, respectively. The generic topology of a low-pass circuit is shown in Fig. 10a as a cascade of L-type LC networks, and its typical frequency response is illustrated in Fig. 10b where flat or low-ripple response can be achieved within a wide bandwidth whereas exhibiting a steep attenuation at the harmonic stop-band. It is also well known in the filter theory that higher-order low-pass matching networks lead, in general, wider bandwidth and steeper stopband attenuation [28]. For a narrow-band design, there is adequate degrees of freedom in this low-pass matching network to perform accurate multi-harmonic control and fundamental matching which, as a result, leads to a high-efficiency operation around a single frequency. In this work, two-stage ($n = 4$) low-pass network is implemented for matching Z_{in} to $Z_g = 50\Omega$ and suppressing multiple harmonics for high PCE and low design complexity. The synthesis of the low-pass matching network can be summarized in three main steps as follows

1) The first step is to determine the input impedance Z_{in} and the required fractional bandwidth which is given by

$$\omega = \frac{f_H - f_L}{f_0}, \tag{19}$$

so that achieving the transformation ratio $m = Re(Z_{in})/Z_g$ with an in-band ripple of < 0.1 dB based on only two stages. This requires the values of f_L and f_H around the center frequency f_0. All can be done by using the tabulated data presented in [29].

2) The second step is to design a m:1 real-to-real Chebyshev low-pass matching network within the determined bandwidth. In this step, a prototype of the two-stage m:1 transformer is first extracted with g-elements as shown in Fig. 11a. This prototype indicates a low-pass transformer in a normalized system with 1Ω source impedance and 1-rad/s angular frequency [28]. Then, the prototype is scaled to the desired system, as shown in Fig. 11b, with the 50Ω source impedance and operating frequency f_0 based on

$$L_k = g_{2k-1}\frac{50}{\omega_0} \tag{20}$$

$$C_k = g_{2k}\frac{1}{50\omega_0} \tag{21}$$

3) The third step is to perform a post-optimization of the real-to-real transformer in the second step, which provides a good starting point to form a real-to-complex transformer. The second termination is now set to Z_{in} and a computer-aided design (CAD) optimization is needed to obtain the desired Chebyshev response.

IV. IMPLEMENTATION, SIMULATION, AND MEASUREMENT

For verification, a rectifier implementing the proposed topology is designed at an ISM band frequency of

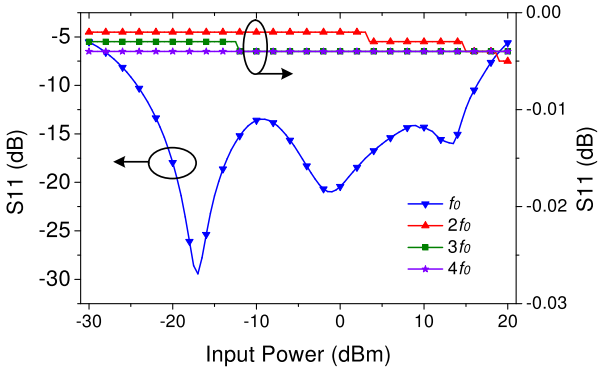

FIGURE 13. Simulated reflection coefficient of the complete circuit versus input power at fundamental and harmonic frequencies ($f_0 = 915$ MHz).

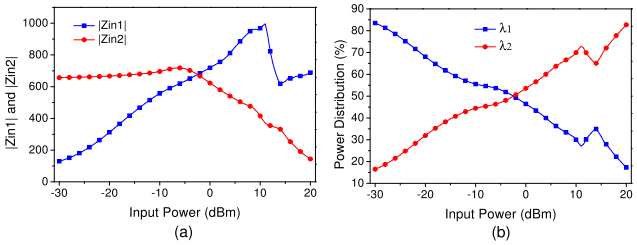

FIGURE 14. a) Simulated input impedance variation at each diode path and b) corresponding power distribution.

$f_0 = 915$ MHz. The diodes HSMS2850 and HSMS2860 whose SPICE models are provided in Table 1, are utilized for low-power diode D_1 and high-power diode D_2, respectively. The optimal parameters of TL_1 for an efficient APD operation are: $\theta_1 = 83^o$, $Z_1 = 100\Omega$. Note that this transmission line can be replaced with an inductor for more compact realization which, however, is difficult to obtain such an ideal component in case of high inductance value due to restriction in its resonant frequency. The two-stage low-pass matching network is conducted to match $Z_{in} = 483 - j151\ \Omega$ to the 50Ω source with a bandwidth from $f_L = 815$ MHz to $f_H = 1.015$ GHz. The matching impedance value Z_{in} is given at an input excitation of 8.5 dBm. The value of the lumped components are extracted based on the steps in section III-B which is listed in Table 2 together with information of their available chip model. The low-pass network is then combined with other parts to form a complete circuit as shown in Fig. 12 which is ultimately implemented on the TLY-5 substrate ($\epsilon_r = 2.2$ and $\tan\delta = 0.0009$).

For simulation, the optimal dc load is determined to be 460Ω. Due to variation of Z_{in} with input power and frequency, the reflection coefficient S_{11} versus input power is extracted first as shown in Fig. 13 in order to verify the matching capability of the low-pass network across the target input power range from -30 dBm to 20 dBm. It can be seen that S_{11} is achieved at a value of < -10 dB throughout most of the input power range at the fundamental frequency while very high S_{11} of nearly 0 dB is observed at the harmonics, which indicates a good fundamental matching and a high-level harmonic suppression as well as an efficient power recycling mechanism in the design. The impedance variation

TABLE 3. Comparison of this work with the relevant previous designs.

Year	Ref.	Freq. (GHz)	Number of diodes	Diode Model	Peak PCE (%)	Input Power (dBm)	DR for PCE> 50% (dB)	Electrical Size (λ^2)	Harmonic Cotrol	Methodology
2013	[30]	0.8	1	Schottky/ SMS3923	60	16	8	N/A	Yes	Class-E
2015	[20]	2.45	4	Schottky/ HBAT540B	70	27	10.1	N/A	No	RCN
2019	[21]	0.9	2	Schottky/ HSMS2852 &HSMS2820	60	13	18.5	0.2439	No	APD
2019	[31]	0.433	1	Schottky/ HSMS2850	64.4	5	18.9	0.000092	No	Time Domain Modeling
2021	[32]	0.5	2	Schottky/ HSMS2862	75	22	19	0.0004	No	Virtual Battery
2022	[18]	5.8	1	Schottky/ HSMS2860	73	21	11.5	0.1167	Yes	Diode-Connected MESFET
2023	[11]	2.45	1	Schottky/ HSMS2860	82.2	15	17.5	0.038	Yes	Class F
2023	[23]	0.88	2	Schottky/ HSMS2850 &HSMS2860	61.55	-8	20	0.009	No	Frequency Switching
2023	This work	0.915	2	Schottky/ HSMS2850 &HSMS2860	75.5	9.5	21.5	0.0172	Yes	APD

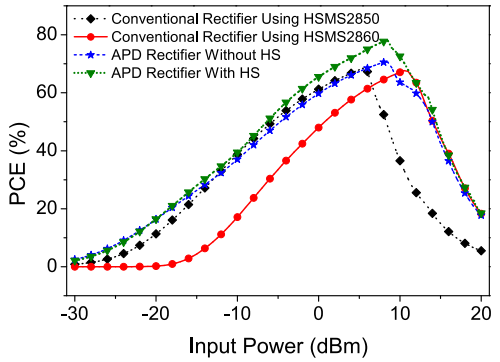

FIGURE 15. Simulated PCE performance of the proposed rectifier in comparison with conventional single diode-based ones.

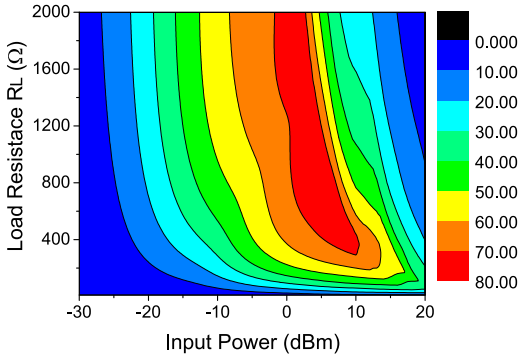

FIGURE 16. Simulated PCE contours as a function of input power and load resistance. The color bar stands for PCE (unit: %).

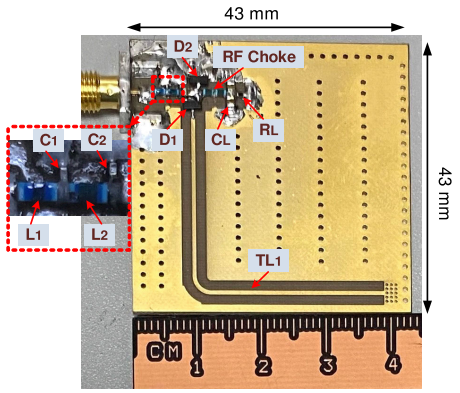

FIGURE 17. Photograph of the fabricated rectifier prototype.

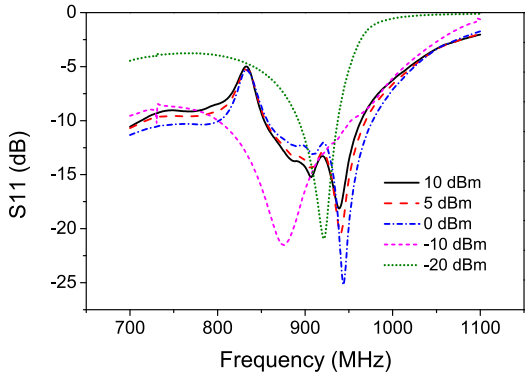

FIGURE 18. Measured reflection coefficient S_{11} at different input powers.

and power distribution during the input power range are provided in Fig. 14 where $\lambda_1 = P_{in1}/(P_{in1} + P_{in2})$ and $\lambda_2 = P_{in2}/(P_{in1} + P_{in2})$ denote the power percentage delivered for P_{in1} and P_{in2} as the input power changes, respectively. With APD operation, $|Z_{in1}|$ and $|Z_{in2}|$ change oppositely to each other as expected in the proposed design. As a result, a high portion of input power is delivered to D_1 at low values of input power and to D_2 at high input power levels. The simulated PCE is then plotted in Fig. 15. The PCE performance of the conventional single-diode rectifiers is also added for comparison. As provided, the rectifiers using HSMS-2850

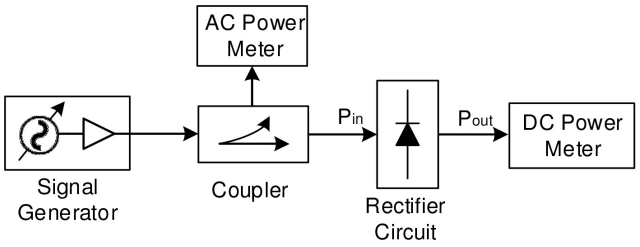

FIGURE 19. Measurement setup for testing the proposed rectifier.

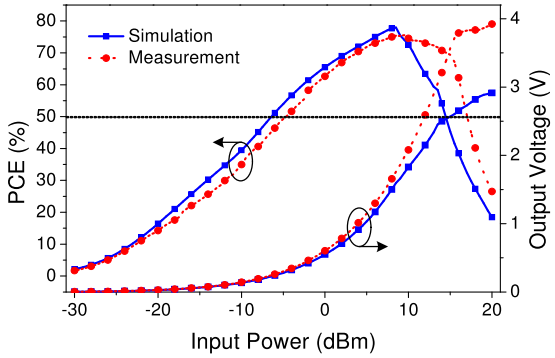

FIGURE 20. Simulated and measured performance of the proposed rectifer with implementation on TLY-5 substrate.

or HSMS-2860 yield PCE curves optimized at low and high input power regions, respectively, with similar peak PCE and DR. The effectiveness of the proposed rectifier can be seen in two cases, i.e., APD operation without harmonic suppression, namely APD rectifier without HS (HS stands for harmonic suppression); and APD operation with the low-pass Chebyshev matching network, namely APD rectifier with HS. By deploying APD, the rectifier matched by the conventional matching method without high-level harmonic suppression can operates in a wider DR for any specific value of PCE. For example, DR for PCE$>$ 50% can be extended from 13.5 dB in both the conventional single-diode rectifiers to 18.5 dB. In addition, with implementation of the low-pass Chebyshev network, PCE is further improved, especially around the saturation point. For instance, peak PCE is about 78% at 8.5 dB input power which presents a PCE gain of 7.5% as compared to the case of APD rectifier without HS. The PCE contours as a function of input power and dc load resistance is shown in Fig. 16. As observed, high PCE region (PCE$>$ 70%) is located within around 3-10 dBm input power range and $>$ 400Ω load resistance R_L.

For measurement, at the load side, two series-connected high-inductance inductors (LQW18ANR39G00) are used as a RF choke combined with two parallel-connected high-capacitance capacitors (C08BL242X-5UN-X0T) to form the dc-pass filter for flattening the output voltage. Fig. 17 provides the photograph of the proposed rectifier with a fabricated dimension of 43 $\times$ 43mm^2. The optimal load for highest PCE measurement changes slightly to 580Ω. The measured S_{11}, as shown in Fig. 18, is lower than -10 dB for all observed input power levels, which, as a result, leads to negligible mismatch loss. Fig. 19 provides measurement setup for measuring the rectifier in terms of output voltage and PCE. RF signal is generated by a signal generator and fed through a coupler to the rectifier device. Then, the output voltage is measured by a dc meter and PCE is calculated as PCE$=$ $V_o^2/(R_L P_{in})$. As shown in Fig. 20, the measured performance agrees well with the simulation one. The peak PCE is around 75.5% at an input power of 9.5 dBm. Also, the proposed rectifier exhibits a wide DR of 21.5 dB for which PCE is higher than 50%. Comparison between the proposed rectifier and the other reported works is summarized in Table 3. The proposed circuit achieves a highest DR for PCE$>$ 50% while peak PCE is higher than most of others. Especially, as compared to the design of [21] with the similar ADP operation, diode model and operating frequency, our rectifier outperforms in terms of all performance parameters.

V. CONCLUSION

The paper introduces a novel methodology for designing a compact, high PCE and wide DR rectifier with low complexity. The proposed structure contains two rectifying paths with implementation of different-type diodes which is operated by APD, fundamental matching and harmonic suppression mechanisms based on only passive components. The APD is achieved by manipulating the diodes's input impedance while a two-stage low-pass matching network is designed for simultaneously achieving fundamental matching and multi-harmonic suppression. The fabricated prototype shows significant advantages over the conventional rectifier designs in terms of high peak PCE, wide DR for PCE$>$ 50%, and compactness.

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DANG-AN NGUYEN (Graduate Student Member, IEEE) was born in Thanh Hoa, Vietnam. He received the degree from the School of Electronics and Telecommunications, Hanoi University of Science and Technology (HUST), Vietnam. He is currently pursuing the Ph.D. degree with Soongsil University, South Korea, with a focus on microwave signal processing, radar systems, power amplifiers, rectifiers, and non-Foster circuits. He has three years of experience as a Senior Member with the Signal Processing and Radio Communication Laboratory, HUST.

GIA THANG BUI (Graduate Student Member, IEEE) received the B.Sc. (Eng.) degree in electronics and telecommunication engineering from the School of Electronics and Telecommunication, Hanoi University of Science and Technology, Hanoi, Vietnam, in 2021. He is currently pursuing the M.Sc. degree with the Department of Information and Telecommunication, Soongsil University, Seoul, South Korea. His research interests include microwave wireless power transfer, microwave rectifiers, high-input power rectifiers, microwave power amplifiers, and low-noise amplifiers.

HYUNGSEOK NAM (Graduate Student Member, IEEE) was born in Seoul, South Korea, in 1993. He received the B.S. degree from the School of Electronic Engineering, Soongsil University, Seoul, in 2017. He is currently pursuing the integrated M.S. and Ph.D. degree with the Department of Information and Communication Convergence, Soongsil University. His current research interests include the design of high-efficiency and broadband/multiband power amplifiers, low-noise amplifiers, rectifiers, and electromagnetic compatibility.

CHULHUN SEO (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from Seoul National University, Seoul, South Korea, in 1983, 1985, and 1993, respectively. From 1993 to 1995, he was with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, as a Technical Staff Member. From 1993 to 1997, he was with Soongsil University, Seoul, as an Assistant Professor. From 1999 to 2001, he was a Visiting Professor with MIT. From 1997 to 2004, he was an Associate Professor with Soongsil University, where he has been a Professor in electronic engineering, since 2004. He is also the Director of the Wireless Power Transfer Research Center, Seoul, supported by the Korean Ministry of Trade, Industry, and Energy, and the Director of the Metamaterials Research Center, Seoul, supported by the Basic Research Laboratories through the NRF Grant funded by the MSIP. His research interests include wireless communication technologies, RF power amplifiers, and wireless power transfer using metamaterials. He served as the Chairperson for the IEEE MTT Korea Chapter, from 2011 to 2014.