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RESEARCH ARTICLE

# A Synchronization Shift Phase-Locked Loop Strategy for Three-Phase Grid-Tied Inverters Under Unbalanced Grid Voltage Scenarios

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**ABSTRACT** The phase-locked loop (PLL) is one of the most commonly used approaches for the inverter to achieve grid-connected operation. However, when unbalanced grid voltages occur, the double-line frequency oscillation exists in the system. With the conventional PLL method, the synchronous reference frame (SRF) voltage will be oscillated because of the double-line frequency oscillation. As a result, the electrical angle of the grid cannot be estimated accurately. Moreover, inverter output currents will be distorted and the current total harmonic distortion (iTHD) will be increased. To solve this issue, an enhanced synchronization shift phase-locked loop (SSPLL) strategy is proposed in this paper. With the proposed SSPLL, the inherent double-line frequency oscillation in the control loop can be eliminated. Therefore, the electrical angle of the grid can precisely be calculated, whereas the current THD can be suppressed. The developed SSPLL can be realized by the digital signal processor (DSP) without adding extra circuits and components. Comprehensive theoretical analysis and mathematical derivations of the SSPLL are also revealed. Eventually, both simulation and experimental results obtained from a 5kVA prototype circuit will be presented to verify the performance and feasibility of the proposed SSPLL. Compare to conventional PLL methods, a maximum 65.22% improvement of current THD and a maximum 51.2% improvement of the controller execution time can be achieved with the proposed strategy.

**INDEX TERMS** Three-phase grid-tied inverter, phase-locked loop, unbalanced grid voltages.

## I. INTRODUCTION

To achieve carbon neutral and net zero emission, renewable energy systems (RESs) have received significant attention in recent years [1], [2], whereas the energy storage systems (ESSs) are often included in the RESs [3], [4]. In order to regulate the electrical energy of the renewable energy source, the battery and the grid, power electronic technologies and grid-tied inverters play vital roles in the system [5], [6]. In addition, grid-connected power converters provide the capability of active and reactive power compensating, which can stabilize the voltage amplitude and frequency of the power grid [7], [8]. Besides, during the grid-fault occurs, the inverter with the low-voltage ride-through (LVRT) capability contributes to the recovery of the grid [9], [10]. In other words, the power system quality can be increased by the adoption of grid-tied inverters. To ensure the stable operation of the grid-tied inverter, simultaneous diagnosis methods and the voltage sag state estimation of the inverter are also necessary [11], [12], [13].

The phase-locked loop (PLL) is a commonly adopted function for the grid-tied inverter to estimate the electrical angle of the grid. With PLL, the phase-shift between the inverter output current and the grid voltage can be controlled, whereas the active and reactive power of the inverter can be regulated [14]. Generally, the synchronous reference frame phase-locked loop (SRF-PLL) is one of the most commonly used methods for the three-phase system [15], [16].

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With SRF-PLL, the three-phase ac components will be converted into two dc components, whereas the control can be simplified.

However, when the grid fault occurs, the three-phase voltage might be unbalanced. The double-line frequency oscillation exists in the system under unbalanced grid voltage scenarios. Unfortunately, the double-line frequency oscillation can also be observed in the output signals of SRF-PLL. The electrical angle of the grid will inaccurately be estimated. As a result, the output currents will be distorted and the total harmonic distortion (THD) of inverter output currents will be increased.

Some literatures focused on improving the performance of the grid-tied inverter under weak grid conditions [17], [18]. First, a passivity enhancement method to attain the positive output resistance of the grid-connected inverter (GCI) in the qq channel was proposed in [17]. Besides, GCI's complete harmonic state-space (HSS) model considering PLL under the asymmetrical network was established in [18]. With eigenvalue locus analysis, the stability boundaries of the system's critical parameters involving the current reference, current controller, and PLL controller are determined under different grid impedance asymmetrical indexes. In these two literatures, a prefilter and an impedance phase regulator were included to remove the oscillation of the PLL control loop.

In addition, the PLL-based and PLL-less control strategies were analyzed and compared in [19] and [20]. These two articles revealed that the PLL-less method falls behind in two conditions: 1) when the grid frequency offsets occur and 2) when unbalanced grid voltage faults occur. Therefore, a band-pass filter (BPF) was introduced for the PLL-less control to achieve the same performance of the PLL-based control under weak grid conditions. The conclusion is that the PLL-based approach is still a superior choice if the controller and the PLL are designed well. Therefore, the PLL-based control will be selected in this paper.

On the other hand, the dual second-order generalized integrator phase-locked loop (DSOGI-PLL) was proposed to suppress the double-line frequency oscillation in the control loop [21], [22]. However, this method is relative complex. With DSOGI-PLL, it is necessary to include an extra conversion frame and two second-order generalized integrators (SOGIs). Consequently, the control complexity and the MCU calculating period will be increased.

This paper proposes an enhanced synchronization shift phase-locked loop (SSPLL) strategy for three-phase inverters under unbalanced grid voltages. One of the main features of the proposed SSPLL is the simplicity. With the SSPLL, the double-line frequency oscillation can be eliminated without adding extra circuits, components, and complex computing processes. Moreover, the electrical angle of the grid can precisely be estimated. Comprehensive theoretical analysis, operational principles and mathematical derivations of the proposed control strategy will be presented in this paper. Finally, a 5kVA prototype circuit of a three-phase T-type inverter will be implemented. Both simulation and experimental results verify the performance and feasibility of the proposed strategy. From the comparison results, a maximum 37.9% improvement of current THD can be confirmed with the proposed SSPLL strategy.

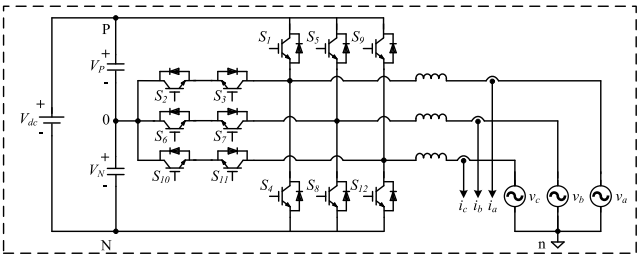



**FIGURE 1.** The circuit diagram of the T-type three-phase grid-tied inverter.

## II. THE THREE-PHASE GRID-TIED INVERTER AND CONVENTIONAL PLL UNDER UNBALANCE GRID VOLTAGES

Fig. 1 shows the circuit diagram of the T-type three-phase grid-tied inverter. It can be seen that twelve power switches, two dc capacitors and three ac inductors are included in the circuit. Fig. 2 shows the control block diagram of the conventional SRF-PLL. With the SRF-PLL, three-phase ac voltage signals, $v_a$, $v_b$, and $v_c$ will be converted into two dc components, $v_d$ and $v_q$, by the synchronous reference frame, $T_{dq}$. The conversion equation can be expressed as:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \tag{1}$$

In Fig. 2, $\omega_{ff}$ is the feedforward line frequency, which is set the same as the line frequency. $\omega_o$ is the estimated line frequency from PLL. $\theta_{PLL}$ is the angle calculated by PLL.

Under normal condition, three-phase voltages are balance. The amplitude of three-phase voltages should be equal, and there should be a 120 degree out of phase shift between each phase. However, non-ideal conditions, such as unbalanced power loads and grid faults might cause unbalanced grid voltages. If the unbalanced grid fault occurs, both positive-sequence and negative-sequence voltage components exist in the power system. There will be double-line frequency oscillation on the d-axis and q-axis voltages. In addition, the average value of the d-axis voltage will be decreased due to the grid voltage attenuation, as shown in Eq. (2).

$$v_a = A \cdot \sin(\theta);\ v_b = B \cdot \sin(\theta - \frac{2\pi}{3});\ v_c = C \cdot \sin(\theta + \frac{2\pi}{3})$$
$$v_d = \frac{1}{3}(A + B + C) - \frac{1}{3}(\mathrm{A} \cdot \cos(2\theta) + \mathrm{B} \cdot \cos(2\theta + \frac{2\pi}{3}) + \mathrm{C} \cdot \cos(2\theta - \frac{2\pi}{3}))$$

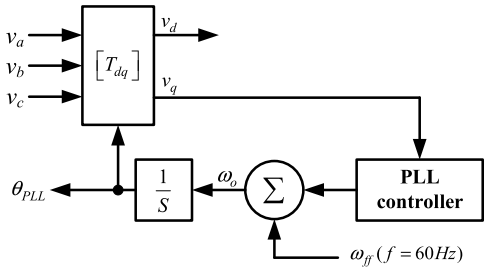



**FIGURE 2.** The control block diagram of the conventional PLL.

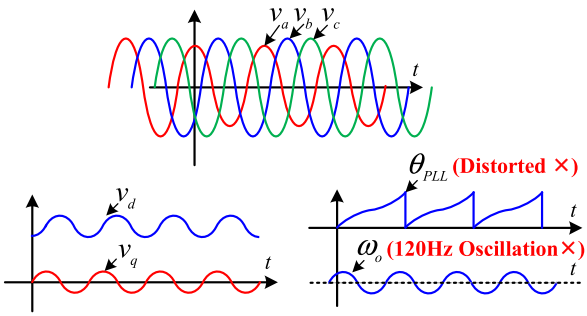



**FIGURE 3.** Relation diagrams of $v_d$, $v_q$, $\theta_{PLL}$, and $\omega_o$ under unbalanced grid voltages.

$$v_q = 0 + \frac{1}{3}(\mathrm{A}\cdot\sin(2\theta) + \mathrm{B}\cdot\sin(2\theta+\frac{2\pi}{3}) + \mathrm{C}\cdot\sin(2\theta-\frac{2\pi}{3})). \quad (2)$$

Besides, if the unbalanced phase of grid voltages occurs, the double-line frequency oscillation can still be observed in $v_d$ and $v_q$, as shown in Eq. (3).

$$\begin{aligned} v_a &= v\cdot\sin(\theta+\theta_a);\ v_b = v\cdot\sin(\theta-\frac{2\pi}{3});\ v_c \\ &= v\cdot\sin(\theta+\frac{2\pi}{3}) \\ v_d &= \frac{2v}{3} - \frac{v}{3}[\cos(2\theta+\theta_a) - \cos(2\theta) - \cos(\theta_a)] \\ v_q &= 0 - \frac{v}{3}[\sin(2\theta+\theta_a) - \sin(2\theta) - \sin(\theta_a)], \end{aligned} \quad (3)$$

where $\theta_a$ represents the diverged phase angle under the unbalanced grid phase scenarios.

Fig. 3 shows relation diagrams of $v_d$, $v_q$, $\theta_{PLL}$, and $\omega_o$ under unbalanced grid voltages. It can be seen that the double-line frequency oscillation occurs on $v_d$ and $v_q$. As a result, $\omega_o$ is oscillated while $\theta_{PLL}$ will be distorted.

Due to the oscillation of $\omega_o$ and the distortion of $\theta_{PLL}$, the three-phase current commands will be distorted, whereas unexpected harmonic components will be generated, as shown in Fig. 4. From Fig. 4, it can be confirmed that the first-order and the third order harmonic components are main factors to distort current commands. It is worth mentioning that the first-order harmonic will cause error amplitude of current commands while the third order harmonic increases the current THD. According to Eq. (2) and Eq. (3), it can be observed that the more severe the unbalanced grid voltage is,

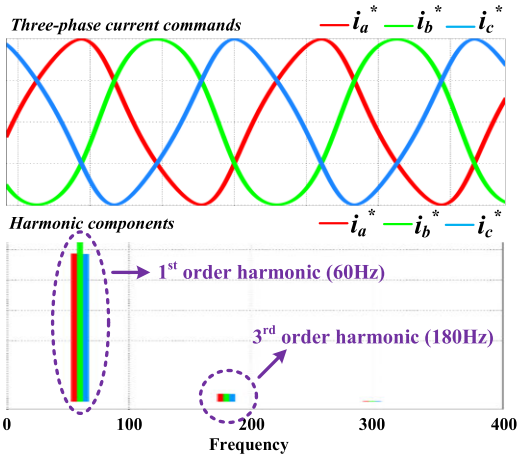



**FIGURE 4.** Conceptual diagram of distorted current commands and harmonic components caused by the $\theta_{PLL}$ oscillation.

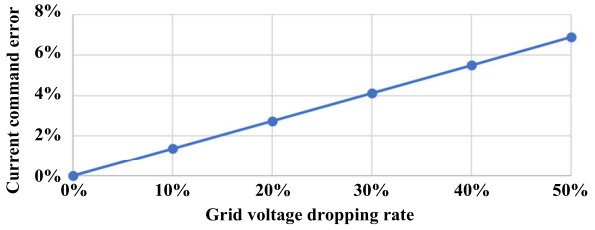



**FIGURE 5.** The relation between the current command error and the grid voltage dropping rate.

the larger the line frequency ($\omega_o$) error will be. Therefore, there will be a linear relationship between the current command error and the phase voltage drop, as depicted in Fig. 5.

## III. THE PROPOSED SYNCHRONIZATION SHIFT PHASE-LOCKED LOOP STRATEGY

In order to eliminate the line frequency ($\omega_o$) error and the PLL angle ($\theta_{PLL}$) distortion, the synchronization shift phase-locked loop (SSPLL) is proposed. Fig. 6 shows the control block diagram of the proposed SSPLL. The main difference between the conventional PLL and the proposed one is to include an adaptive high-pass filter (AHPF) in the control block. From Fig. 6, the $v_d$ signal will be fed into the AHPF and a new signal, $v_d^*$ will be generated. Then, the summation of $v_d^*$ and $v_q$ will be utilized for the PLL controller. It should be mentioned that the double-line frequency oscillation will be removed with the adopting of AHPF. There is no need to modify the inherent controller parameters. As a result, $\omega_o$ error and $\theta_{PLL}$ distortion can be eliminated under unbalanced grid voltages with the proposed SSPLL. In the following, operational principles of the AHPF will be described in detail.

The control block diagram of the proposed AHPF is shown in Fig. 7. First, from Eq. (1) and Eq. (2), it can be confirmed that the average value of $v_d$ will be decreased due to the grid voltage attenuation or the grid phase diversion. Besides, the double-line frequency oscillation occurs on both $v_d$ and $v_q$. According to mathematical derivations and Fig. 3, it can be

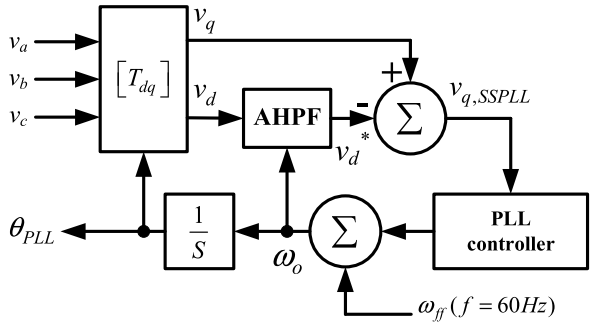



**FIGURE 6.** The control block diagram of the proposed SSPLL.

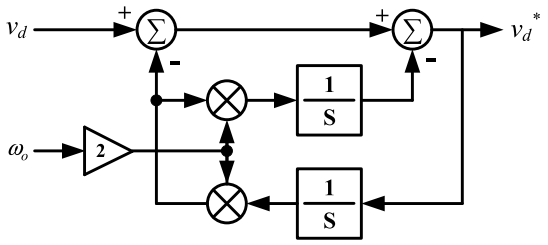



**FIGURE 7.** The control block diagram of the proposed AHPF.

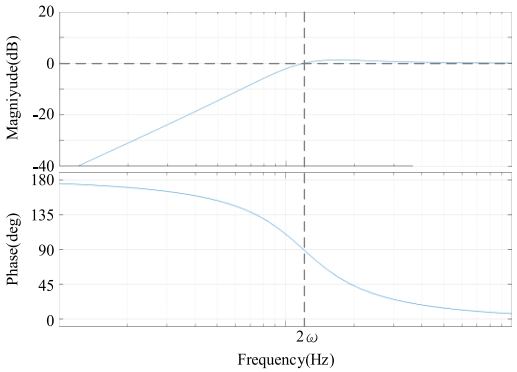



**FIGURE 8.** The frequency response bode plot of the AHPF.

observed that there is a 90 degree out of phase shift between the oscillated $v_d$ and $v_q$ waveform. Therefore, the major objective of the AHPF is to produce a 90 degree out of phase shift between the input signal and the output signal.

From Fig. 7, the transfer function, H(s), of the AHPF can be derived as Eq. (4). The frequency response bode plot of the AHPF can be depicted in Fig. 8.

$$\mathrm{H(s)}=\frac{v_d^*}{v_d}=\frac{s^2}{s^2+2\omega s+(2\omega)^2}. \tag{4}$$

The conceptual diagram of the AHPF is shown in Fig. 9. $v_d^*$ represents the output signal of the AHPF. It is worth mentioning that using a high pass filter with a setpoint crossover frequency can remove the DC offset. However, this is still not enough for the proposed SSPLL. There are two main purposes of the AHPF: (1) Remove the dc offset of the signal and (2) Create a 90° out of phase shift from the input signal. Compare to the conventional high pass filter, the AHPF can

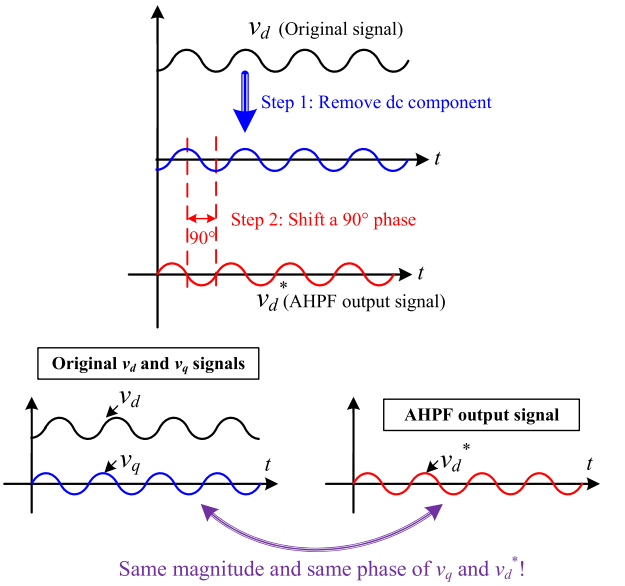



**FIGURE 9.** The conceptual diagram of the AHPF.

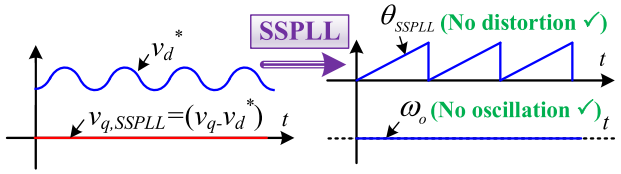



**FIGURE 10.** Relation diagrams of $v_d^*$, $v_{q,SSPLL}$, $\theta_{SSPLL}$, and $\omega_o$ with the proposed SSPLL under unbalanced grid voltages.

not only remove the dc offset but also achieve a 90° out of phase shift. It should be mentioned that there is an inherent 90° phase shift between the original $v_d$ and $v_q$ signal under unbalanced grid conditions, as shown in Fig. 9. In Fig. 9, it can be confirmed that the AHPF output signal ($v_d^*$) is with the same magnitude and same phase of $v_q$. That is to say, the oscillation of $v_q$ can be eliminate via the integration of $v_d^*$ ($v_q$ - $v_d^*$ =0).

The $v_d^*$ and $v_q$ under the grid voltage magnitude unbalanced can be expressed as:

$$\begin{aligned} v_d^* &= \frac{1}{3}(\mathrm{A}\cdot\sin(2\theta)+\mathrm{B}\cdot\sin(2\theta+\frac{2\pi}{3})+\mathrm{C}\cdot\sin(2\theta-\frac{2\pi}{3})) \\ v_q &= \frac{1}{3}(\mathrm{A}\cdot\sin(2\theta)+\mathrm{B}\cdot\sin(2\theta+\frac{2\pi}{3})+\mathrm{C}\cdot\sin(2\theta-\frac{2\pi}{3})). \end{aligned} \tag{5}$$

Besides, $v_d^*$ and $v_q$ under the grid voltage phase unbalanced are derived as:

$$\begin{aligned} v_d^* &= \frac{v}{3}[\sin(2\theta+\theta_a)-\sin(2\theta)-\sin(\theta_a)] \\ v_q &= \frac{v}{3}[\sin(2\theta+\theta_a)-\sin(2\theta)-\sin(\theta_a)]. \end{aligned} \tag{6}$$

According to Eq. (5) and Eq. (6), it can be seen that $v_d^*$ and $v_q$ will be equal under both grid voltage magnitude unbalanced and grid voltage phase unbalanced scenarios.

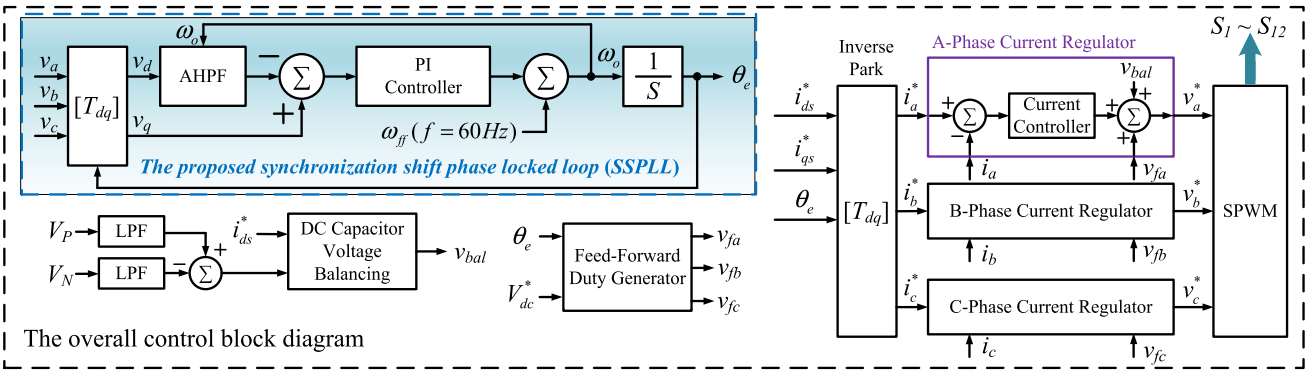



**FIGURE 11.** Overall control block diagrams of the proposed circuit and control strategy.

**TABLE 1.** State of the art comparison of different PLL methods under unbalanced grid voltages.

| | The PLL-Less [19] | The PLL-Less with BPF [19] | The SRF-PLL [15], [16] | The enhanced SRF-PLL [17], [18] | The DSOGI-PLL [21], [22] | **The proposed SSPLL** |
|---|---|---|---|---|---|---|
| Cancellation of $\omega_o$ error | × | ✓ | × | ✓ | ✓ | ✓ |
| Suppression *of* $\theta_{PLL}$ distortion | × | ✓ | × | ✓ | ✓ | ✓ |
| iTHD | High | Neutral | Neutral | Low | Low | **Low** |
| Controller response | Fast | Neutral | Fast | Neutral | Slow | **Fast** |
| Control complexity | Simple | Neutral | Simple | Neutral | Complex | **Simple** |
| A band-pass filter (BPF) | Not required | Required | Not required | Not required | Not required | **Not required** |
| A prefilter and an impedance phase regulator | Not required | Not required | Not required | Required | Not required | **Not required** |

**TABLE 2.** Circuit specifications of the three-phase grid-tied inverter.

| **Parameters** | **Value** |
|---|---|
| Rated power | 5kVA |
| Input DC voltage | 800 V |
| Output Line-to-line grid voltages (Normal condition) | 220$V_{rms}$/60Hz |
| Output Line-to-line grid voltage (Unbalanced grid voltages) | 154$V_{rms}$/60Hz (Scenario I)<br>110$V_{rms}$/60Hz (Scenario II) |
| DC-link capacitance | 0.825mF |
| Output inductance | 2mH |
| Switching frequency | 20 kHz |
| Switch model | 10-FZ12NMA080SH01-M260F |

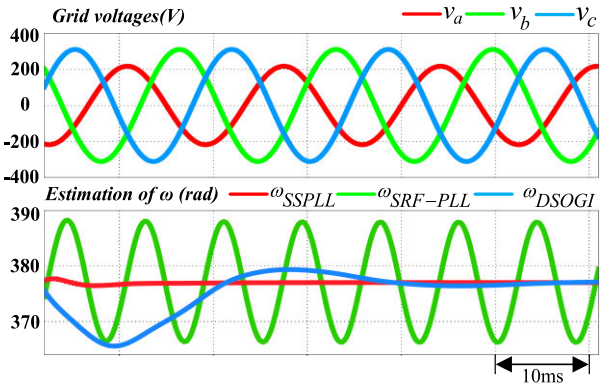



**FIGURE 12.** Simulation waveforms of unbalanced grid voltages and the line frequency with different PLL methods under Scenario I.

Therefore, the difference between $v_d^*$ and $v_q$ will be zero, as indicated in Eq. (7).

$$v_{q,SSPLL} = v_q - v_d^* = 0. \tag{7}$$

From Eq. (7), the ac component can be removed via the proposed SSPLL and AHPF. That is to say, the oscillated ac component will not be fed into the PLL controller. Fig. 10 shows relation diagrams of $v_d^*$, $v_{q,SSPLL}$, $\theta_{SSPLL}$, and $\omega_o$ with the proposed SSPLL under unbalanced grid voltages. It can be confirmed that with the proposed strategy, $\theta_{PLL}$ will not be distorted, whereas $\omega_o$ will not be oscillated. As a result, the inverter output current distortion can be mitigated.

According to the above analysis, the line frequency ($\omega_o$) error and the PLL angle ($\theta_{PLL}$) distortion can easily be

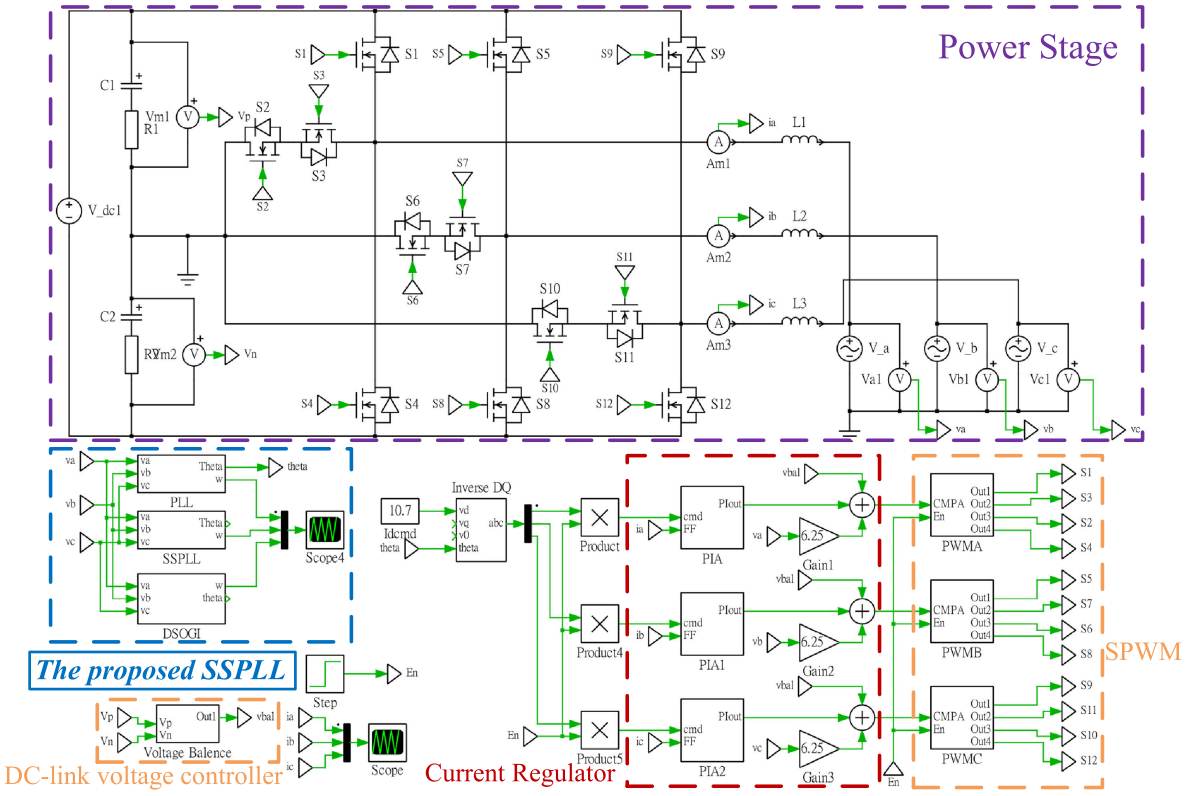



**FIGURE 13.** Circuit diagrams of the T-type three-phase grid-tied inverter and the proposed SSPLL in PLECS.

**TABLE 3.** Current THD comparison of different PLL Strategies with different load conditions under scenario I.

| Load | | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 100% |
|---|---|---|---|---|---|---|---|---|---|---|---|
| iTHD (%) | SRF-PLL | 17.57 | 9.73 | 7.03 | 5.6 | 4.7 | 4.17 | 3.7 | 3.4 | 3.17 | 2.93 |
| | DSOGI-PLL | 12.97 | 6.83 | 4.63 | 3.7 | 3.03 | 2.57 | 2.17 | 1.93 | 1.77 | 1.63 |
| | SSPLL | 12.2 | 6.6 | 4.53 | 3.53 | 2.9 | 2.53 | 2.17 | 1.87 | 1.73 | 1.57 |

**TABLE 4.** Current THD comparison of different PLL Strategies with different load conditions under scenario II.

| Load | | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 100% |
|---|---|---|---|---|---|---|---|---|---|---|---|
| iTHD (%) | SRF-PLL | 23.23 | 13.5 | 9.8 | 7.9 | 6.77 | 5.97 | 5.4 | 4.97 | 4.63 | 4.4 |
| | DSOGI-PLL | 12.6 | 6.93 | 4.67 | 3.67 | 3 | 2.67 | 2.23 | 2 | 1.8 | 1.63 |
| | SSPLL | 12.3 | 6.6 | 4.5 | 3.6 | 2.9 | 2.5 | 2.17 | 1.93 | 1.73 | 1.53 |

compensated via SSPLL under unbalanced grid voltages. Compare to the conventional SRF-PLL and DSOGI-PLL, only one filter, the AHPF, should be included with the proposed strategy. There is no need to add extra circuits and components. Moreover, the AHPF and SSPLL can be implemented in the digital signal processor (DSP) without adding external circuits. Eventually, iTHDs can effectively be suppressed while the circuit performance can be increased.

Overall control block diagrams of the proposed circuit and control strategy are shown in Fig. 11. The proposed SSPLL control, the DC capacitor voltage balancing control, the feed-forward duty generator, three-phase current regulators, and the sinusoidal pulse-width-modulation (SPWM) are included in the system control diagram. It is worth mentioning that the three-phase individual control is adopted in this work. The proportional-integral (PI) control is adopted for the current controller. The transfer function of the current controller is expressed in Eq. (8).

$$G_c(s) = K_p + \frac{K_i}{s + \omega_i}, \tag{8}$$

**TABLE 5.** Current THD comparison of different PLL strategies with different load conditions under scenario III.

| Load | | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 100% |
|---|---|---|---|---|---|---|---|---|---|---|---|
| iTHD (%) | SRF-PLL | 11.93 | 6.87 | 5.17 | 4.3 | 3.73 | 3.43 | 3.1 | 2.97 | 2.87 | 2.7 |
| | DSOGI-PLL | 15.93 | 8.4 | 5.8 | 4.4 | 3.67 | 3 | 2.67 | 2.37 | 2.13 | 1.93 |
| | SSPLL | 14.6 | 7.7 | 5.4 | 4.13 | 3.4 | 2.8 | 2.43 | 2.17 | 2.03 | 1.83 |

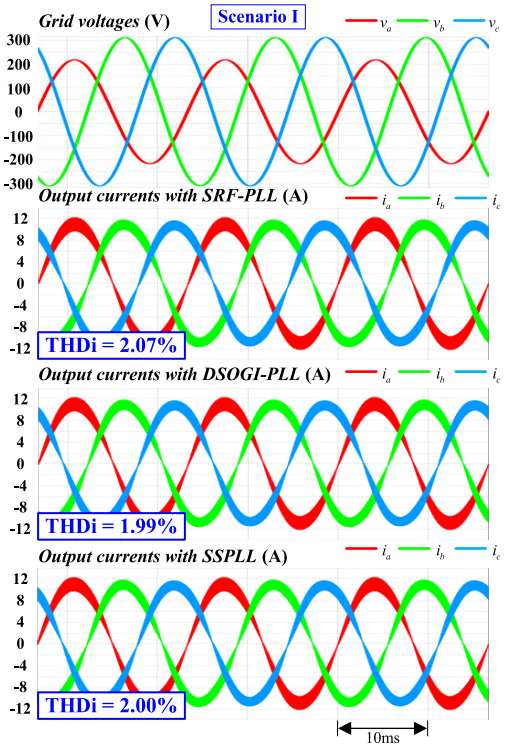



**FIGURE 14.** Simulation results of different PLL strategies in full load operation under Scenario I.

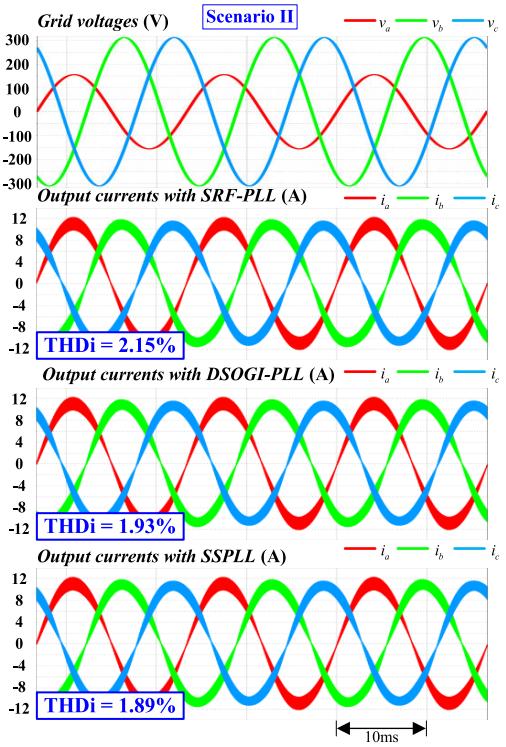



**FIGURE 15.** Simulation results of different PLL strategies in full load operation under Scenario II.

where $K_p$ and $K_i$ are the proportional gain and the integral gain, respectively. $\omega_i$ is a shifted frequency of the current controller. Traditionally, the pole of the PI controller is located at 0Hz. However, in order to prevent the unexpected dc-bias component in the control loop, $\omega_i$ is introduced. With the adoption of $\omega_i$, the pole can be located in higher frequency, whereas the low-frequency gain can be suppressed. It should be noticed that in Fig.11, $v_{bal}$ is the dc-link voltage balancing comment and it is not only used in the Phase-A current regular, but also included in the B-phase and C-phase current regulator.

In order to highlight the contribution and feasibility of the proposed SSPLL strategy, comparative analysis with respect to the state-of-art will be presented. Different PLL methods are investigated and compared, as illustrated in Table 1. First, main features of the PLL-less and the SRF-PLL control are the simplicity and fast response. However, $\omega_o$ error and $\theta_{PLL}$ distortion cannot be neglected with the PLL-less and the SRF-PLL control under unbalanced grid voltages, whereas the iTHD might be increased. To overcome this issue, the PLL-less with BPF [19] and the enhanced SRF-PLL [17], [18] were developed. These two methods can improve the iTHD. However, extra filters or an impedance phase regulator are required. Finally, Both DSOGI-PLL and the proposed SSPLL provide the ability to eliminate $\omega_o$ error, $\theta_{PLL}$ distortion and to reduce iTHD. However, the control of DSOGI-PLL is relative complex while the controller response will be decreased. On the other hand, with the proposed SSPLL, $\omega_o$ error, $\theta_{PLL}$ distortion can be eliminate with simple control and fast response.

It is worth mentioning that there is almost no impact on the controller response and complexity with the adoption of AHPF, and it will be verified in the experiments.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

A T-type three-phase grid-tied inverter is implemented to verify the proposed circuit and control strategy. Table 2 shows circuit specifications of the three-phase grid-tied inverter. The rated power is 5kVA. The input DC voltage is set as 800V. The output three-phase line-to-line voltages are $220V_{rms}$/60Hz. The DC-link capacitance and the output inductance are 0.825mF and 2mH, respectively. The switching frequency is

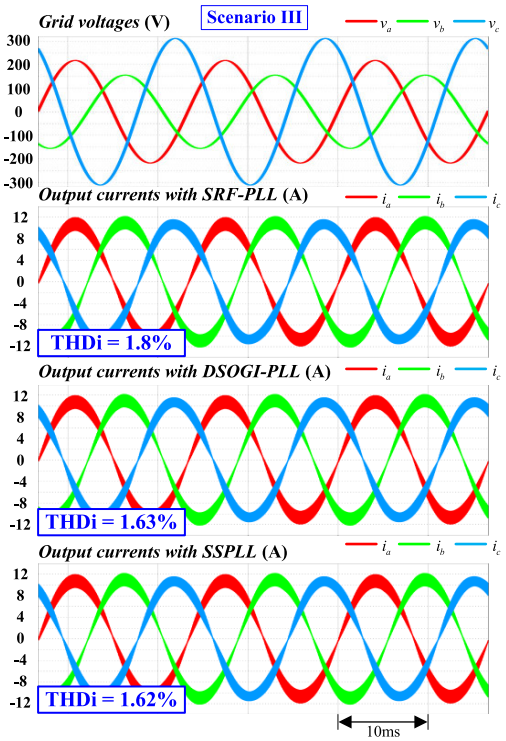



**FIGURE 16.** Simulation results of different PLL strategies in full load operation under Scenario III.

set as 20kHz. The IGBT module, 10-FZ12NMA080SH01-M260F, is chosen as the main circuit switches. The sampling time of the proposed circuit is 50us and it is set the same as the switching period.

In order to verify the proposed SSPLL, three voltage unbalanced scenarios will be built. For Scenario I, the a-phase voltage is decreased to 0.7p.u. ($154V_{rms}$). For Scenario II, the a-phase voltage is decreased to 0.5p.u. ($110V_{rms}$). Scenario III demonstrates the two-phase voltage unbalanced condition. In this case, a-phase voltage is decreased to 0.7p.u. ($154V_{rms}$) while the b-phase voltage is set as 0.5p.u. ($110V_{rms}$). Under this scenario, all three voltages are unequal together.

It should be noticed that because of the limitation of the experimental equipment, the distorted or dc-biased grid voltage conditions are not presented. However, the cross-over frequency of the controller is designed as 1kHz. The gain with the controller will be greater than 0dB in the grid distortion frequency range, whereas the range is usually within 300Hz∼500Hz. Besides, the dc gain of the controller will be very large, which can eliminate the dc-biased component of the grid voltage. That is to say, the designed controller has the ability to compensate and suppress the harmonic distortion and the dc-biased components of the grid voltage theoretically.

In the following, both simulation and experimental results will be presented to demonstrate the performance and feasibility of the proposed SSPLL.

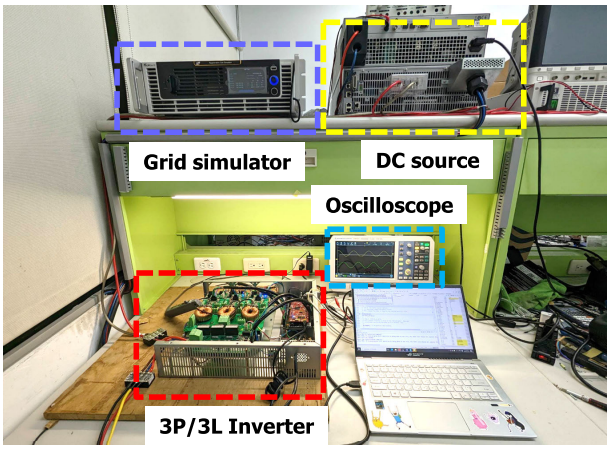



**FIGURE 17.** The photo of the experimental setup.

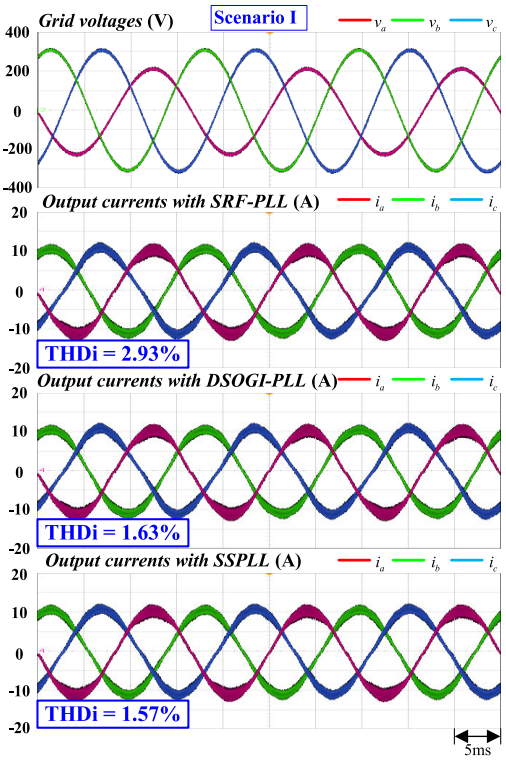



**FIGURE 18.** Experimental results of different PLL strategies in full load operation under Scenario I.

### A. SIMULATION RESULTS

The computer simulation software, PLECS, is selected for verifying the proposed strategy. Fig. 12 shows simulation waveforms of the grid voltages and the estimation of $\omega$ under Scenario I. In this scenario, a-phase voltage is decreased to 0.7p.u. ($154V_{rms}$). It can be seen that the double-line frequency oscillation exists in the line frequency with the conventional SRF-PLL. This oscillation can be removed by the DSOGI-PLL. However, a certain response time is required to reach the steady-state operation with the DSOGI-PLL.

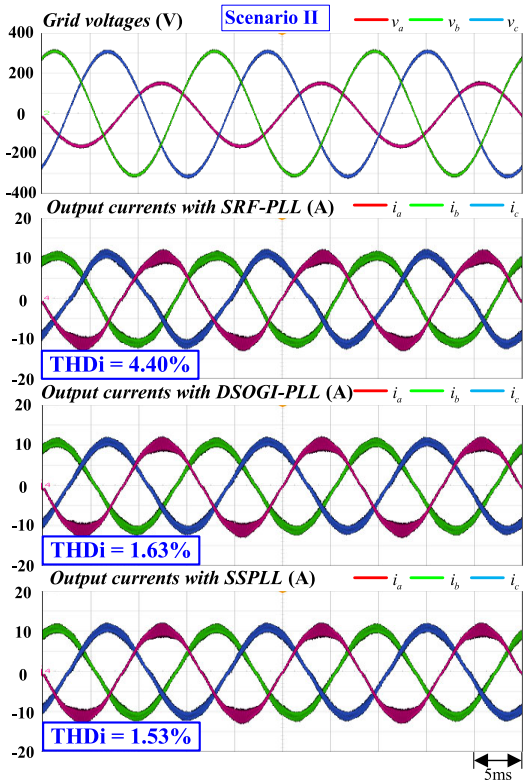



**FIGURE 19.** Experimental results of different PLL strategies in full load operation under Scenario II.

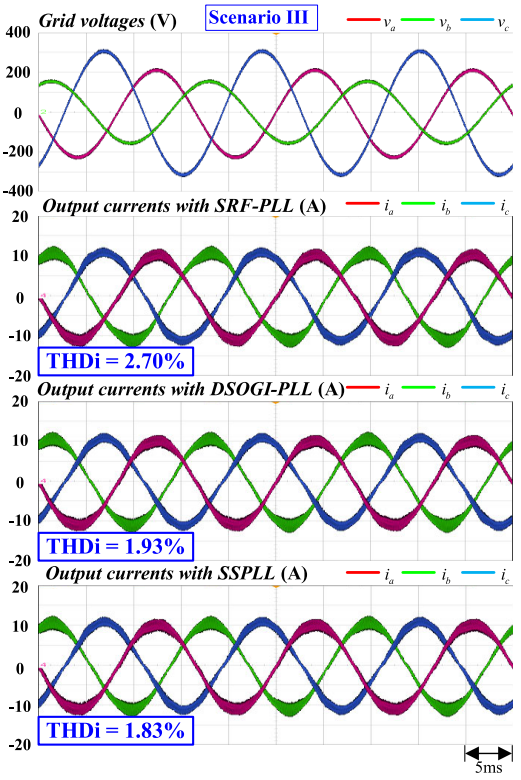



**FIGURE 20.** Experimental results of different PLL strategies in full load operation under Scenario III.

On the other hand, with the proposed SSPLL, the double-line frequency oscillation can effectively be eliminated with faster dynamic response. The key factor to affect the dynamic response will be the controller execution time, and it will be verified via experiments. Besides, circuit diagrams of the T-type three-phase grid-tied inverter and the proposed SSPLL with PLECS are shown in Fig. 13.

Simulation results of grid voltages, output currents with different PLL strategies under Scenario I are shown in Fig. 14. It can be seen that output currents with conventional SRF-PLL will be significantly distorted. However, the current distortion phenomenon can be mitigated by both the DSOGI-PLL and the proposed SSPLL. Simulation results of Scenario II are shown in Fig. 15. In this scenario, $v_a$ is decreased to 0.5p.u. ($110V_{rms}$). Therefore, compare to Scenario I, $\omega_o$ error and the output current distortion will be increased. On the other hand, simulation results of Scenario III are shown in Fig. 16. In this scenario, $v_a$ is decreased to 0.7p.u. ($154V_{rms}$) while $v_b$ is decreased to 0.5p.u. ($110V_{rms}$). it can be confirmed that the proposed SSPLL is still effectively under the two-phase voltage unbalanced condition.

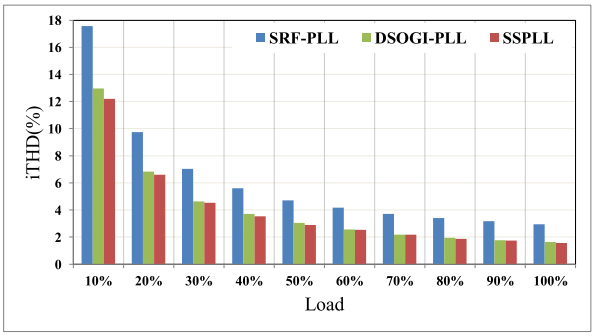
### B. EXPERIMENTAL VALIDATIONS

In this section, experimental validations will be presented. Fig. 17 shows the experimental setup. The DC source, Keysight RP7953A, is connected to the input of the inverter. The grid simulator, Chroma 61815 is connected to the output of the inverter. The IEC 61000-4-7 regulation is adopted for the current THD measurement.

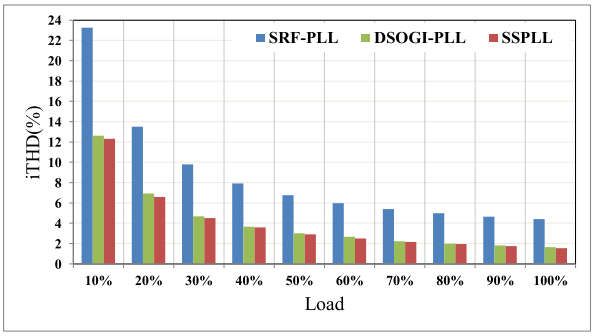
Experimental waveforms of grid voltages and output currents with different PLL strategies in full load operation under Scenario I are shown in Fig. 18. From the results, it can be confirmed that with full load operation under Scenario I, the current THD with the conventional SRF PLL is 2.93%. However, the current THD is reduced to 1.63% and 1.57% with the DSOGI-PLL and the proposed SSPLL, respectively, under the same operating condition. Experimental waveforms of grid voltages and output currents with different PLL strategies under Scenario II are shown in Fig. 19. Under this scenario, the current THD with the conventional SRF-PLL is 4.4%. The current THD with the DSOGI-PLL is 1.63%, whereas the current THD with the proposed SSPLL is decreased to 1.53%. Finally, experimental waveforms of grid voltages and output currents with different PLL strategies in full load operation under Scenario III are presented in Fig. 20. In this case, the current THD of the SRF-PLL, the DSOGI-PLL and the proposed SSPLL are measured as 2.7%, 1.93% and 1.83%, respectively.

### C. PERFORMANCE COMPARISON

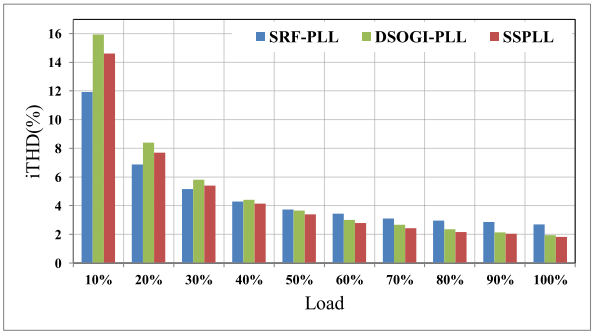
In order to comprehensively demonstrate the feasibility of the proposed PLL strategy, performance comparisons will be presented in this section. Current THD comparisons of




(a)

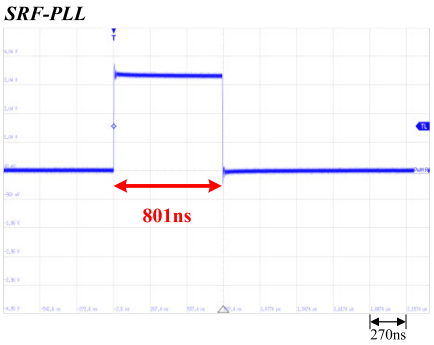



(b)

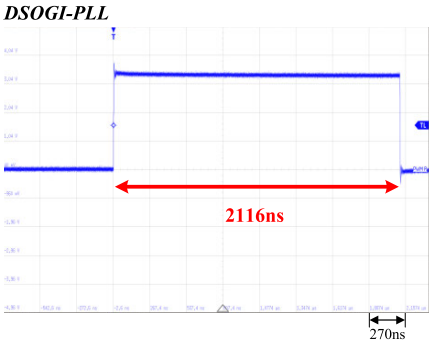



(c)

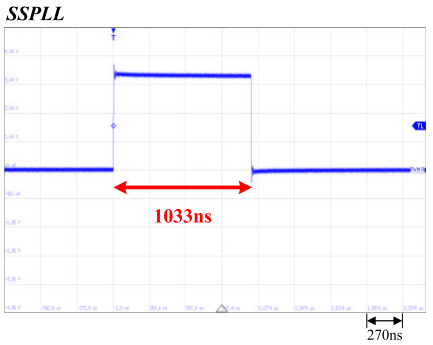
**FIGURE 21.** The current THD comparison under different load conditions. (a) Scenario I. (b) Scenario II. (c) Scenario III.




(a)




(b)




(c)

**FIGURE 22.** The execution time comparison of different PLL strategies. (a) The SRF-PLL. (b) The DSOGI-PLL. (c) The proposed SSPLL.

different PLL strategies with different load conditions and different scenarios are shown in Table 3, Table 4 and Table 5. The measured results in Table 3, Table 4 and Table 5 are also depicted in Fig. 21(a), Fig. 21(b), and Fig. 21(c), respectively.

From Table 3, Table 4, Table 5 and Fig. 21, it can be confirmed that under different unbalanced voltage scenarios and different load conditions, the proposed SSPLL strategy can effectively reduce the current THD. Under the full load operation of Scenario II, the maximum current THD improvement rate can be obtained, which is calculated as 65.22%.

Fig. 22 shows the execution time comparison of different PLL strategies. First, the execution time of the conventional SRF-PLL is 801ns, as shown in Fig. 22(a). The execution time of the DSOGI-PLL is measured as 2116ns, as indicated in Fig. 22(b). Finally, Fig. 22(c) shows the execution time of proposed SSPLL, which is 1033ns. It can be confirmed that the SSPLL execution time is slightly higher than the execution time of the SRF-PLL, but is much lower than the execution time of the DSOGI-PLL. Both of the DSOGI-PLL and the proposed SSPLL provide the ability to suppress iTHD under unbalanced grid conditions. However, with the proposed SSPLL, the execution time can be improved with 51.2%. In other words, the dynamic response can be increased while the executing loading of the controller can be decreased with the proposed control strategy.

## V. CONCLUSION

In this paper, an enhanced synchronization shift phase-locked loop (SSPLL) strategy is proposed. Under unbalanced grid voltage scenarios, the line frequency error and the PLL angle distortion can be eliminated with the proposed strategy, whereas the current THD can be suppressed. Compare to the conventional PLL method, only one adaptive high-pass filter should be included in the controller. Moreover, the SSPLL

can be implemented in the DSPs. There is no need to add extra circuits and components. Thorough theoretical analysis and mathematical derivations are revealed in this paper. Finally, both simulation and experimental results obtained from a 5kVA prototype circuit verify the performance and feasibility of the proposed SSPLL strategy.

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