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RESEARCH ARTICLE

Design and Implementation of Spectrally Efficient Frequency Division Multiplexing Receiver

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ABSTRACT Compared to orthogonal frequency division multiplexing (OFDM), spectrally efficient frequency division multiplexing (SEFDM) provides higher spectrum efficiency, which has been regarded as a promising waveform for future wireless communications. Against this background, the design of SEFDM receiver is investigated in this paper, considering its sampling frequency synchronization (SFS), timing synchronization, phase recovery, and detector design. Specifically, a two-step SFS module, which consists of a coarse sampling frequency offset (SFO) compensation and a frequency domain zero-forcing based fine estimation, is proposed first. Next, a low-complexity timing synchronization scheme is designed to avoid excessive multipliers and look-up-tables. Furthermore, an SFO-based phase recovery is proposed, which shares the compensation and SFO estimation with SFS module, thus further reducing the complexity of SEFDM receiver. Moreover, the truncated singular value decomposition-fixed sphere decoder (TSVD-FSD) based detector has been studied to efficiently eliminate intercarrier interference. Simulation results demonstrate the superiority of our proposed SEFDM receiver, where the transmission rate can be improved by 25% at a loss of only 0.7dB bit error ratio compared to OFDM. Finally, field programmable gate array (FPGA) based implementation is carried out to verify the effectiveness of our proposed SEFDM receiver in practice.

INDEX TERMS Spectrally efficient frequency division multiplexing (SEFDM), sampling frequency synchronization (SFS), low-complexity implementation structure, field programmable gate array (FPGA).

I. INTRODUCTION

With the rapid development of wideband emerging services, such as cloud computing, virtual reality, metaverse, digital twin, etc., next generation wireless communication faces great challenges on the ever-increasing demand of transmission throughput [1]. As a result, an increasing focus has been paid to spectral efficient transmission schemes exemplified by faster-than-Nyquist (FTN) and spectrally efficient frequency division multiplexing (SEFDM) [2], [3], [4]. In particular, the SEFDM [5], which reduces the spacing between subcarriers compared to orthogonal frequency division multiplexing (OFDM), can enhance the spectral efficiency significantly. To be noticed, such spectral efficient enhancement approach has shown that the signaling rate can be increased by 25% without performance degradation compared to its OFDM counterpart [6]. In recent years, SEFDM has been studied to facilitate several communication scenarios such as wireless communication [7] and optical communication [8].

Benefiting from the non-orthogonality between subcarriers, SEFDM shows extremely high bandwidth efficiency. However, such non-orthogonality also introduces severe intercarrier interference (ICI), which deteriorates the transmission performance significantly. To tackle this problem, many works concerning signal detection have been proposed to improve the reception performance of SEFDM system. For example, a maximum likelihood (ML) detector for

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TABLE 1. Comparison of different receiver schemes.

	[12]	[16]	[19]	[20]	Proposed scheme
Timing synchronization			✓	✓	✓
Carrier recovery			✓	✓	✓
Sampling frequency synchronization					✓
Phase recovery				✓	✓
Detector	✓	✓	✓	✓	✓

SEFDM was proposed in [5] to guarantee optimal reliable signal detection at the cost of unacceptable complexity. To reduce the complexity, the sphere decoding (SD) and fixed SD (FSD) based detectors were proposed, which avoid redundant operations by setting a limited search radius [9], [10]. In addition, the simple linear detectors, such as zero-force (ZF) detector and minimum mean square error (MMSE) detector, were proposed [11], [12]. However, both ZF detector and MMSE detector are sensitive to the ill-conditional subcarrier correlation matrix, thus leading to serious performance degradation. To address this issue, the truncated singular value decomposition (TSVD) was utilized to handle the subcarrier correlation matrix, which improves the detection performance obviously [13].To further enhance the performance of FSD detector, the TSVD-FSD detector was proposed, which applies the estimation of TSVD detector as the initialization of FSD detector [14]. Subsequently, several improved detectors, such as ID-FSD detector [15], [16], trellis detector [17], and factor graph-based iterative detector [18], were proposed to improve detection performance. Nevertheless, the above SEFDM detectors highly relies on a perfect synchronization, which is hard to realize in practice.

To be noticed, the multicarrier systems are typically sensitive to synchronization error, which makes accurate synchronization important to SEFDM system. Due to the severe ICI caused by SEFDM modulation and demodulation, the synchronization performance of SEFDM is usually limited. To solve this problem, the method of [20] utilized the OFDM symbol preambles for synchronization, which ignores the effect of ICI. However, to guarantee the demodulation performance, a specific preambles structure is required, which increases the complexity of SEFDM receiver obviously. Furthermore, the SEFDM receiver suffers from a large resource consumption when existing detector algorithms are adopted. Thus, the low-complexity structure of synchronization based on SEFDM symbol preambles should be studied for SEFDM system.

To realize effective timing synchronization, the Schmidl and Cox (S&C) timing synchronization algorithm [21] was commonly utilized in SEFDM system, where the correlation of two specific part of preamble is employed to estimate the timing offset [19]. Due to their similarity in cyclic prefixes and synchronization metric functions, SEFDM and OFDM exhibit similar timing metric curves with flat top. Accordingly, there exists a large estimation error for S&C algorithm. Aiming at reducing the estimation error, several timing synchronization methods, such as Minn algorithm, Park algorithm, etc., were applied in OFDM system [22], [23], [25], [26], [31]. By designing appropriate timing synchronization preamble and synchronization metric function, the peak of timing metric curve became more sharp and recognizable, thus leading to an improve timing synchronization accuracy. In particular, the methods in [22], [23], [25], [26], and [31] can also be adopted in SEFDM system by setting an SEFDM symbol preamble. However, the above algorithms need two parts of preamble, which reduces the throughput especially under small signal to noise ratio (SNR).

The above timing synchronization algorithm cannot eliminate the sampling frequency offset (SFO) caused by the difference between oscillator frequencies at transmitter and receiver. The authors in [27] show that the SFO in multicarrier system can be expressed as a phase rotation in frequency domain. Subsequently, several sampling frequency synchronization (SFS) algorithms were proposed to estimate the SFO with the help of pilot signals [28], [29]. However, these works only utilize the phase differences to estimate the SFO, the performance of which is limited when SFO is large. Furthermore, the SFO estimation suffers from severe inherent ICI in SEFDM system, thus leading to an inevitable accuracy degradation.

In this paper, we design and implement a novel SEFDM receiver structure. Our main contributions are boldly and explicitly contrasted to the state-of-the-art in Table 1 at a glance as well as in more detail below:

- A two-step SFS module concerning both frequency domain and time domain processing is proposed. In particular, a ZF-SFS algorithm is utilized for fine SFO estimation in frequency domain, and a coarse adjustment controlled by fine SFO estimation is designed in time domain.
- SFO based phase recovery method is investigated for the proposed SEFDM receiver. By sharing the SFO estimator and compensator with the SFS module, the implementation complexity of our proposed phase recovery module can be greatly reduced.
- The implementation structure of the proposed SEFDM receiver using field programmable gate arrays (FPGAs) is presented. Compared to OFDM, the bit error rate (BER) performance loss of our proposed SEFDM is only 1.2 dB when packing factor $\alpha = 0.8$.

The remainder of this paper is organized as follows. In Section II, we present the system model of SEFDM system.

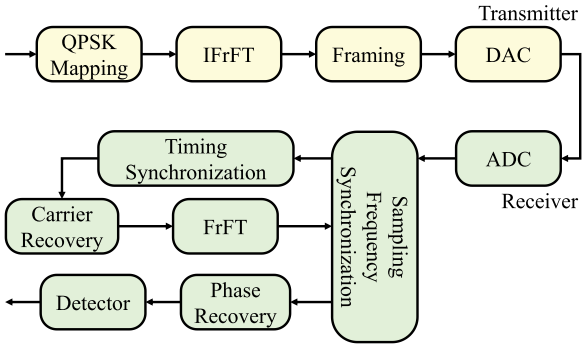

FIGURE 1. The block diagram of the SEFDM modem structure.

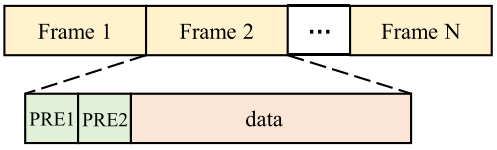

FIGURE 2. Frame structure for SEFDM.

In Section III, a novel SEFDM receiver structure is designed. In Section IV, simulation results and implementation results are presented. Finally, conclusions are drawn in Section V.

II. SYSTEM MODEL

The proposed SEFDM system structure is depicted in Fig. 1. At the transmitter, the information bits are mapped into multiple phase shift keying (MPSK) or multiple quadrature amplitude modulation (MQAM) symbols. The mapped symbols are allocated into N subcarriers by a serial-to-parallel (S/P) conversion and fed to the inverse fractional Fourier transform (IFrFT) module.[1]

Consequently, the equivalent baseband SEFDM signals can be presented as

$$x(t) = \sqrt{\frac{1}{T}} \sum_{n=0}^{N-1} s_n e^{\frac{i2\pi\alpha nt}{T}}, \tag{1}$$

where s_n is the transmitted symbol of the nth subcarrier, $0 < \alpha \leq 1$ is the packing factor, and T is the SEFDM signal duration.

The frame structure of the proposed SEFDM system is given in Fig. 2. The preamble is inserted every N_d SEFDM symbols, where the first preamble duration $PRE1$ contains N_s symbols and the second preamble duration $PRE2 = \text{conj}(PRE1)$ with conj$(\cdot)$ denoting the conjugate operation.

The received signal at time t can be expressed as

$$r(t) = x(t) + w(t), \tag{2}$$

where $w(t)$ denotes additive white Gaussian noise (AWGN) with zero mean and variance σ_0^2.

[1]The transmitted symbols can be implemented by IFrFT operation, which can also be replaced by an inverse fast Fourier transform (IFFT) with higher implementation efficiency [30].

At the receiver, the output matrix of the fractional Fourier transform (FrFT) module can be expressed as

$$Y = \mathbf{C}S + W, \tag{3}$$

where $S = [s_0, s_1, \ldots, s_{N-1}]$ denotes the $N \times 1$ transmitted symbol, and W is the $N \times 1$ independent Gaussian noise samples. $\mathbf{C}$ is the $N \times N$ sub-carrier correlation matrix, given by

$$\mathbf{C} = \begin{bmatrix} c_{0,0} & c_{0,1} & \cdots & c_{0,N-1} \\ c_{1,0} & c_{1,1} & \cdots & c_{1,N-1} \\ \vdots & \vdots & \ddots & \vdots \\ c_{N-1,0} & c_{N-1,1} & \cdots & c_{N-1,N-1} \end{bmatrix}, \tag{4}$$

where $c_{m,n}$ is the cross correlation between the mth and nth element, given by

$$c_{m,n} = \frac{1}{N} \sum_{k=0}^{N-1} f_{n,k} \hat{f}_{k,m}, \tag{5}$$

where $f_{n,k} = e^{-\frac{j2\pi nk\alpha}{N}}$ and $\hat{f}_{k,m} = e^{\frac{j2\pi km\alpha}{N}}$.

III. LOW-COMPLEXITY SEFDM RECEIVER

In this section, a novel SEFDM receiver structure is proposed, which consists of a two-step SFS, a low-complexity timing synchronization, a phase recovery, and a TSVD-FSD detector.

A. SAMPLING FREQUENCY SYNCHRONIZATION

The received signal with SFO can be expressed as $y(t - \Delta\phi nT')$, where $\Delta\phi = \phi_n - \phi_{n-1}$ represents the SFO with ϕ_n denoting the phase of nth subcarrier. T' denotes the sampling clock at receiver. The output of the FrFT can be expressed as

$$\begin{aligned} Y_n &= \sqrt{\frac{1}{N}} \int_0^{T'} y(t - \Delta\phi nT') e^{\frac{-i2\pi\alpha nt}{N}} dt \\ &= \sqrt{\frac{1}{N}} \int_0^{T'} y(t - \Delta tnT' - \Delta\hat{\phi} nT') e^{\frac{-i2\pi\alpha nt}{N}} dt \\ &= A\sqrt{\frac{1}{N}} \int_0^{T'} y(t - \Delta tnT') e^{\frac{-i2\pi\alpha nt}{N}} dt, \end{aligned} \tag{6}$$

where $\Delta tnT'$ is a multiple of T, and Δt is the integral part of SFO. $\Delta\hat{\phi}$ is the decimal part of SFO. $A = e^{\frac{-i2\pi\alpha\Delta\hat{\phi}nT'}{N}}$ indicates phase rotation caused by the decimal part. The integral part results in a input sequence disruption as $y(t - \Delta tnT')$, which influences all the subcarriers and is hard to eliminate.

To estimate the SFO accurately, a two-step SFS, as shown in Fig. 3, is proposed for SEFDM receiver. The newly proposed SFS consists of a time domain coarse adjustment and a frequency domain fine estimation, which will be detailed as follows.

1) TIME DOMAIN COARSE ADJUSTMENT

The time domain coarse adjustment is designed for eliminating the integral part of SFO, which can be realized by

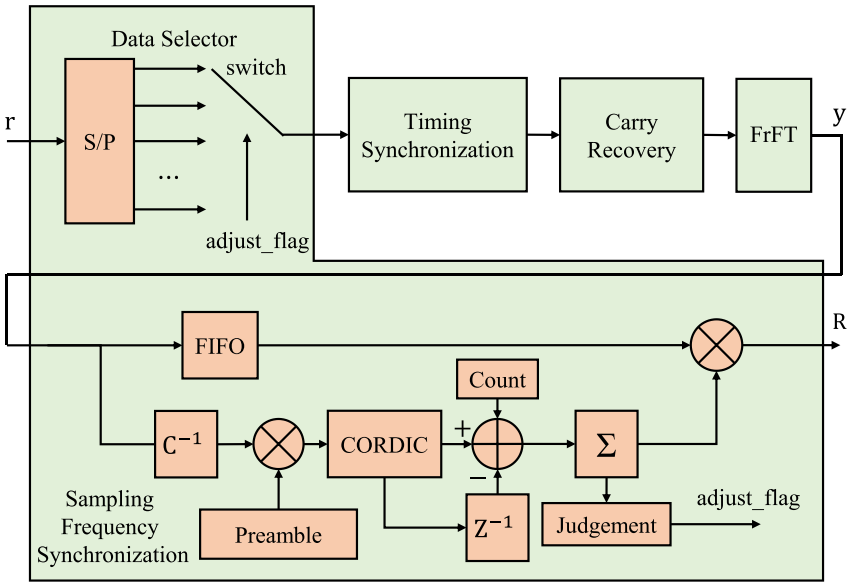

FIGURE 3. The structure of SFS module.

controlling the location of the input data r. To implement the coarse adjustment, a data selector is utilized in the time domain, which contains a S/P convertor and a switch. The S/P converter groups the serial data into $N_{ds} = R_{ua}/R_{ud}$ blocks, where R_{ua} is the upsampling rate of analog-to-digital converter (ADC), and R_{ud} is the upsampling rate of the input data of timing synchronization.

The data selector should be adjusted according to the *adjust_flag* provided by the frequency domain fine estimation. The switch is used to select the output path. When *adjust_flag* is setting as 0 or 1, the switch would move forward or backward, respectively.

2) FREQUENCY DOMAIN FINE ESTIMATION

The integral part of SFO has been eliminated by the time domain coarse adjustment. As a result, the signal calculated by FrFT can only be influenced by the decimal part of SFO, given by

$$Y_n = e^{\frac{-i2\pi\alpha\Delta\hat{\phi}nT'}{N}}\sqrt{\frac{1}{N}}\int_0^{T'} y(t)e^{\frac{-i2\pi\alpha nt}{N}}dt. \tag{7}$$

The traditional preamble-based SFS algorithms calculate the phase difference between adjacent subcarriers of Y_n. However, owing to the loss of orthogonality between subcarriers, the constellation points from FrFT deviate from their ideal locations, which influences the calculation of phase difference and causes a performance degradation in SFS module. To mitigate ICI, the inverse of the inherent ICI matrix is used to eliminate the inherent ICI before the preamble-based SFS algorithm, which can be mathematically expressed as

$$F = \mathbf{C}^{-1}Y. \tag{8}$$

For the mth SEFDM preamble symbol, the estimated SFO can be expressed as

$$\Delta\phi_m = \frac{1}{N-1}\sum_{n=1}^{N-1} arctan\frac{D_{m,n} - D_{m,n-1}}{1 + D_{m,n}D_{m,n-1}}, \tag{9}$$

where $D_{m,n} = imag(F_{m,n}\tilde{F}_{m,n})/real(F_{m,n}\tilde{F}_{m,n})$, $real(\cdot)$ means the real operation, $imag(\cdot)$ means the imaginary operation. $F_{m,n}$ is the input preamble of nth subcarrier and $\tilde{F}_{m,n}$ is the nth stored frequency domain subcarrier preamble.

The final estimated SFO can be calculated as

$$\Phi = \frac{1}{2N_s}\sum_{m=0}^{2N_s-1}\Delta\phi_m, \tag{10}$$

The structure of the SFS is shown in Fig. 3. More specially, the inverse of the inherent ICI matrix $\mathbf{C}$ and the frequency domain preamble are stored in the read-only memories (ROMs), and the phase differences are calculated by the CORDIC core. Because the phase differences calculated by CORDIC core are between $-\pi$ and π, the accumulated value should be compensated. When the phase difference is more than π or less than $-\pi$, the accumulation q will be extended to 2π or -2π as follows.

$$q = \begin{cases} q - 2\pi & e_m > \pi \\ q + 2\pi & e_m < -\pi \\ q & otherwise, \end{cases} \tag{11}$$

where e_m denotes the calculated phase difference.

The Judgement module controls the *adjust_flag*. When the estimated SFO is less than a lower threshold, *adjust_flag* is set as 0. Besides, when the estimated SFO is greater than an upper threshold, *adjust_flag* is set as 1. The lower threshold and upper threshold can be set as $-\pi/2$ and $\pi/2$, respectively.

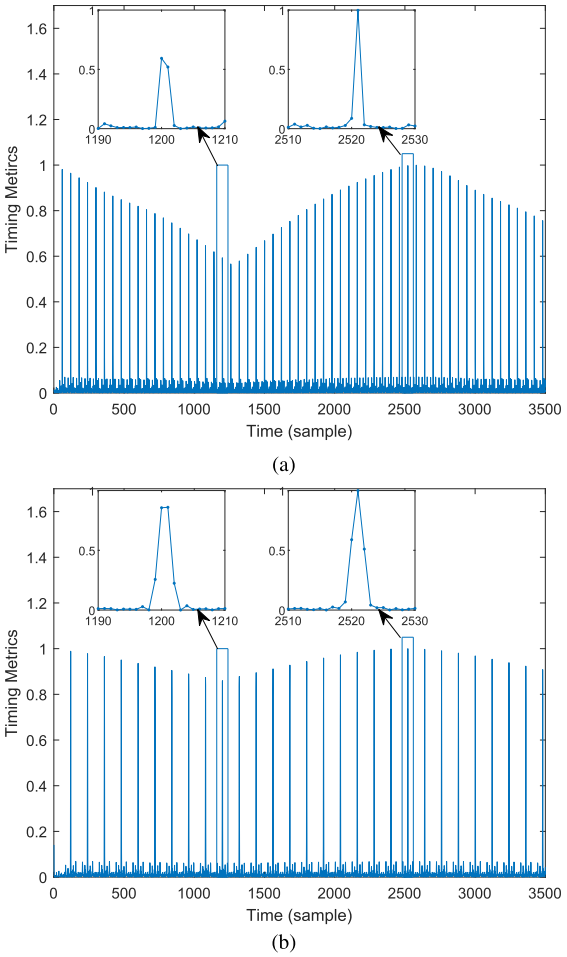

FIGURE 4. The correlation curves in the different data sample ratio as (a) $R_c = 1$, (b) $R_c = 2$.

B. TIMING SYNCHRONIZATION

The timing synchronization can estimate the timing offset in the SEFDM system. The existing algorithms, such as S&C algorithm, Minn algorithm, Park algorithm, etc., typically require two halves of time domain preambles, thus reducing the length of correlation. To fully utilize the preamble in timing synchronization, the designed timing synchronization technique needs to store the whole preambles. To find the starting of the SEFDM symbol, the maximum point of the timing metric should be estimated. In the designed timing synchronization, the timing metric is given by

$$M_d(d) = \frac{|P(d)|^2}{B^2(d)}, \tag{12}$$

where d is a time index, $B(d)$ denotes the average energy of the input data $[b_d, b_{d-1}, \ldots, b_{d-2N_s+1}]$, and $P(d)$ is given by

$$P(d) = \frac{1}{2N_s} \sum_{m=0}^{2N_s-1} (b_{d-m} \check{b}_m^*), \tag{13}$$

where $\check{b}_m$ denotes the mth stored time domain preamble, and $(\cdot)^*$ indicates the conjugate operation.

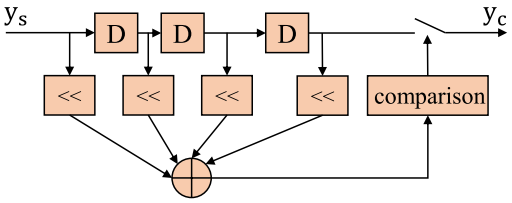

FIGURE 5. The structure of timing synchronization.

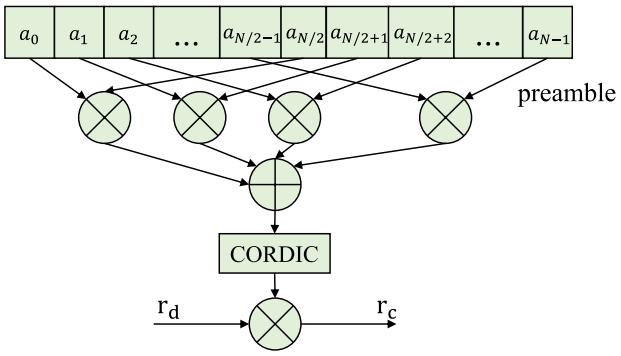

FIGURE 6. The structure of carrier recovery.

Due to the sampling bias, the input data gradually deviates from its best sampling point. Thus, the data upsampling rate will influence the maximum point of the timing metric. Fig. 4 shows the timing metric M_d in the different data upsampling rate. To visualize the changes in correlation peaks, the input data is set as the period of the preamble. The data upsampling ratio are set as $R_{uc} = 1$ and $R_{uc} = 2$, respectively. It can be seen that the correlation peaks in Fig. 4(b) are higher than that in Fig. 4(a). To find the maximum point of the timing metric more accurately, the data upsampling rate in the designed timing synchronization structure must be equal or greater than 2.

From (13), it can be known that the calculation of $P(d)$ requires $L_s = 2NN_d$ complex multipliers. To reduce the computational complexity, we quantize the signal amplitude and then employ shift operation to approximate the multiplication. The structure of timing synchronization is shown in Fig. 5, and the output preamble can be obtained directly from the D flip-flop without waiting for long serial output.

C. CARRIER RECOVERY

The parallel preamble obtained by timing synchronization is divided into two groups $[a_0, a_1, \cdots, a_{N/2-1}]$ and $[a_{N/2}, a_{N/2+1}, \cdots, a_{N-1}]$. The accumulation of conjugate multiplication with two groups of preamble is expressed as

$$E = \sum_{n=0}^{N/2-1} a_n a_{N/2+n}. \tag{14}$$

By calculating the angle of the E, i.e. $O = \angle E$ with $\angle(\cdot)$ representing the angle operation, the carrier frequency offset can be obtained.

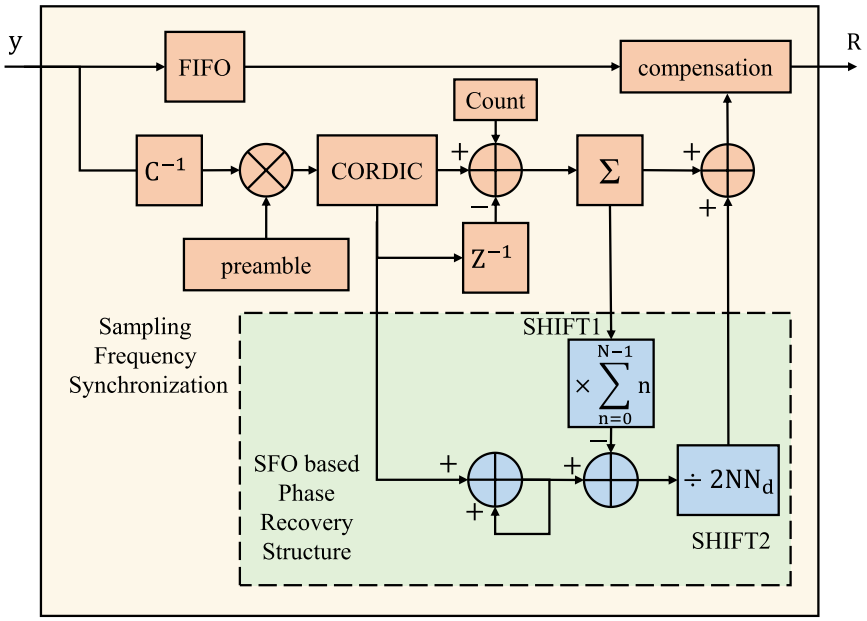

FIGURE 7. The structure of joint sampling frequency synchronization and phase recovery.

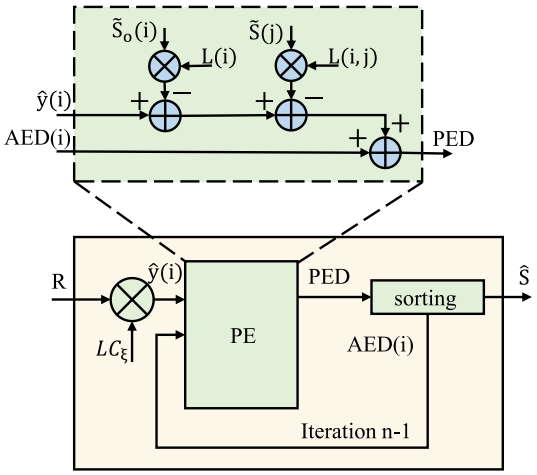

FIGURE 8. The block diagram of detector.

The structure of carrier recovery is shown in Fig. 6, where the signal can be compensated by a direct digital synthesizer module according to the estimated carrier frequency offset.

D. PHASE RECOVERY

In this section, we design an SFO based phase recovery structure. To reduce its complexity, modules exemplified by first-in first-out (FIFO), CORDIC core, and multiplier in phase recovery are shared with SFS module.

The relationship between the phase offset and the SFO in the lth SEFDM symbol and nth subcarrier can be obtained as

$$e_{l,n} + \hat{\Phi}_n = \angle(Y_{l,n}\check{Y}^*_{l,n}), \tag{15}$$

where $e_{l,n}$ is the phase offset. $\check{Y}_{l,n}$ denotes the stored frequency domain preamble sequence. $\hat{\Phi}_n$ is the accumulation of SFO, which can be expressed as $\hat{\Phi}_n = n\Phi$. The Φ can be gained by (10). Accordingly, the estimated phase offset can be presented as

$$e_{l,n} = \angle(Y_{l,n}\check{Y}^*_{l,n}) - n\Phi. \tag{16}$$

By averaging the phase offsets, the estimated phase offset in each frame can be expressed as

$$\overline{e} = \frac{1}{L_s}\sum_{n=0}^{N-1}\sum_{l=0}^{N_d-1} e_{l,n}. \tag{17}$$

The structure of SFO based phase recovery is shown in Fig. 7, where *SHIFT*1 and *SHIFT*2 represent the formula $n\Phi$ and $1/L_s$, respectively.

E. DETECTOR

We employ the TSVD-FSD algorithm to detect the signals, which can achieve acceptable detection performance with low implementation complexity. In TSVD-FSD algorithm, the initial radius of the search hypersphere in FSD algorithm is calculated by TSVD algorithm, which can be expressed as

$$g = \|R - \mathbf{C}S_{TSVD}\|^2, \tag{18}$$

where R is the input data of detector, and the estimation of TSVD algorithm S_{TSVD} is expressed as

$$S_{TSVD} = \lfloor \mathbf{C}_\xi R \rceil, \tag{19}$$

where $\lfloor\cdot\rceil$ is the slicing operation. The TSVD based pseudoinverse of $\mathbf{C}$, denoted by $\mathbf{C}_\xi$, can be calculated as

$$\mathbf{C}_\xi = \mathbf{V}\Sigma_\xi^{-1}\mathbf{U}^*, \tag{20}$$

where $\Sigma_\xi = diag(1/\sigma_1, 1/\sigma_2, \cdots, 1/\sigma_\xi, 0, \cdots, 0)$ and $\xi < N$ is truncation index. Using the SVD operation to the

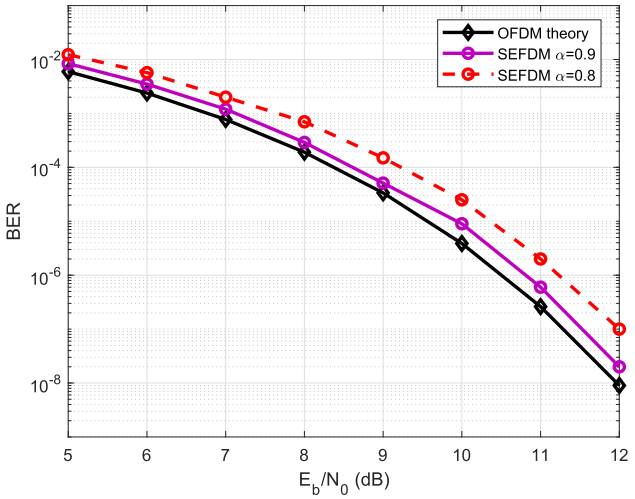

FIGURE 9. BER performance of the proposed SEFDM system.

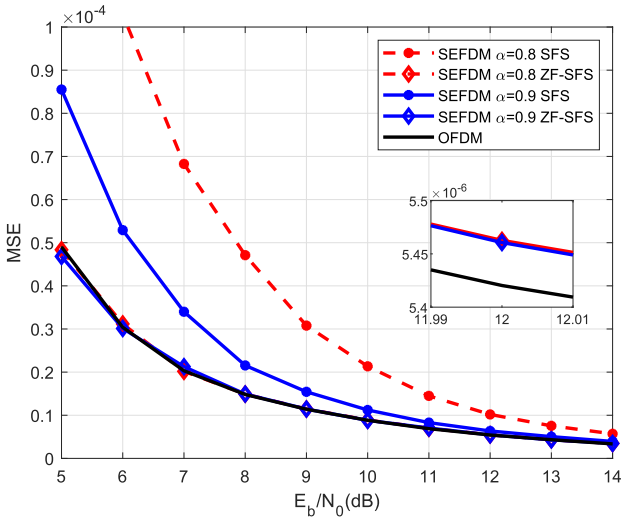

FIGURE 10. MSE of SFOs in ZF-SFS algorithm and SFS algorithm.

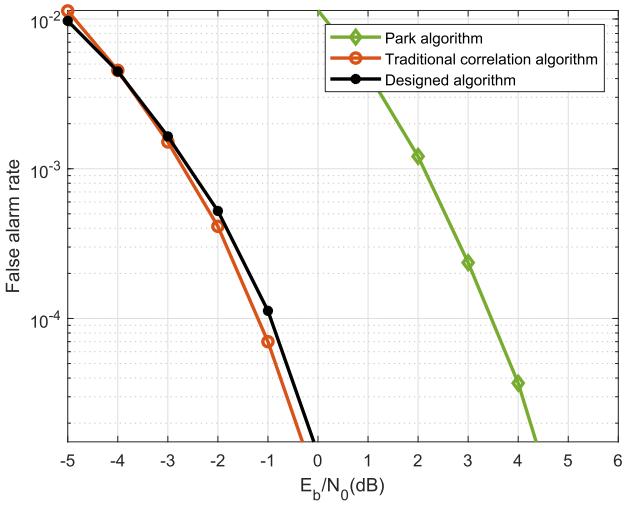

FIGURE 11. False alarm rate of Park algorithm, traditional correlation algorithm and designed algorithm in timing synchronization.

inherent ICI matrix $\mathbf{C}$, the perematers $\mathbf{V}$, Σ_ξ, and $\mathbf{U}$ can be executed as

$$\mathbf{C} = \mathbf{U}\Sigma\mathbf{V}^*, \tag{21}$$

where $\Sigma = diag(\sigma_1, \sigma_2, \cdots, \sigma_N)$, σ_i is the ith singular value of $\mathbf{C}$.

By calculating initial radius, the TSVD-FSD algorithm is defined as

$$\begin{aligned} S_{TSVD-FSD} &= arg \min_{\tilde{S}\in Q} \|R - \mathbf{C}\tilde{S}\|^2 \le g \\ &= arg \min_{\tilde{S}\in Q} \|\mathbf{L}(\tilde{S}_{TSVD} - \tilde{S})\|^2 \le g \end{aligned} \tag{22}$$

where $\mathbf{L}$ is an $N \times N$ upper triangular matrix defined by chol$\{\mathbf{C}^*\mathbf{C}\} = \mathbf{L}^*\mathbf{L}$, chol$\{\cdot\}$ donates the Cholesky decomposition, and Q is the constellation cardinality.

The block diagram of TSVD-FSD is shown in Fig. 8. The processing element (PE) calculates the partial Euclidean distance (PED), while the AED, which means the accumulated PED, is calculated by sorting. The $\tilde{S}_o$ means the ordered constellation points.

IV. SIMULATION RESULTS AND IMPLEMENTATION

In this section, the performance of the proposed SEFDM receiver is presented, as well as the experiential results of its FPGA implementation.

A. SIMULATION RESULTS

According to previous studies [31], [32], the parameters of the simulation are shown as follows. The number of subcarriers is $N = 12$, and the modulation scheme is quadrature phase shift keying (QPSK). The preamble is inserted every $N_d = 60$ SEFDM symbols, where the length of each preamble is $N_s = 5$ SEFDM symbols. To adapt the proposed two-step SFS structure, the upsampling rate of ADC is $R_{ua} = 8$, and the upsampling rate of the data selector is $R_{ud} = 2$.

The BER performance of the proposed SEFDM receiver structure is shown in Fig. 9, where the packing factors α are set as 0.8 and 0.9, respectively. It can be seen that the BER performance of the proposed SEFDM receiver with $\alpha = 0.9$ is close to that of the OFDM system, while the transmission rate can be increased by 11%. When $\alpha = 0.8$, the BER performance loss is only 0.7dB with transmission rate increasing 25%, which suggests the proposed structure can achieve considerable transmission rate with acceptable BER performance loss.

In Fig. 10, the sampling frequency performance realized by SFS algorithm in [28] and our proposed ZF-SFS are compared, where the performance of OFDM system with SFS algorithm is also plotted as a benchmark. It can be observed that the proposed ZF-SFS algorithm outperforms SFS. In particular, the performance gain becomes more apparent as the packing factor α becomes smaller, which validates the superiority of the proposed method.

The timing synchronization performance is presented in Fig. 11. The judgement threshold of correlation is set as

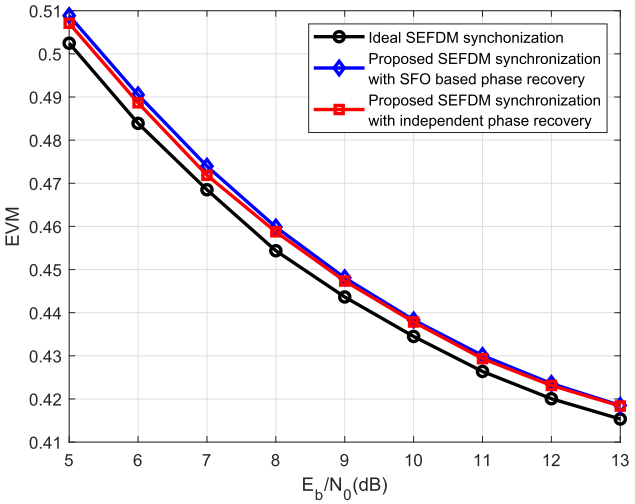

FIGURE 12. The comparison of EVM performance.

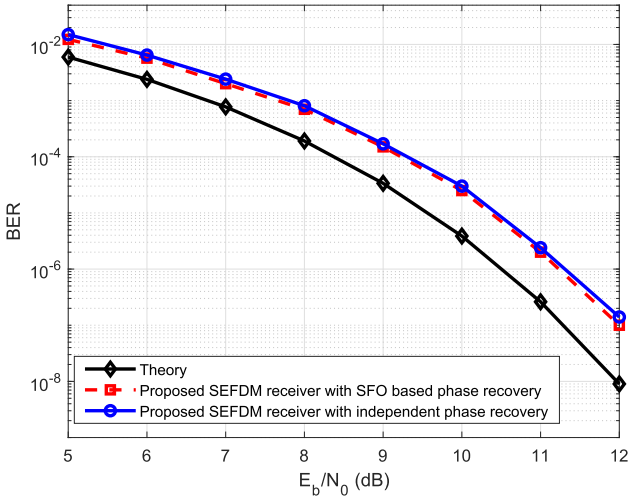

FIGURE 13. The BER performance with the proposed SFO based phase recovery and the independent phase recovery.

$T_h = (C_{max,1} + C_{max,2})/2$ without noise. $C_{max,1}$ and $C_{max,2}$ represent the maximum peak value and the second-maximum peak value of timing metric in one frame, respectively. The complex multipliers in traditional timing synchronization structure will be replaced by adders, thus reducing hardware cost.

The comparison of the false alarm rates between the designed timing synchronization algorithm, the traditional correlation algorithm and the Park algorithm are shown in Fig. 11. Because of the same length of preambles, the correlation length of Park algorithm is half of the other two algorithms, resulting in a worse timing synchronization performance. Particularly, the false alarm rate gap between designed algorithm and Park algorithm is about 4.5 dB. By contrast, the false alarm rate of designed algorithm is similar to traditional correlation algorithm with the gap at about 0.2 dB.

In Fig. 12, we compare the error vector magnitude (EVM) of the proposed synchronization structure with SFO based phase recovery and independent phase recovery, where the EVM achieved by ideal synchronization is also plotted as a benchmark. It is observed that the proposed SFO based phase recovery has a similar EVM to the independent method, and the complexity of the proposed structure is much lower. Compared to the ideal synchronization, the proposed synchronization structure leads to a 0.5 dB loss. To further verify the effectiveness of the SFO based phase recovery, the BER performance of the SEFDM system with the proposed SFO based phase recovery is shown in Fig. 13. It can be seen that the SEFDM receiver with SFO based phase recovery performs a similar BER performance compared to the independent phase recovery. The proposed phase recovery structure ignores the phase offset caused by the SFS module, which leads to a 0.1 dB loss of BER performance.

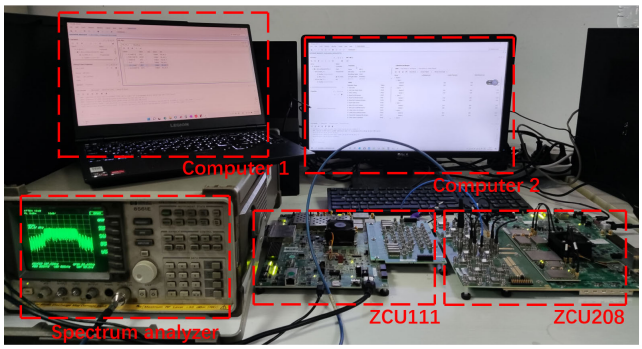

FIGURE 14. The experimental setup of the proposed SEFDM communication system.

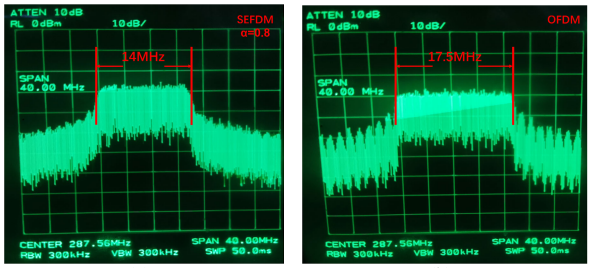

FIGURE 15. The measured spectrum: (a) SEFDM spectrum, (b) OFDM spectrum.

B. FPGA IMPLEMENTATION

Finally, Zynq UltraScale+ RFSoC ZCU208 Evaluation Kit and Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit are utilized to implement the SEFDM transmitter and receiver, respectively. Fig. 14 depicts the experimental setup of our designed SEFDM communication system.

Moreover, the sampling rate of ADC is configured as $R_{adc} = 140$MSPS, and the bit data rate is $R_b = 35$Mbps, which means that the QPSK symbol rate is $R_s = 17.5$MSPS. After the data selector, the sampling rate is set as $R_c = 35$MHz. The carrier frequency is $f_c = 280$MHz. Other parameters are the same as that in Section IV-A.

The spectrum of OFDM signal and SEFDM signal based on the above system parameters are shown in Fig. 15. It can

TABLE 2. Resource utilization of the proposed SEFDM receiver hardware design.

Resource	Utilization	Available	Utilization rate
LUTs	129938	425280	30.6%
FFs	213939	850560	25.1%
BRAM	44	1080	4%
DSP48s	2958	4272	69.2%

TABLE 3. Computational complexity of timing synchronization.

Operation	CMs	CAs
Park algorithm	N_d	$N_d - 1$
Traditional correlation algorithm	$2N_d$	$2N_d - 1$
Designed algorithm	0	$2N_d - 1$

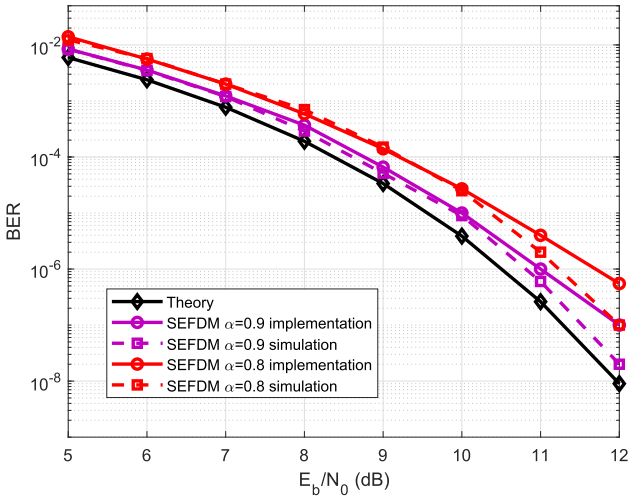

FIGURE 16. The BER performance of the proposed SEFDM system implemented in FPGA.

be seen that the SEFDM signal has a smaller bandwidth compared with the OFDM signal. Table 2 shows the resource utilization of the FPGA-implemented proposed SEFDM receiver structure in terms of LUTs, FFs, DSP48s and block RAM (BRAM). To have a comprehensive understanding of the computational complexity of the proposed SEFDM receiver, the total numbers of complex multipliers and complex adders in timing synchronization are detailed in Table 3. From Table 3, it is evident that the designed timing synchronization algorithm requires less complex multipliers when compared to the Park algorithm and traditional correlation algorithm.

The implemented BER performance as a function of E_b/N_0 for the proposed SEFDM system in FPGA is shown in Fig. 16. The parameter α is set to 0.9 and 0.8, respectively. It can be seen that the performance gap between the implementation structure and simulation structure is about 0.5 dB, which is caused by the performance loss of analog devices. Compared with the BER performance of the OFDM system, the implemented SEFDM receiver with $\alpha = 0.9$ has a loss of 0.8 dB and the implemented SEFDM receiver with $\alpha = 0.8$ has a loss of 1.2 dB. Nevertheless, the spectrum efficiency gain is 11% and 25%, respectively.

V. CONCLUSION

In this paper, we proposed a low-complexity SEFDM receiver, consisting of synchronization modules and detector design. As for synchronization, a novel two-step SFS is presented and a ZF-SFS algorithm is proposed for the SEFDM system. Then, a low-complexity timing synchronization structure and an SFO based phase recovery structure are proposed to reduce resources cost. The performance of the proposed SEFDM receiver was evaluated by simulations and then implemented in FPGA. It is demonstrated that the proposed SEFDM receiver is able to improve the spectrum efficiency by 25% with about 1.2 dB BER performance loss, which verifies the effectiveness of our proposed SEFDM receiver.

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