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RESEARCH ARTICLE

Origin of Low-Frequency Noise in Si n-MOSFET at Cryogenic Temperatures: The Effect of Interface Quality

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ABSTRACT This study investigates the origin of low-frequency (LF) $1/f$ noise in Si n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs) under cryogenic operation. The fluctuation of the drain current increased with decreasing temperature, exhibiting LF $1/f$ noise of more than two orders of magnitude higher at 2.5 K compared with that at 300 K. As revealed by the temperature dependence of the normalized current spectral density, the LF $1/f$ noise at 2.5 K is primarily governed by carrier number fluctuations. To obtain insight into the carrier trapping centers under cryogenic operation, we investigate the effect of oxide/Si interface states on the LF $1/f$ noise by utilizing Si n-MOSFETs with different surface orientations, i.e., different interface trap densities (D_{it}). The LF $1/f$ noise is comparable between the surface orientations at 300 K, whereas excess noise was observed at 2.5 K for the surface orientation with higher D_{it} in the order of (100)<(120)≤(110)-orientations. This indicates that the LF $1/f$ noise at cryogenic temperatures originates from oxide/Si interface defects and disorders, that is, the interface states and band tail states. These states are localized at the conduction-band edge, which contributes to noise generation as the Fermi level approaches the conduction-band edge at cryogenic temperatures. This study demonstrates the significance of the oxide/Si interface quality in suppressing the LF $1/f$ noise in Si MOS devices operated at cryogenic temperatures.

INDEX TERMS Quantum computer, cryogenic temperature, Si spin qubit, MOSFET, low-frequency 1/f noise, surface orientation, interface states, band tail states.

I. INTRODUCTION

Quantum computers have attracted significant attention because of their faster computation ability compared with classical computers for socially important issues, such as material and chemical calculations, pharmaceutical development, and optimization problems. Among the various types of quantum bits (qubits), Si spin qubits have an advantage in the large-scale integration of qubit due to its compatibility with the Si CMOS manufacturing technology [1], [2], [3].

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To develop a Si quantum computer, the coherence time of the Si spin qubits, that is, the time to maintain their quantum states must be improved. Because quantum states are fragile and easily lose coherence under the influence of various noises, noise elimination is a technological challenge for any type of solid-state qubit. In the case of Si spin qubits, the obvious factor of noise that limits the coherence time is the magnetic noise caused by interactions with nuclear spins in the base material of the quantum dot [4]. Natural Si comprised three stable isotopes, ^{28}Si (92.2 %), ^{29}Si (4.7 %), and ^{30}Si (3.1 %) [5], of which only ^{29}Si has a nuclear spin that causes magnetic noise. An isotopically enriched ^{28}Si wafer to cancel the magnetic noise has been developed [6], [7] and the coherence time of the Si spin qubit has been increased to the millisecond order [8].

In an environment free of magnetic noise realized by isotopically enriched ^{28}Si, the remaining factor limiting the coherence time is the charge noise. Recent experimental studies revealed that the LF $1/f$ noise becomes the exclusive factor of decoherence as charge noise [8], [9]. Thus, the suppression of charge noise in Si spin qubits is crucial and must be addressed to improve the performance of Si quantum computers. However, the validation of the intrinsic source of charge noise using spin-qubit measurements based on isotopically enriched ^{28}Si is challenging and the physical origin of charge noise still remains unclear.

In this study, as a first step to address the noise issue in Si spin qubits, we systematically investigate the source of charge noise in the Si MOS structure. Since the basic unit of Si spin qubit is MOS structure, LF $1/f$ noise generated in Si spin qubits should be also observed in Si MOSFET as a drain current fluctuation under the cryogenic operation. In addition, clarifying the source of charge noise in the Si MOS structure is essential not only for the Si spin qubit but also the cryogenic CMOS circuits for qubit control and readout. Cryogenic CMOS circuits are principally analog or mixed-signal circuits [10]; thus, they are highly susceptible to noise, which is directly linked to errors in quantum calculations. Although numerous experimental studies on LF $1/f$ noise in Si MOSFETs have been reported (for example, ref. [11], [12], [13], [14], [15], [16], [17]), limited studies on the analysis of LF $1/f$ noise at several kelvins or less have been reported [18], [19], [20]. Thus, the generation mechanism of the LF $1/f$ noise at cryogenic temperatures is yet to be fully examined. In this experiment, we characterize the LF $1/f$ noise in Si n-MOSFETs over a wide temperature range from 300 to 2.5 K to understand the effect of temperature on LF $1/f$ noise generation (Section III-A). We investigate the effect of the oxide/Si interface states on the LF $1/f$ noise by utilizing MOSFETs fabricated on Si wafers with different surface orientations exhibiting different D_{it} to identify the physical origin of the LF $1/f$ noise observed at cryogenic temperatures (Section III-B). Compared with the previously published technical digest [21], detailed analytical data on the noise are added and a physical understanding of the increased low-frequency $1/f$ noise at cryogenic temperatures is discussed (Section III-C).

II. EXPERIMENTAL DETAILS

Bulk Si n-MOSFET fabricated on the (100)-oriented wafer (p-type, resistivity 1-5 Ωcm) was used as a test device for noise measurement and analyses in this experiment. A thermally oxidized SiO_2 layer and polysilicon electrode with thicknesses of 6 and 150 nm, respectively, were used as the gate stack (W/L=100/2 μm). The source/drain regions were formed by P^+ implantation and activation annealing at 950°C for 20 s in N_2 ambient. The MOS capacitor fabricated on the same wafer exhibits D_{it} of 4 $\times 10^{10}$ $eV^{-1}cm^{-2}$ (E-E_V = 0.2 eV), which is confirmed by room temperature (RT) capacitance-voltage measurements. The fabricated Si n-MOSFET was wire-bonded to a printed circuit board for cryogenic measurements. Current–voltage (I-V) measurements were conducted using a cryostat (OptistatDry BLV) with a semiconductor parameter analyzer (4200-SCS) equipped with a fast I-V measurement unit.

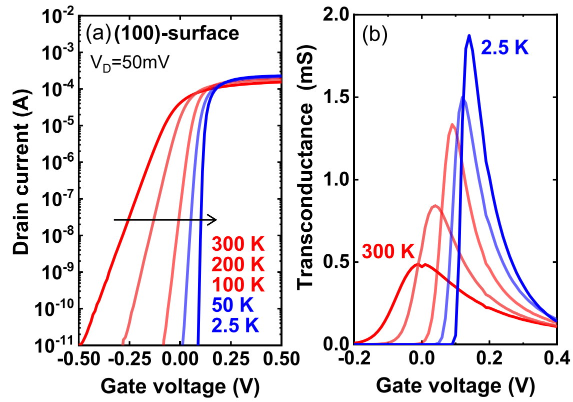


FIGURE 1. (a) I_D-V_G and (b) g_m-V_G characteristics of (100)-oriented Si n-MOSFET at the measurement temperature of 300, 200, 100, 50, 2.5 K (V_D = 50 mV).

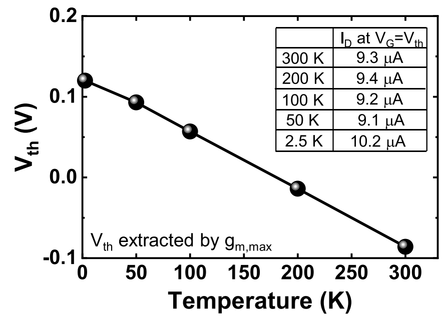


FIGURE 2. Threshold voltage extracted by the $g_{m,max}$ method as a function of temperature. The inset shows the drain current at the gate voltage of V_G = V_{th} at each temperature.

III. RESULTS AND DISCUSSIONS

A. TEMPERATURE DEPENDENCE OF LF 1/f NOISE

The temperature dependence of the drain current-gate voltage (I_D-V_G) characteristics of the (100)-oriented Si n-MOSFET is shown in Fig. 1(a). Well-behaved transfer characteristics were observed from 300 to 2.5 K. The threshold voltage (V_{th}) shifted to the forward voltage by lowering the temperature (Fig. 2). This is the general trend of the V_{th} shift in MOSFET under low-temperature (LT) operation [22], [23], reflecting the increase in the bulk Fermi potential (φ_B) at LT. The on-current increases with decreasing temperature because the carrier mobility increases at LT owing to reduced phonon scattering [24], enhancing the peak transconductance (g_m), as shown in Fig. 1(b). In this study, the noise properties were characterized using the drain current spectral density (S_{ID})

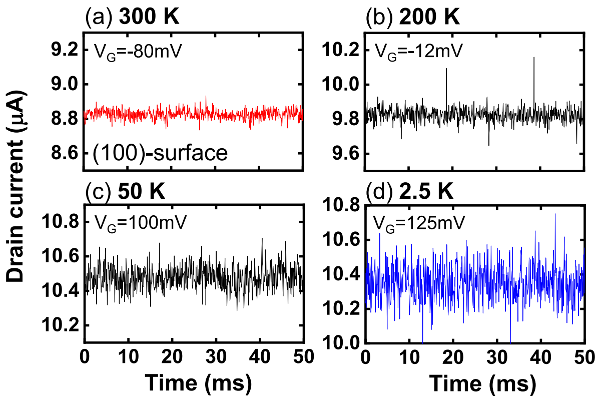


FIGURE 3. Drain current transient of (100)-oriented Si n-MOSFET at a fixed I_D of ∼10 μA at the measurement temperature of (a) 300 K, (b) 200 K, (c) 50 K, and (d) 2.5 K.

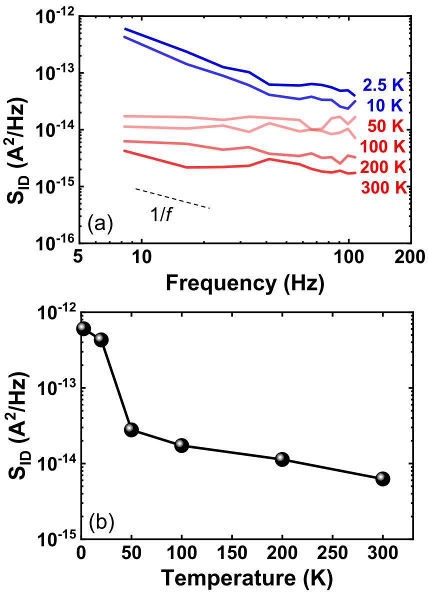


FIGURE 4. (a) S_{ID} of (100)-oriented Si n-MOSFET at measurement temperatures from 300 to 2.5 K with a frequency range of 8 to 100 Hz. (b) S_{ID} as a function of temperature at f = 8 Hz.

from the Fourier transform of the drain current fluctuation. A fixed I_D of ∼10 μA was chosen for current-time (I-t) sampling, which is the drain current under the gate voltage near V_{th} at each temperature (inset in Fig. 2).

The drain current transient of the (100)-oriented Si n-MOSFET at a drain voltage (V_D) of 50 mV is shown in Fig. 3. To avoid the initial excess current response that would be originating from the freeze-out effect at LT [21], [25], I-t sampling commenced after the drain current was sufficiently settled. The drain current fluctuation increased with decreasing temperature and a much larger fluctuation was observed at 2.5 K compared with that at 300 K. The S_{ID} obtained from the I-t sampling in Fig. 3 is shown in Fig. 4(a). The S_{ID} of the Si n-MOSFET increased significantly at temperatures below 50 K, exhibiting an S_{ID} of two orders of magnitude higher at 2.5 K compared with that at 300 K (Fig. 4(b)). The

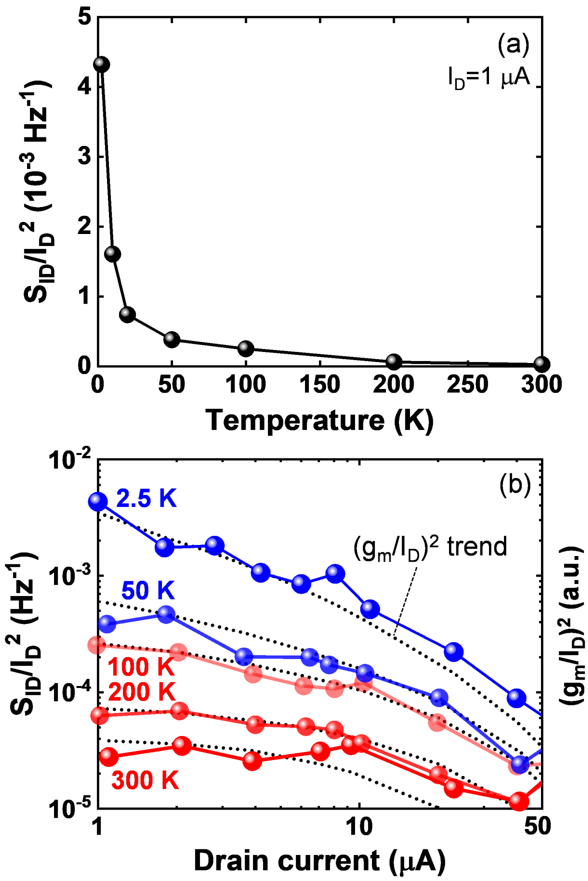


FIGURE 5. (a) Temperature dependence and (b) drain current dependence of the normalized current noise spectral density at measurement temperatures from 300 to 2.5 K at f = 40 Hz. The dotted lines in (b) represent the $(g_m/I_D)^2$ trend at each temperature. The $(g_m/I_D)^2$ trend well fitted to the experimental data, indicating that the carrier number fluctuation is the main mechanism of LF 1/f noise.

observed jump in the LF 1/f noise at LT cannot be explained by the existing MOSFET noise model.

We investigated the normalized current noise spectral density (S_{ID}/I_D^2) to obtain insights into the generation mechanism of the LF 1/f noise at cryogenic temperatures. When noise was generated by the carrier number fluctuation (CNF) caused by tunneling transitions between the channel and trap states, S_{ID}/I_D^2 is expressed as follows, which was modeled by McWorther [26]:

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{FB}} \tag{1}$$

The flatband voltage noise S_{VFB} is given as

$$S_{V_{FB}} = \frac{q^2 kT \lambda N_t}{f^{\gamma} WLC_{ox}^2} \tag{2}$$

where q is the electric charge, k is the Boltzmann constant, T is the temperature, λ is the tunneling attenuation length, N_t is the trap density, f is the frequency, and C_{ox} is the oxide capacitance. In the inversion ($V_G > V_{th}$), S_{ID}/I_D^2 can

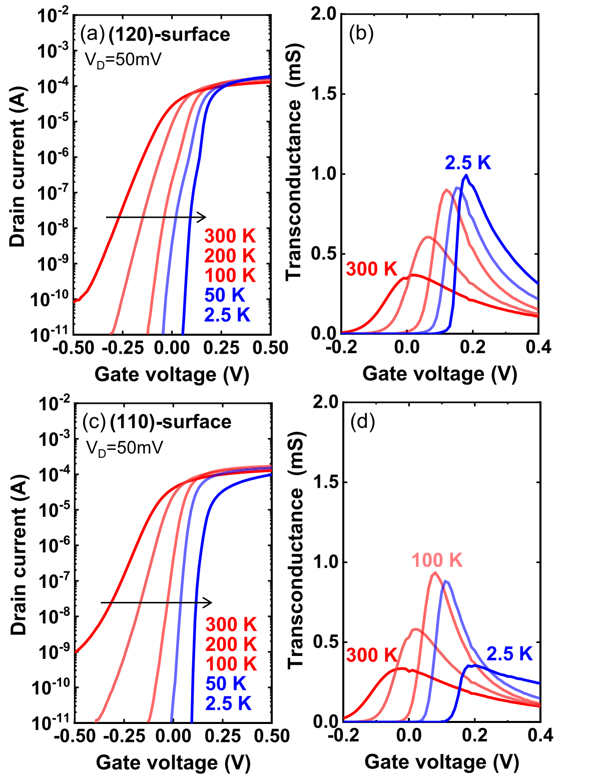


FIGURE 6. (a),(c) I_D-V_G and (b),(d) g_m-V_G characteristics of (120)- and (110)-oriented Si n-MOSFETs with V_D = 50 mV, respectively. Measurement temperatures were 300, 200, 100, 50 K, and 2.5 K.

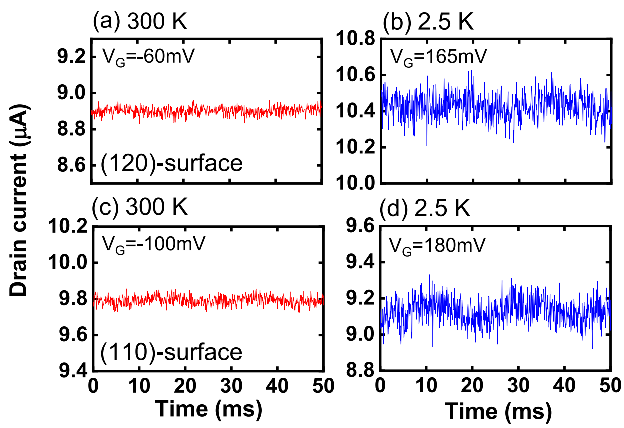


FIGURE 7. Drain current transient of Si n-MOSFETs for (a) (120)-orientated,300 K, (b) (120)-oriented, 2.5 K, (c) (110)-oriented, 300 K, and (d) (110)-oriented, 2.5 K at a fixed I_D of ~10 μA.

be approximated as

$$\frac{S_{I_D}}{I_D^2} = \frac{1}{(V_G - V_{th})^2} \frac{q^2 kT \lambda N_t}{f^{\gamma} WLC_{ox}^2} \tag{3}$$

The improved and generalized trapping noise model combining the CNF with the correlated mobility fluctuation was proposed by Ghibaudo et al., which is modeled as [27], [28]:

$$\frac{S_{I_D}}{I_D^2} = (1 + \alpha_{SC} \mu_{eff} C_{ox} \frac{I_D}{g_m})^2 (\frac{g_m}{I_D})^2 S_{VFB} \tag{4}$$

where α_{SC} is the scattering parameter and μ_{eff} is the effective mobility. S/I_D^2 is proportional to $(g_m/I_D)^2$ when the noise

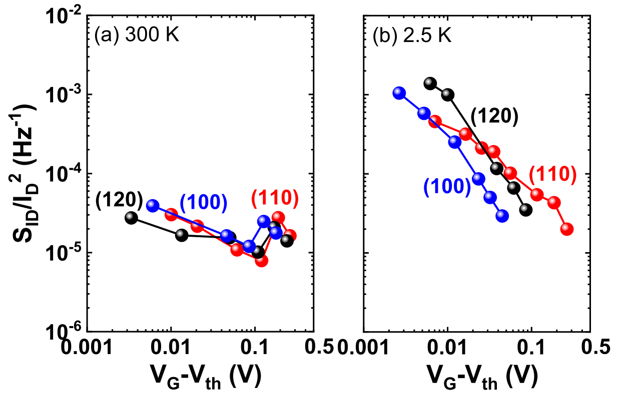


FIGURE 8. Normalized current noise spectral density as a function of gate overdrive voltage for (100)-, (120)-, and (110)-oriented Si n-MOSFETs at temperatures of (a) 300 K and (b) 2.5 K at f = 40 Hz.

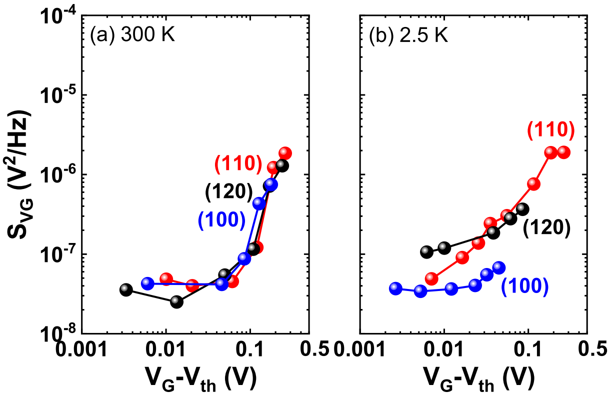
originates from the CNF. S_{ID}/I_D^2 is expressed using Hooge's formula when noise is governed by mobility fluctuation (MF) as follows [29]:

$$\frac{S}{I_D^2} = \frac{q\alpha_H \mu_{eff} V_D}{fL^2 I_D} \tag{5}$$

where α_H is the Hooge parameter. According to Hooge's model, S_{ID}/I_D^2 is inversely proportional to the drain current. Measured S_{ID}/I_D^2 as a function of the temperature is shown in Fig. 5(a). The exponential increase of S_{ID}/I_D^2 with decreasing temperature was observed. Figure 5(b) shows the drain current dependence of S_{ID}/I_D^2 with the temperature from 300 to 2.5 K. The S_{ID}/I_D^2 decreased with increasing drain current and well fitted to the $(g_m/I_D)^2$ trend (dotted line in Fig. 5(b)) below 200 K, implying the generation mechanism of the LF 1/*f* noise at 2.5 K is mainly explained by the CNF model rather than the MF model. The S_{ID}/I_D^2 slightly deviates from the $(g_m/I_D)^2$ trend with increasing drain current (I_D >10 μA), which would be due to the influence of correlated mobility fluctuation. These results indicate that the existence of considerable active trapping centers at cryogenic temperatures.

B. SURFACE ORIENTATION DEPENDENCE OF LF 1/f NOISE

The Possible factors that induce carrier trapping and de-trapping in Si MOS devices are the trap states inside the gate oxide or at the oxide/Si interface. We experimentally examined the impact of oxide/Si interface states on the LF 1/*f* noise to validate the physical origin of the LF 1/*f* noise under cryogenic operation. Thus, we utilized n-MOSFETs fabricated on Si wafers with different surface orientations that exhibited different D_{it} values at the oxide/Si interface. In addition to the (100)-oriented Si n-MOSFET, (120)- and (110)-oriented devices were fabricated using the process described in Section II to obtain different D_{it} values while maintaining the same oxide trap density. The extracted D_{it} values for the (120)- and (110)-oriented devices were 1.2×10^{11} $eV^{-1}cm^{-2}$ and 1.9×10^{11} $eV^{-1}cm^{-2}$, respectively. These are higher than that of the (100)-oriented device (0.4×10^{11} $eV^{-1}cm^{-2}$).



(c)

	(100)	(120)	(110)
300 K	4.2×10^{-8}	5.4×10^{-8}	4.5×10^{-8}
2.5 K	6.7×10^{-8}	1.8×10^{-7}	3.0×10^{-7}

S_{VG} (V^2/Hz) at V_G - V_{th}= 0.05 V

FIGURE 9. Equivalent input referred voltage noise as a function of gate overdrive voltage for (100)-, (120)-, and (110)-oriented Si n-MOSFETs at temperatures of (a) 300 K and (b) 2.5 K at f = 40 Hz. (c) Comparison of S_{VG} with V_G-V_{th} = 0.05 V for 300 K and 2.5 K.

The I_D-V_G and g_m-V_G characteristics of (120)- and (110)-oriented Si n-MOSFETs at temperatures ranging from 300 to 2.5 K are shown in Fig. 6. Below 100 K, the peak g_m differs depending on the surface orientation. g_m increased with decreasing temperatures from 300 to 100 K for all surface orientations; however, the peak g_m at 2.5 K for the (120)-orientation was significantly lower than that for the (100)-orientation. In addition, it turns to decrease below 100 K for the (110)-oriented Si n-MOSFET, which has the highest D_{it}. Therefore, the transfer characteristics of Si n-MOSFETs at cryogenic temperatures are severely influenced by the oxide/Si interface quality, which was also validated by the temperature dependence of the effective carrier mobility [24]. The drain current transients of the (120)- and (110)-oriented Si n-MOSFETs at 300 and 2.5 K are shown in Fig. 7. The drain current fluctuation at 2.5 K increases compared with that at 300 K for both surface orientations as well as (100)-orientation. As seen from the difference in the gate voltage for I-t sampling (V_G = 125 mV, 165 mV, 180 mV for the (100)-, (120)-, and (110)-orientations at an I_D of ∼10 μA), the operating conditions of the MOSFET (that is, weak or moderate inversion) differ depending on the surface orientation. To compare the noise magnitudes, S_{ID}/I_D^2 was plotted as a function of the gate overdrive voltage (Fig. 8). S_{ID}/I_D^2 was comparable at 300 K between the different orientations, indicating a negligible influence of oxide/Si interface states on the LF 1/*f* noise at RT. In contrast, S_{ID}/I_D^2 increases at 2.5 K compared with that at 300 K and varied depending on the surface orientation. The noise magnitude is in the order of (100)<(120)≤(110)-orientation, which is in the order of D_{it}. Further, we compared the noise magnitude with the equivalent input referred voltage noise (S_{VG}). Under the assumption of CNF model, the S_{VG} is given as follows:

$$S_{V_G} = S_{V_{FB}} = \frac{S_{I_D}}{g_m^2} \tag{6}$$

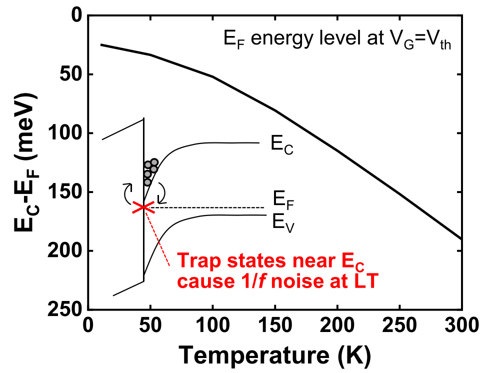


FIGURE 10. Calculated Fermi level from the conduction band edge as a function of temperature (300 to 10 K). The Fermi level becomes closer to the conduction band edge at cryogenic temperatures, which is within 25 meV below 10 K.

The orientation dependence of S_{VG} as a function of the gate overdrive voltage at 300 and 2.5 K are shown in Figs. 9(a) and 9(b), respectively. A weak gate voltage dependence of S_{VG} was observed at the low gate overdrive voltage (V_G-V_{th} <0.05 V), further confirming that the generation mechanism of LF 1/*f* noise in this gate voltage range likely results from CNF rather than MF [27]. Comparing the S_{VG} with the fixed gate overdrive voltage of V_G-V_{th} = 0.05 V, the S_{VG} at 2.5 K increased for the orientation with higher D_{it}, whereas it is comparable at 300 K (Fig. 9(c)). According to the equation (2), the difference in the S_{VG} reflects the number of effective trap density when the CNF model governs the 1/*f* noise. Therefore, the influence of oxide/Si interface states is significant on the noise magnitude under cryogenic operation. Although the influence of correlated mobility fluctuation should be considered for the rigorous derivation of the 1/*f* noise parameters at LT, we can conclude that the oxide/Si interface states are the dominant source of LF 1/*f* noise at cryogenic temperatures.

C. POSSIBLE EXPLANATION OF INCREASED LF 1/f NOISE AT CRYOGENIC TEMPERATURES

The LF 1/*f* noise increased at temperatures below 50 K by more than two orders of magnitude compared with that at 300 K, indicating that the trap states contributing to the drain current fluctuation increased at cryogenic temperatures. Although the energetic distribution and the amount of trap states within the bandgap should be independent of the temperature, the energetic position contributing to the LF 1/*f* noise changes with the temperature. As shown in Fig. 2, V_{th} shifts positively with decreasing temperatures and thus a higher gate voltage is required to obtain a fixed I_D of 10 μA at LT. This means that the Fermi level shifts to the conduction band edge at LT, and the trap states located near the band edge cause the current fluctuation under cryogenic operation. The calculated temperature dependence of the Fermi level at the gate voltage of V_{th} is shown in Fig. 10. The Fermi level position is calculated using the relation E_C-E_F = $E_g/2+\psi_S-\varphi_B$, in which surface potential (ψ_S) equals $2\varphi_B$ at the V_{th}. φ_B was calculated considering bandgap widening and incomplete ionization of the dopant [22] under the assumption of Boltzmann statistics. The Fermi level at 300 K was approximately 200 meV from the conduction band edge and it approached the conduction band edge within 25 meV when the temperature was lowered below 10 K. Generally, defects and disorders at the oxide/Si interface form exponentially increasing states near the band edge as localized interface states and band tail states. These band edge states would be attributed to trapping/de-trapping at cryogenic temperatures because these states are scanned by Fermi level near the threshold. Although the trapping/de-trapping time of band edge states are quite short to be observed at the room temperature measurement, the time constant of trapping/de-trapping increases as the temperature decrease and thus the band edge states behave as the source of low-frequency noise under cryogenic operation. This is also verified by the temperature-dependent random telegraph noise measurement using short channel Si MOSFETs [30]. The band edge states would become crucial under cryogenic operations that are not of concern at RT, also modeled as the physical origin of subthreshold swing saturation at cryogenic temperatures [31], [32].

The shift in the Fermi level and localized states near the conduction band edge are suggested as the physical origins of the increased LF $1/f$ noise in Si MOS devices at cryogenic temperatures. Hence, the oxide/Si interface quality is crucial for the Si spin qubit, which limits the coherence time as a source of charge noise, and for cryogenic CMOS devices for qubit control and readout. Thus, the oxide/Si interface should be carefully controlled to suppress the LF $1/f$ noise, such as the orientation optimization of the Si quantum dot, including the fin sidewall and surface passivation, from the perspective of LT operation to improve the performance of Si quantum computers.

IV. CONCLUSION

This study investigated the origin of LF $1/f$ noise in Si n-MOSFETs at cryogenic temperatures. The drain current fluctuation significantly increased at LT, exhibiting S_{ID} that is two orders of magnitude higher at 2.5 K compared with that at 300 K. The excess LF $1/f$ noise was observed at 2.5 K for the orientation with higher D_{it} by comparing the noise magnitude in Si n-MOSFETs with different surface orientations. This indicates the interface states and band tail states, which are localized near the conduction band edge, are responsible for trapping and de-trapping under cryogenic operation owing to the shift in the Fermi level. This study highlights the importance of oxide/Si interface engineering for Si spin qubits and cryogenic CMOS devices.

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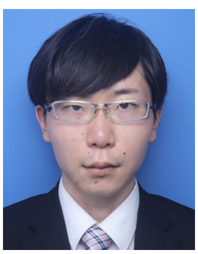

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