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RESEARCH ARTICLE

A Switched-Capacitor Multi-Level Inverter With Variable Voltage Gain Based on Current-Fed Dickson Voltage Multiplier

YOUSEF NIAZI[1], AMIRHOSSEIN RAJAEI[1], (Member, IEEE), VAHID MORADZADEH TEHRANI[1], MOKHTAR SHASADEGHI[1], SALEH MOBAYEN[2], (Senior Member, IEEE), AND PAWEŁSKRUCH[3], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Shiraz University of Technology, Shiraz 71557-13876, Iran
[2]Graduate School of Intelligent Data Science, National Yunlin University of Science and Technology, Douliou, Yunlin 640301, Taiwan
[3]Department of Automatic Control and Robotics, AGH University of Science and Technology, 30-059 Kraków, Poland

Corresponding author: Saleh Mobayen (mobayens@yuntech.edu.tw)

ABSTRACT A voltage boost switched-capacitor multi-level inverter (SCMLI) structure is planned which is able to control the voltage gain. The structure is based on Current-fed Dickson Voltage Multiplier (CFDVM). The CFDVM at the input stage limits the capacitor peak current and increases the voltage gain compared to other SCMLIs. Furthermore, high frequency operation significantly reduces the size of capacitors. The other main advantage is the same output impedance at all the voltage levels due to similar capacitor values and output current path. Selective Harmonic Elimination (SHE) technique is applied to improve output power quality. The operation principles and modulation strategy are described and the converter relations are derived. Also, the relations for component selection, capacitor voltage ripple and system efficiency are included. Comparative research of the suggested converter with similar state of the art converters is provided which shows that the proposed SCMLI has fewer power switches, gate drivers, and voltage sources. Furthermore, analysis of the cost function shows the economic nature of the proposed SCMLI. A 13-level laboratory prototype is built to verify the effectiveness of the suggested SCMLI.

INDEX TERMS Multi-level inverter, switched-capacitor converter, Dickson voltage multiplier.

I. INTRODUCTION

Nowadays, inverters are extensively used in various industries and renewable resources, for instance, solar, wind, and fuel cell systems [1], [2], [3]. However, increasing limited voltage and generating a near sinusoidal waveform are two significant challenges. A common solution is incorporating a transformer, but it increases the size and cost and reduces efficiency [4], [5], [6]. To address these challenges, researchers have proposed Multi-Level Inverters (MLIs), which can operate at higher power levels, lower THD, lower Electromagnetic Interference (EMI), lower dv/dt stress on devices, lower output filter size, lower power losses, and higher efficiency compared to two-level inverters [1], [7], [8], [9].

Conventional MLIs are classified into three chief groups, Neutral point clamps (NPC), Flying capacitor (FC), Cascade H-bridge (CHB), which are used for specific applications [2]. However, they require numerous components and lack inherent voltage boost capability [10], [11]. To overcome these limitations, researchers have proposed new MLIs with fewer components based on reduced device count (RDC) [8], [12], less voltage stress on the devices by using an H-bridge at the output stage [13], improved efficiency and simplified control strategy [14]. A comprehensive study of MLIs with reduced device counts and different categories is provided in [15]. Moreover, to improve the voltage gain of conventional MLIs,

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auxiliary circuits (front-end boost converters or impedance networks) are added to these converters [16]. However, these methods increase the converter's cost and size as well as its overall complexity [8], [17].

Switched-capacitor (SC) multi-level inverters are proposed as a solution to address the mentioned problems for conventional MLIs and reduced device count methods [18], [19]. These inverters use capacitors as a substitute for DC voltage sources and have advantages such as high-power density and high voltage gain. SCMLIs require fewer components and don't need auxiliary circuits for capacitor voltage balancing [1], [14]. However, they have high voltage stress on the components, particularly in high voltage applications, and input current spikes [10]. Solutions such as increasing the frequency [20], using limiting resistance and small inductance simultaneously in the charging path of the capacitor [21], [22], or operating power switches in the linear mode [23] and quasi-resonant inductances [24] have been proposed to address these challenges. In order to increase the voltage gain and produce different voltage levels in SCMLIs, the capacitors are placed in series, which causes unequal output impedance for different voltage levels [11]. Moreover, in most of SCMLIs, the capacitors are charged with the fundamental frequency of the inverter, which requires bulky capacitors and causes high voltage ripple [7]. Rapid charging of the capacitors also makes it hard to control the capacitor's voltage level and consequently the output voltage. Therefore, the output voltage control is accomplished by the modulation index (m_a), which can't generate some voltage levels at low modulation indexes [4], [25].

SCMLIs have many practical applications, such as battery charge stabilization, high voltage gain converters, renewable energy systems, fuel cells, energy harvesting, Internet of Things (IoT) systems, and electric cars (EVs) [18], [19]. However, there is still room for improvement in terms of reducing voltage stress on components, reducing input current spikes, and improving voltage gain and output voltage control.

This study proposes a new SCMLI structure according to the Current-fed Dickson Voltage Multiplier (CFDVM). The CFDVM at the input stage limits the capacitors peak current and increases the voltage gain compared to [7] and [9]. Unlike previously proposed structures that use modulation index or output voltage levels to control the output voltage peak and RMS, the proposed structure can control the output voltage using duty cycle of boost converter based on the gain equation. Therefore, it can operate at a constant modulation index and output voltage levels. Hence, the control strategy is simplified and THD is improved. Furthermore, operating with high frequency which is independent to the fundamental frequency of the inverter, significantly reduces capacitors voltage ripple. So, the proposed SCMLI incorporates small capacitors compared to similar structures, while maintaining lower voltage ripple. Nevertheless, in the proposed SCMLI each voltage level is produced by an independent capacitor, and no series connection is needed to step-up the voltage. Therefore, the proposed structure has the same output impedance in all voltage levels due to equality in capacitors value and output current path. Thus, the output voltage regulation is improved because of the lower output impedance and faster capacitor discharge time. Additionally, by using Selective Harmonics Elimination (SHE) modulation method and being multi-level, higher frequency harmonics were removed and therefore THD is further improved.

The paper is formed in the subsequent manner: Section II provides details regarding the structure and principles of operation, accompanied by key waveforms, major relationships, and an efficiency analysis. In Section III, a comparison is made between the recommended architecture and top converter topologies currently in use. Section IV involves the validation of theoretical concepts by conducting experiments using a laboratory prototype.

II. CONFIGURATION AND OPERATING PRINCIPAL OF THE PLANNED SC-CONVERTER

The generalized structure of a k-stage CF-DVM is illustrated in Fig.1. Accordingly, the input voltage source (V_{in}), inductor (L), and the switch (Q), Diode D_1 and Capacitor C_1 forms a boost converter at the input stage, and each stage of the DVM consists of two diodes and two capacitors. For better understanding, the detailed steady-state analytical waveforms of a one-stage CF-DVM are exposed in Fig. 2 and the current paths are clearly shown in equivalent circuit of Fig. 3. According to the waveforms, three operating modes are identified in the converter at every switching period as discussed below. In order to simplify the analysis, it is supposed that all capacitors are large enough and their voltage ripple are neglected. Furthermore, all elements are considered as ideal.

*Mode*1: In this mode as shown in Fig. 3 (a), Q is ON. So, the voltage across L is positive; therefore, its current (iL) increases. Simultaneously, C_1 and C_2 are in series. Hence, C_2 is charged by C_1. Meanwhile, C_3 discharge current provides the load current. This mode lasts as long as D_2 is forward-biased.

*Mode*2: In this mode as shown in Fig. 3 (b), Q is still ON and the inductor is still being charged. All diodes are reversed-biased. Thus, C_1 and C_2 are floating and their voltage remain constant. Furthermore, the load is supplied through C_3.

Mode 3: In this mode as illustrated in Fig. 3 (c), Q is OFF. The inductor is discharged with the source to the load and its

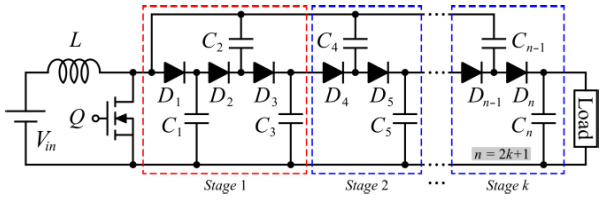

FIGURE 1. The generalized structure of CF-DVM.

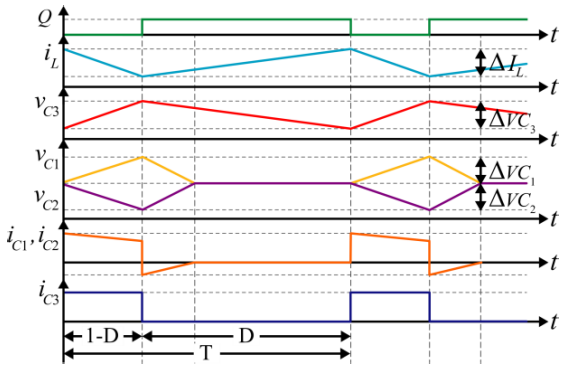

FIGURE 2. Steady state waveforms of basic CF-DVM converter.

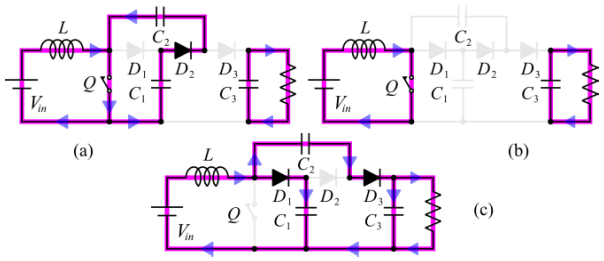

FIGURE 3. Different operating modes of basic CF-DVM converter (a) mode 1, (b) mode 2, (c) mode 3.

current decreases. Also, the stored energy in C_2 is delivered to C_3 and C_1 is charged through D_1.

According to [26], the voltage equations for C_1 and C_3 are denoted by:

$$\begin{cases} V_{c1} = \dfrac{V_{in}}{(1-D)} \\ V_{c3} = v_{out} = \dfrac{2V_{in}}{(1-D)} \end{cases} \tag{1}$$

where $\boldsymbol{D}$ is the duty cycle of Q. Also, the inductor current equation is given by:

$$i_{in} = i_L = \frac{2v_{out}}{R\,(1-D)} \tag{2}$$

The voltage and current ripple are given by:

$$\begin{cases} \Delta i_L = \dfrac{(v_{in} - v_{C1})(1-D)}{Lf} \\ \Delta v_c = \dfrac{v_{C3}D}{RCf} \end{cases} \tag{3}$$

using (3), inductor value can be obtained as:

$$L = \frac{(v_{in} - v_{C1})(1-D)}{f\,\Delta i_L} \tag{4}$$

The odd-index capacitors in the generalized structure of CF-DVM can act as voltage sources with different voltage levels and their voltage equation is given by (5). Also the maximum voltage stress of the capacitors are given by (5) and (6) for odd and even capacitors respectively. Accordingly, voltage levels of C_1 and C_5 are $\boldsymbol{V_{C1} = V_{in}/(1-D)}$ and $\boldsymbol{V_{C5} = 3V_{in}/(1-D)}$, respectively.

$$V_{cn} = \frac{n+1}{2}\frac{V_{in}}{(1-D)} = \frac{n+1}{2}V_{cc} \tag{5}$$

$$V_{cn} = \frac{n+2}{2}\frac{V_{in}}{(1-D)} = \frac{n+2}{2}V_{cc} \tag{6}$$

where $\boldsymbol{n}$ is the index number of capacitors. Also, the voltage gain equation is given by:

$$Gain = \frac{n+1}{2}\frac{V_{in}}{(1-D)} \tag{7}$$

where $\boldsymbol{n}$ is the index of odd capacitors.

A. THE PLANNED SCMLI

The generalized structure of the suggested SCMLI is shown in Fig. 4. Accordingly, by extending the structure to five-stages as exposed in Fig. 5, the suggested converter studied in this paper is achieved. The voltage of each odd capacitor with respect to the input voltage can be calculated by (5). For instance, the voltage at the final stage is $6V_{in}/(1-D)$. The purpose of the H-bridge used at the output is to generate an alternative waveform with $2k+3$ voltage levels, where k is the number of stages. Moreover, the output voltage waveform of the proposed SMLI is demonstrated in Fig. 6. Accordingly, by using a five-stage converter, a 13-level waveform can be obtained. In the operation of the converter Q operates at a high frequency with a constant duty cycle and charges the capacitors. The operation of Q is

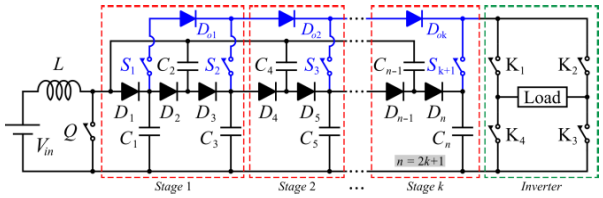

FIGURE 4. The generalized structure of the planned SCMLI.

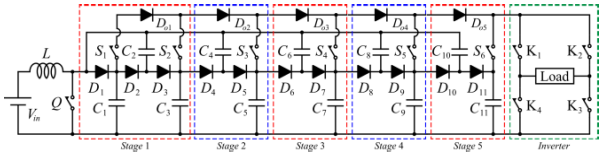

FIGURE 5. Structure of the proposed 5-stage SCMLI.

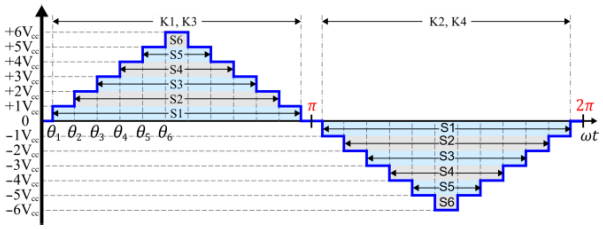

FIGURE 6. Output waveform of 13 level SCMLI.

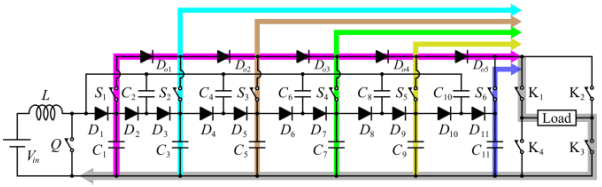

FIGURE 7. Modes of operation for SC-MLI.

completely independent to the output frequency or voltage level of the inverter. However, by adjusting the duty cycle, the output peak voltage and RMS can be controlled. Therefore, modulation index of the inverter is considered constant to achieve the lowest THD and simplify the control strategy.

Furthermore, to generate zero-voltage at the output, switches $S_1 - S_6$ as well as the inverter switches $K_1 - K_4$ needs to be turned OFF. Furthermore, to generate voltage levels of $(\pm i \times V_{in}/(1-D))$, only the corresponding switch $(S_1 - S_6)$ needs to be turned ON as shown in Fig. 7. Therefore, only one of the odd capacitors supplies the load. Hence, the output impedance remains constant for all voltage levels. It is mentioned that in the non-zero voltage levels, the inverter controls the output voltage polarity. Therefore, an alternative waveform can be generated.

B. VOLTAGE RIPPLE AND OPTIMAL SIZE OF THE CAPACITOR

In SCMLIs, the capacitor size is calculated based on the desired output voltage ripple that, depends on operating frequency, maximum output current and maximum discharge time. However, there are limitations such as cost, size and losses of the capacitors. For simplifying the calculations, voltage ripple of the capacitor with the slowest discharge time is considered to calculate the desired capacitor value.

Accordingly, the voltage ripple of the capacitor with the slowest discharge time is calculated as follows:

$$\Delta v_i = \frac{1}{c_i}\int_{t_1}^{t_2} i_{oi} dt \tag{8}$$

where t_1 and t_2 are the start and end time of capacitor discharge interval. In the proposed topology, each capacitor is discharged in the $[0 - \pi/2]$ interval and supplies the output load. Therefore, the voltage ripple for each capacitor is considered as follows:

$$\Delta v_i = \frac{vc_i}{16 f_1 R c_i}(2\theta_i) = \frac{vc_i\,(2\theta_i)}{16 \times 2 f_o R_o c_i} \tag{9}$$

where i is the capacitor number, θ_i is the conduction angle of the corresponding capacitor, R_0 is the output resistance and f_1 is the half cycle of the fundamental frequency $(f_1 = 2f_0)$. Accordingly, it is concluded that the voltage ripple is inversely proportional to the capacitor value. Therefore, the maximum charge of the capacitor is given by:

$$Q_i = \frac{vc_i\,(\theta_i)}{16 f_o R_0} \tag{10}$$

Considering the voltage ripple as a coefficient of the capacitor voltage, then equation can further be expressed as:

$$\Delta \mathrm{v_i} = \mathrm{K} V c_i \tag{11}$$

where K is a coefficient between $[0 - 1]$. Therefore, using the following relationship, the optimal capacitor value is obtained:

$$C_{opt} \geq \frac{Q_i}{KVc_i} \tag{12}$$

C. MODULATION STRATEGY

Various modulation methods used in multi-level inverters (MLIs) to achieve a sinusoidal waveform. Two common types of modulation methods are High Frequency Modulation (HFM) and Fundamental Frequency Modulation (FFM), but the latter is preferred due to its efficiency. The Selective Harmonic Elimination (SHE) approach is employed in this paper to eliminate harmonics and provide a near sinusoidal output voltage. Model techniques significantly affect the dynamic behavior, THD, switching losses, cost, and size of the filter in MLIs. For a staircase waveform with x number of steps, the Fourier transform is written as follows:

$$v(w,t) = \frac{4v_{in}}{\pi}\sum_k [\cos(k\theta_1) + \cos(k\theta_2) + \ldots + cos(k\theta_x)]\frac{sin(kwt)}{k} \tag{13}$$

where $k = 1, 3, 5, 7, \ldots$ are the odd numbers. $\theta_1, \theta_2, \ldots, \theta_x$ are the conducting angles for each voltage level. The overall (main) content and the maximum achievable amplitude can be obtained from the following relations:

$$v_1(w,t) = \frac{4v_{in}}{\pi}\sum_z [cos(\theta_1) + cos(\theta_2) + \ldots + cos(\theta_x)]sin(kwt) \tag{14}$$

$$V_{1max} = \frac{4x}{\pi}V_{in} \tag{15}$$

The idea of the SHE technique is to correctly calculate the conducting angles θ_1 to θ_x to eliminate the selected harmonics. Therefore:

$$cos(m\theta_1) + cos(m\theta_2) + \ldots + cos(m\theta_x) = 0 \tag{16}$$

where m is the selected harmonic number.

Considering the value of the modulation of $m_a = v_1/V_{max}$, where v_1 is the intended output voltage. Also, using the conducting angles θ_1 to $\theta_x, x - 1$ high order harmonics of the output voltage can be removed. Therefore, according to the proposed inverter with 13 levels, the 3rd, 5th, 7th, 11th, and 13th harmonics can be removed. The equations are as follows:

$$\begin{aligned} &cos(\theta_1) + cos(\theta_2) + cos(\theta_3) + cos(\theta_4) + cos(\theta_5) + cos(\theta_6) = 6m_a \\ &cos(3\theta_1) + cos(3\theta_2) + \ldots + cos(3\theta_6) = 0 \\ &\ldots \quad \ldots \quad \ldots \quad \ldots = 0 \\ &cos(13\theta_1) + cos(13\theta_2) + \ldots + cos(13\theta_6) = 0 \end{aligned} \tag{17}$$

Eventually, for different modulation coefficient of m_a, different conducting angles can be obtained. THD is calculated based on the following equation [14]:

$$THD = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1} = \sqrt{\sum_{n=3,5,7,11,13,\ldots} \left(\frac{V_{rms}}{V_{1rms}}\right)^2} \tag{18}$$

D. LOSS CALCULATIONS

1) SWITCHING LOSSES FOR DIODES AND SWITCHES

As a result of the non-ideality of the power switch and the presence of a delay in turning on or off completely, the voltage and current waveforms overlap in the transient time. This leads to switching losses. The equations for calculating switching losses for all switches and diodes of the suggested converter are described in this subsection.

a: SWITCHING LOSSES OF DVM

The switch (Q) operates at high frequency and has higher switching losses compared to other switches. switching losses are as follow:

$$\begin{aligned} P_{sw.son} &= \frac{1}{6} f_s v_{sw} I_{sw} t_{on} \\ P_{sw.soff} &= \frac{1}{6} f_s v_{sw} I_{sw} t_{off} \\ P_{sw.s} &= P_{sw.son} + P_{sw.soff} \end{aligned} \tag{19}$$

b: SWITCHING LOSSES OF H-BRIDGE

The H-bridge includes four switches that turn on and off in pairs once per every 50Hz cycle. Therefore, we have:

$$\begin{aligned} P_{sw.Hon} &= 4[\frac{1}{6} f_o v_{sw} I_{sw} t_{on}] \\ P_{sw.Hoff} &= 4[\frac{1}{6} f_o v_{sw} I_{sw} t_{off}] \\ P_{swH} &= P_{sw.Hon} + P_{sw.Hoff} \end{aligned} \tag{20}$$

c: SWITCHING LOSSES OF STAIRCASE SWITCHES OF INVERTER

The six switches are used to make output voltage levels. The operating frequency of these switches is twice of the main frequency. Equations For these switches are given by:

$$\begin{aligned} P_{sw.Qon} &= 12\left[\frac{1}{6} f_o v_{sw} I_{sw} t_{on}\right] = \sum_{i=1}^{6} \frac{2}{6} v_{si} I_i t_{on} f_f \\ P_{sw.Qoff} &= 12\left[\frac{1}{6} f_o v_{sw} I_{sw} t_{off}\right] = \sum_{i=1}^{6} \frac{2}{6} v_{si} I_i t_{off} f_f \\ P_{swQ} &= P_{swQon} + P_{sw.Qoff} \end{aligned} \tag{21}$$

Also, switching losses for diodes are obtained from the following equation:

$$\begin{aligned} P_{SWD} &= \sum_{i=1}^{n} \frac{Q_{rr} V_{rri}}{T_i} \\ P_{swv} &= P_{sw-s} + P_{sw-H+} P_{sw-Q} + P_{sw-D} \end{aligned} \tag{22}$$

E. CONDUCTIVE LOSSES OF SWITCHES AND DIODES

For a 13-level inverter, there are 11 switches and 16 diodes in the circuit. Therefore, conduction losses are given by:

$$\begin{aligned} P_{con-sw} &= \sum_{i=1}^{11} R_{ons} I_{swi}^2 \\ P_{con-D} &= \sum_{i=1}^{n} r_{don} I_{Di}^2 \\ P_{con-tot} &= P_{con-sw} + P_{con-D} \end{aligned} \tag{23}$$

F. TOTAL STANDING VOLTAGE (TSV) CALCULATION

The total maximum voltage stress applied on the switches is called TSV. Also, it's per unit value is defined as follows:

$$\begin{aligned} TSV &= \sum_{k=1}^{N_s} V_{block(k)} \\ TSV_{pu} &= \frac{TSV}{V_{block}(max)} \end{aligned} \tag{24}$$

where N_s is the total number of converter switches and $V_{block(k)}$ is the blocking voltage of k_{th} switch. For the proposed converter, the TSV value is calculated from the following equation:

$$\begin{cases} TSV = 1 + 4\,(j+2) + \sum_{i=1}^{j+2} i \\ TSV_{pu} = \dfrac{TSV}{(j+2)\,V_{in}} \end{cases} \tag{25}$$

where, j is the number of steps added to the converter as a voltage booster. For the proposed converter with 13 levels, the number of steps is $j = 4$ and the TSV value is as follows:

$$\begin{cases} TSV = 1 + 4\,(4+2) + \sum_{i=1}^{4+2} i = 46 \\ TSV_{pu} = \dfrac{TSV}{(j+2)\,V_{in}} = \dfrac{46}{6} = 7.6 \end{cases} \tag{26}$$

III. COMPARATIVE STUDY

Recently, various MLI topologies based on SC structures have been introduced. These structures focus on increasing voltage gain and self-balance voltage of the capacitors. In order to prove the merits of the planned SCMLI, a complete comparison with other existing structures, with symmetrical voltage sources, in terms of components count, TSV and voltage gain is done. Because under study topologies do not have the same voltage gain and output voltage levels, a comparative cost study according to the cost function (CF), boost factor (B) and the function ($CF/(N_l * B)$) was considered to evaluate SCMLIs. The relationships related to the cost

TABLE 1. Number of components in numeric in symmetric way.

Reference	N_l	N_{DC}	N_{sw}	N_{Diode}	N_{cap}	N_{dri}	TSV_{pu}	$CF/B*N_l$		*Gain*
								α=0.5	α=1.5	
[5]	13	2	14	2	4	14	6	1.89	2.2	3
[6]	13	2	16	2	4	16	5.6	2.09	2.37	6
[8]	9	1	10	2	2	10	4.5	1.45	1.7	2
[4]	13	3	18	3	3	18	5	5.13	5.71	2
[29]	13	3	18	6	6	18	4	5.76	6.23	2
[28]	13	3	21	12	6	21	4.5	7.18	7.7	2
[30]	13	2	16	4	4	16	5.3	2.18	2.45	3
[31]	13	2	20	0	6	16	5.3	4.57	5.12	1.5
[32]	17	4	20	4	4	20	5	5.94	6.52	2
[33]	13	2	14	4	4	14	5.3	1.48	1.69	4
[34]	17	2	18	2	4	14	5	2.38	2.67	2
Pro	**13**	**1**	**11**	**11**	**11**	**11**	**7.6**	**0.33**	**0.38**	**12**

TABLE 2. The comparative study of proposed converter with other topologies.

parameters	[5]	[6]	[8]	[4]	[29]	[28]	[30]	[31]	[32]	[33]	[34]	pro
Capacitor voltage stress	Vin	Vin	Vin/ 2	Vin	Vin	Vin	Vin	Vin	2Vin	Vin	Vin/ 2	$\frac{n+1}{2}v_{cc}$
Capacitor voltage ripple	21.1	20.3	5	33	5	1.75	7.3	1-5	16	8	5	1.3
Voltage booster	high-fix	Low-fix	Low-fix	Low-fix	Low-fix	Low-fix	Low-fix	Low -fix	Low-fix	Med-fix	Low -fix	High-Vari
Output impedance	Vari	Vari	Vari	Vari	Vari	Vari	Vari	Vari	Vari	Vari	Vari	CNST
Control of spike current	no	no	no	no	no	no	no	no	no	no	no	yes
Charging frequency (Hz)	50	50	50	50	50	50	400	50	50	50	50	50000
Efficiency	92.1E	91.E	97.1 E	NA	97T 94E	NA	97.1T 95E	NA	90T 87E	NA	95E	98.2T
Capacity(uF)	2500	2500	1700	2200	4700	4700	470	2200 4400	1800	1870	1000	200
Input voltage	30	10 40	100	9.2 46	180 90	120	48	100	50 150	50	150	10
Output voltage control	ma	ma	ma	no	no	no	no	ma	no	no	no	duty cycle

***(NA)NotAvailable,(T)Theoretical,(E)Experimental,(ma)modulation index, (Vari) variable,(CNST)constant,(Med)medium**

function are as follows:

$$CF = \left(N_{sw} + N_{dr} + N_{cap} + N_{diode} + \alpha TSV\right) N_{DC}$$
$$B = \frac{V_{omax}}{\sum_{i=1}^{N_{DC}} V_{ini}} \tag{27}$$

where α is the weighting coefficient of TSV that $\alpha = 0.5$ and $\alpha = 1.5$ are considered for it. TABLE 1 illustrates comparative analysis of the suggested converter's components along with the compared converters.

As shown in TABLE 1, in term of input sources, switches and gate drives, the proposed converter has the minimum number of components compared to other structures. Only in [10], the number of sources is the same and also the switches and drives are fewer than the proposed converter, but it produces 9 levels. Furthermore, the proposed SCMLI incorporates more capacitors compared to other structures. The comparative study of the performance of the proposed converter is presented in TABLE 2. Based on TABLE 2, the capacitors are significantly smaller in value compared to similar structures, while maintaining lower voltage ripple by using high frequency modulation. Also, in TABLE 1 the value of TSV for the suggested converter is relatively higher than the others, but is in the range of other converters. Compared to converters with H bridge [2], [5], [27], [28], [29] it has the same voltage stress of switches that are equal to the output voltage. However, the number of diodes in the suggested converter are more than other converters except [30]. The voltage stress of all diodes is equal to the output voltage of the boost converter stage (V_{cc}). In addition, similar to other converters, the proposed converter is also capable to work with inductive-resistive ($R-L$) loads.

Accordingly, as depicted in TABLE 2, the proposed converter has the lowest voltage ripple as well as the smallest capacitor size. Furthermore, as show in Fig. 8 the proposed converter has controllable and the highest voltage gain among competitors which, can effectively attenuating input voltage fluctuations and output load variations. Furthermore, by investigating the cost function compared to other comparative converters, it was found that the proposed converter has much lower values for different weighting coefficients (α). For example, in [10] of TABLE 1, for $\alpha = 0.5$, the value of $CF/(N_l * B)$ is equal to $W = 1.45$ and for the proposed

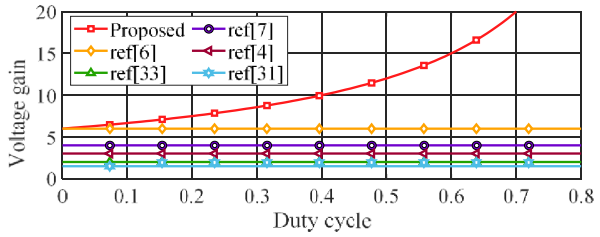

FIGURE 8. Gain vs duty cycle.

converter it is equal to $W = 0.33$. As it is clear, the proposed converter has significant advantages over other compared converters.

Additionally, Based on TABLE 2, the proposed converter can damp the current spikes of the input source by the inductor of boost stage, reduce EMI and increase the lifetime of capacitors. However, it is evident that the capacitor voltage stress for the proposed converter will increase with an increase in voltage levels. Unlike other structures that use series connection of capacitors to enhance the voltage gain, the suggested structure provides the output power of each level from one separate capacitor. Therefore, it has the same output impedance in all voltage levels due to equality in capacitors value and output current path. Moreover, by reducing switching states number, it is possible to use switches with low operating frequency and very low on resistance (r_{on}) and as a result achieve lower losses. Furthermore, it is possible to control the output voltage level even with a constant modulation coefficient (m_a) and maintain all the voltage levels even in desired low output voltages. The voltage stress of the high-frequency switch (Q) is equal to V_{cc}, the voltage stress of the bridge switches are equal to the output voltage, and the voltage stress of the multilevel switches are equal to $m * V_{cc}$, where m is the index number of MLI switches ($S_1 - S_6$).

IV. EXPERIMENTAL RESULTS

In this section, to confirm and evaluate the performance of the planned converter, a laboratory prototype with 13 levels for battery voltage level application is established. The practical setup system is shown in Fig. 9. Main parameters of the planned converter are exposed in Table 3. Accordingly, the value of the capacitors is chosen as $200\mu F$. For the modulation technique, the SHE method has been used with a 70% modulation index (m_a). The output frequency of inverter has been selected to be $50Hz$ and the boost converter's switching frequency as $50kHz$. The operating angles of voltage levels for different modulation coefficients (m_a) are given in Table 4. With selected modulation coefficient 70% for experimental test, the operation angles and the states of switches has been obtained according to Table 4. The output voltage waveform with duty cycle changes at constant ma are shown in Fig. 10.

A. RESISTIVE WITH LOW INDUCTANCE LOAD

As the output load, a resistive load $R = 83\Omega$ with low inductance ($3mH$) is selected. The waveforms of the input source

TABLE 3. Parameters of the converter prototype.

Parameters	Value
Input voltage	$V_{in} = 10$ V
Duty cycle	D = 0.66 – 0.68
Gain ratio	n=17
Capacitor	$C = 200$ µF
Switching frequency	$f_{sw} = 50$ kHz
Output frequency	$f_{out} = 50$ Hz
Output power	$P_{out} = 150$ W
Diode forward voltage	$V_f = 0.15$ V
Internal resistance of diode	$r_{on} = 0.03\ \Omega$
On-state resistance of MOSFET	$R_{on} = 0.005\ \Omega$

TABLE 4. Switching angles (degree).

θ / m_a	θ_1°	θ_2°	θ_3°	θ_4°	θ_5°	θ_6°
0.4	23.28	27.64	47.09	51.11	71.91	82.08
0.7	21.92	28.25	44.62	56.54	68.95	84.54
0.8	20.44	28.39	41.76	57.23	65.29	87.04

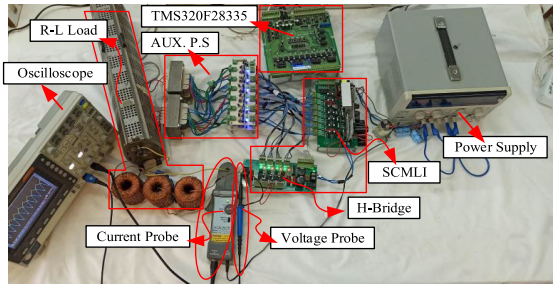

FIGURE 9. The experimental setup for proposed SCMLI.

and inductor voltage and current are illustrated in Fig. 11(a) and Fig. 11(b), correspondingly. The waveform related to the voltage ripple of the capacitors are shown in Fig. 11(c)-(h) for odd capacitors $C_1 - C_{11}$ respectively. The voltage ripple for C_1=0.33V and a maximum ripple value is for C_9=1.9V. The maximum voltage ripple of capacitors has been calculated less than 1.33%. Also, the current and voltage stresses for switches and diodes are illustrated in Fig. 12. In Fig. 12(a) the voltage and current of switch (Q) are shown and in Fig. 12(b)-(d) current and voltage of diodes D_1, D_{11} and D_{16} is depicted respectively. The results of intermediate switches (S_1) and (S_6) prove the theoretical and simulation waveforms as well as the waveforms of high and low side of H-bridge switches. These waveforms are exposed in Fig. 13(a) to Fig. 13(d), respectively. In Fig. 14(a), the converter output voltage is shown and the RMS voltage is equal to 109 volts, which the simulation results obtained in $110V$.

According to the FFT analysis of output voltage, the THD value is equal to 7% and, the value of the output current that shown in Fig. 14(a), is equal to 5%.

The Theoretical efficiency versus output power is illustrated in Fig. 15(a). Accordingly, the proposed converter

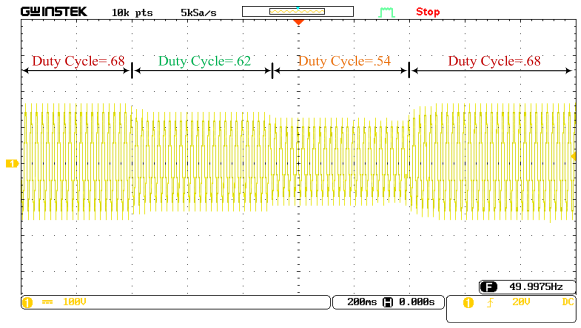

FIGURE 10. The output voltage for different values of duty cycle.

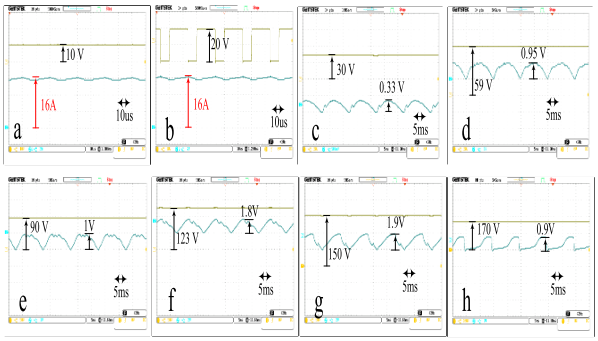

FIGURE 11. Experimental results for presented converter: (a) input voltage and current, (b) inductor voltage and current, (c-h) output voltage and ripple of odd capacitors.

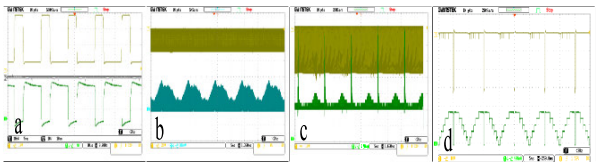

FIGURE 12. Experimental results of (a) the voltage and current of switch (Q), (b-d) current and voltage of diodes D_1, D_{11} and D_{16} correspondingly.

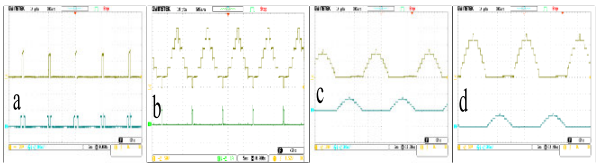

FIGURE 13. Experimental results for voltage and current of intermediate switches: (a) S_1, (b) S_6, (c-d) high and low side of H-bridge switches.

has 98.2% efficiency at light loads and 96.49% efficiency at 150W load.

Power losses versus output power have been calculated and depicted in Fig. 15(b). From Fig. 11(a), input current is continuous and have a small ripple. In addition, by changing the duty cycle of the boost converter, the output voltage level is changed without reducing the number of levels and keeping the value of the (m_a) constant.

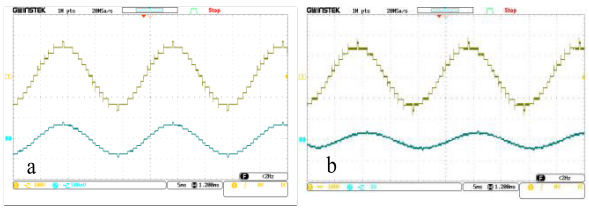

FIGURE 14. Experimental results for Output voltage and current of the converter: (a) resistive with low inductance load, (b) resistive-inductive (R-L) load.

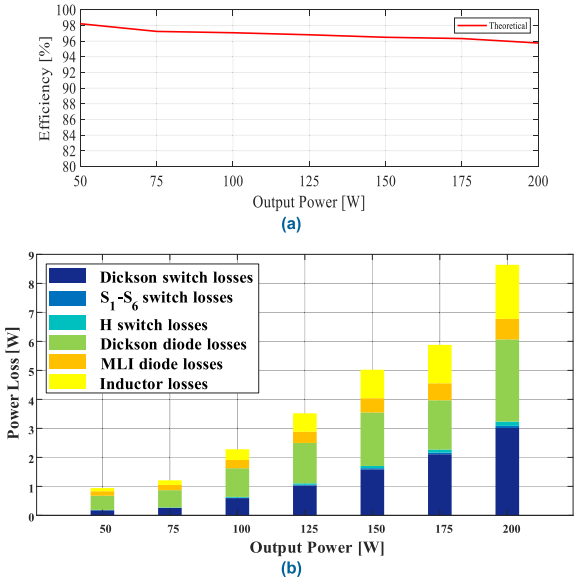

FIGURE 15. The diagram (a) efficiency versus output power (b) converter loss at different output power.

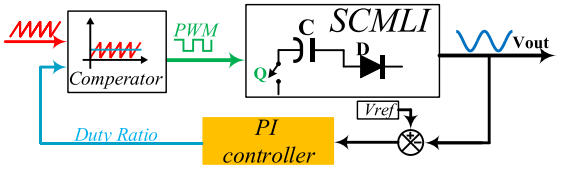

FIGURE 16. Block diagram of converter control system using a PI controller.

B. RESISTIVE-INDUCTIVE (R-L) LOAD

In this section, with the same conditions, a Resistive-Inductive load ($R= 83\Omega - L= 50mH$) has been used. The output waveforms of voltage and current of the converter are demonstrated in Fig. 14(b). The output RMS voltage of the converter is equal to 109 volts. According to the FFT analysis of output voltage, the value of THD is equal to 5%, and THD of the current waveform is 3% that is near sinusoidal. In this condition because the load is $R - L$, the current respect to the voltage is lagging. Also, all the diodes in converter have the same voltage stress level equal to $V_{in}/(1-D)$. With an inductance at input stage, there is no current spike for current switches and capacitors.

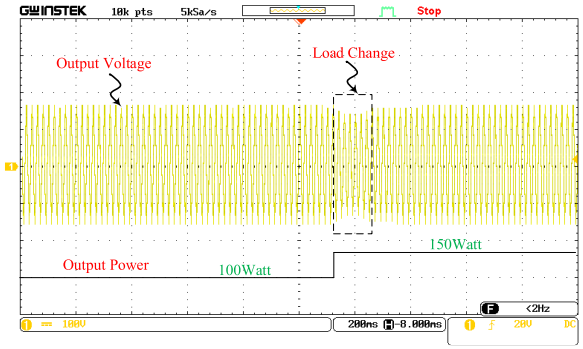

FIGURE 17. Experimental result for output voltage while changes in output power changes from 100 watts to 150 watts.

C. OUTPUT VOLTAGE REGULATION

A Proportional-Integral (PI) controller is used to control the output voltage. The block diagram of closed loop control is shown in Fig. 16. In Fig. 17, the experimental result for output voltage while output power changes from 100 watts to 150 watts is shown.

V. CONCLUSION

In this study, a new SCMLI structure based CFDVM has been planned. The CFDVM at the input stage limits the capacitors peak current and increases the voltage gain in comparison with the other SCMLIs. Therefore, the planned structure has much higher voltage gain compared to competitors. Using a single voltage source and n steps of the DVM, $2n+3$ voltage levels can be produced at the output. The presence of the boost converter at the input of this SCMLI allows the converter to work at constant m_a. Furthermore, unlike other similar SCMLIs, the suggested converter can control the output voltage gain by using duty cycle of the boost converter. Therefore, the proposed converter has a straightforward control algorithm without needing multiple calculations of the switching angles and modulation indexes. Additionally, by using this method to control the output voltage level, the number of voltage levels remains constant and does not decrease at low output voltages. Using the SHE modulation method, several voltage harmonics were eliminated at the output. A comparative study was conducted with recently introduced converters, shows that the proposed converter has fewer components than other converters with symmetrical sources. The cost function for the planned converter has a much lower value in comparison with other topologies, and this shows economic nature of the suggested structure. To investigate the performance of the suggested converter, a 13-level laboratory prototype was built, that verified the allowable ripple value and THD of the output voltage and current are in high agreement with the theoretical calculations.

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YOUSEF NIAZI was born in 1993. He received the B.Sc. and M.Sc. degrees in electrical engineering from Ilam University, Ilam, Iran, in 2015 and 2017, respectively. He is currently pursuing the Ph.D. degree in power electronics research domain with the Shiraz University of Technology, Shiraz, Iran. His research interests include design, modeling, simulation and fabrication of power electronics converters, voltage multiplier circuits, and renewable energy.

AMIRHOSSEIN RAJAEI (Member, IEEE) was born in Jahrom, Iran. He received the B.Sc. degree in electrical engineering from Shiraz University, Shiraz, Iran, in 2006, and the M.Sc. and Ph.D. degrees in electrical engineering from Tarbiat Modares University, Tehran, Iran, in 2009 and 2013, respectively. He is currently an Associate Professor with the Shiraz University of Technology, Shiraz. His research interests include power converters, modeling and design, and their applications in microgrids. He is a frequent Reviewer of IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

VAHID MORADZADEH TEHRANI was born in Shiraz, Iran, in September 1997. He received the B.Sc. degree in electrical engineering from the Firouzabad Institute of Higher Education, Firuzabad, Iran, in 2019. He is currently pursuing the M.Sc. degree in electrical engineering with the Shiraz University of Technology, Shiraz. His research interests include modeling and designing DC/DC converters, DC/AC inverters, renewable energy power conversion, and motor drive systems.

MOKHTAR SHASADEGHI is currently an Associate Professor with the Shiraz University of Technology, Shiraz, Iran. His research interests include fuzzy control, linear matrix inequalities, and optimization.

SALEH MOBAYEN (Senior Member, IEEE) was born in Khoy, Iran, in 1984. He received the B.Sc. and M.Sc. degrees in electrical engineering (area: control engineering) from the University of Tabriz, Tabriz, Iran, in 2007 and 2009, respectively, and the Ph.D. degree in electrical engineering (area: control engineering) from Tarbiat Modares University, Tehran, Iran, in January 2013. From January 2013 to December 2018, he was an Assistant Professor and a Faculty Member of the Department of Electrical Engineering, University of Zanjan, Zanjan, Iran, where he has been an Associate Professor in control engineering with the Department of Electrical Engineering, since December 2018. From July 2019 to September 2019, he was a Visiting Professor with the University of the West of England (UWE), Bristol, U.K., with financial support from the Engineering Modelling and Simulation Research Group, Department of Engineering Design and Mathematics. Since 2020, he has been an Associate Professor with the National Yunlin University of Science and Technology (YunTech), Taiwan, and collaborated with the Future Technology Research Center (FTRC). He has published several articles in national and international journals. His research interests include control theory, sliding mode control, robust tracking, non-holonomic robots, and chaotic systems. He is a member of the IEEE Control Systems Society and serves as a member for the program committee of several international conferences. He is an associate editor of several international scientific journals and has acted as the symposium/track co-chair of numerous IEEE flagship conferences.

PAWEŁSKRUCH (Senior Member, IEEE) received the M.S. degree (Hons.) in automation control from the Faculty of Electrical Engineering, Automatics, Computer Science and Electronics, AGH University of Science and Technology, Krakow, Poland, in 2001, and the Ph.D. degree (summa cum laude) and the D.Sc. (Habilitation) degree in automatics and robotics from the AGH University of Science and Technology, in 2005 and 2016, respectively. He is currently a Professor in control engineering with the AGH University of Science and Technology and the Advanced Engineering Manager AI & Safety of the Aptiv Technical Center, Krakow. His current research interests include dynamical systems, autonomous systems, artificial intelligence, machine learning, modeling and simulation, and applications of control theory to software systems.