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APPLIED RESEARCH

Three-Phase Bidirectional Isolated AC–DC Matrix-Converter With Full Soft-Switching Range

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ABSTRACT Galvanically isolated ac-dc converters are crucial for integrating distribution generation, energy storage, dc microgrids, and electric vehicles with ac distribution system. The typical industrial approach involves a two-stage setup (ac-dc/dc-dc) with a bulky dc link capacitor, and dual-active bridge converter (dc-dc) for isolation. However, this leads to increased power losses due to multiple power processing stages. To overcome this issue, this paper proposes a three-phase bidirectional isolated ac-dc matrix-converter, as a candidate solution. This topology employs a high-frequency link, eliminating the need for a traditional intermediate dc link found in a standard two-stage solution. As a main contribution, a quasi-resonant modulation strategy is introduced to allow all semiconductors to operate under soft-switching for a wide operating range. A 3.5 kW prototype was built to compare proposed one with the two-stage ac-dc converter. The experimental results show that the proposed converter achieved 96.5% efficiency at nominal power, outperforming the conventional converter, which reached 95.4% efficiency, mainly due to the extra power processing stage in the two-stage solution.

INDEX TERMS Direct matrix type, isolated rectifier, matrix-converter, three-phase power factor correction (PFC) converter.

I. INTRODUCTION

In last few years, there has been an increase adoption of electric vehicles (EVs), and residential-scale renewable energy sources (RES), such as photovoltaics (PV) [1], [2]. These RES are often combined with energy storage solutions to compensate for their intermittent energy production [3]. In addition, PVs, battery energy storage, and many modern appliances inherently operate on dc [1]. Therefore, they can be easily integrated into a dc microgrid, as depicted in Fig. 1. This dc microgrid concept finds utility in residential energy buildings, offering advantages such as reduced power processing stages, resulting in lower conversion losses, cost savings, and improved system reliability, since there are no reactive power and synchronization issues [1], [4], [5], [6], [7].

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To perform a dc electrical installation, active front-end converters (ac-dc) are used to connect ac utility grid and dc distribution inside buildings. These power converters operate as power factor control, and in addition, must provide isolation between ac and dc parts, according to standard in NPR9090 [1].

Reference [1] presents an overview related to standards and requirements for isolated active front-end (i-AFE) converters in dc energy buildings. This reference can be used and can be used in a complementary way to this paper. In addition, Fig. 2 shows different possibilities of i-AFE converters. The most straightforward approach, depicted in Fig. 2 (a) is based on a non-isolated ac-dc converter followed by a line frequency transformer. While this setup has the advantage of number of components, and reliability, it comes with important drawbacks. The line frequency transformer introduces significant volume, weight, and costs, which may not be suitable for residential applications [1].

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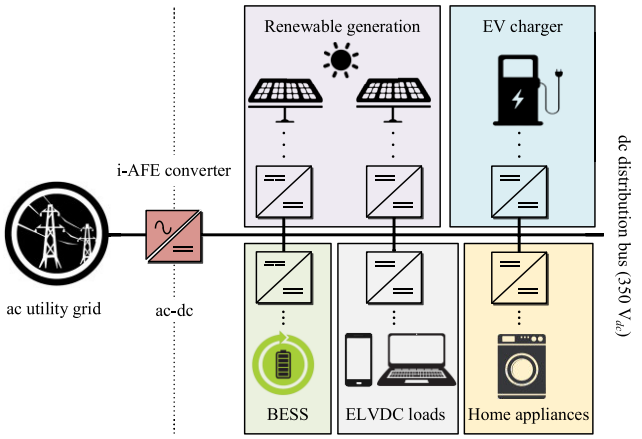

FIGURE 1. Power distribution inside dc energy buildings, considering battery energy storage systems (BESS), renewable generation, and different dc loads. An isolated active front-end (i-AFE) converter (ac-dc) is used as interface between dc distribution inside building, and ac utility grid.

High-frequency transformers offer a promising solution to reduce size and weight. In traditional two-stage configuration, such as presented in Fig. 2 (b), a high-frequency transformer is employed for isolation in a dc-dc stage, followed by a non-isolated rectifier that connects to the ac grid [8], [9]. However, these two conversion stages must be decoupled by a dc link capacitor. Unfortunately, these capacitors are typically made from electrolytic or film materials, which can be susceptible to failure and contribute to system cost and size [10], [11].

Alternatively, single-stage ac-dc converters utilize a high-frequency link as an emerging solution [12]. In this setup, an active-bridge is used to link the dc side and high-frequency transformer (HFT), while the ac side the HFT connects to a matrix-converter, which sinusoidally modulates the currents and steps down the frequency to line frequency [13], [14], [15].

Two fundamental topologies exist for achieving single-stage isolated ac-dc conversion, based on voltage-fed and current-fed approaches [1]. The voltage-fed topology employs an *LC* filter (−40 dB/dec) as an input and is based on dual-active bridge configuration with phase-shift control [15], [16]. On another hand, the current-fed is straightforward controlled, based on the input current, and in addition can be based on *LCL* filters, which naturally has highest attenuation factor (−60 dB/dec) [1]. This paper is focused on the study of current-fed matrix-converter.

While the concept of such converters was introduced some time ago, practical industrial adoption has been hindered by challenges related to voltage spikes caused by the leakage inductance of the transformer [17]. To address the issue of voltage spikes in three-phase current-fed matrix-converters, a variety of soft-switching methods have been developed. These methods enable the operation of the matrix switches on the current-fed side with either no voltage spikes or reduced voltage spikes, achieved through soft-switching [18], [19], [20], [21], [22], [23].

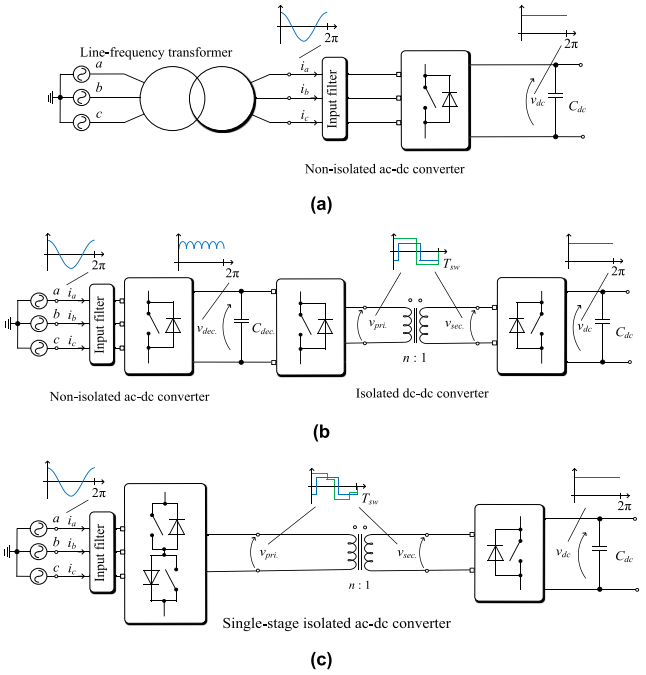

FIGURE 2. i-AFE converters solutions for dc energy buildings: (a) non-isolated ac-dc converter followed by a line frequency transformer; (b) conventional two stage ac-dc, including a high-frequency isolated dc-dc converter; (c) emerging single-stage solution where high-frequency isolation is provided with direct ac-dc conversion.

Nevertheless, there are significant voltage oscillations due to resonance between leakage inductance and output capacitance of the matrix-converter semiconductors. These oscillations are usually either not addressed or solved with additional snubber circuits [17]. In most modulations, the dc side transistors operate under zero-voltage switching (ZVS-on) that consider only the output capacitance of the switches and hard switched turn-off. In [24] and [25] lossless snubbers are incorporated in parallel with the switches to mitigate turn-off losses. These snubbers are then recharged using a quasi-resonant (QR) state. However, this state is introduced only at low loads and suffers from the drawback of unnecessary circulating energy during an enhancement interval.

To operate effectively as a bidirectional interface, the three-phase isolated matrix-converter (3P-IMC) requires a properly modulation scheme. However, most existing modulations focus solely on the dc-to-ac power flow. There is a need for further research to develop a modulation method suitable for bidirectional operation. Recently, [16] introduced a modulation method suitable for ac-to-dc operation, but it involves hard-switching on the dc side.

To address this issue, this paper proposes a new modulation strategy, based on quasi-resonant switching state. This modulation allows soft-switching for full operation range, including zero voltage (ZVS) and zero-current switching (ZCS). This approach enables both ac-to-dc and dc-to-ac operation modes, using the same modulation strategy. Unlike [16], it does not require multi-mode operation and avoids an

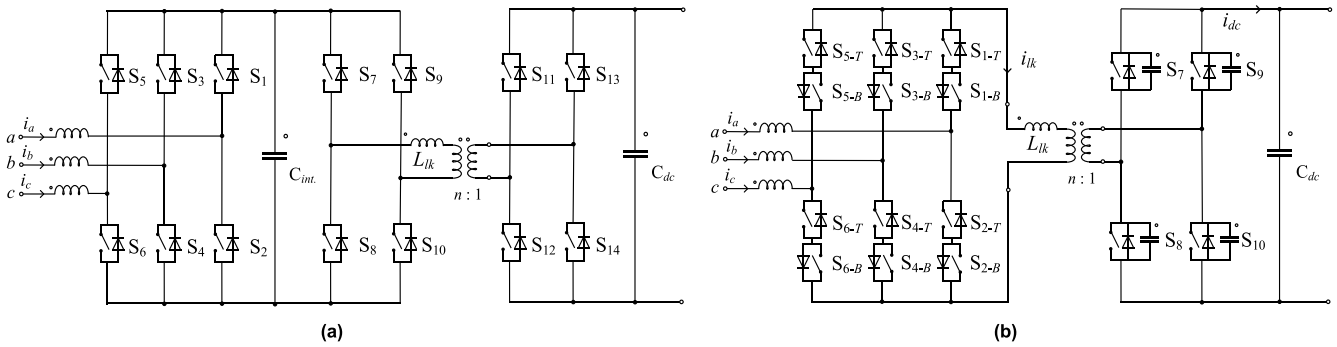

FIGURE 3. Power circuits of different i-AFE converters: (a) conventional two-stage solution, based on two-level voltage-source converter (ac–dc) and dual-active bridge (dc–dc) to provide high-frequency isolation; (b) single-stage based on matrix-converter at ac side.

enhancement stage, contributing to reduce circulating energy. Furthermore, one of the matrix-converter's phases is clamped according to the selected sector. It means that the matrix-converter's switches operate with only 5/6th of the switching frequency, contributing to improving the converter efficiency.

The proposed modulation strategy represents a significant advancement for single-stage ac-dc converters technology. This approach offers advantages compared to the previously literature, because it results in an improved efficiency and flexibility, making it more practical and efficient for bidirectional applications. To evaluate it experimentally, a 3.5 kW prototype was built, and laboratory tested. The single-stage converter was compared with the conventional solution for dc energy buildings, the two-stage ac-dc converter. While the single-stage resulted in 96.5 % of efficiency, the industrial two-stage solution ensure only 95.4 %. In addition, the experimental results demonstrate that with the quasi-resonant modulation, the resulted efficiency curve remains nearly flat across the entire operation range, which is not possible with conventional ones.

In the following, the paper is organized as follow: Section II describes the converter operating principles and commutation. Section III describes the converter design. Section IV shows the results from an experimental prototype. Section V provides some discussion concludes the paper.

II. CONVERTER OPERATION

Fig. 3 presents the diagram of different power converters, which can be candidates to operate as i-AFE. Fig. 3 (a) presents the standard two-stage solution, while Fig. 3 (b) presents the proposed single-stage. The two-stage solution includes a two-level voltage-source converter (2L-VSC) in the power-factor correction (ac-dc) stage, and a dual-active bridge (dc-dc), to ensure isolation.

In the single-stage converter, a matrix-converter is used in the ac side, including six pairs of anti-series semiconductors. The anti-series configuration is forming a four-quadrant switches, which allows to totally control the input current. On the dc side, a full-bridge converter is used to create a square voltage waveform in the transformer's secondary side. To introduce the proposed modulation, initially, the existing methods are discussed in the following subsection, and later the proposed method is presented in detail.

A. EXISTING SOLUTIONS AND PROBLEM MAPPING

The dc side switches operate with fixed duty-cycle, including a dead-time to avoid short-circuits in series semiconductors. The matrix-converter unfolds the high frequency square wave and sinusoidally modulates it to generate a properly current to the ac side. As can be seen in Fig. 3, the matrix-converter is essentially a two-level converter, composed of a pair of full-controlled switches (monolithic ones, or anti-series). Because of the current-fed characteristic, there is no need for dc blocking capacitors in series to the transformer, as commonly used in conventional dual-active bridge converters, or voltage-fed ones [15].

As this is a three-wire system, the leg with the highest current reference can be clamped to the transformer winding allowing two switches to operate at reduced frequency. On the matrix-converter side, the current-fed nature allows zero-current switching (ZCS-off) for all semiconductors. For the dc side, snubber capacitors are used in parallel to the switches, as shown in Fig. 3. The total output capacitance is represented by the equivalent capacitance C_{eq}. The turn-off losses at dc side are limited by the snubber capacitors. However, there is a tradeoff as the snubber must be recharged before the turn-on of the device to have zero voltage switching (ZVS-on). The ZVS-on condition is defined in (1), where L_{lk} and i_{lk} are the transformer leakage inductance and current.

$$\frac{1}{2} \cdot L_{lk} \cdot (i_{lk})^2 \geq \frac{1}{2} \cdot C_{eq} \cdot v_{dc}^2 \tag{1}$$

According to (1), is clear that the ZVS-on is dependent on the transformer current (i_{lk}), and equivalent output capacitance. This is particularly relevant at light loads when the transformer current is not enough to completely discharge the switches output capacitances.

There are a few ways in literature to extend the ZVS-on for this family of topology. In [23] and [26] the leakage inductance provides the energy to recharge the dc side switch capacitance and allow ZVS turn on. However, at light loads this is no longer possible as the leakage inductance cannot

supply enough energy for ZVS. In [27] the magnetizing current is used, at the cost of additional circulating energy, which reduces efficiency, especially at low load. Both the leakage and magnetizing inductance solutions require specific and carefully controlled parasitic parameters of the magnetics, due to the relation (1). Auxiliary circuits are also possible [28], [29], however, this increases the component count, cost, and complexity of the solution.

Therefore, there is a lack of modulation strategies in the current literature that do not require auxiliary circuits, and at the same time, reduce circulating current. This contributes to reducing the switching and conduction losses across a wide operating range. In the proposed paper, the recharge of the dc side output capacitors is provided by imposing a shoot-through state on the matrix-converter side. This introduces a quasi-resonant state between the output capacitance and leakage inductance. The current in the converter rises to a value above the nominal, allowing to recharge the output capacitors at any processed current, or even at no load.

As main advantages of the proposed modulation include not requiring auxiliary circuits, not dependent on a specific leakage or magnetizing inductance, simplifying the transformer's design. Furthermore, there is no additional circulating energy in the converter and the control is quite simple, as described in the following.

B. PROPOSED MODULATION SEQUENCE

Due to the anti-series connected switches, is not possible to provide a freewheeling path for the processed current at the matrix-converter side. Therefore, both the top and bottom switches must have an overlap time when both are turned-on. This allows for the distribution of current from the top leg to the bottom, and vice versa, ensuring a path for processed current. This sun-stage is analogous to the concept of dead-time in voltage-fed converter topologies.

To ensure soft-switching the modulation scheme can be summarized in four primary stages, plus four additional steps during the quasi-resonant period. The described analysis takes as reference phase a, being each phase selected according to the selection of the sector. The space-vector modulation necessary for the sectors' selection, and resonant interval are described in the following subsections. In the following, the main primary stages are described in detail. The commutation scheme is shown in Fig. 4 and described below.

Stage 1(*Fig. 4a*), t_0-t_1: the first stage starts when the matrix-converter conducts through the top arm (S_{1-T}-S_{1-B}), transferring power from the ac to dc side. The semiconductor on the top side, S_{1-T}, initially operates with synchronous rectification, being turned off at the end of this stage.

Stage 2 (Fig. 4b), t_1-t_2: when S_{1-T} is turned off, its blocking voltage is clamped by the body diode, which is directed polarized. Simultaneously, the switches on the bottom arm, S_{2-T}, S_{2-B}, are turned on, putting the converter in the shoot-through state. After the turn-on, the current in S_{2-T}, and S_{2-B} S_4 starts to increase linearly, being limited by the transformer leakage inductance. It allows both semiconductors being switched under a soft condition, since their current is initially zero. The transformer voltage is clamped to zero at the ac side,

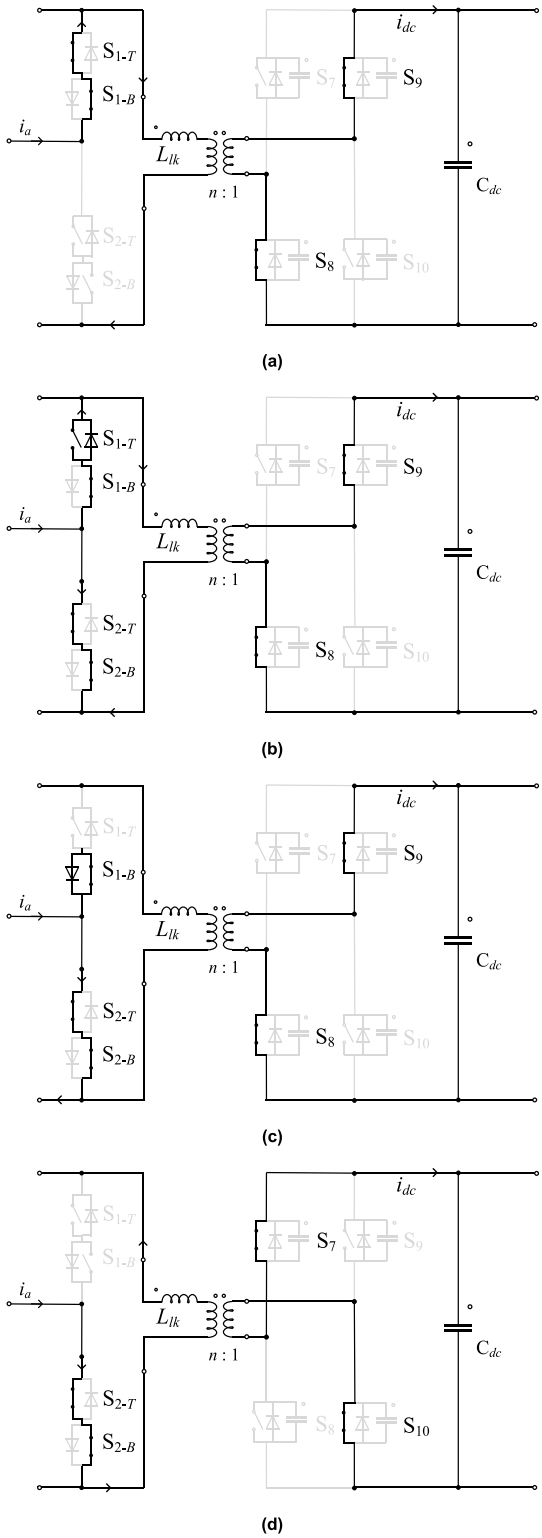

FIGURE 4. Equivalent circuits of the proposed modulation scheme, considering as refence the phase (*a*): (a) Stage 1; (b) Stage 2; (c) Stage 3; (d) Stage 4. ∗ Each phase is selected according to the sectors described in a space-vector modulation.

imposing the dc voltage on the leakage inductance, through S_7 and S_{10}. This redistributes the current of the matrix-converter leg, from the top to the bottom arm. This stage ends when the current in the top arm achieves zero level.

Stage 3(*Fig. 4c*), t_3-t_4: once the current in the top arm is zero, S_{1-T} blocks the input voltage through his anti-parallel diode, allowing S_{1-B} to be turned off under ZCS.

Stage 4(*Fig. 4d*), t_4-t_5: the final state is reached after the commutation of the dc side, inverting the polarity of the voltage on the transformer. The matrix-converter leg is ready to repeat the commutation in the opposite direction, redistributing the current from bottom to top arm.

The processed commutation sequence ensures that only one single body diode is ever in conduction, leading to just one reverse-recovery event. To achieve soft-switching, it is necessary that the voltage applied to the leakage inductance during the shoot-through state reverses the output current (i_{dc}). Therefore, the appropriated commutation of the converter's leg depends on connecting the ac phase to the appropriate transformer terminal, either the top or bottom one, prior to the leg commutation. This determination is contingent on various factors, including the direction of the phase current, transformer voltage polarity, and whether the converter is operating as an inverter or rectifier. The necessary condition is described by (2),

$$K_i = \text{sgn}(v_{p-x}, i_{p-x}), \tag{2}$$

where K_i positive corresponds to connect the phase to the top transformer terminal, and negative to the bottom.

For each switching period, the proposed sequence is applied in two of the matrix-converter legs, whereas the third one with the greatest current reference is clamped to the transformer terminal and is used to initiate the quasi-resonant transient. In the following subsection, the quasi-resonant state is described.

C. QUASI-RESONANT STAGE

According to the proposed modulation scheme, while two legs are used to create a high-frequency ac link, the third one can be used as auxiliary, to provide an additional quasi-resonant stage. The quasi-resonant stage is necessary to ensure soft-switching for the secondary side (S_7-S_{10}). For example, supposing that phase *b* and *c* are used to the power transfer, phase *a* should be used as auxiliary to provide the quasi-resonant stage. Fig. 5 presents the equivalent circuits, during the quasi-resonant transient.

Stage 1(*Fig. 5a*), t_0-t_1: the first stage starts when the matrix-converter are transferring energy from the ac to dc side thought phases *b* and *c*. Phase *a* keeps the top arm turned off (S_{1-T}- S_{1-B}), while the S_7 and S_{10} are turned on.

Stage 2 (Fig. 5b), t_1-t_2: when S_7 and S_{10} are turned off, simultaneously, S_{1-T} is turned on to create a shoot-thought state in the matrix-converter side. In this moment, a quasi-resonant transient occurs between leakage inductance (L_{lk}), and semiconductors' output capacitances at dc side (S_7-S_{10}).

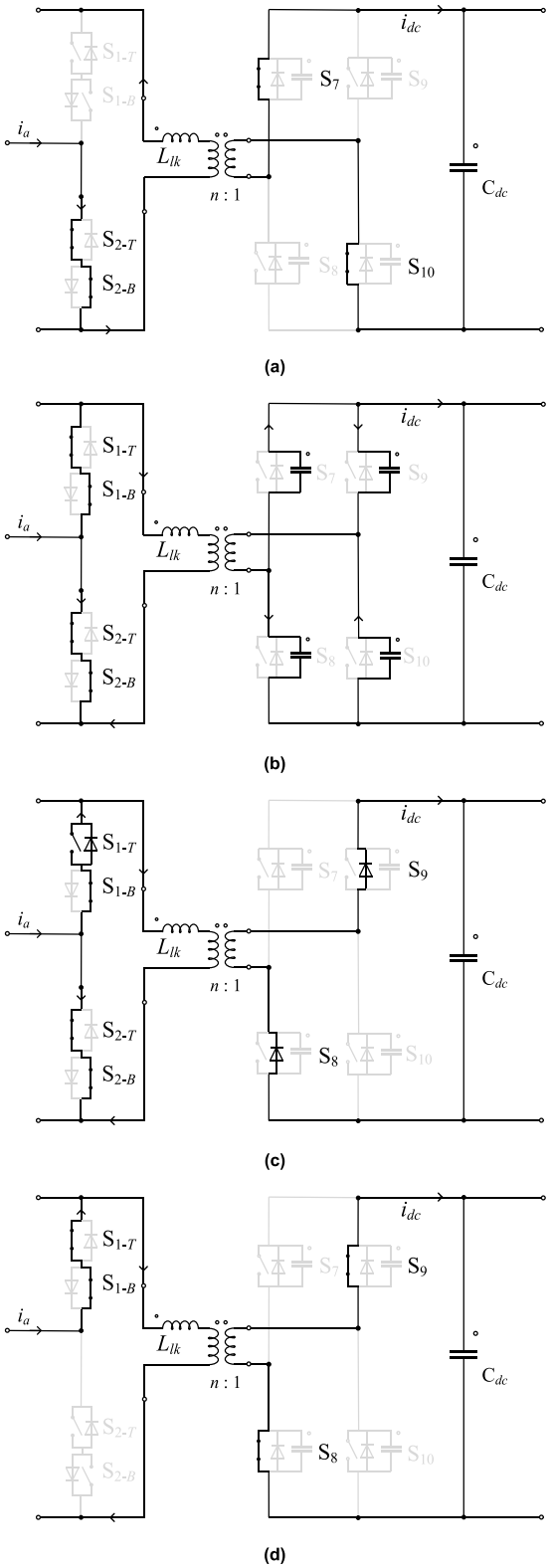

FIGURE 5. Equivalent circuits of the quasi-resonant transient, applied to charge/discharge the semiconductors' output capacitances at secondary side (dc): (a) Stage 1; (b) Stage 2; (c) Stage 3; (d) Stage 4.

The shoot-thought state at the primary side (ac) allows the processed current rises above the load current, accelerating the capacitors' recharge process.

Stage 3(*Fig. 4c*), t_3-t_4: once the capacitors' voltage of S_8 and S_9 decreases close to zero, their body diodes are directly polarized, taking over the transformer leakage current (i_{lk}).

Stage 4(*Fig. 4d*), t_4-t_5: the final state, with both diodes directly polarized, S_8 and S_9 can be turned on under zero voltage switching.

The quasi-resonant stage can be applied in both, inverter (dc-to-ac) and rectifier (ac-to-dc) operation modes. However, due to (2), during the inverter operating (dc-to-ac), the leg commutation will always increase the absolute value of the transformer current (i_{lk}), while it will decrease for the rectifier operation mode (ac-to-dc).

As consequence, the converter will always operate at zero state with transformer current equal zero, after the dc side commutation, during the inverter operation mode. For the rectifier operation a shot-thought state is used to ensure it before the dc side switches commutation, decreasing the absolute value of i_{lk}. Fig. 6 presents the main theoretical waveforms for both operation modes.

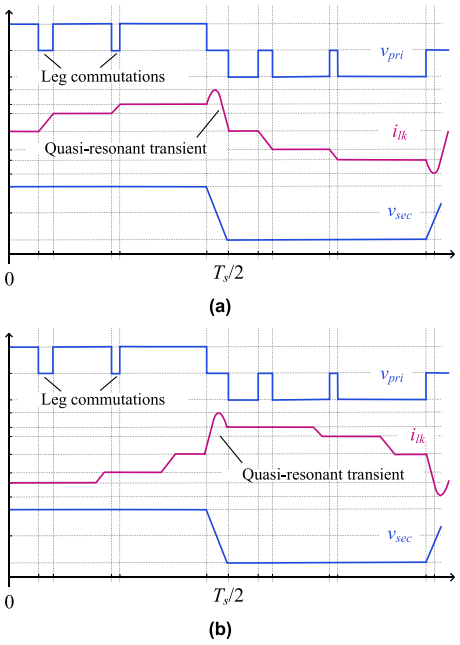

FIGURE 6. Theoretical waveforms, including the transformer primary-voltage (v_{pri}), leakage current (L_{lk}), and secondary voltage (v_{sec}): (a) inverter operation mode (dc-to-ac); (b) rectifier operation mode (ac-to-dc).

In addition, is necessary to note that, during the converter operation, always two switches are kept fixed, turned on or off, according to the processed power flow. The leg with highest reference current is the one that contains clamped switches. Assuming a balanced three phase system, all switches will spend 1/6 of a grid frequency period clamped, effectively reducing the switching frequency of the matrix-converter to 5/6 of the switching frequency. The clamping of one leg means that only three voltage vectors, in this case two active vectors and a zero state, are imposed by the converter. This feature also contributes to the converter efficiency.

Due to the absence of a dc link in this system, the passive components of interest are the transformer and grid inductors. As illustrated in Figure 6, both the dc side and matrix-converter switches contribute to the voltage imposed on the grid side inductors. This results in doubling the switching frequency seen by the inductors, effectively reducing the filtering requirements. Considering the average switching frequency is reduced to 5/6 because of the clamped leg, the ratio of switching frequency at the load and semiconductors' average switching frequency is 2.4.

The duration of the quasi-resonant transient is defined by (3), I_{lk} is the instantaneous current in the leakage inductance at the beginning of the quasi-resonant stage.

$$t_{res} = 2 \cdot \sqrt{L_{lk} \cdot C_{eq}} \left(\frac{\pi}{2} \arctan \left(\frac{n \cdot I_{lk} \cdot L_{lk}}{v_{dc} \cdot C_{eq}} \right) \right) \tag{3}$$

Fig. 7 presents a contour plot of the time necessary to recharge the semiconductors output capacitances with zero initial transformer current. As expected, highest values of capacitances result in highest duty-cycle losses. In this sense, there is a tradeoff between the turn-off losses and duty-cycle losses, during the quasi-resonant stage.

The duration of the leg commutation transients can be calculated by (4), where $I_{ac,x}$ is the current of the phase under switching.

$$t_{sc} = \frac{I_{ac,x} \cdot L_{lk}}{v_{dc}} \tag{4}$$

The processed current during the quasi-transient period is given by (5), which solved for the maximum output current, results in (6).

$$i_{ac} = \pm v_{dc} \cdot \sqrt{\frac{C_{eq}}{L_{lk}}} \cdot sin\left(\frac{t}{\sqrt{L_{lk} \cdot C_{eq}}} \right) \pm I_{lk} \cdot \cos\left(\frac{t}{\sqrt{L_{lk} \cdot C_{eq}}} \right) \tag{5}$$

$$I_{lk,max} \cdot = \sqrt{\frac{C_{eq}}{L_{lk}} \cdot {v_{dc}}^2 + I_{lk,o}^2} \tag{6}$$

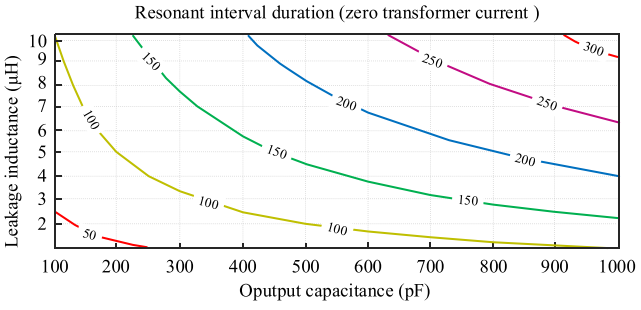

FIGURE 7. Contour plot of QR duration with no initial transformer current.

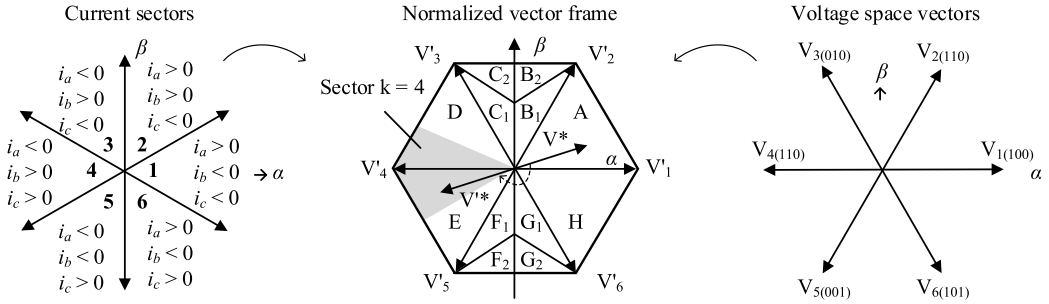

FIGURE 8. Space vector modulation for selecting optimized three vector sequence. The optimal three vector sequence is determined by the region of the reference vector in the normalized space vector frame, and then the real vectors are obtained by transforming the normalized vectors according to the current sector. Contour plot of QR duration with no initial transformer current.

TABLE 1. Optimized three vector sequence in normalized reference frame.

	A	B_1	B_2	C_1	C_2	D	E	F_1	F_2	G_1	G_2	H
V_x	V_7'	V_4'	V_4'	V_3'	V_3'	V_4'	V_4'	V_5'	V_5'	V_4'	V_4'	V_7'
V_y	V_2'	V_7'	V_3'	V_0'	V_2'	V_3'	V_5'	V_0'	V_6'	V_7'	V_5'	V_6'
V_z	V_1'	V_2'	V_2'	V_1'	V_1'	V_0'	V_0'	V_1'	V_1'	V_6'	V_6'	V_1'

TABLE 2. Normalized space vector.

	V_0'	V_1'	V_2'	V_3'	V_4'	V_5'	V_6'	V_7'
k = 1	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7
k = 2	V_7	V_2	V_3	V_4	V_5	V_6	V_1	V_0
k = 3	V_0	V_3	V_4	V_5	V_6	V_1	V_2	V_7
k = 4	V_7	V_4	V_5	V_6	V_1	V_2	V_3	V_0
k = 5	V_0	V_5	V_6	V_1	V_2	V_3	V_4	V_7
k = 6	V_7	V_6	V_1	V_2	V_3	V_4	V_5	V_0

D. SPACE VECTOR MODULATION

The space vector modulation for the three-phase isolated matrix-converter is conceptually identical to the conventional three-phase two-level voltage-source converter (2L-VSC). This is necessary to synthesize a sinusoidal current for the ac grid side. The current sector imposes some constraints on possible vector sequences to allow ZCS of the matrix-converter switches. The optimized sequence must ensure that these constraints are fulfilled, as well as using the vectors adjacent to the refence vector and minimizing the zero vector when used. The optimized vector sequence for space vector modulation was first derived for the non-isolated high-frequency link converters in [29]. This sequence is presented in Fig. 8, while Table 1 and Table 2 presents the optimized vector sequence in the reference frame, and the normalized space vector, respectively. In this strategy, one active voltage vector is suppressed by being placed immediately before the dc side commutation. The result is a three-vectors sequence. This suppressed vector corresponds to the clamped leg used during the quasi-resonant transient.

As in any three-phase ac-dc converter, the voltage reference is rotated with a phase-angle of $\Delta\theta = (k\text{-}1) \cdot \pi / 3$, where k is the current sector, and placed in a normalized vector frame composed of V', where the corresponding real voltage vector which depends on the current sector. The normalized zero vectors depend on the polarity of the current with highest reference value, i.e., the current with direction opposite to the other two, seen in Fig. 8. With positive current the zero vector remains unchanged whereas with negative reference the zero vectors V_0 and V_7 are exchanged.

The resulting optimal vector sequence depends on the reference voltage regions shown in Fig 8. For load angles near 0 or π radians it is always possible to use two adjacent vectors and a zero vector. On the other hand, at load angles near $\pm\,\pi\,/\,2$, the zero vector is either the middle vector or not used at all. When operating near unity power factor in inverter operation, regions A and H, the first vector is always a zero vector. Instead, rectifier operation corresponds to regions D and E wherein the last vector is always a zero vector.

The duty cycles (δ_x) are calculated according to (7), while the real vector sequences are obtained from the current sectors, described in Fig. 8.

$$\begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} = \begin{bmatrix} V'_{x,\alpha} & V'_{y,\alpha} & V'_{z,\alpha} \\ V'_{x,\beta} & V'_{y,\beta} & V'_{z,\beta} \\ 1 & 1 & 1 \end{bmatrix}^{1} \begin{bmatrix} V'^{*}_{\alpha} \\ V'^{*}_{\beta} \\ 1 \end{bmatrix} \tag{7}$$

To reduce computational burden the inverse matrix can be preloaded to a look-up table in the signal processor/controller. The current sectors' boundaries and space vectors are 30 degrees out of phase, resulting in twelve different operating sectors. These 12 sectors consider not only the six possible voltage polarities but also the ratio of voltages of the same polarity.

III. APPLICATION REQUIREMENTS, STANDARDS, AND CONSIDERATIONS FOR COMPONENTS SELECTION

One of the main contributions of this paper is the proposal of the three-phase isolated matrix-converter as a candidate solution to act as an i-AFE converter for residential dc energy buildings. In this application, specific design requirements are defined according to standards for dc electrical installations. Currently, the is a lack of standardization that cover all aspects related to dc energy buildings, since some of these standards are still under development, while others, even if established, have not yet gained widespread adoption in the industry. However, certain design criteria are considered common sense in several projects [30], including isolation requirements, voltage specifications, and power levels [1].

A. APPLICATION REQUIREMENTS

Currently, the main directives to standardize dc energy buildings are found in IEC 6034 [31], and NPR 9090 [31]. Following these standards, the isolation between ac and dc parts is a mandatory criterion. Because of this reason, the current industrial solution is based on two-stage converters, as presented in Fig. 3 (a). On another hand, following the presented analysis, the single-stage solution can present some benefits, including better and flat efficiency, provided by the full soft-switching operation.

1) CONVERTER EFFICIENCY

Reference [33] provides insights into efficiency curve patterns for i-AFE converters. For applications in dc energy buildings, is necessary to ensure not just high peak efficiency, but also maintain very flat efficiency curves. This is important because dc energy buildings often require the i-AFE converter to operate at low power levels for long periods.

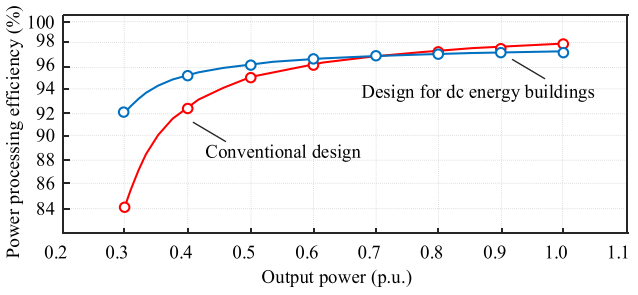

FIGURE 9. Examples of i-AFE converters' efficiency curves for different applications.

While other applications like uninterrupted power supplies and electrical vehicles primarily prioritize peak efficiency at maximum power levels, dc energy building demand a multi-objective focus. They need to ensure not only high efficiency at peak power but also maintain high efficiency at lower power levels. To illustrate it, Fig. 9 presents an example to compare designs for conventional and dc energy building applications. This efficiency profile is essential to support sustained operation and energy efficiency in DC energy building applications, where power demand can vary widely over time.

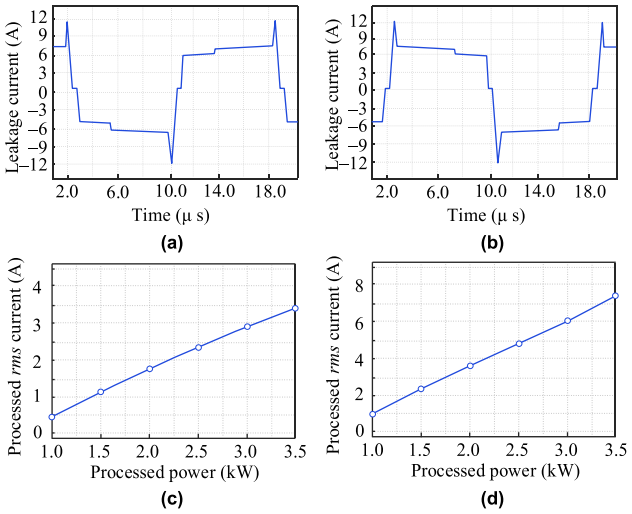

FIGURE 10. Simulation results, including: (a) transformer leakage current, during the inverter operation mode; (b) transformer leakage current during the rectifier operation mode; (c) *rms*current for the primary-side switches (S_1-S_6); and (d) *rms*current for the secondary-side switches (S_7-S_{10}).

2) NOMINAL POWER

Reference [33] presents a statistical analysis of the power demand profile inside energy buildings. Following the suggested power levels, the i-AFE converters should be designed to operate between 2 and 5 kW, being 3.5 kW a common parameter for different projects.

3) INPUT VOLTAGE AND POWER QUALITY AC SIDE

Are defined by the ac grid standards. The ac voltage is commonly within 110-240 V_{rms} for single-phase and 380-400 V_{rms} for three-phase systems. For the input current, the maximum allowed total harmonic distortion should be less than 5%, within a range of 50% to 100% of the nominal power, while the power factor ideally should be unitary.

4) DC VOLTAGE

NPR9090 covers a range of voltage levels, being 350 V_{dc} the current standard for dc distribution inside builds.

Following, the discussed parameters, Table 3 summarize the main design requirements for a i-AFE converter. In the following a preliminary simulation is presented to validate the proposed modulation strategy, and to evaluate the components stress over different operation points.

B. SIMULATION RESULTS AND COMPONENTS SELECTION

According to the presented parameters, the single-stage converter was simulated on PSIM software. A 50 kHz switching frequency was selected, while the simulation step is equal to 10 *n*s. For the transformer turns ratio (n:1), is necessary to note that, the clamping of a leg, and use of only two adjacent voltage vectors and the zero vector extends the linear modulation range to 1.154. With a line-to-line *rms* voltage of 400 V ($V_{max-rms}$), the required turns ratio is:

$$V_{max-rms} = n \cdot \frac{v_{dc}}{\sqrt{2}} \tag{8}$$

TABLE 3. Main specifications and parameters of the designed prototype.

Parameter/component	Value/Specification
Input voltage (*ac*)	230 V_{rms} (phase-neutral)
Nominal power (P)	3.5 kW
Allowed *THD*	5 %
Output voltage (*dc*)	350 V_{dc}

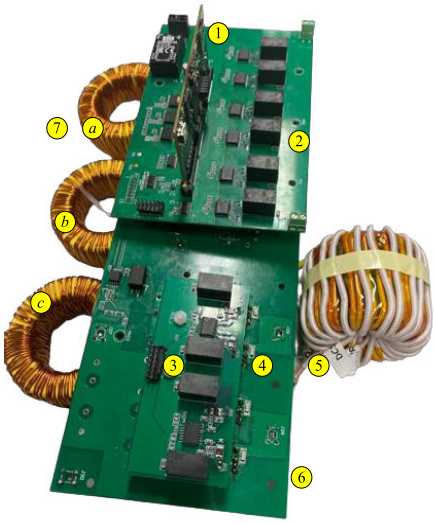

FIGURE 11. Experimental prototype, being: (1) control board; (2) driver circuits – dc side; (3) driver circuits – ac side; (4) power board; (5) high-frequency transformer; (6) heatsinks and semiconductors are in the bottom side; (7) inductive filters, including phases *a, b, and c*.

From (8), the calculated turns ratio (n:1) is 1.62: 1. However, to compensate duty-cycle losses during the dead-time, and quasi-resonant transients, n was set was 1.82.

Fig. 10 presents the main simulation results. Initially, the main waveforms were verified to check the converter operation modes. Fig. 10 (a) presents the transformer current for the inverter operation mode, when the quasi-resonant transient is verified before the zero state. Fig. 10 (b) presents the simulation result for the rectifier operation mode, showing the quasi-resonant state occurring after the zero current level.

Additionally, Fig. 10 (c) and Fig. 10 (d) presents the simulated results for *rms* current in the primary, and secondary switches for different power levels.

Related to the component's selection, the peak line-to-line voltage is 570 volts at ac side. However, the matrix-converter switches suffer from a well-known problem of resonance between the output capacitance of the switches and the leakage inductance of the transformer. On the dc side there is no ringing problem, and 350 V is the resulted blocking voltage for the semiconductors. In additional, external capacitors can be added to increase the output capacitance. It allows to provide soft-switching. Due to this, the output capacitance of the switch is of little concern as it does not have a significant impact on switching losses. However, is necessary to note that, external capacitors must have good performance under dc bias conditions and tolerate high ripple current.

Based on these design considerations, the main converter parameters can be selected, including transformer, semiconductors, and filter inductors. In the following the experimental prototype is described and experimental results presented.

IV. EXPERIMENTAL RESULTS

The built prototype was used to verify the performance of the proposed modulation and design. The parameters and specifications of the experimental prototype are summarized in Table 4. The converter design considers 350 V_{dc} as output voltage, following the NPR9090 requirements. In addition, reference [1] presents an overview related to design requirements for i-AFE converters, and can be used as complementary reference, to define the main converter design parameters. This allows to adequate the converter design to other industrial projects, and to compare the results with other cited papers.

In the following, the converter waveforms were obtained to demonstrate the soft-switching transients, and modulation strategy. The converter's waveforms were obtained with an oscilloscope Tektronix DPO4034 and efficiency with a power analyzer WT 1800.

A. SOFT-SWITCHING RESULTS

Fig. 12, Fig. 13, and Fig. 14 presents the quasi-resonant (QR) transient, which occurs during the shoot-through state. Three different tests were performed for high, medium, and low power levels. This allows to evaluate the soft-switching conditions for a wide operation range.

Fig. 12 (a) presents the experimental results at nominal power (3.5 kW). At a high-power, there is enough processed power to fast recharge the output capacitance at the dc side. In this case, the quasi-resonant effect results in a minimum transient current, due to the fastest output capacitance charge. This can be verified in detail in Fig. 12 (b). The transformer's voltage on the primary side (v_{pri}), is briefly clamped to zero, due to the shoot-trough state. In addition is possible to note that, a voltage ringing occurs due to the resonance between output capacitances of the matrix-converter switches and leakage inductance (L_{lk}).

TABLE 4. Main specifications and parameters of the designed prototype.

Parameter/component	Value/Specification
Input voltage (*ac*)	230 V_{rms} (phase-neutral)
Nominal power (*P*)	3.5 kW
ac filter (*L*)	1.3 mH
Allowed *THD*	5 %
Primary side switches (S_1-S_6)	IMW120R220M1H (1200 V/9.5 A)
Secondary side switches (S_7-S_{10})	C3M0120065k (1200 V/22 A)
Switching frequency (f_s)	50 kHz
HF transformer	Pri: 31 turns Sec: 17 turns Turns ratio (n:1): 1.82: 1 Core: 2 × TDK EPCOS N87 Leakage inductance: 8 µH
Output voltage (*dc*)	350 V_{dc} (following NPR9090)
Output current (i_{dc})	10 A
Output capacitance (C_{dc})	60 µF
Driver circuits	UCC21521

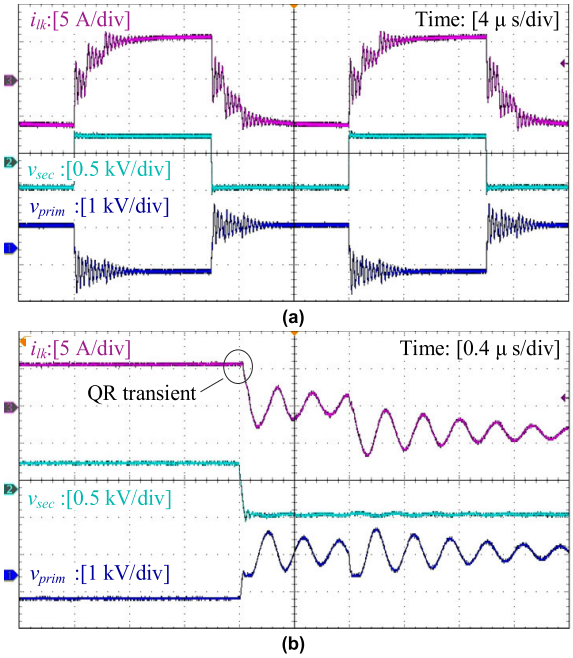

FIGURE 12. Experimental results for the quasi-resonant state, at 3.5 kW: (a) transformer leakage current (i_{lk}); primary (v_{pri}), and secondary voltages (v_{sec}); (b) transient details.

Fig. 13 (a) presents the experimental results of the quasi-resonant transient at medium power (1.0 kW), while Fig. 13 (b) presents the details during the dead-time stage. In this case, is noticeable that the transformer current increase above the processed value, during the dead-time. It allows to accelerate the recharge of output capacitances at secondary side.

Similar results are found in Fig. 14 (a) and (b), where presents an extreme case, at very low power (50 W). In this case, almost of all processed energy is used to recharge the output capacitances, providing by the quasi-resonant stage. However, is still possible to achieve ZVS-on, even almost no-load current.

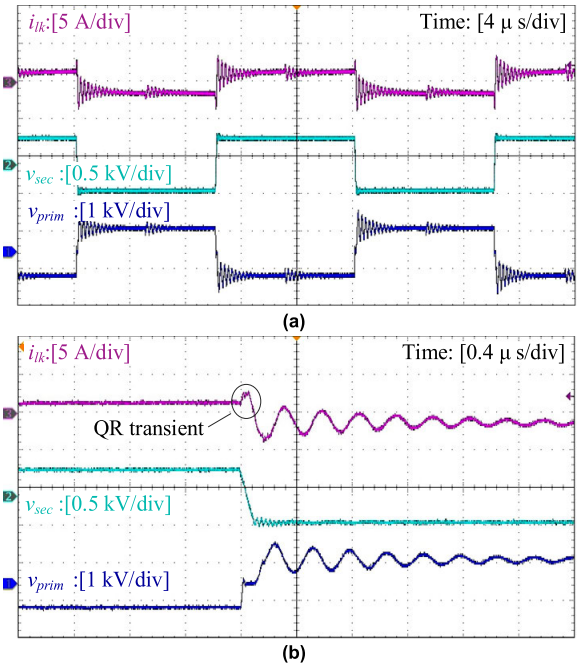

FIGURE 13. Experimental results for the quasi-resonant state, at 1.0 kW: (a) transformer leakage current (i_{lk}); primary (v_{pri}), and secondary voltages (v_{sec}); (b) transient details.

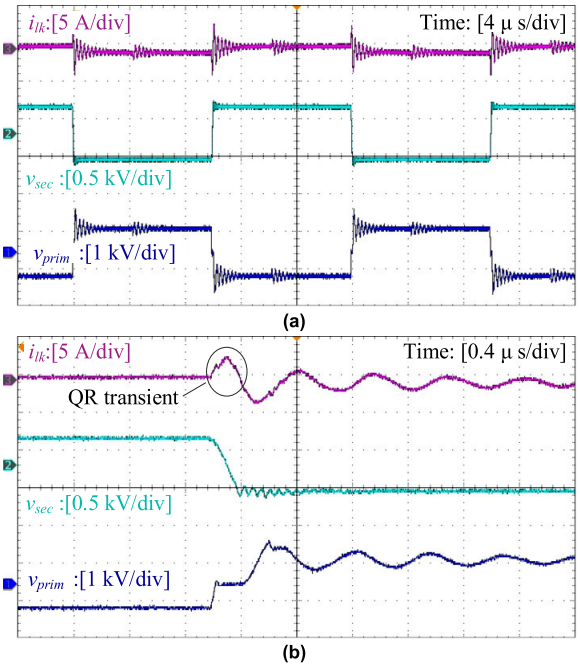

FIGURE 14. Experimental results for the quasi-resonant state, at 50 W: (a) transformer leakage current (i_{lk}); primary (v_{pri}), and secondary voltages (v_{sec}); (b) transient details.

To evaluate the soft-switching operation, Fig. 15 presents the transients results of the semiconductors switching at dc side. Fig. 15 (a), which presents the gate-source signal (v_{gs-S7}), drain-source current (i_{ds-S7}) and blocking voltage (v_{ds-S7}), for the semiconductor S_7. According to the experimental results, when the semiconductor is turned off, the

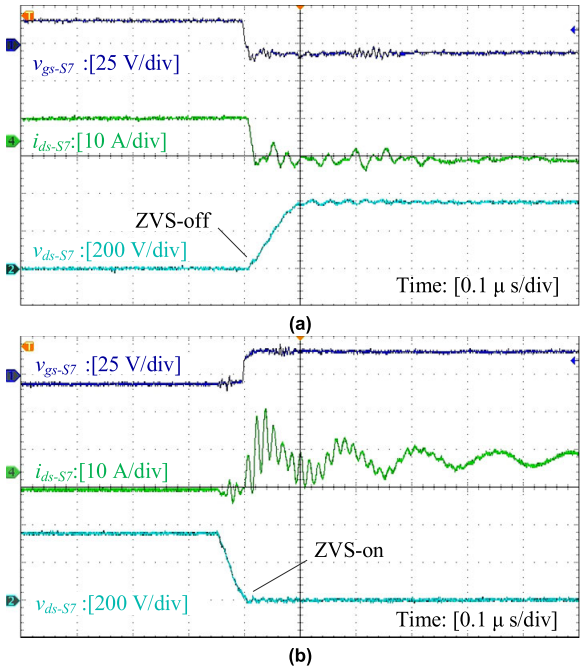

FIGURE 15. Soft-switching conditions for the dc side switches: (a) gating signal (v_{gs-S7}), drain-source current (i_{ds-S7}), and drain-source voltage (v_{ds-S7}); (b) transient details.

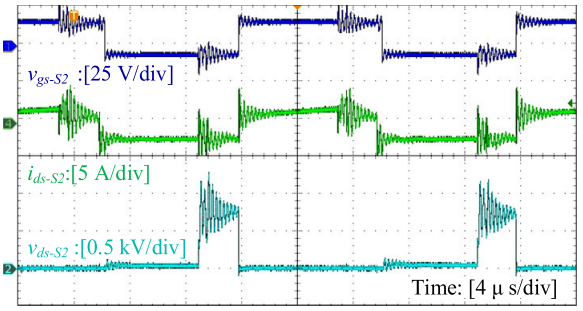

FIGURE 16. Soft-switching (ZVS-off) of S_2, at the matrix-converter side, including gating signal (v_{gs-S2}), drain-source current (i_{ds-S2}), and drain-source voltage (v_{ds-S2}).

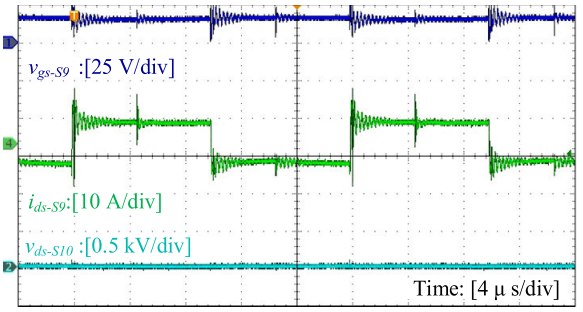

FIGURE 17. Experimental results for the clamped leg, during the quasi-resonant transient, including gating signal (v_{gs-S9}), drain-source current (i_{ds-S9}), and drain-source voltage (v_{ds-S9}).

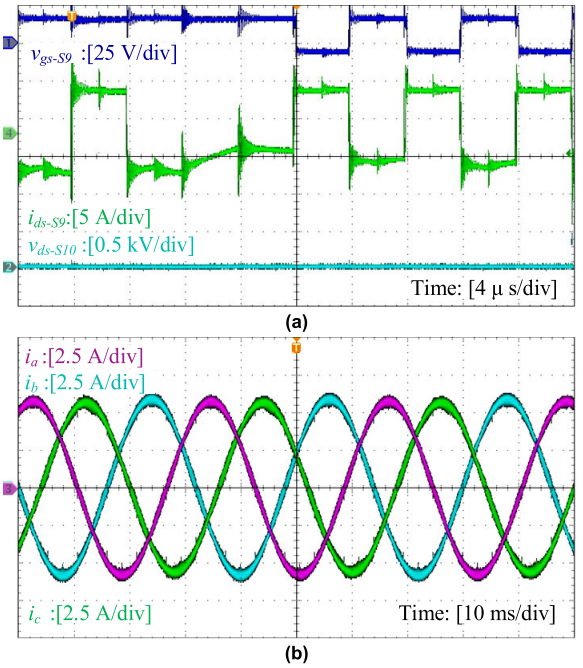

FIGURE 18. Experimental results for space vector modulation necessary to synthesize the ac current: (a) sectors change: (b) resulted ac currents.

current starts to decrease, but the voltage derivative is limited by the output capacitances, reducing the turn-off losses. Fig. 15 (b) presents the soft-switching condition during the turn-on. Initially, the output capacitors are fully discharged, resulting in zero voltage before the gating signal (v_{gs-S7}) being applied in S_7. When S_7 is turned-on, the current beings to rise with $v_{ds-S7} = 0$, charactering ZVS-on.

Fig. 16 presents the experimental results for the ac side. During the overlap stage, the ac side switches current starts to decrease until achieve zero. After being blocked by the synchronous rectification stage, the drain-source current (i_{S2}) of S_2 is kept at zero, allowing the ZCS-off.

Fig. 17 presents the experimental results for the clamped leg, used for the quasi-resonant stage. Here is important to note that two switches are not switched constantly. These switches continuously conduct the processed current and are not subjected to any switching stress or reverse recovery problem, which also contributes to the conversion efficiency.

Fig. 18 (a), shows the experimental results for the sector change. Fig. 18 (b) presents the resulted sinusoidal currents at the ac side. During the converter operation, the sectors must be changed 12 times according to the grid period (50 Hz). According to the sector changes, a path must always be ensured for the ac grid current.

To ensure this, an intermediate freewheeling state is used between the different sectors. It allows to create a path for the inductor currents. When the sector changes, small distortions can be observed in the input current. However, is necessary to note that the selected switching frequency is high enough to avoid generating any THD issues, which is also a design parameter, previously defined in Table 2. According to the experimental results, the measured THD was 4.2% at 1.75 kW which represent 50% of the nominal power.

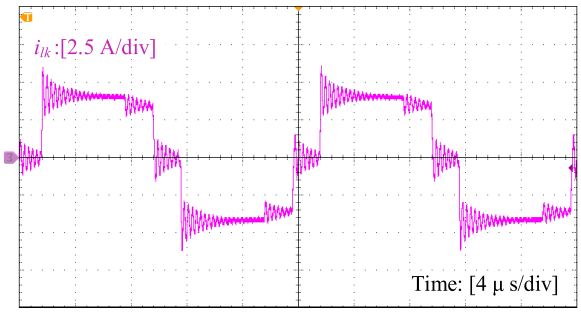

FIGURE 19. Transformer leakage current during the rectifier operation mode.

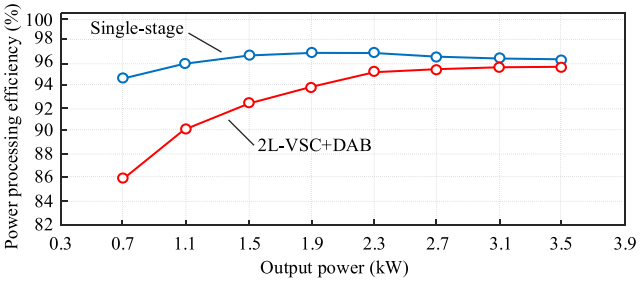

FIGURE 20. Experimental efficiency curves.

To compare the waveforms for both operation modes, inverter (dc-to-ac) and rectifier (ac-to-dc), Fig. 19 presents the transformer current (i_{lk}) during the rectifier operation. In this case, the leg commutation will always decrease the absolute value of the transformer current, while the previously results presented the current decreasing during the rectifier operation mode. This is according to the present theoretical waveforms, proving the bidirectionality of the proposed converter.

B. EFFICIENCY EVALUATION AND DISCUSSION

To evaluate the converter efficiency, the experimental prototype was tested over a wide power range, and the data were acquired with the power analyzer Yokogawa WT 1800. In addition, to compare the experimental results with an industrial approach, a second prototype was built based on a two-stage solution (ac-dc/dc-dc), including a two-level voltage-source converter (2L-VSC) at the ac-dc stage, and a conventional dual-active bridge (DAB) converter for isolation. To provide a fair comparison, both prototypes were designed following the parameters presented in Table 2, including same semiconductors, transformer, inductors, and switching frequency.

Fig. 20 presents both measured efficiency curves. Initially is noticed that due to the full soft-switching range, provided by the proposed modulation sequence, the single-stage solution presents a very flat efficiency curve, being higher than 95% from 700 W, which represent 20 % of the nominal power. The peak efficiency was measured at 2.3 kW, resulting in 96.7 %, and at nominal power 96.5%.

For the two-stage solution, is not possible to ensure a flat efficiency curve. It can be explained because, the dual-active bridge converter, applied on the isolation stage have limitations in terms of circulating current, and soft-switching at low power. These issues are extensively discussed in the current literature, and readers seeking additional insights can refer to [34] as a supplementary reference for further information.

Furthermore, it is observed that the peak efficiency, measured at nominal power, is 95.4%. The lower efficiency in this solution is primarily due to the presence of two power processing stages. In the single-stage solution, the total input current is processed only once, at the matrix-converter stage. However, the two-stage solution requires processing the same current twice, resulting in increased conversion losses.

V. CONCLUSION

Single-stage isolated dc-ac converters based on three-phase high-frequency link topology can be an attractive alternative to widely adopted two-stage converter with intermediate dc link. Topologies with matrix-converter of a current-source type offer the advantage of reduced conduction losses and computation burden. At the same time, the problems related to voltage spikes, switching losses and lack of optimal modulation methods suited for bidirectional operation hindered their adoption in practical applications.

To contribute to further development of such topologies, this paper presented a modulation strategy to provide full-range soft switching and low energy circulation, which ensures high and flat efficiency curve under all operation range. The proposed method provides the following benefits:

- ZVS turn-on and soft turn-off of the dc-side transistors at all loads, reducing their switching losses.
- All matrix stage switches will spend 1/6 of a grid frequency period in the on-state, effectively reducing the switching frequency of the matrix-converter to 5/6 of the switching frequency.
- The method uses only matrix-converter for the current regulation and does not require a modulation scheme change with variation of ac voltage, dc voltage or power level. The same underlying principle provides both rectifier and inverter operation using the same hardware design.

At the same time, there are several design challenges that must be considered. The voltage ringing problem at the matrix-converter still remains and in general, cannot be completely solved with modulation scheme only. Slight voltage overrating approach used in this paper can be an acceptable solution. The transformer leakage inductance should preferably be minimized to reduce the duty-cycle loss related to matrix-converter commutations.

The experimental results with 3.5 kW prototype demonstrated that, despite abovementioned challenges, with the proposed modulation it is possible to develop isolated ac-dc interface converter that features relatively flat efficiency curve and reaches peak value of 96.7% at 2.3kW, while the conventional two-stage solution results in only 95.4% of peak

efficiency. The properties of SiC MOSFETs have improved the performance of matrix-converter stage due to superior reverse recovery behaviour and reduced conduction losses at part load. Such characteristics are exactly what is required for i-AFE application, where a large amount of energy is processed at low power levels. With the emerging of monolithic bidirectional devices, like GaN-based HEMTs, the required semiconductor count can be potentially reduced by 37.5%, making the concept even more attractive for the industry. Therefore, isolated ac-dc converter based on a three-phase high frequency link topology can be a suitable solution for such emerging applications as battery storage, EV chargers and i-AFE stage for dc microgrids.

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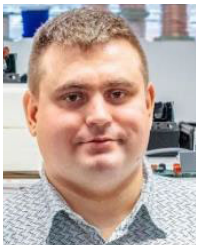

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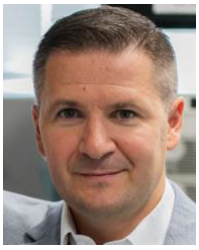

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