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RESEARCH ARTICLE

High Step-Up Common Grounded Switched Quasi Z-Source DC–DC Converter Using Coupled Inductor With Small Signal Analysis

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ABSTRACT In this article, a new common grounded switched quasi Z-source DC-DC converter is proposed. In the proposed converter, an additional switch and a diode are used compared to the conventional quasi Z-source converter. The proposed converter provides some benefits by using a coupled inductor and switched capacitor unit. These features are providing voltage-boosting capability using a small range of duty cycles, low voltage stress on semiconductors (switches and diodes), and continuous input current waveform. In this topology, the null of the load is connected to the negative terminal of the input DC source, directly. So, the common mode voltage is kept constant. In this case, the proposed DC-DC converter is suitable for photovoltaic (PV) power generation systems to boost the voltage of PV panels. In this paper, the proposed converter and operation modes are described completely. Also, in order to show the advantages and differences of the proposed topology with other DC-DC high-step up converters, a comparative comparison study is considered. Also, the small signal analysis and control strategy of the proposed converter are provided. In addition, design considerations of the used components are given. Then, the power loss analysis of the converter is provided. Finally, in order to prove the accurate performance of the suggested topology and verify the advantages and analysis, an experimental prototype is built at 250 W output power and the related results are provided.

INDEX TERMS DC-DC converter, common grounded converter, coupled inductor, quasi Z-source converter.

I. INTRODUCTION

Recently, high step-up power electronics converters are most applicable in various fields such as electric vehicles (EVs), photovoltaic (PV) grid-tied systems, microgrids, and uninterruptible power supplies (UPSs) [1], [2], [3], [4], [5], [6], [7], [8]. For this purpose, many types of research and articles are published regarding to the high step-up DC-DC converters with different topologies [9], [10], [11], [12], [13]. In isolated DC-DC topologies, increasing the turns ratio of the transformer leads to emerging a large parasitic inductance, which can generate high voltage spikes, high switching losses, and intensify the electromagnetic interference (EMI) [14]. These topologies have some benefits such as high step-up feature, and isolation of the input DC supply from the output. Meanwhile, compared with non-isolated structures, these topologies usually have lower power density, higher voltage and current stress on the semiconductors, higher cost per watt, higher power losses, and lower overall efficiency [15].

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Compared with single-stage topologies, multi-stage converters have some drawbacks such as higher power losses and lower efficiency, lower reliability, and using a large number of circuit components [16]. As a result, the single-stage structures with the reduced number of circuit components provide low cost and a large value of duty cycle (close to 1). This issue leads to low efficiency with high value of current ripple.

Some other high step-up non-isolated single-stage switched inductor-based, switched capacitor-based, or coupled inductor-based DC-DC converters with large duty cycles have been presented in [17], [18]. Among single-stage topologies, the Z-source converters usually operate with a low range of the duty cycle (less than 0.5) [19]. Note that, Z-source topologies can be used as DC-DC converters [20]. In order to overcome the drawbacks of Z-source topology, a quasi Z-source structure with continuous input current has been introduced in [21]. Meanwhile, Z-source-based topologies provide low voltage gain and high voltage stress on the power switches and diodes.

In order to improve the voltage gain and decrease the voltage stress of the semiconductors, some other topologies based on quasi Z-source structure are proposed. An isolated quasi Z-source-based converter using an H-bridge inverter is presented in [22]. This converter uses a large count of switches and diodes, but it cannot provide the voltage boosting feature. Furthermore, to enhance the voltage gain, the turns ratio of the transformer should be increased which causes high parasitic inductance and low efficiency. A new isolated Z-source topology has been presented in [23]. This topology uses two power switches and the range of the duty cycle is more than 0.5. Note that, this converter cannot provide high step-up voltage feature. In [24], a cascaded quasi Z-source DC-DC converter is processed which has low efficiency due to the large number of elements. A wide input voltage range quasi Z-source DC-DC converter with two switches is proposed in [25] which can't produce high voltage gain and the voltage stress on switches is high.

In addition, in [26] and [27], new Z-source structures using switched inductor and switched capacitor units are proposed. All these converters are introduced with the aim of voltage gain increasing and have own disadvantages such as high voltage stress on switches and lack of common ground between input and output. In [28], a non-isolated Z-source converter with a coupled-inductor leads to low voltage stresses on the semiconductors. But this topology requires more components and the ground nodes of load and input ports are not the same. A switched quasi Z-source converter with small duty cycle is presented in [29], which cannot reach high voltage gain. Also, the voltage across the switches is high and the topology is not common ground. In [30], a new Z-source switched capacitor-based topology has been introduced. This converter provides a high voltage boosting gain using two power switches. The topology uses a large number of inductors and capacitors. This issue leads to increase the total power loss, volume and cost of the system. Also, the power density and overall efficiency are decreased.

In this paper, a new high step-up common ground switched quasi Z-source converter with a coupled inductor and a voltage multiplier cell is proposed. This converter can reach high voltage gain with a small range of duty cycle, continuous input current, low voltage stress across power switches and the output diode. In addition, it doesn't need high turns ratio for the coupled inductor to realize high voltage levels. Note that, this paper is the expansion of our previous conference paper [10] where the theoretical analysis and comparison study are improved, the small signal model and closed-loop control are added, and comprehensive experimental tests are performed.

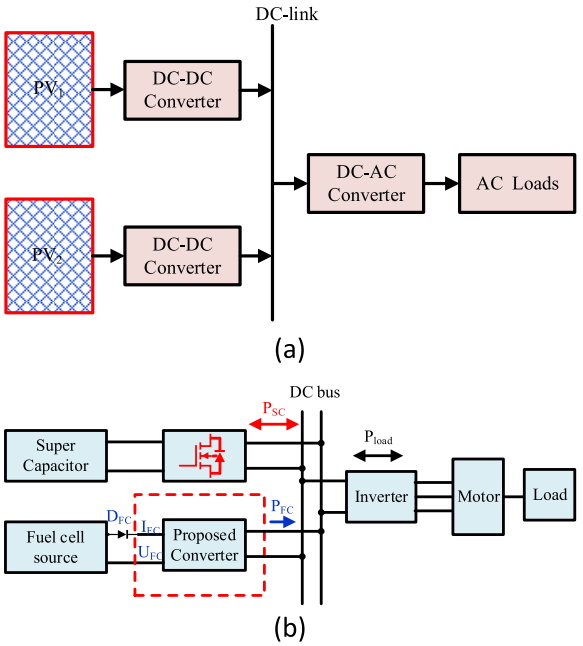


FIGURE 1. (a) Photovoltaic panels with DC-DC converters, (b) Fuel cell vehicles with DC-DC converter.

In most of the coupled inductor-based converters, leakage inductance is one of the critical issues; because, increasing the leakage inductance causes higher output voltage drop, higher current passing through the power switches, large duty cycle. All these disadvantages induce the converter operation with high losses and low efficiency. The higher turns ratio and the number of windings turns are important factors for higher leakage creation. In the proposed converter, the magnetic inductance of the coupled inductor is low in the continuous conduction mode (CCM) operation which causes a smaller number of windings turns for the primary side of the coupled inductor. On the other hand, the turns ratio of the coupled inductor is low due to the high voltage gain. Consequently, the leakage inductance of the presented converter is lower than the most of other high step-up converters. High voltage gain with small duty cycle, low leakage inductance of coupled inductors, continuous input current, low voltage stress

on power switches, low voltage stress on some diodes, low voltage stress of some capacitors, common ground between input voltage source and output terminals are the main advantages of the proposed converter.

For the above-mentioned properties, the proposed converter can be used in renewable energy applications such as photovoltaic panels which is illustrated in Fig. 1(a). When one photovoltaic panel is connected to a DC-DC converter, it needs a large duty cycle to increase the level of the input voltage source to the desired DC link voltage value. In the proposed converter not only the total conduction losses of the switches will be decreased due to the lower duty cycle, but also the cost of the converter will be decreased. These advantages decrease the total losses of the converter and decrease the volume and cost of the DC-DC converter instead of a converter with a large duty cycle and low efficiency. As well as in Fig. 1(a), the DC link can be considered as a high voltage DC micro-grid that can be connected to the AC grid or AC load with an inverter.

In addition, the proposed converter can be utilized in the electrical fuel cell vehicles which have two input voltage sources. These two input voltage sources consist of a supercapacitor and a fuel cell. In this case, the proposed converter can be used instead of the converters with fuel cell voltage sources which are shown in Fig. 1(b). To return the energy from the output port to the supercapacitor or input energy source and better operation, the diodes of the proposed converter are replaced with the power MOSFETs and a diode is connected to a fuel cell in series. Using a series diode in a fuel cell is an important way to connect a common ground DC-DC converter between a high voltage DC link and a fuel cell. As a result, the proposed topology can be an interesting converter for these kinds of industries. For EV applications with battery or supercapacitors input source, it is better to use isolated bidirectional DC-DC converters. This kind of application is used in reference [25], because the input voltage of the presented converter can be in a wide range, and the output voltage can be controlled for a constant voltage of the DC link.

For the proposed converter, the operating principle and steady-state analysis are evaluated in detail. Also, parameters design and the comparison with some Z-source DC-DC converters are given. Finally, the experimental results are presented which verifies the theoretical analysis.

II. SUGGESTED TOPOLOGY, STEADY STATE ANALYSIS, AND OPERATION MODES

Fig. 2 illustrates the proposed switched quasi Z-source topology. Considering this figure, the proposed converter uses two power switches, five diodes, five capacitors, one inductor, and one coupled inductor. Compared with the basic topology of the Z-source topology, the proposed converter uses an additional power switch and one more diode. Furthermore, the proposed converter uses a switched capacitor unit. Considering Fig. 2, the Z-source network consists of the capacitors C_1 and C_2, switch S_2, diode D_1, input inductor L_{in}, and the primary side of the coupled inductor L_p. Based on Fig. 2, the primary side of the coupled inductor is modeled by a leakage inductance L_{lk} .Note that, the magnetizing inductance and secondary side of the coupled inductor L_s is applied to boost the voltage level which is tied to the diodes D_3, $D_4$and capacitor C_3. Considering Fig. 1, it can be seen that the switched capacitor consists of two capacitors (C_3 and C_4) and two diodes (D_3 and D_4). In the proposed converter, the output capacitor (C_O) is considered with a high capacitance value. The suggested topology operates in the CCM. As a result, the input inductor is chosen large enough and the input voltage is fixed to a constant value. In a full switching cycle, the proposed converter has four operational modes. Fig. 3 illustrates the voltage and current waveforms of the proposed topology. Moreover, the operation modes of the proposed converter are depicted in Fig. 3. In the following, the description of each operation mode is provided completely.

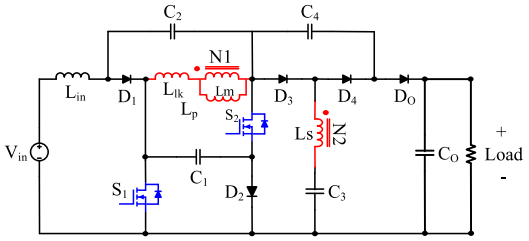


FIGURE 2. The power circuit of the proposed converter.

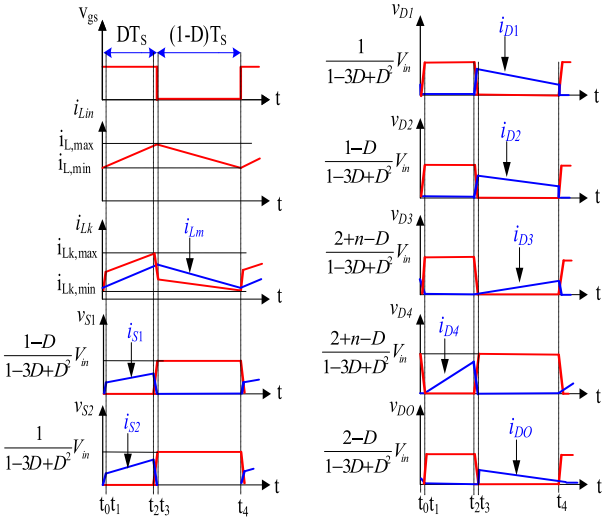


FIGURE 3. Voltage and current operational waveforms of proposed converter.

A. FIRST OPERATION MODE [t_0 - t_1]

The First operation mode is shown in Fig. 4 (a). In this operation mode, the power switches S_1 and S_2 are in the on-state. Also, the diodes D_3 and D_O are in the on-state, and the diodes D_1, D_2 and D_4 are in the reverse bias. During this operation mode, the input inductor is charged through the capacitors C_1 and C_2, and the input DC source (V_{in}). Also,

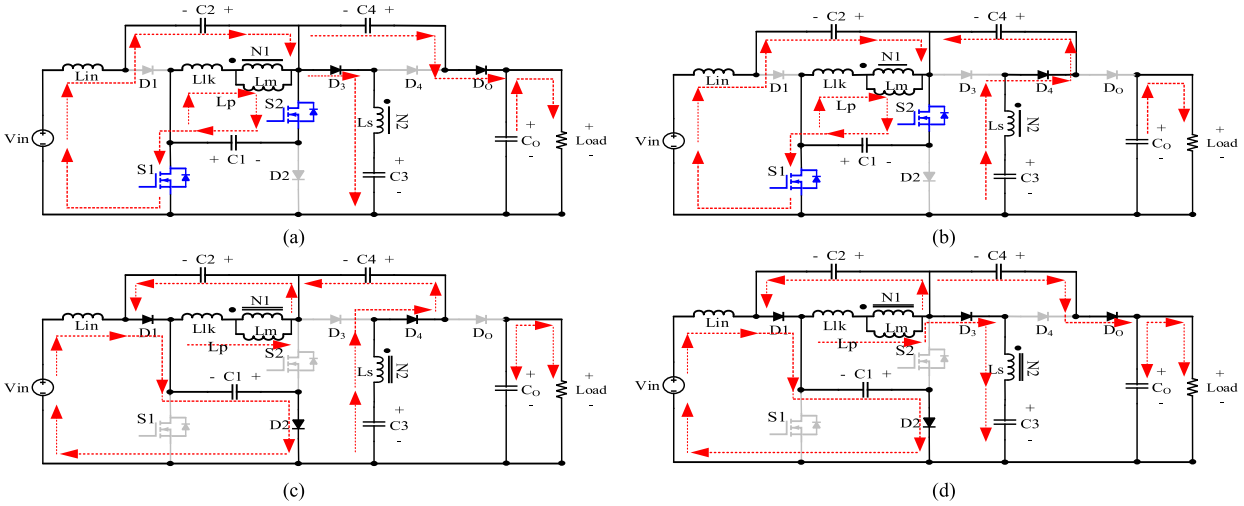


FIGURE 4. The equivalent circuits of the proposed converter: (a) First mode; (b) Second mode; (c) Third mode; (d) Forth mode.

the inductor L_m is charged by the stored energy of capacitor C_1 during this mode. In addition, the stored energies of the capacitors C_1, C_2 and C_4 are pumped to the output terminal. Note that, this operation mode ends at the moment t_1.

B. SECOND OPERATION MODE [t_1 - t_2]

The electrical schematic of the second operation mode is demonstrated in Fig. 4(b). Based on this figure, it can be seen that in this mode the switches S_1 and S_2 should be turned on. Moreover, the diodes D_1, D_2, D_3 and D_O are in the off-state and the diode D_4 turns on. In this mode, the input inductor is in the charging state as the same as the first operation mode. As a result, the current of L_{in} increases linearly.

Furthermore, the primary side of the coupled inductor is still in the charging state through the capacitor C_1. During this mode, the currents of the leakage inductor and magnetizing inductor increase linearly. The capacitor C_4 is in the charging state through the capacitors C_1 and C_3; hence, the current of the secondary side of the coupled inductor reduces. Moreover, the output load is supplied by the stored energy of the output capacitor C_O.

C. THIRD OPERATION MODE [t_2 - t_3]

The electrical circuit of this operation mode is illustrated in Fig. 4(c), where the switches S_1 and S_2 are in the off-state. Also, the diodes D_1, D_2, and D_4 are in the on-state and the diodes D_3 and D_O are in the off-state. Note that, the capacitor C_1 is in the charging state through the input power supply and input inductor. In this mode, the capacitor C_2 is in the charging state through the primary side of the coupled inductor. It should be mentioned that, mode three ends at the moment t_3.

D. FOURTH OPERATION MODE [t_3 - t_4]

The current path of this operation mode is expressed in Fig. 4(d). Considering this figure, the switches S_1, S_2 and the diode D_4 are in the OFF state. Also, the diodes D_1, D_2, D_3 and D_O are in the on-state. Regarding Fig. 4(d), the capacitor C_1 is still in the charging state by the stored energy of the input inductor and the input DC source. In addition, the capacitor C_2 is charged by the primary side of the coupled inductor; therefore, the primary side current reduces linearly. In this mode, the capacitor C_O and the load are fed by the input DC source, L_{in}, the primary side of the coupled inductor and capacitor C_4.

Regarding the second and fourth operation modes, as the main CCM operational modes, and applying the voltage-second balance law to the aforementioned inductors in a full switching period, the voltage values of the capacitors C_1, C_2 are attained with respect to the input voltage V_{in} as follows:

$$\begin{cases} V_{C1} = \dfrac{1-D}{1-3D+D^2} V_{in} \\ V_{C2} = \dfrac{D}{1-3D+D^2} V_{in} \end{cases} \tag{1}$$

In the above equations, D denotes the switching duty cycle of the involved switches. The equations of the voltage across L_{in}, V_{LP}, V_{LS}, and V_{LO} can be obtained by using KVL in the fourth operation mode. By using these obtained equations and (3), and by omitting the L_{lk}, the voltage across the capacitor C_3 can be expressed as

$$V_{C3} = \frac{1+nD}{1-3D+D^2} V_{in} \tag{2}$$

Here, $n = N_2/N_1$ denotes the turns ratio of the coupled inductor. By considering the Kirchhoff voltage law (KVL) in the second operation mode, and applying (1), and (2), the voltage across the capacitor C_4 is obtained as:

$$V_{C4} = \frac{2+n-D}{1-3D+D^2} V_{in} \tag{3}$$

By substituting (1), (3), and the equations of the voltage across L_{in}, V_{LP}, V_{LS}, and V_{LO} which can be obtained by using

KVL, the output voltage of the proposed converter is obtained as:

$$V_O = \frac{3+n-D}{1-3D+D^2} V_{in} \tag{4}$$

Hence, the voltage gain of the suggested topology is concluded as:

$$G = \frac{V_O}{V_{in}} = \frac{3+n-D}{1-3D+D^2} \tag{5}$$

Assuming that the losses are negligible and by applying the Kirchhoff voltage law (KVL) in the second operation mode, the input current of the converter can be expressed as:

$$I_{in} = \frac{3+n-D}{1-3D+D^2} I_O \tag{6}$$

Then, the average value of the input inductor current is equal to I_{in}:

$$i_{Lin} = \frac{3+n-D}{1-3D+D^2} I_O \tag{7}$$

Using KCL law in the fourth operation mode, the average current of L_{lk}, magnetizing inductance and the secondary side of the coupled inductor are calculated as:

$$\begin{cases} i_{lk-off} = i_{C2-off} + {}_{C3-off} + {}_{C4-off} \\ i_{lk-off} = \dfrac{2-(3-n)D+D^2}{\left(1-3D+D^2\right)(1-D)} I_O \\ i_{Lm} = i_{lk-off} + n i_{NS-off} \\ i_{Lm} = \dfrac{2+n-(2n+3)D+(1+n)D^2}{\left(1-3D+D^2\right)(1-D)} I_O \end{cases} \tag{8}$$

In one switching cycle, the average current of the inductor L_m is constant.

III. DESIGN OF PARAMETERS

For the appropriate operation of the proposed converter, the input inductor, the magnetizing inductance and the capacitors should be designed. By using the voltage and current equations (which can be obtained by applying KVL rule in the second operation mode) and (7) for the input inductor, the value of the input inductance can be calculated as follows:

$$L_{in} = \frac{D\left(2-3D+D^2\right)V_{in}^2}{\left(1-3D+D^2\right)P_{in} f_S I_r} \tag{9}$$

In addition, by ignoring the leakage inductance and using the voltage and current equation (which can be obtained by applying KVL and KCL in the fourth operation mode) and (8) for the magnetizing inductor, the magnetizing inductance can be calculated as follows:

$$L_m = \frac{D(1-D)^2(3+n-D)V_{in}^2}{\left(1-3D+D^2\right)\left(2+n-(2n+3)D+(1+n)D^2\right)P_{in} f_S I_r} \tag{10}$$

where, P_{in} is the input power, f_S is the switching frequency, and I_r is the current ripple percentage of the inductors.

By consideration of the equations (1)-(3), all capacitors can be designed as below:

$$\begin{cases} C_1 \geq \dfrac{\left(1+n+(2-n)D-D^2\right)(3+n-D)}{(1-D)\left(1-3D+D^2\right)V_r f_S R_L} \\ C_2 \geq \dfrac{(3+n-D)^2}{\left(1-3D+D^2\right)V_r f_S R_L} \\ C_3 \geq \dfrac{(3+n-D)}{(1+nD)V_r f_S R_L} \\ C_4 \geq \dfrac{(3+n-D)}{(2+n-D)V_r f_S R_L} \\ C_o \geq \dfrac{D}{V_r f_S R_L} \end{cases} \tag{11}$$

where, R_L is the load resistance, V_r is the voltage ripple percentage of the capacitors, and f_S is the switching frequency.

IV. SMALL SIGNAL ANALYSIS AND CONTROL METHOD

In the proposed converter, the input and the magnetizing inductors currents (i_{Lin} and i_{Lm}), and the capacitors voltages (V_{C1} and V_{C2}) are chosen as state variables. Therefore, the state variables vector (x), input vector (u), and output vector (y) are considered as follows:

$$\begin{cases} x^T = [i_{\mathrm{Lin}} i_{\mathrm{Lm}} V_{C1} V_{C2}] \\ u^T = [d] \\ y^T = [V_{out}] \end{cases} \tag{12}$$

By using the main modes for the presented converter (modes 2 and 4), the average state space of the system can be considered as $\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases}$.
where, matrixes A, B, C and D are constant and can be attained as (13) and (14).

$$\begin{bmatrix} \frac{di_{Lin}}{dt} \\ \frac{di_{Lm}}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{2d-1}{L_{m1}} & \frac{d}{L_{m1}} \\ 0 & 0 & \frac{d}{L_{m2}} & \frac{d-1}{L_{m2}} \\ \frac{1-d}{C_1} & \frac{-d}{C_1} & -\frac{(3+n)(2+n)}{C_1 R_{Load}} & -\frac{(2+n)^2}{C_1 R_{Load}} \\ \frac{-d}{C_2} & \frac{1-d}{C_2} & -\frac{(3+n)(2+n)}{C_2 R_{Load}} & -\frac{(2+n)^2}{C_2 R_{Load}} \end{bmatrix} \times \begin{bmatrix} i_{Lm1}(t) \\ i_{Lm2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{in}} \\ 0 \\ 0 \\ 0 \end{bmatrix} [u_{in}(t)] \tag{13}$$

$$y^T = [V_{out}] = [00\,(3+n)\,(2+n)] \begin{bmatrix} i_{Lin}(t) \\ i_{Lm}(t) \\ u_{C1}(t) \\ u_{C2}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [u_{in}(t)] \tag{14}$$

Based on the method of small-signal modeling, the state variables, output, input voltages and duty cycles contain of two parts of DC ($\bar{X}$, $\bar{Y}$, $\bar{U}$, $\bar{D}$) and AC ($\tilde{x}$, $\tilde{y}$, $\tilde{u}$, $\tilde{d}$).

It is supposed that the AC values are small and do not change considerably during one switching period. Therefore, the small-signal model can be displayed as $\begin{cases} \dot{\tilde{x}} = A'\tilde{x} + B'\tilde{u} \\ \tilde{y} = C'\tilde{x} + D'\tilde{u} \end{cases}$.

TABLE 1. The nominal resistance values of various components.

Devices	values
Power MOSFETs S_1 & S_2	R_{DS} = 0.097Ω t_f = 74 *ns* , t_r = 105 *ns*
Diode D_1	R_{D1} = 0.0047Ω V_{FD1} = 1.1 V
Diode D_3, D_4 & D_O	R_D = 0.025Ω V_{FD1} =0.95 V
Diode D_2	R_D = 0.025Ω V_{FD1} =0.95 V
Capacitors	$r_{C1} = r_{C2} = r_{C3} = r_{C4} = r_{CO}$ = 0.02Ω
L_{in},	r_{Lin} = 0.02Ω
L_{lk} & L_{NS}	$r_{Llk} = r_{LNS}$ = 0.02Ω

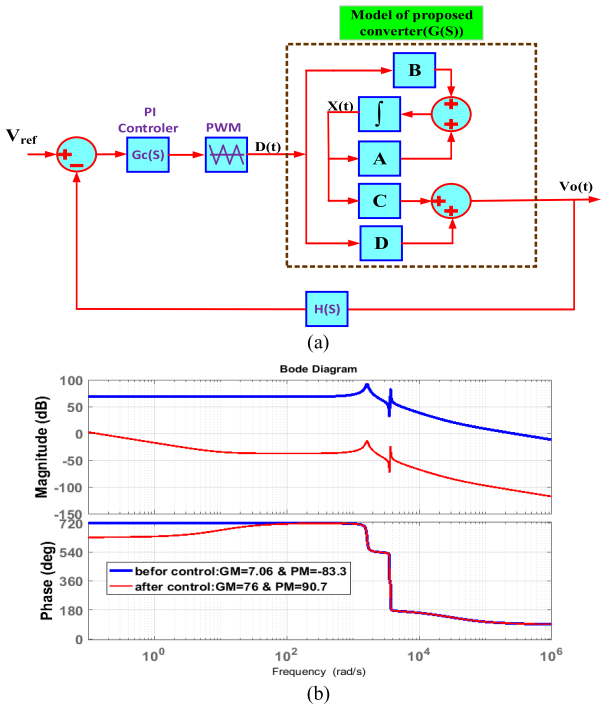


FIGURE 5. (a) Bode plots of presented converter (b) Closed-loop control system block diagram.

where, A', B' and C' are calculated in (15) and (16).

$$A' = \begin{bmatrix} 0 & 0 & \frac{2\bar{D}-1}{L_{in}} & \frac{\bar{D}}{L_{in}} \\ 0 & 0 & \frac{\bar{D}}{L_{m2}} & \frac{\bar{D}-1}{L_{m2}} \\ \frac{1-\bar{D}}{C_1} & \frac{-\bar{D}}{C_1} & -\frac{(3+n)(2+2n)}{C_1 R_{Load}} & -\frac{(2+n)^2}{C_1 R_{Load}} \\ \frac{-\bar{D}}{C_2} & \frac{1-\bar{D}}{C_2} & -\frac{(3+n)(2+2n)}{C_2 R_{Load}} & -\frac{(2+n)^2}{C_2 R_{Load}} \end{bmatrix} \quad (15)$$

$$B' = \begin{bmatrix} \frac{2\bar{V}_{C1}+\bar{V}_{C2}}{L_{m1}} \\ \frac{\bar{V}_{C1}+\bar{V}_{C2}}{L_{m2}} \\ -\frac{\bar{I}_{Lin}}{C_1} - \frac{\bar{I}_{Lm}}{C_1} \\ -\frac{\bar{I}_{Lin}}{C_2} - \frac{\bar{I}_{Lm}}{C_2} \end{bmatrix}, C' = [00\,(3+n)\,(2+n)] \quad (16)$$

Considering the specifications of the devices from Table 1, the matrixes A', B' and C' can be calculated. Therefore, the transfer function of the presented converter before the implementation of the control system can be attained as (17).

$$G(s) = \frac{-2.5\times10^5 s^3 + 7.5\times10^9 s^2 - 3.3\times10^{12} s + 9.6\times10^{16}}{s^4 + 114.9 s^3 + 1.6\times10^7 s^2 + 1.3\times10^9 s + 3.6\times10^{13}} \quad (17)$$

According to (52), it can be observed that all the poles are located on the left side of the $j\omega$ axis; however, some of them are close to the imaginary axis. This means the open-loop system is stable, but it is not desirable. The control block diagram for the presented converter is shown in Fig. 5(a). According to the closed-loop system, $G_C(s)$ is the PI (Proportional-Integral) controller transfer function, $H(s)$ is the feedback transfer function, V_{ref} is the voltage reference signal and V_O is the output voltage signal.

In the PI controller, K_i (integrator coefficient) is set as 0.0002, K_p (proportional coefficient) is set as 0.00001 and $H(s)$ is considered as 0.5. Therefore, the corresponding transfer function of the voltage-loop control system can be expressed in (18), as shown at the bottom of the next page.

The bode plots of the presented converter before and after applying the control system are illustrated in Fig. 5(b). The phase margin (PM) and gain margin (GM) should be positive (PM>0, GM>0) in order to achieve stability. However, these values are −83.3° and 7.6 dB, respectively, for the suggested converter before applying control system. After applying the control system, the values of the PM and GM reach to 90.7° and 76 dB, respectively. Therefore, the closed-loop gain and phase margins are positive and the overall system with PI controller would be desirably stable.

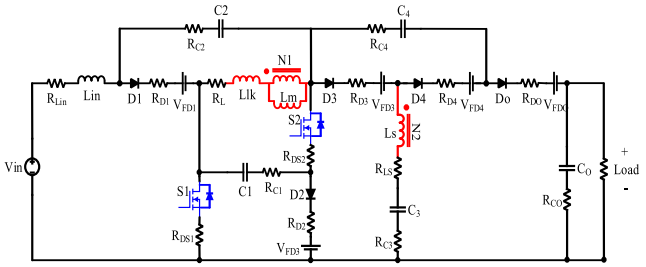


FIGURE 6. Proposed converter with resistances consideration for loss calculation.

V. POWER LOSS ANALYSIS

In this section, the power losses for all components are calculated. Then, the efficiency of the proposed converter with respect to the output power and the associated total losses can be achieved. At last, the theoretical efficiency is compared with experimental efficiency. Fig. 6 shows the proposed converter with all series resistances for each component to calculate the losses. The nominal resistance values and RMS current values for various components are summarized in Table 1 and Table 2, respectively. By using these nominal values and considering Table 2, the power losses for the power switches, diodes, capacitors and inductors, and the

TABLE 2. RMS Current values for various components.

Device	RMS currents
S_1	$\frac{1+nD}{(1-3D+D^2)D}\sqrt{D}I_O$
S_2	$\frac{1+n+(2-n)D-D^2}{(1-3D+D^2)D}\sqrt{D}I_O$
D_1	$\frac{3+n-D}{(1-D)(1-3D+D^2)}\sqrt{1-D}I_O$
D_2	$\frac{1+n+(2-n)D-D^2}{(1-3D+D^2)(1-D)}\sqrt{1-D}I_O$
D_3	$\frac{\sqrt{1-D}}{1-D}I_O$
D_4	$\frac{\sqrt{D}}{D}I_O$
C_1	$\left(\frac{1+n+(2-n)D-D^2}{(1-3D+D^2)}\right)\sqrt{\frac{1}{D(1-D)}}I_O$
C_2	$\frac{(3+n-D)}{(1-3D+D^2)}\sqrt{\frac{D}{(1-D)}}I_O$
C_3 & C_4	$\frac{1}{\sqrt{D(1-D)}}I_O$
C_O	$\sqrt{\frac{D}{1-D}}I_O$
L_{in},	$\sqrt{\frac{1}{3}[(2GI_o)^2-GI_o^2+(DV_o/2Lf_sG)^2]}$
L_{lk}	$i_{Lk}=\sqrt{i_{Lm}^2+(nI_O)^2\left(\frac{1}{D(1-D)}\right)}$
L_{NS}	$i_{LNS}=\frac{I_O}{\sqrt{D(1-D)}}$

total power loss are calculated as

$$\begin{cases} P_S = P_{Con} + P_{Sw} = R_{DS-on} i_{S,RMS}^2 \\ \quad +0.5 f_s \left(t_r + t_f\right) i_{S,av} V_s \\ P_D = \sum_1^n \left(V_{FD} i_{Dn,av} + r_d i_{Dn,RMS}^2\right) \\ P_C = \sum_1^n r_C i_{Cn,RMS}^2 \\ P_L = r_{Lin} i_{Lin,RMS}^2 + r_{Llk1} i_{Llk1,RMS}^2 + r_{Llk2} i_{Llk2,RMS}^2 \\ P_{Loss-Total} = P_S + P_D + P_C + P_L \end{cases} \tag{19}$$

By using above mentioned equations, the power losses of switches S_1, and S_2, total power losses of diodes, total power losses of capacitors, power losses of inductors, and total power losses of proposed converter can be obtained and are equal to 0.7W, 1.71W, 10.66W, 1.47W, 1.2W, and 15.74W,

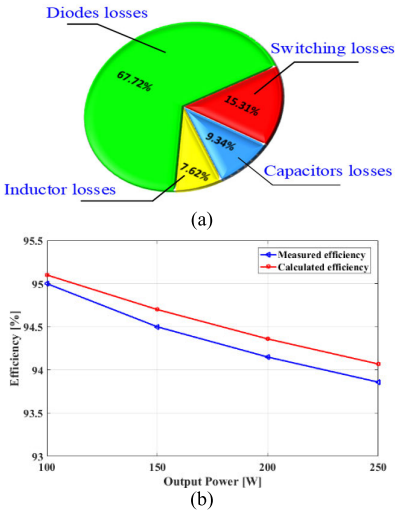


FIGURE 7. (a) Different component Loss for proposed converter, (b) measured efficiency of proposed converter.

respectively. Therefore, the theoretical efficiency of the proposed converter is obtained and equal to 94.07%. From the theoretical equations and nominal values for the omponent, the calculated efficiency at output power of 250 W is obtained as 94.07%. Furthermore, the loss distribution for all components is depicted in Fig. 7(a). Moreover, Fig. 7(b), shows the experimental measured efficiency of the proposed converter for various output power values. The maximum efficiency for the proposed converter is about 95% at 100 W and the measured efficiency at 250 W is about 93.86% where it is 0.39% lower than the estimated efficiency.

VI. COMPARISON STUDY FOR PROPOSED CONVERTER

In this section, in order to show the features of the proposed converter and its differences from other topologies, a comprehensive comparison is done. This comparison is based on some items such as the number of components, voltage gain, duty cycle limitation, maximum normalized voltage stress across the switches and output diode, and component stress for the presented converter and other Z-source-based converters which are listed in Table 3. The numbers of the magnetic cores in the presented converters in [25], [28], [30], and [31] are more than the proposed converter and other converters, considering that an extra magnetic core increases the total losses and cost of the system.

The numbers of the capacitors in [28], [30], and [31] are more than the proposed converter and other converters. Also, the number of switches in [25], [27], [29], [30], and [31] and the proposed converter are the same. Although,

$$G_{CV}(s) = G_C(s)\,G(s)\,H(s) = \frac{-1.2s^4 + 3.7\times10^4 s^3 - 1.5\times10^7 s^2 + 4.7\times10^{11} s + 9.4\times10^{12}}{s^5 + 114.9s^4 + 1.6\times10^7 s^3 + 1.3\times10^9 s^2 + 3.6\times10^{13} s} \tag{18}$$

TABLE 3. Comparison of proposed converter with Z-source based converters.

Ref	Number of				Voltage gain (G)	Duty cycle limitation	Maximum Normalized Stress		Component stress			
	M	C	S	D			V_{Switch}	I_{Switch}	V_{Diode}	I_{Diode}	V_{C1}	i_{Lin}
[21]	2	3	1	2	$\frac{1}{1-2D}$	0<D<0.5	GV_{in}	$\frac{G^2}{(G-1)}I_{in}$	$D_O = GV_{in}$ $D_1 = GV_{in}$	$D_O = I_O$ $D_1 = GI_O$	GV_{in}	GI_O
[25]	3	4	2	3	$\frac{2n}{3-4D}$	0.5<D<0.7	$\frac{GV_{in}}{2n}$	$\frac{(3G-2n+2)G}{(3G-2n)}I_{in}$	$D_2 = GV_{in}$ $D_3 = \frac{GV_{in}}{2}$ $D_1 = \frac{GV_{in}}{2n}$	$D_1 = GI_O$ $D_2 = I_O$ $D_3 = I_O$	$\frac{GV_{in}}{2n}$	GI_O
[27]	2	5	2	5	$\frac{3-3D}{1-3D}$	0<D<0.33	$\frac{(G-1)V_{in}}{2}$	$\frac{4G^2-9G+3}{G(G-3)}I_{in}$	$D_1 = D_2 = \frac{(G-1)V_{in}}{2}$ $D_3 = D_4 = \frac{(G-1)V_{in}}{2}$ $D_O = (G-1)V_{in}$	$D_1 = (G-1)I_O$ $D_2 = D_3 = GI_O$ $D_4 = D_O = I_O$	$\frac{(G-3)V_{in}}{6}$	$(G-1)I_O$
[28]	3	7	1	5	$\frac{1+2n-D}{1-2D}$	0<D<0.5	$\frac{(2G-1)V_{in}}{1+4n}$	$\frac{(2G-1)^2}{G(G-2n-1)}I_{in}$	$D_1 = \frac{(2G-1)V_{in}}{1+4n}$ $D_2 = D_3 = \frac{n(2G-1)V_{in}}{1+4n}$ $D_4 = D_O = \frac{n(2G-1)V_{in}}{1+4n}$	$D_1 = GI_O$ $D_2 = D_3 = I_O$ $D_4 = D_O = I_O$	$\frac{(2G-1)V_{in}}{1+4n}$	GI_O
[29]	2	3	2	3	$\frac{1}{1-4D}$	0<D<0.25	GV_{in}	$\frac{4G}{(G-1)}I_{in}$	$D_O = GV_{in}$ $D_1 = D_2 = GV_{in}$	$D_1 = GI_O$ $D_2 = I_O$ $D_3 = I_O$	GV_{in}	GI_O
[30]	4	7	2	5	$\frac{3+2D}{1-2D}$	0<D<0.5	$\frac{(G+1)V_{in}}{4}$	$\frac{(G-1)(1+G)}{G(G-3)}I_{in}$	$D_1 = D_2 = \frac{(G+1)V_{in}}{4}$ $D_3 = \frac{(G+1)V_{in}}{2}$ $D_4 = D_O = \frac{(G+1)V_{in}}{2}$	$D_1 = GI_O$ $D_2 = GI_O$ $D_4 = D_3 = I_O$ $D_5 = I_O$	$\frac{(G+1)V_{in}}{4}$	$\frac{GI_O}{2}$
[31]	4	6	2	4	$\frac{2}{1-2D}$	0<D<0.5	$\frac{GV_{in}}{2}$	$\frac{2G}{(G-2)}I_{in}$	$D_1 = D_3 = GV_{in}$ $D_2 = D_4 = \frac{GV_{in}}{2}$	$D_1 = D_2 = \frac{GI_O}{2}$ $D_4 = D_3 = I_O$	$\frac{GV_{in}}{2}$	$\frac{GI_O}{2}$
[32]	2	5	1	4	$\frac{2+n}{1-2D}$	0<D<0.5	$\frac{GV_{in}}{2+n}$	$\frac{(4+2n)G-2n^2-6n-4}{(G-n-2)(2+n)}I_{in}$	$D_1 = D_O = \frac{GV_{in}}{n+2}$ $D_3 = D_4 = \frac{(n+1)GV_{in}}{n+2}$	$D_1 = GI_O$ $D_4 = D_3 = I_O$ $D_O = I_O$	$\frac{GV_{in}}{n+2}$	GI_O
[33]	3	4	1	5	$\frac{M+1}{(1-D)^2}$	0<D<1	$\frac{GV_{in}}{M+1}$	$D(2-D)Iin$	$D_{M1} = D_{M2} = D_O = \frac{GV_{in}}{M+1}$ $D_1 = D_2 = \frac{DGV_{in}}{M+1}$	$D_1 = DGI_O$ $D_2 = (1-D)GI_O$ $D_O = I_O$	$\frac{(1-D)GV_{in}}{M+1}$	GI_O
[34]	2	3	2	3	$\frac{1+D}{(1-D)^2}$	0<D<1	$\frac{(1-D)GV_{in}}{1+D}$ GV_{in}	$\frac{G}{1-D}Iin$	$D_1 = D_2 = \frac{(1-D)GV_{in}}{1+D}$ $D_O = \frac{(1+D)GV_{in}}{2}$	$D_1 = \frac{(1-D)}{(1+D)}GI_O$ $D_2 = \frac{(1-D)}{D(1+D)}GI_O$ $D_O = I_O$	$\frac{(1-D)GV_{in}}{1+D}$	GI_O
proposed	2	5	2	5	$\frac{3+n-D}{1-3D+D^2}$	0<D<0.38	Eqs (20)-(21)	Eq (22)	Eq (23)-(26)	$D_1 = GI_O$ $D_2 = I_{S2}$ $D_4 = D_3 = I_O$ $D_O = I_O$	$V_{C1} = V_{D2}$	GI_O

S: switch, D: Diode, C: Capacitor, M: Magnetic core, Cm Gnd: Common Ground.

$$I_{S1} = \frac{2G\left(2G^2+3nG^2-nG-G\sqrt{5G^2+(6+4n)G+1}\right)I_O}{\left(3G+2nG+1\sqrt{5G^2(6+4n)G+1}\right)\left(3G-1-\sqrt{5G^2(6+4n)G+1}\right)},\quad I_{S2} = \frac{G\left(2G^2-2nG^2-2nG-28G-1+(2G+2nG+2)\sqrt{5G^2+(6+4n)G+1}\right)I_O}{\left(3G+2nG+1\sqrt{5G^2(6+4n)G+1}\right)\left(3G-1-\sqrt{5G^2(6+4n)G+1}\right)}$$

$$D = \frac{2G-\sqrt{4G^2-4G(G-M-1)}}{2G}\ for[33],\quad D = \frac{2G+1-\sqrt{8G+1}}{2G}\ for[34]$$

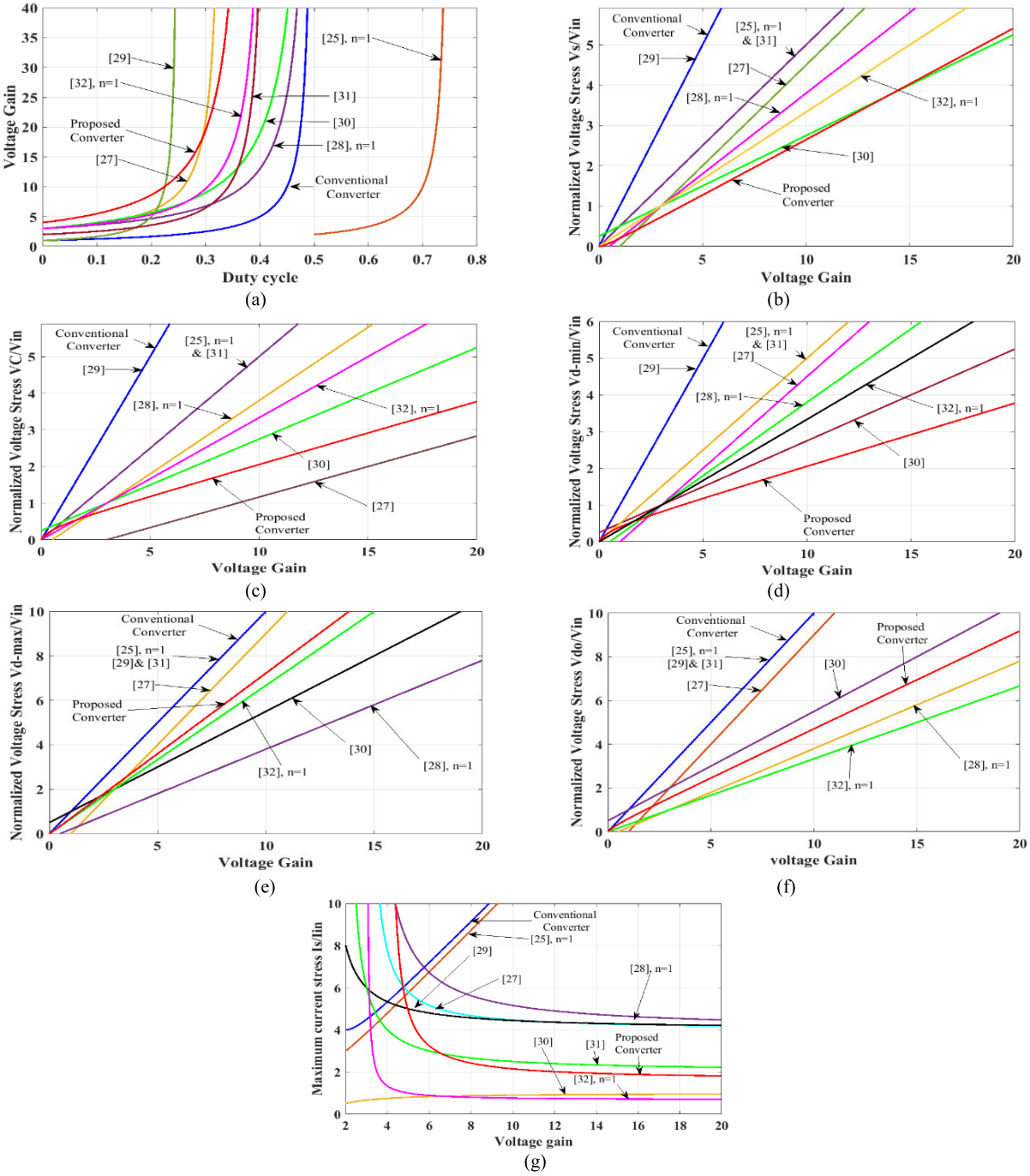


FIGURE 8. Comparison result (a) Voltage gain, (b) Maximum voltage stress of power switches, (c), Voltage stress of main capacitor, (d) Minimum voltage stress of diodes, (e) Maximum voltage stress of diodes, (f) Voltage stress of output diode, (g) Maximum current stress of switches.

the presented converter in [28] have a single power switch, the number of its magnetic cores is higher than the proposed converter. In compare to converters in [33] (considering M = 1) and [34], the proposed converter not only can achieve high voltage gain but also the voltage stresses on semiconductors are lower. Also, the number of inductors in reference [33] are larger than the presented converter which causes higher losses and lower efficiency.

From table 4, the output power and efficiency of the presented converter is higher than the converters in [33] and [34].

Considering Table 3, the equations (20)-(26) can be expressed as follows:

$$V_{S1} = \frac{\left(G - G^2 + G\sqrt{5G^2\left(6+4n\right)G+1}\right)V_{in}}{\left(3G + 2nG + 1 + \sqrt{5G^2\left(6+4n\right)G+1}\right)} \quad (20)$$

TABLE 4. Efficiency Comparison of proposed converter with otherZ-source based converters.

Ref	Frequency (Hz)	Input voltage (V)	Output voltage (V)	Output power (W)	Efficiency (%)	Common ground
[21]	50	24	120	40	94.5	Yes
[25]	10	60	400	800	87	No
[27]	100	40	240	140	98	No
[28]	50	24	300	100	89	No
[29]	25	45	225	185	92.4	No
[30]	100	20	300	200	78	No
[31]	50	40	400	200	92.3	No
[32]	50	60	650	500	96.1	Yes
[33]	50	12	96	40	88	Yes
[34]	50	12	69	150	92	Yes
proposed	40	48	410	250	93.8	Yes

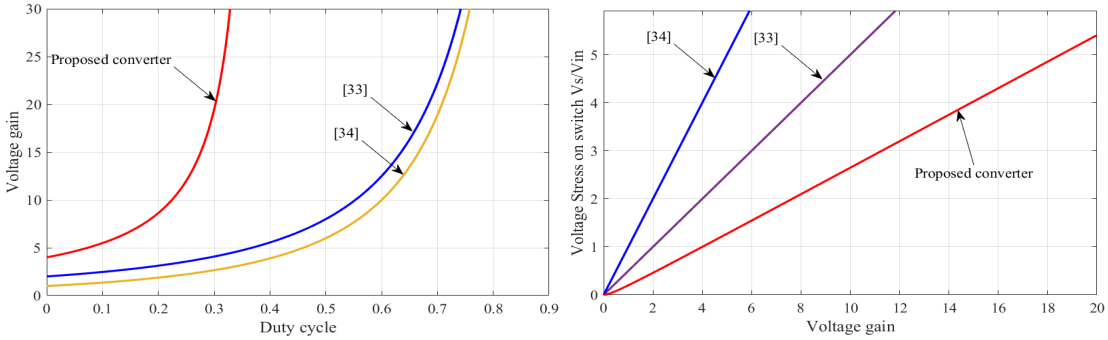


FIGURE 9. Comparison results of proposed converter with quadratic converters, a) Voltage gain, b) Maximum voltage stress on power switch.

TABLE 5. Specifications of devices for experiment.

Components	Specifications
Output Power	250 W
Input-output voltage	48V
Output voltage	410 V
Switching frequency	40 kHz
Capacitors $C1$&$C2$	220 µF
Capacitors $C3$&Co	100µF
Capacitor $C4$	68µF
Input inductor	Lin=550 µH
Coupled inductor	Lm=250 µH & L_{lk}=3µH Turns ratio $N1$:$N2$=1:1
Power MOSFETS	IRFP4668PbF
Power diode for D_1,	DSEI60-06A
Power diode for D_2	*SFAF2004G*
Power diode for D_4, D_3,& D_O	*SFAF1606G*

$$V_{S2} = \frac{2G^2 V_{in}}{\left(3G + 2nG + 1 + \sqrt{5G^2\,(6+4n)\,G + 1}\right)} \tag{21}$$

$$\frac{\left(2G + 3nG - n - \sqrt{5G^2\,(6+4n)\,G + 1}\right) I_{in}}{\left(3G + 2nG + 1 + \sqrt{5G^2\,(6+4n)\,G + 1}\right) D} \tag{22}$$

$$D_1 = \frac{2G^2 V^{in}}{3G + 2nG + 1 + \sqrt{5G^2\,(6+4n)\,G + 1}} \tag{23}$$

$$D_2 = \frac{\left(G - G^2 + G\sqrt{5G^2 + (6+4n)\,G + 1}\right) V_{in}}{3G + 2nG + 1 + \sqrt{5G^2\,(6+4n)\,G + 1}} \tag{24}$$

$$D_3 = \frac{\left(G + 2nG^2 + G\sqrt{5G^2 + (6+4n)\,G + 1}\right) V_{in}}{3G + 2nG + 1 + \sqrt{5G^2\,(6+4n)\,G + 1}} \tag{25}$$

$$D_O = \frac{\left(G^2 + G + G\sqrt{5G^2 + (6+4n)\,G + 1}\right) V_{in}}{3G + 2nG + 1 + \sqrt{5G^2\,(6+4n)\,G + 1}} \tag{26}$$

Comparison of the voltage gain of the proposed converter with other topologies is illustrated in Fig. 8(a). Regarding to Fig. 8(a), it can be seen that the proposed converter has the highest voltage gain in lower range of duty cycle compared with other converters. Also, the maximum voltage stress across the power switches of the converters is shown in Fig. 8(b). Considering this figure, under the same input voltage for all converters, the slop of the voltage stress curve for the proposed converter is less than the other topologies. Therefore, the maximum voltage stress of the power switches for proposed converter is lower than the others.

Although, at the voltage gain of greater than 15, the maximum voltage stress across the power switches of the proposed converter is higher than the presented structure in [26], this converter not only isn't common grounded, but also the number of its elements is more than the proposed converter that may result in high conduction losses and cost. The comparison of the voltage stress of main capacitor of the proposed converter with other topologies is illustrated in Fig. 8(c). Regarding to this figure, it can be understood that compared to other structures, except the converter presented

in [27] for high voltage gain range, the voltage stress of the main capacitor of the proposed structure has the lowest value.

The comparison of the minimum voltage stress across the diodes for all suggested converters is shown in Fig. 8(d). The voltage stress of the output diode for the converter in [29], and the conventional converter is equal to the output voltage and higher than the others. Based on Fig. 8(d), the minimum voltage stress across the output diode of the proposed converter is the lowest value compared with other converters.

Fig. 8(e) illustrates the comparison of the maximum voltage stress of the diodes in terms of the voltage gain with other converters. Considering Fig. 8(e), the maximum voltage stress of the diodes for the converters in [25], [29], and [31], and the conventional converter is equal to the output voltage and higher than the others. As well, the voltage stress across the output diode in [27] is higher than the proposed converter.

Fig. 8(f) shows the comparison of the normalized voltage stress of the output diode in terms of the voltage gain for the proposed converter with other topologies. Regarding to this figure, it can be seen that the normalized voltage stress for the converters in [25], [29], and [31] are the same and higher than the others. Also, compared with topologies in [25], [27], [29], [30], and [31], the proposed converter has the lower value of normalized voltage stress.

The comparison of maximum current stress of the switches for the proposed converter with other structures is indicated in Fig. 8(g). Considering this figure, it can be seen that compared other topologies, expect [30], and [32], the proposed converter has the lowest value of maximum current stress of the switches. In general, the voltage gain of proposed converter is higher than the abovementioned converters and its switches and output diode voltage stresses are lower.

Comparison of the voltage gain of the proposed converter with topologies [33], and [34] is illustrated in Fig. 9(a). Considering this figure, the proposed converter has the largest gain voltage between topologies [33] and [34]. Also, the maximum voltage stress across the power switches of the proposed converter, [33], [34] is shown in Fig. 9(b). Considering this figure, under the same input voltage for all converters, the slop of the voltage stress curve for the proposed converter is less than the topologies [33] and [34]. Therefore, the maximum voltage stress of the power switches for proposed converter is lower than the converters of [33] and [34].

In addition, the efficiency, frequency, output voltage, input voltage, power and common grounding features of the proposed converter and the other competitors are gathered in Table 4. As can be seen, the efficiency of the proposed converter is higher than the most recent converters. Although the efficiency in the converters of [27] and [32] is better than the proposed converter, the output voltage and power of the converter in [27] are less than the proposed converter. Also, the input voltage and output voltage in converter of [32] is higher than the proposed converter which causes lower passing current through the elements. Therefore, in the same condition for both converters, they may have same efficiency. Based on Table 4, in the proposed converter, topologies of [21] and [32], the neutral point of output is connected to the input DC source directly. So, the proposed converter, [21] and [32] can provide common grounded feature. However, other compared topologies cannot provide common grounded feature.

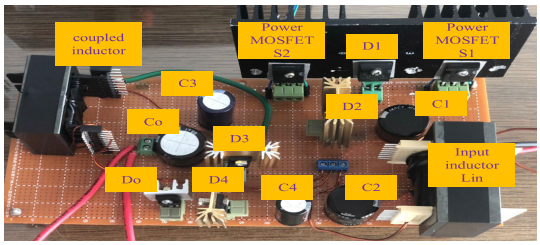


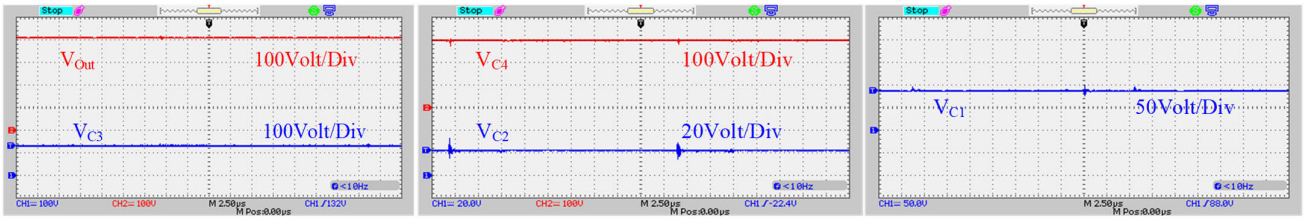
FIGURE 10. The photograph of experimental prototype of proposed converter.

VII. EXPERIMENTAL RESULTS

Based on the theoretical analysis, the experimental prototype of 250 W has been tested in the laboratory to validate the performance of the proposed converter which is demonstrated in Fig. 10. As well, the utilized devices specifications for the proposed converter are tabulated in Table 4. According to the voltage gain relationship, the duty cycle is set in 0.21 under the approximated 40 kHz switching frequency and the input voltage is 48 V. The output voltage and the voltage of all capacitors are shown in Fig. 11. As it can be seen from Fig. 11(a), the output voltage is approximately 410 V and the voltage of capacitor C_3 is about 133V. From theoretical analysis, the voltage gain value of the presented converter is about 9.15 and the experimental voltage gain value is about 8.54. Based on Fig. 11(a), it can be seen that the experimental value is near to theoretical value and they verify each other. Fig. 11(b), shows the voltage of capacitors C_2 and C_4 which are 22 V and 300 V approximately. The voltage of capacitor C_1 is shown in Fig. 11(c), which is about 88 V. All these capacitors voltage values comply the theoretical equations.

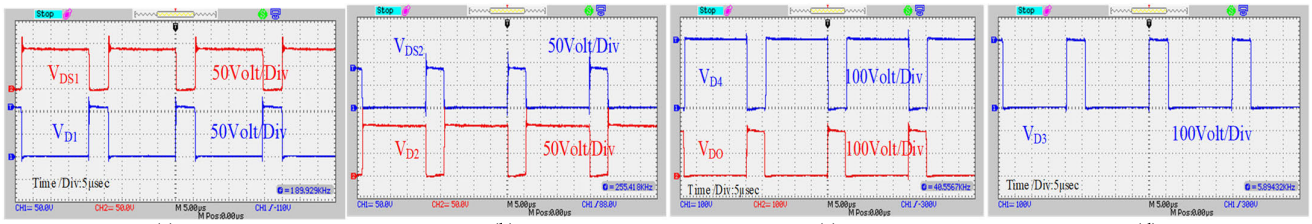
Fig. 12, shows the experimental waveforms of the voltage stress of the switches and diodes. It can be seen from Fig. 12(a), the voltage of drain-source for the S_1 switch (V_{S1}) is about 88 V and the voltage stress of diode D_1 is about 110 V. Also, from Fig. 12(b), the voltage of drain-source for the S_2 switch (V_{S2}) and voltage stress of diode D_2 are about 110 V and 88 V, respectively. In addition, the voltage stress across the diodes D_4 and D_O are shown in Fig. 12(c), which are about 300 V and 200 V, respectively. It can be observed that the output diode voltage is half of the output voltage. Fig. 12(d), shows the voltage waveform of diode D_3 and it is about 300 V. All these experimental values are near to theoretical equations and affirm the performance of the suggested converter.

The experimental current waveforms of the input inductor L_{in} and the coupled inductor are shown in Fig. 13. It is noted from Fig. 13(a), when switches are ON, the input inductor current is raised linearly and when switches are OFF, the input inductor current is decreased linearly. The maximum amount of input inductor current is about 6.4 A and the minimum is



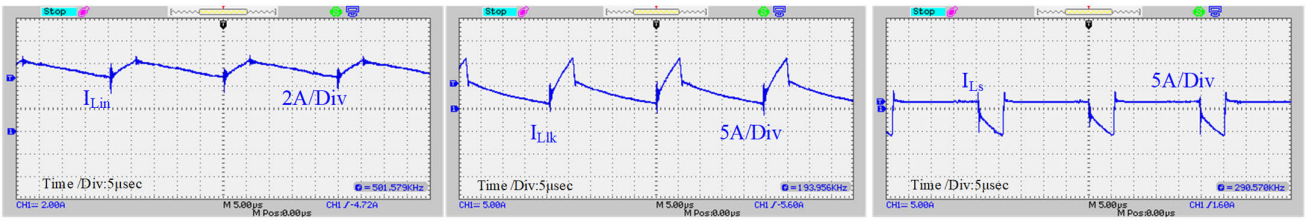
(a) (b) (c)

FIGURE 11. The voltage waveforms of output and capacitors (a) Output voltage and voltage of capacitor C3, (b) Voltage of capacitor C2 and C4, (c) Voltage of capacitor C_1.



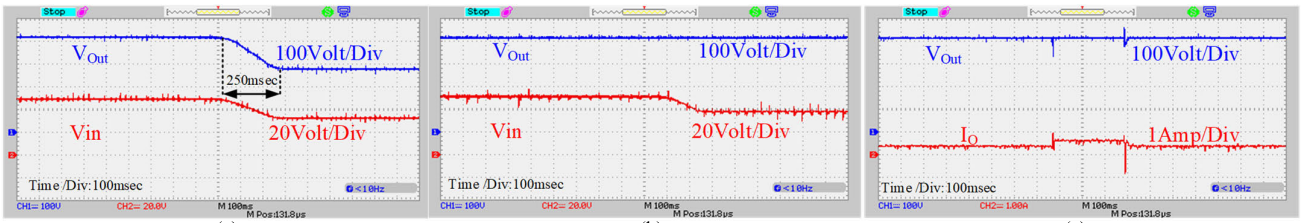
(a) (b) (c) (d)

FIGURE 12. The voltage stress waveforms of semiconductors (a) Power switch S_1 and diode D_1, (b) Power switch S_2 and diode D_2, (c) Diodes D_4 and D_O, (d) Diode D_3.



(a) (b) (c)

FIGURE 13. The current waveforms of inductors (a) Current of inductor L_{in}, (b) Current of primary side of coupled inductor L_{lk}, (c) Current of secondary side of coupled inductor L_S.



(a) (b) (c)

FIGURE 14. Experimental results: (a) the output voltage waveform with change in input voltage in open loop control system. Output voltage control of the proposed structure: (b) Changing input voltage, and (c) Changing the output load.

about 4.72 A. Also, the average value of this current is about 5.56 A. The experimental current waveforms of the primary and secondary side of the coupled inductor are observed in Fig. 13(b) and 13(c), respectively. As it can be seen, these currents change linearly and when the switches are ON the slope of the primary side current is positive and the current of the secondary side is negative.

In Fig. 14(a), the dynamic response of the open-loop system of the second proposed structure is evaluated. In this figure, initially when the input voltage is 48 V, the output voltage is 408 V and the output power is 250 W. After a short time interval, the input voltage suddenly drops to 32 V and the output voltage drops to 280 V after 250 mSec. and remains constant. Therefore, the time of transient changes in this converter is about 250 mSec., after which the voltage is stabilized and the voltage gain follows the theoretical values and the output power reaches 60 W.

Finally, the results of the control system of the closed-loop system of the proposed structure are evaluated in Fig. 14 (b) and (c). As can be seen in Fig. 14(b), by changing the input voltage from 48 V to 32V, the output voltage is constant and it is not changed. During this period, the output voltage of the converter is fixed at 408 V. As can be seen in Fig. 14 (c), by changing the output load, the load current first increases and reaches to the full load (0.6 A) value, and then decreases to the half load value (0.3 A). During this period,

when the load has changed, the output voltage of the converter is fixed at 408 V.

VIII. CONCLUSION

In this paper, a high gain switched quasi Z-source DC-DC converter with a coupled inductor and a switched capacitor cell is proposed which has added one extra diode and one power switch to the quasi Z-source network. In addition, this converter can reach the following characteristics: high voltage gain with small duty cycle, continuous input current, low voltage stress across the power switches, low voltage stress on the output diode and common ground between the load and input energy source. The presented converter has been compared with other Z-source based converter comprehensively and experimental results of 250 W prototype prove the above-mentioned characteristics. Also, the control strategy and stability of the proposed converter are evaluated. Eventually, the calculated and measured efficiency have been provided. As consequence, the measured efficiency is near to the calculated amount and the full load efficiency is 93.86%.

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