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RESEARCH ARTICLE

A 1–18-GHz High-Gain and Low-Voltage Down-Conversion Mixer in 0.18-μm CMOS Technology

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ABSTRACT This study presents a wideband down-conversion mixer chip covering the frequency range of 1–18-GHz by TSMC 0.18-μm CMOS technology. The design of multiband mixers has attracted significant research interest. The main advantage is that it can share circuits, save chip area, and reduce power consumption and cost. The architecture implemented in this study is based on that of a double-balanced switched transconductance (SwGm) mixer. To lower the supply voltage and DC consumption, an LO CMOS series-parallel switching architecture was used in the proposed design. Transformer coupling technology was used at the node between the transconductance and local oscillator switch stages, which can effectively increase the switching current above a frequency of 10-GHz and improve the conversion gain when the power supply voltage is less than 1-V. The measured results for the proposed mixer show a power conversion gain of 10.1–15.9-dB, input third-order intercept point (IIP3) of −4∼−9.2-dBm, double side-band (DSB) noise figure of 10.3–14.5-dB, and RF bandwidth range of 1–18-GHz. The total DC power consumption of this mixer including the output buffer was 6.8-mW, and its core power consumption was 2.3-mW; the output buffer power consumption was 4.5-mW, and the total die size was 0.917 × 1.1-mm^2. The mixer exhibited excellent performance characteristics, such as low power consumption, high bandwidth, and high gain.

INDEX TERMS CMOS, down-conversion mixer, double side-band, transformer coupling, wideband.

I. INTRODUCTION

In recent years, the research and development of multiband, multistandard wireless communication systems has become a popular topic [1]. This research design includes a 1–18 GHZ down-conversion mixer, which covers the communication frequency range between the main wireless communication products, such as Bluetooth, UWB, WLAN, 5G, and Ku-band satellites, and the frequency band of the most popular Starlink satellites. The design of multiband mixers has received significant research interest. The main advantages of such mixers include their capability to share circuit, save chip area, and reduce power consumption and cost. This study used an active mixer design; the active mixer is based on single-balanced and double-balanced mixers as the main structures. Single-balanced active mixers have inherent flaws in their architecture. The LO signals leak into the IF output, resulting in poor LO-IF isolation, which is an inherent disadvantage of the single-balanced active-mixer architecture. The double-balanced active mixer, also known as a Gilbert Cell (GmSw) circuit, is composed of two sets of single-balanced active mixers based on its structure. The input signal at the RF end is a differential signal, despite comparable working principles. The two primary forms of double-balanced Gilbert cell-mixer topologies are double-balanced Gilbert-cell switching transconductor (SwGm) and double-balanced Gilbert-cell (GmSw) mixers. The conversion gain of the conversion mixer (GmSw) can be expressed as [2]

$$\mathrm{CG} = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_m \mathrm{R_L}, \tag{1}$$

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$$\text{and } g_m = \mu_n C_{ox} \frac{W}{L}(V_G - V_{TH}). \tag{2}$$

where g_m is the transconductance of M_1, $C_{ox}$is the gate capacitance per unit area, W is the gate width, and L is the effective gate length. R_L stands for the load resistance, u_n is the mobility of electrons near the silicon surface, and L is the effective gate length. A SwGm is shown in Figure 1. The conversion gain of the mixer (SwGm) can be expressed as [3], [4]

$$\text{CG} = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_m \text{R}_\text{L} \tag{3}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_G - V_{DS1} - V_{TH}), \tag{4}$$

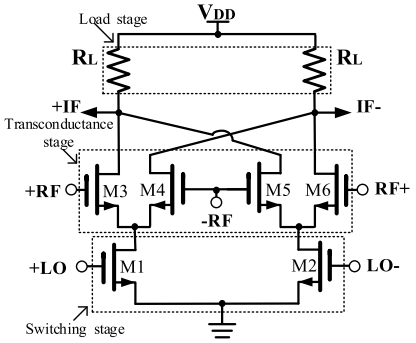


FIGURE 1. CMOS Gilbert-cell switched transconductor mixer (SwGm) [6].

Equations (2) and (4) indicate that the GmSw mixer has a higher conversion gain than the SwGm mixer. Comparing the advantages and disadvantages of the two types, GmSw mixers have higher conversion gains than SwGm mixers, but cannot operate at low voltages. The main advantage of the SwGm mixer is that it can operate at supply voltages below 1 V [5], [6]. The advantages of the mixers designed using MOS transistors include low power consumption, low cost, and low voltage. However, one disadvantage is that the gain is reduced at high frequencies. To improve the frequency response, the channel length of the MOS transistor must be reduced. However, the gain of the mixer designed using this 0.18 μm process is in the high-frequency band above 10 GHz and is greatly attenuated. A high supply voltage is necessary to achieve a high conversion gain over a broad frequency band, which increases power consumption. When the supply voltage is less than 1 V, it was impossible to satisfy the criteria. The RF circuit design has many passive components on the chip, and the area accounts for a large proportion; therefore, an advanced process design is expensive. Therefore, this study describes an improved technique based on the Gilbert-cell mixer topology, which operates in the frequency band of 1–18 GHz. The modified SwGm mixer is suitable for operation at a 1 V supply voltage. This study involves a mature process that reduces the wafer cost and presents the measurement results. The mixer is a three-terminal component; therefore, it is different from other high-frequency circuits in terms of high-frequency parameters and performance considerations. The important parameters to be considered in this design are the conversion gain, linearity, noise figure, isolation, and power consumption [7], [8]. In this study, a wideband mixer topology for a high conversion gain was theoretically analyzed. In Section II, we present the design and analysis of the wideband mixer. Section III presents the experimental results. The final section summarizes the conclusions.

II. CIRCUIT DESIGN AND ANALYSIS

A complete schematic of the proposed mixer-core analysis is shown in Figure 2. The mixer RF and LO substitution will have different results, GmSw operation is higher than 1V supply voltage, SwGm operation is lower than 1V supply voltage. Most of the current literature that inserts an inductor between the LO and RF stages is GmSw [9], [10], [11], [12], [13], but there is no literature on SwGm. There are three ways to increase the mixer gain: increasing the transconductance stage gain (g_m), switching current, and load. Therefore, in this research, the mixer increases the switching stage current, thereby increasing its conversion gain. The switching stages (M_1–M_8) were designed such that when the supply voltage was below 1 V, the transistors could operate between the OFF and triode regions.

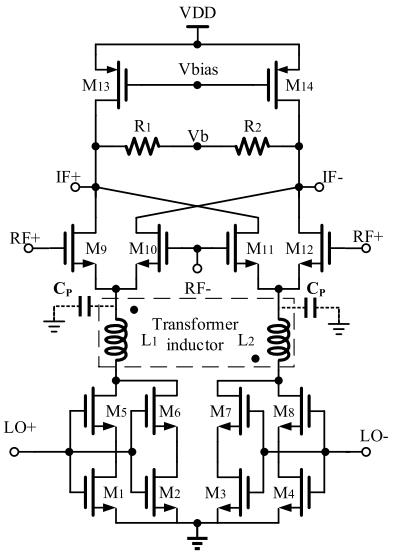


FIGURE 2. Core circuit of the proposed mixer design.

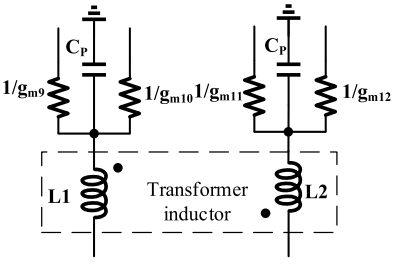
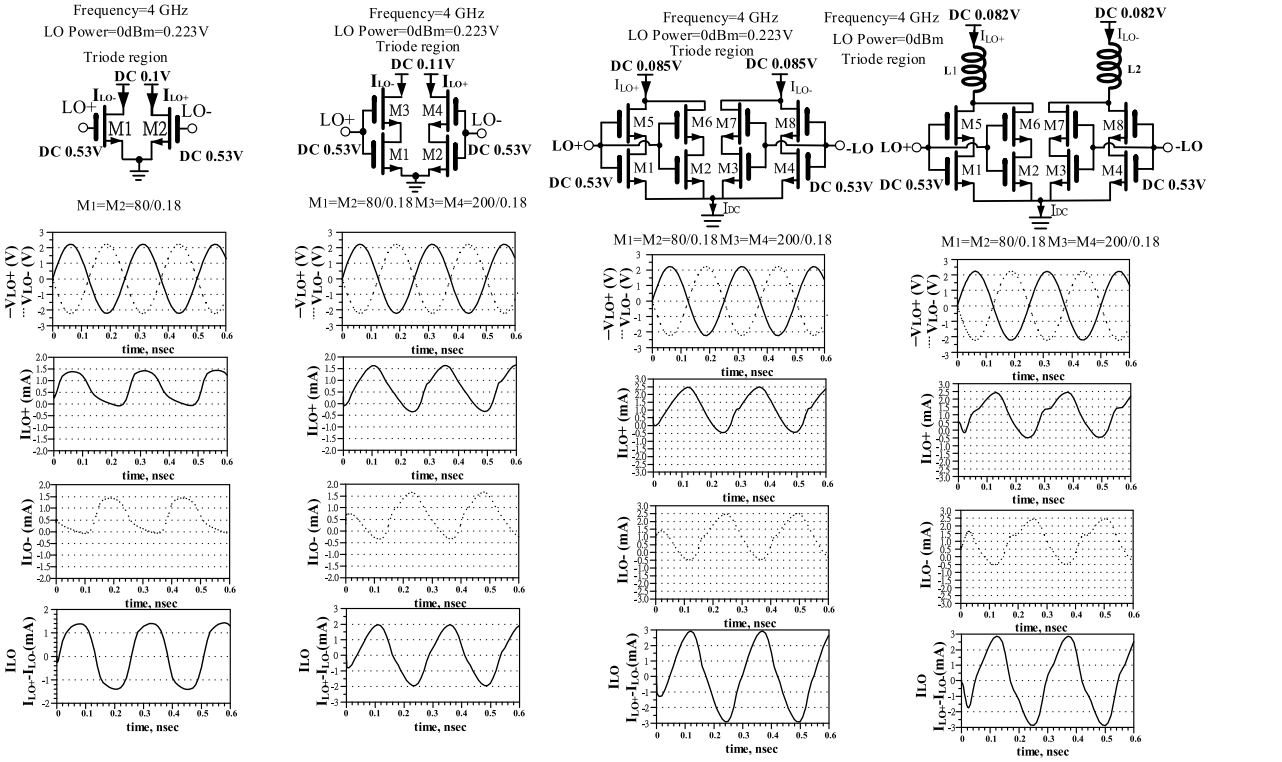


FIGURE 3. Simplified parallel RLC resonator model.

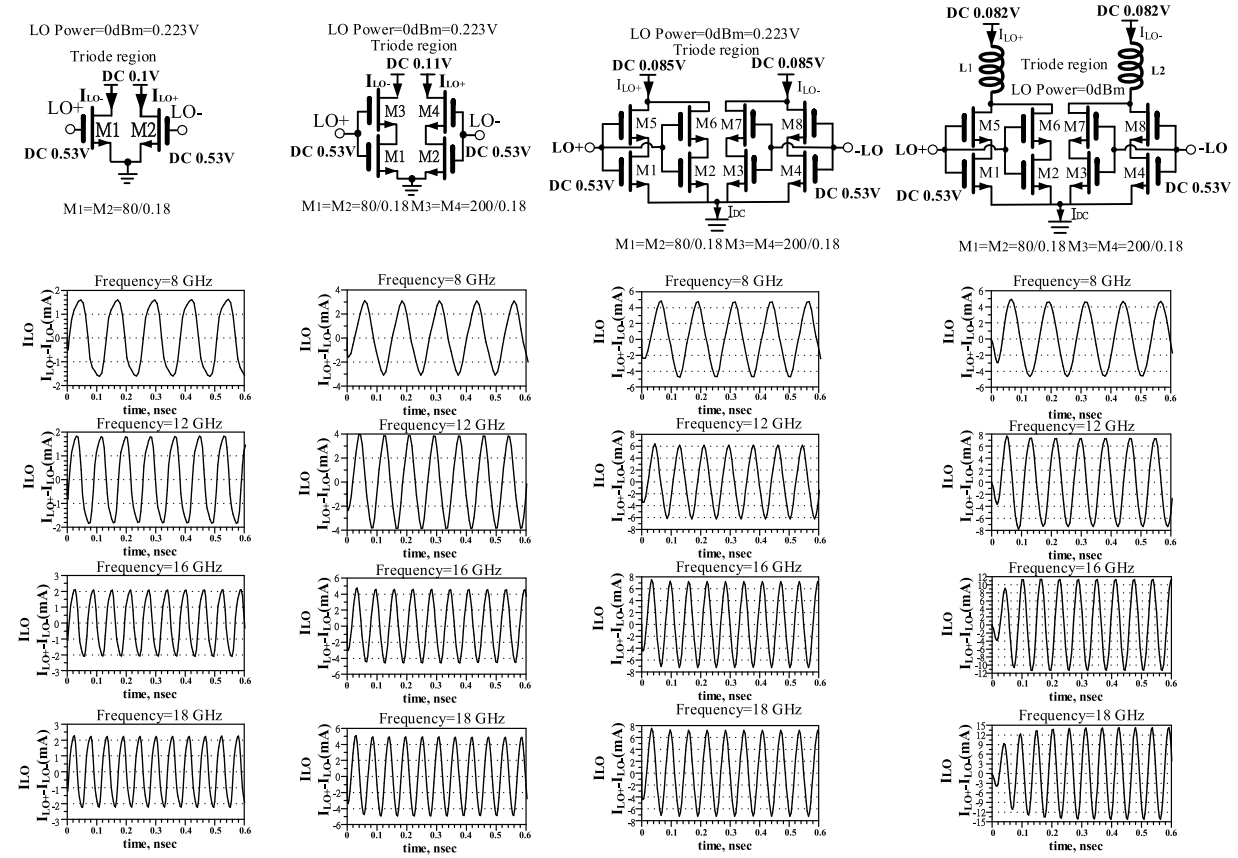
The current was increased by utilizing the charge and discharge characteristics of the parasitic capacitance of the transistor. Therefore, a large W/L ratio was chosen

for M_5–M_8, and the large size of M_5–M_8 will generate a large parasitic capacitance [5], [6]. The LO+ and LO- input signals are 180° out of phase, which generates a 180° phase current. The current in the negative half cycle was generated by capacitive effects. The differential structure of the mixer increases the output current and improves the conversion gain of the mixer. Previously published [5], [6] research results show that this technique can effectively increase the conversion gain when the supply voltage is less than 1 V. However, the previously developed mixers only show a broadband response below 10 GHz and are not suitable for Ku-broadband system applications. This reduction in the mixer gain occurs at high frequencies. Therefore, a set of resonant inductors (L_1–L_2) are connected in series between the LO switching stage and the RF transconductance stage of this study to increase the conversion gain of the mixer and reduce noise. C_P is the tail junction capacitance of the node between the LO switching stage and the RF transconductance stage. This junction capacitance is proportional to the size of the RF transconductance transistor. This causes the capacitor and inductor to resonate as shown in Figure 3. This innovative technology effectively enhances the switching current at high frequencies. A comparison of the current waveforms produced by different switching-stage transistor designs is shown in Figure 4. Figures 4 (a) (b) show the switching waveforms with and without M_3–M_4. As shown in Figure 4(c), the circuit delivers a negative current during the negative half-cycle of the input voltage, and the parallel path reduces the resistance value. The supply voltages for the simulated switching are shown in Figures 4(a)–(d) as 0.1 V, 0.11 V, 85 mV, and 82 mV, respectively. The simulated switching waveforms current ILO+ are 1.4 mA, 2 mA, 3 mA, and 3 mA, respectively, as shown in Figures 4(a)–(d). On comparing Figures 4 (a) and (b), the current I_{LO} of the proposed series-switching stage is found to be 1.43 times higher than that of the single-switching stage. On comparing Figures 4 (b) and (c), the current I_{LO} of the proposed parallel-series switching stage is found to be 1.5 times higher than that of the series switching stage. On comparing Figure 4 (c) and (d), the proposed series-parallel switching mixer current I_{LO} was equal to the resonant inductor switching mixer current at 4 GHz, and the proposed series-parallel switching mixer current was equal to that of the resonant inductor switching mixer current for frequencies below 8 GHz. Figure 5 shows a comparison of the switching-stage current waveforms generated at different LO frequencies. On comparing Figure 5 (a) and (b), the current I_{LO} of the proposed series-switching stage showed a significant boost current compared with a single-switching stage at high frequencies. On comparing Figures 5 (b) and (c), the current I_{LO} of the proposed parallel-series switching stage is found to be 1.6 times higher than that of the series switching stage at high frequency. On comparing Figure 5 (c) and (d), the current I_{LO} of the proposed resonant inductor parallel-series switching stage is found to be 1.75 times higher than that of the parallel-series switching



(a) Single-switched stage (b) Series switched stage (c) Parallel-series switched stage (d) Resonant-inductor parallel-series switched stage

FIGURE 4. Simulated switching stage current waveform at 4 GHz.



(a) Single-switched stage (b) Series switched stage (c) Parallel-series switched stage (d) Resonant-inductor parallel-series switched stage

FIGURE 5. Simulated switching stage current waveform generated at different LO frequencies.

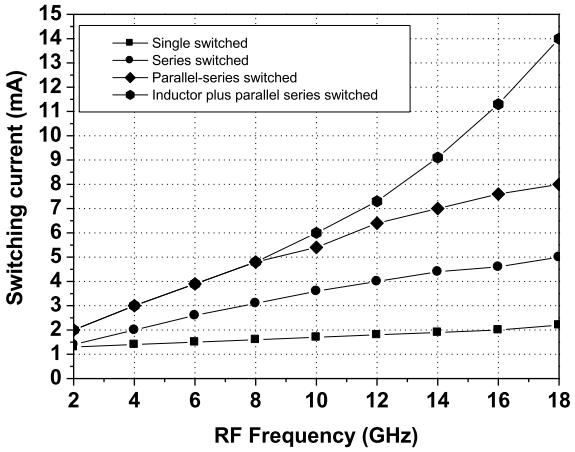


FIGURE 6. Simulated switching current versus LO frequency.

stage at 18 GHz. Figure 6 shows the simulated switching current with respect to the LO frequency. The proposed resonant inductor parallel-series switching stage current was 2–14 mA. This technology effectively increased the switching current and conversion gain of the mixer at high frequencies.

To compute the conversion gain of the mixer, the LO signal can be represented as a square-wave local oscillator signal ($V_{LO} = sq(\omega_{LO}t)$), and the RF signal can be represented as a sine wave signal ($V_{RF} = V_{RF}\ sin(\omega_{RF}t)$). The I_{RF} multiplied by an ideal square-wave current (I_{LO}, $sq(\omega_{LO}t)$) alternates between +K and -K. The conversion gain is derived as follows:

$$CG = 20\log\frac{V_{IF}}{V_{RF}}. \tag{5}$$

$$\text{where } V_{IF} = I_{IF} \times R_L. \tag{6}$$

The intermediate frequency (I_{IF}) differential current can be expressed as

$$I_{IF} = I_{IF+} - I_{IF-} = (I_{D9} + I_{D11}) - (I_{D10} + I_{D12}), \tag{7}$$

$$\text{where } I_{D9} = \left[\frac{I_{DC}}{2} + g_m\left(\frac{V_{RF}}{2}\right)\right] \times I_L, \tag{8}$$

$$I_{D10} = \left[\frac{I_{DC}}{2} - g_m\left(\frac{V_{RF}}{2}\right)\right] \times I_L, \tag{9}$$

$$I_{D11} = \left[\frac{I_{DC}}{2} - g_m\left(\frac{V_{RF}}{2}\right)\right] \times (-I_L), \tag{10}$$

$$\text{and } I_{D12} = \left[\frac{I_{DC}}{2} + g_m\left(\frac{V_{RF}}{2}\right)\right] \times (-I_L). \tag{11}$$

The switching stage performs the frequency-mixing function to down-convert the RF signal to IF, simplified as follows:

$$I_{IF} = g_m V_{RF} \times I_L, \tag{12}$$

$$I_{IF} = g_m V_{RF} \sin(\omega_{RF}t) \times sq(\omega_{LO}t), \tag{13}$$

$$I_{IF} = g_m V_{RF} \sin(\omega_{RF} t) \times k \times \frac{4}{\pi} \sum_{n=0}^{\infty} \frac{\sin(2n+1)\omega_{LO} t}{2n+1}, \tag{14}$$

$$I_{IF} = \frac{2K}{\pi} g_m V_{RF} [cos(\omega_{RF} - \omega_{LO})t + cos(\omega_{RF} + \omega_{LO})t + \ldots..]. \tag{15}$$

Then leave the down frequency signal we need

$$I_{IF} = \frac{2K}{\pi} g_m V_{RF} \cos(\omega_{RF} - \omega_{LO}), \tag{16}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_G - V_{DS1} - V_{TH}). \tag{17}$$

The term with the down-converted frequency at ($\omega_{RF-}\omega_{LO}$) is maintained when $sq(\omega_{LO}t)$ is extended in a Fourier series. When the supply voltage is less than 1 V, the transistors can operate in the triode area because of the switch stages (M_1–M_8). V_{DS5} approaches zero because of the large W/L ratio selected for M_5. The transconductance stages (M_5–M_8) operate in the saturation region when the supply voltage was below 1 V. Equation (16) shows that increasing the I_{IF} current increases the conversion gain. The I_{IF} current was proportional to the transconductance (g_m) and switching current (I_L). The transconductance (g_m) of this transistor decays at high frequencies; thus, the conversion gain decreases. Figure 6 shows the inductor parallel-series switched stage technology, which can effectively increase the switching current above a high frequency of 10 GHz and improve the conversion gain when the power supply voltage is less than 1 V. In contrast to the SwGm mixer, the proposed switched mixer has a conversion gain that is K times larger when Equations (3) and (16) are compared. Suitable for Ku broadband system applications. A schematic of the proposed SwGm mixer is shown in Figure 7. It consists of transconductance stage (M_1–M_4), transformer coupling technology (L_1–L_2), switching stage (M_{16}–M_{23}), load stage (M_{10}–M_{11}, R_2–R_3), common mode feedback (CMFB) circuit (M_5–M_9), the output buffer (M_{12}–M_{15}), the input matching network for RF stage (C_1, C_3, R_5, and L_3), and the input matching network for LO stage (C_5, C_7, R_{10}, and L_5). However, the large impedance observed at the gate of MOS transistors results in a complex broadband impedance-matching network. An LC ladder-matching network is used in this wideband mixer design. In this network, a resistor (R_5) was connected in parallel to achieve good impedance matching. The RF and LO stage-matching impedances were both 50 Ω. Resistance $R_6$was added as the bias voltage resistance. C_1 is a DC isolation capacitor. Inductors L_3, R_5, and C_3 enabled wideband matching. This R_5 value is a trade-off as it introduced noise and loss. If the impedance is too high, the bandwidth is reduced. If it is too small, it causes leakage and noise in the input signal. The resistance of R_5 was designed to be 80 Ω. Table 1 lists the mixer components.

The CMFB circuit sets the common mode voltage. The loop gain must be high enough so that V_m and V_p are approximately equal. The conversion gain is inversely proportional to linearity. This means that when increasing the conversion gain, it may sacrifice some linearity in the circuit and vice versa. Achieving a balance between high conversion gain and good linearity is a common design challenge. This CMFB circuit is a variable gain. Thus, gain flatness can be achieved by controlling the V_m voltage. Moreover, the inductors (L_1 and L_2) occupied a large chip area, particularly in the low-frequency band. Transformer coupling is widely used in radio frequency (RF) circuits [11], [12], [13], [14]. Transformer coupling techniques were used on the inductors (L_1–L_2) to reduce the die area and increase inductance. The mutual inductance increases the impedance load and conversion gain. L_1 and L_2 are implemented on the thick metal layer (M_6) in the standard 0.18 μm CMOS process. The transformer coupling layout is illustrated in Figure 8. The schematic symbol for transformer coupling is shown in Figure 9. The two coupled coils have the same self-inductance, the corresponding mutual inductance, coupling coefficient, and power conversion characteristics. The voltage and current transformation between windings in an ideal transformer are related to the turns ratio can be expressed [11], [15]:

$$n = \frac{I_P}{I_S} = \frac{V_S}{V_P} = \sqrt{\frac{L_S}{L_P}}, \tag{18}$$

$$K = \frac{M}{\sqrt{L_P L_S}}. \tag{19}$$

where n is the number of turns, L_s is the inductance of the secondary windings, L_p is the inductance of the primary windings, M is the mutual inductance between the secondary and primary windings, and K is the strength of the magnetic coupling between the windings. K-factor less than one for physical monolithic transformer. The Keysight Advanced Design System (ADS) simulation software serves the purpose of simulating various parameters related to inductors. It is through the Z-parameter transfer that we can make an estimation of the inductance for each individual inductor.

$$L = L_P = L_S = \frac{img(Z(1,1))}{2\pi f} = \frac{img(Z(2,2))}{2\pi f}, \tag{20}$$

The quality factor (Q) is estimated as follows

$$Q = Q_{PL} = Q_{SL} = \frac{img(Z(1,1))}{real(Z(1,1))} = \frac{img(Z(2,2))}{real(Z(2,2))}, \tag{21}$$

The mutual inductance (L_M) is estimated as follows

$$L_M = \frac{img(Z(2,1))}{2\pi f} \tag{22}$$

The total equivalent inductance is the sum of the self-inductance and mutual inductance. The calculation for the equivalent inductance (L_{total}) is as follows:

$$L_{total} = L_P + L_M. \tag{23}$$

Figure 10 shows the inductor value simulation results. The simulated quality factor is shown in Figure 11. Quality factor, denoted as Q, is a measure of the ratio between energy stored and energy dissipated. As per Equation (21), it becomes evident that an increase in the quality factor, Q, corresponds to a

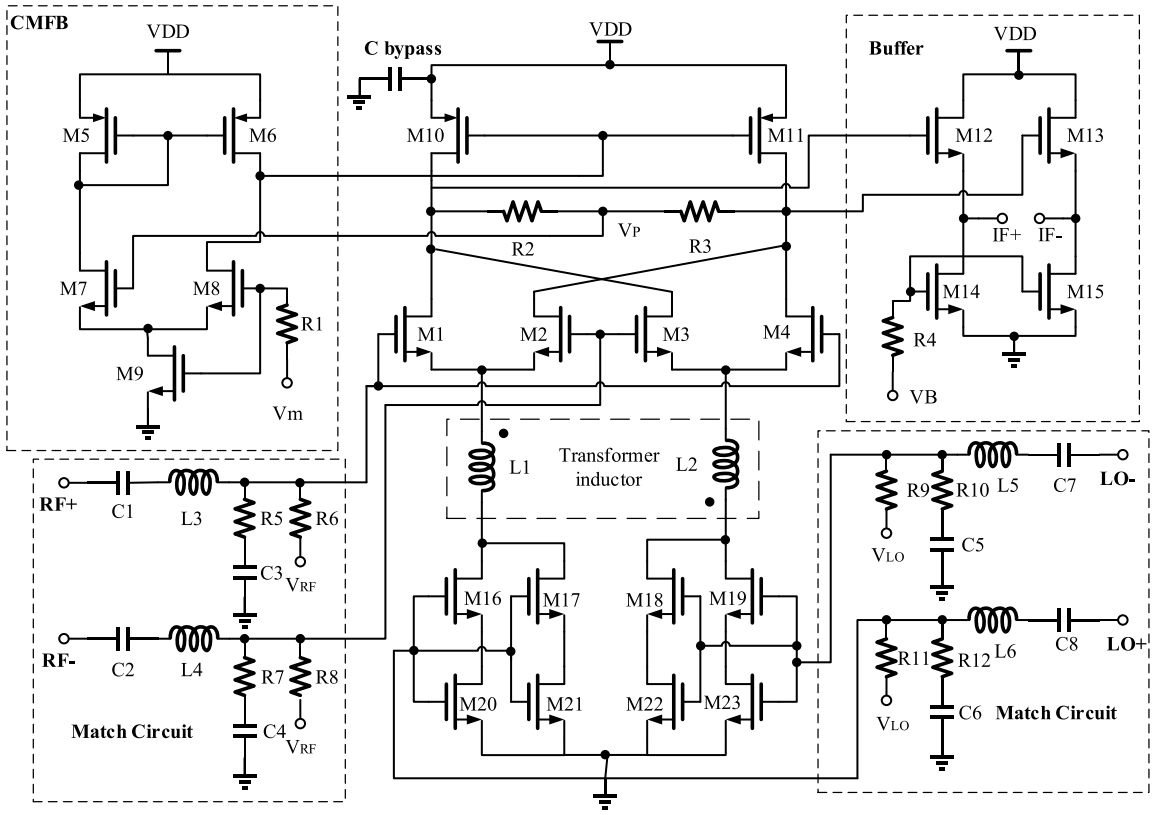


FIGURE 7. Complete schematic of the proposed SwGm mixer.

TABLE 1. Pre-simulation device sizes of the proposed mixer.

Device	Design Values	Device	Design Values
M_{N1}-M_{N4}	70/0.18 (W/L)	R_6, R_8	1.6 KΩ
M_{P5}-M_{P6}	512/0.18 (W/L)	R_9, R_{11}	1.6 KΩ
M_{N7}-M_{N9}	15/0.18 (W/L)	R_{10}, R_{12}	117 Ω
M_{P10}-M_{P11}	512/0.18 (W/L)	C_1,C_2 (l/w)	(30/30)*3 um^2
M_{N12}-M_{N13}	300/0.18 (W/L)	C_3,C_4 (l/w)	(30/30)*1 um^2
M_{N14}-M_{N15}	320/0.18 (W/L)	C_5,C_6 (l/w)	(30/30)*2 um^2
M_{N16}-M_{N19}	200/0.18 (W/L)	C_7,C_8 (l/w)	(30/30)*5 um^2
M_{N20}-M_{N23}	80/0.18 (W/L)	L_3(w/rad/nr)	6/30/2.25
R_1, R_4	1.6 KΩ	L_4(w/rad/nr)	6/30/2.25
R_2-R_3	5.2 KΩ	L_5(w/rad/nr)	6/40/1.25
R_5, R_7	80 Ω	L_6(w/rad/nr)	6/40/1.25

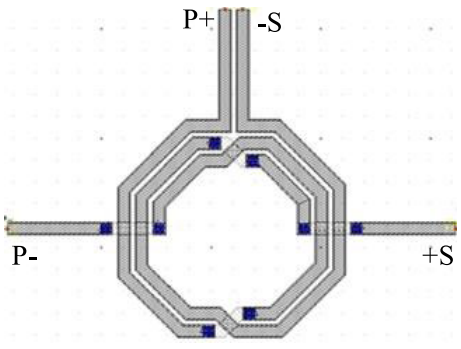


FIGURE 8. Transformer coupling layout.

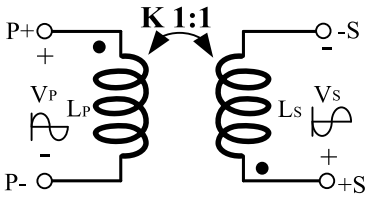


FIGURE 9. The schematic symbols for transformer coupling.

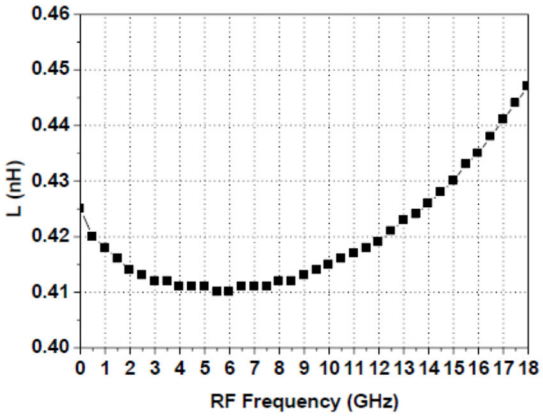


FIGURE 10. Simulated inductor values.

diminished rate of energy loss compared to the energy stored within the resonator. Figure 12 shows the simulated magnetic coupling strength. The simulated mutual inductance value is shown in Figure 13. One noteworthy advantage of transformer coupling lies in its capacity to augment the Q-factor of the resonator while concurrently reducing chip footprint. Furthermore, it can be easily integrated with other circuits

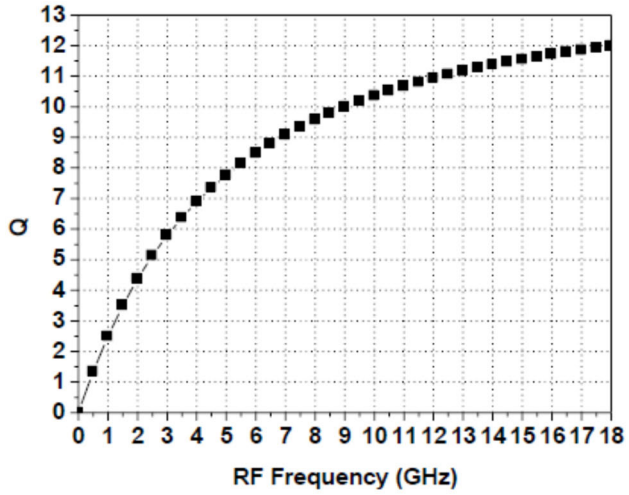


FIGURE 11. The quality factor for the simulation.

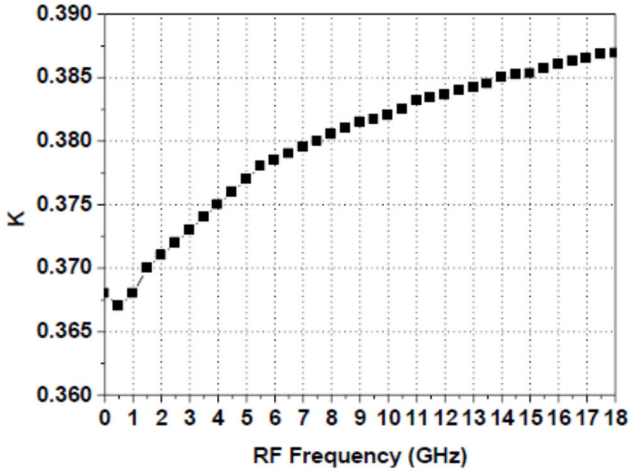


FIGURE 12. Simulated magnetic coupling strength.

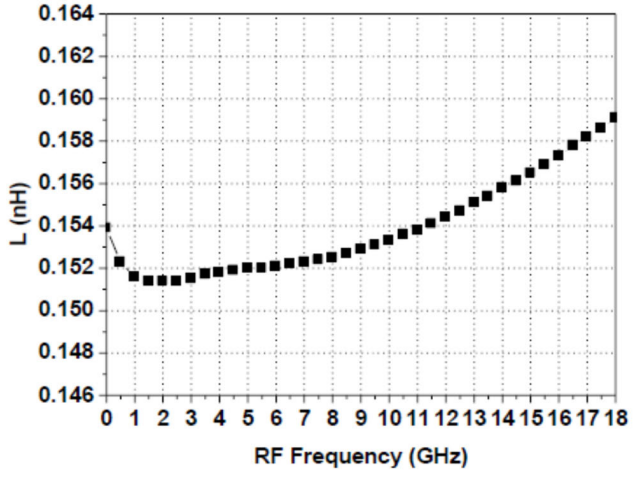


FIGURE 13. Simulated mutual inductance values.

in a single chip. Figure 14 illustrates the simulated conversion gain with and without transformer coupling. Obviously, inductance causes the conversion gain to increase significantly at high frequencies. It is obvious from Figure 15 that

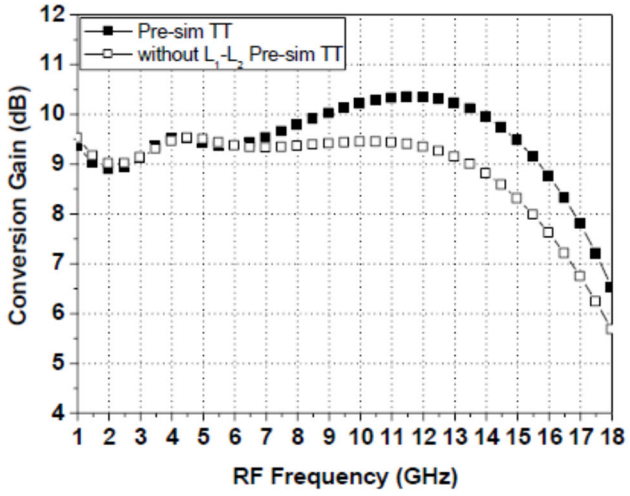


FIGURE 14. Simulated conversion gain with and without transformer coupling.

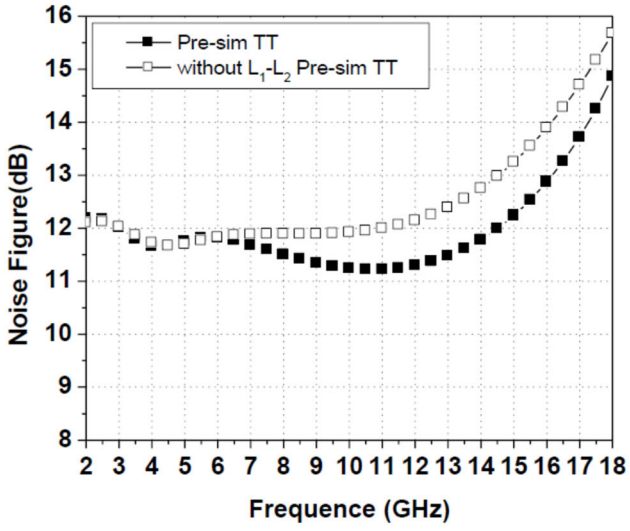


FIGURE 15. Simulated noise figure with and without transformer coupling.

inductance causes the noise coefficient to decrease at high frequencies.

III. MEASURED RESULTS

The proposed low-voltage and low-power L to Ku band mixer was designed and fabricated in TSMC 0.18-μm CMOS technology. The chip was measured using on-wafer testing. The RF and LO port impedance matching was 50 Ω. The supply and bias voltages were connected by means of a 6-pin on-wafer probe with a pitch of 100 μm. The differential RF/LO/IF signals were measured using 100 μm pitch coplanar ground-signal-ground-signal-ground (GSGSG) on-wafer probes. The RF and LO ports were measured using off-chip Tektronix PSPL5315 baluns with a single-to-differential conversion of the input signal. The buffer stage drove a 50-Ω load for measurement. The IF port was measured using off-chip baluns with a differential-to-single conversion at the output signal. An Agilent N5247A network analyzer was used for

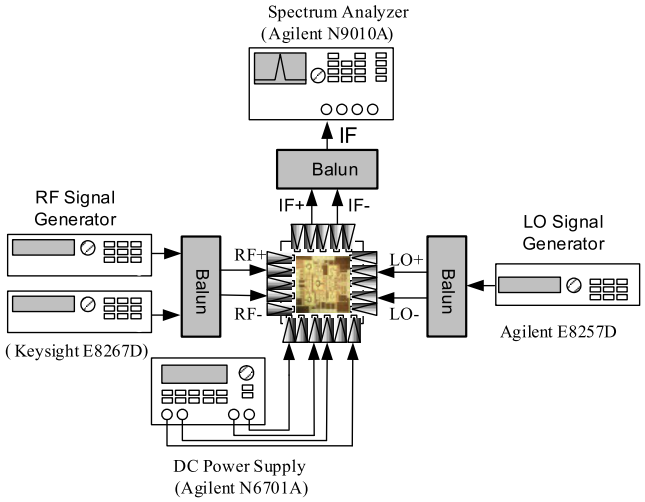


FIGURE 16. Schematic of IIP3 measurement setup.

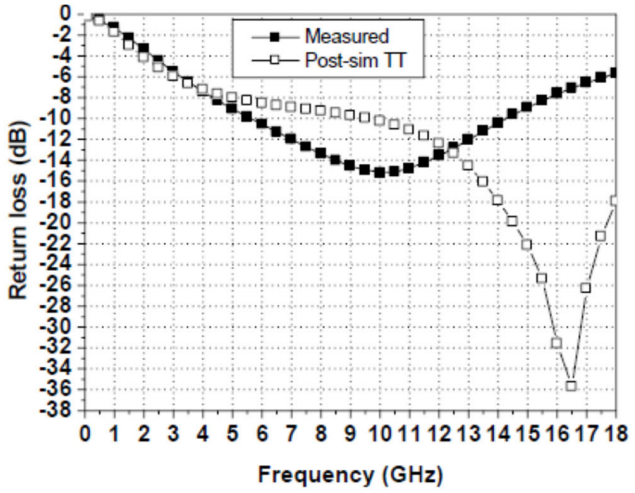


FIGURE 17. Simulation and measurement of RF port return loss.

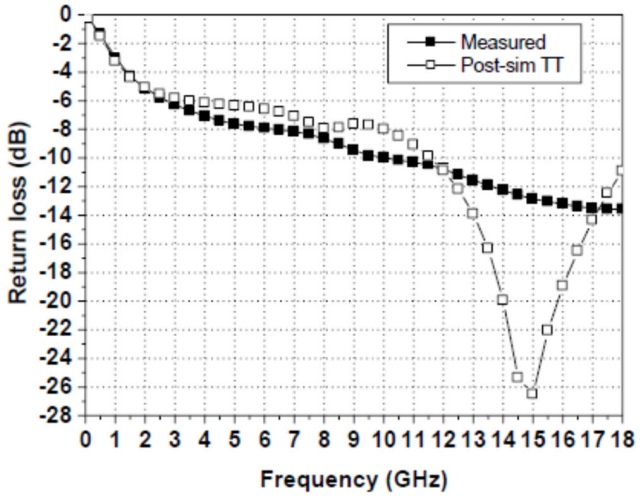


FIGURE 18. Simulation and measurement of LO port return loss.

the return and insertion loss measurements. As illustrated in Figure 16, the linearity was assessed using two Keysight E8267D CW generators and an Agilent N9010A spectrum

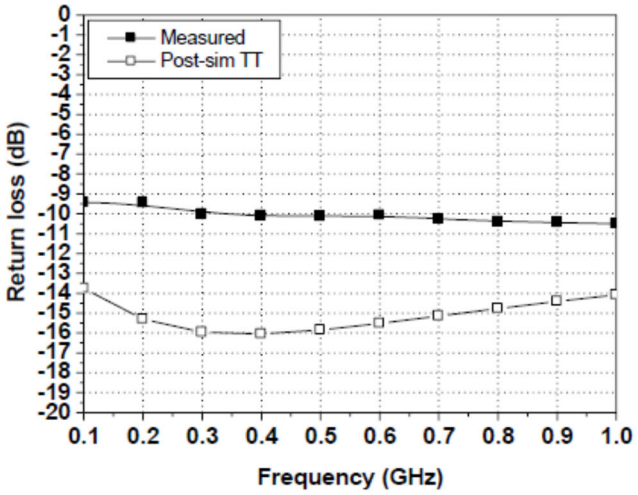


FIGURE 19. Simulation and measurement of IF port return loss.

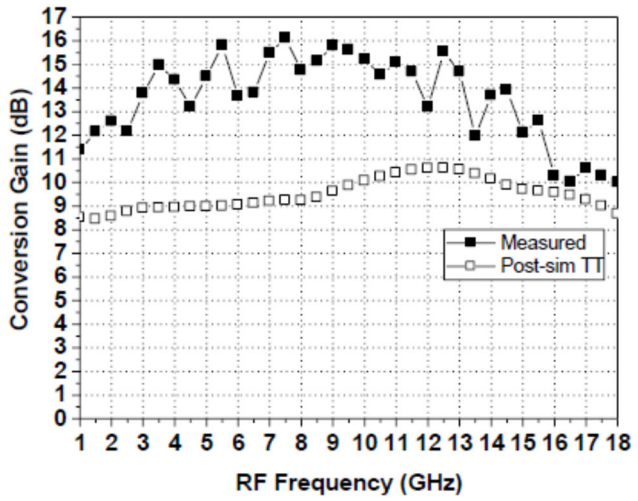


FIGURE 20. Simulation and measurement of conversion gain relative to the RF frequency and an IF frequency of 264 MHz.

analyzer, and the noise figure was measured using an Agilent E4448A meter. The performance of the mixer was measured using an RF signal of −30 dBm and an LO signal of 0 dBm. The fixed IF frequency was 264 MHz, and the LO frequency was swept from 1 to 18 GHz. The total DC power consumption of the mixer, including the output buffer, was 6.8 mW, and its core power consumption was approximately 2.3 mW. Figure 17 shows the measured return loss for the RF port. The measured return loss for the LO port is shown in Figure 18. Figure 19 shows the measured return loss for the IF port. Compare simulated and measured results for RF ports. Post-simulation data due to process drift and parasitics in layout. The return loss of the RF port shifts forward, causing the sweet spot for subsequent gain and noise measurements to shift. The mixer design is broadband, and there are certain differences between the measured results and the simulation results; however, this difference is acceptable within the frequency operating range of the broadband mixer. Figure 20 shows the measured down-conversion gain versus RF

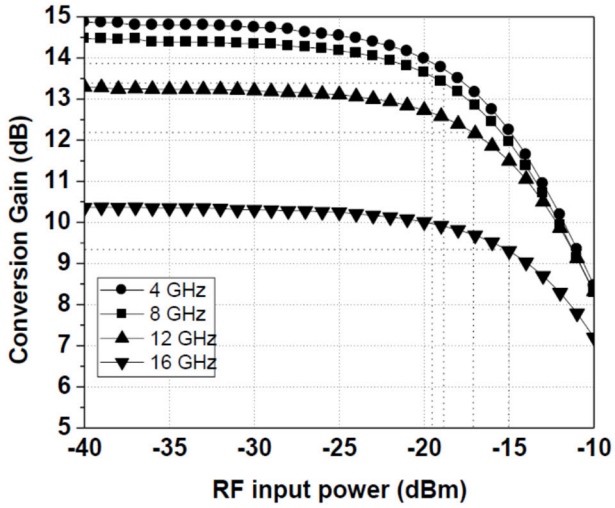


FIGURE 21. Measured conversion gain versus RF power with the LO power of 0 dBm.

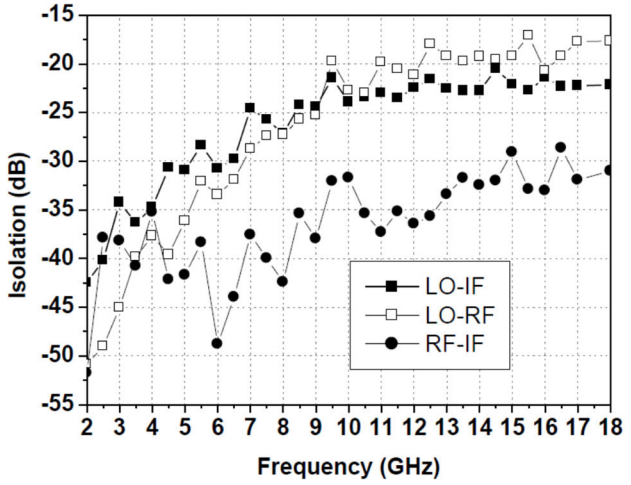


FIGURE 22. Measured port-to-port isolation versus RF frequency with LO of 0 dBm and RF of −30 dBm.

frequency when the LO signal is 0 dBm and the RF signal is −30 dBm. The down-conversion mixer can achieve a conversion gain of 10.1–15.9 dB in the range of 1–18 GHz. Compare simulated and measured results of conversion gain. The conversion gain measurement results are better than the expected simulation results. The main reason is that process drift in the actual manufacturing process may cause changes in component properties. At high frequencies, parasitic capacitance and inductance can significantly affect the behavior of RF circuits, causing transmission line effects to become significant. These parasitic effects are often difficult to model accurately and can lead to simulation and measurement errors. Figure 21 shows the measured conversion gain with respect to the RF power. As shown in this figure, the input P1dB is −19.5∼−15 dBm. The measured port-to-port isolations (LO–RF, LO–IF, and RF–IF) range is 2–18 GHz, as shown in Figure 22. The measured IIP3 is −8 dBm at 2 GHz, as shown

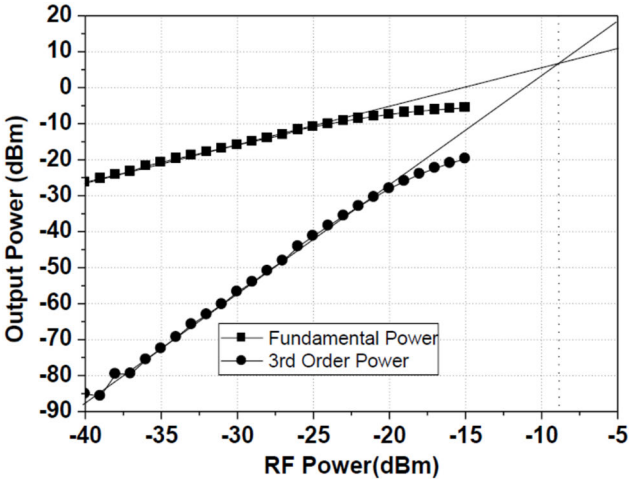


FIGURE 23. Measured IIP3 at 2 GHz.

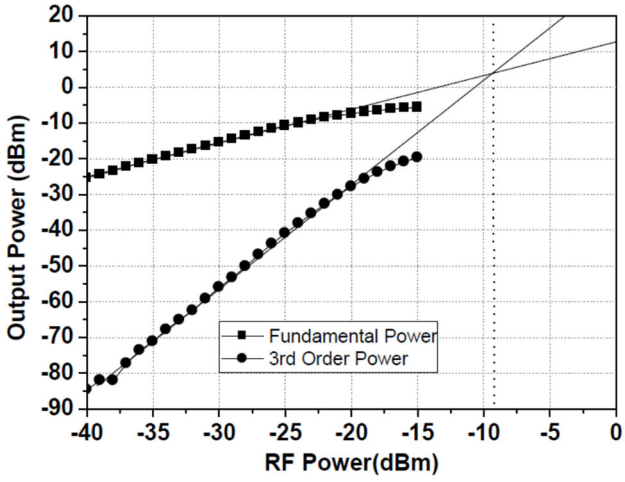


FIGURE 24. Measured IIP3 at 8 GHz.

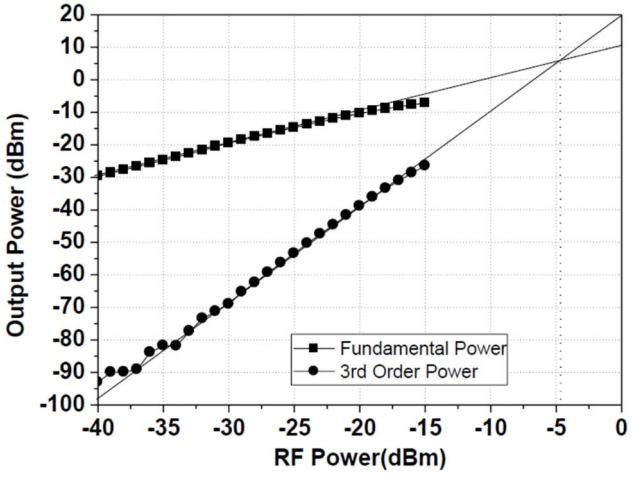


FIGURE 25. Measured IIP3 at 16 GHz.

in Figure 23. Figure 24 shows the measured IIP3 is −9.2 dBm at 8 GHz. The measured IIP3 is −5 dBm at 16 GHz, as shown in Figure 25. The measured linearity from 2 to 18 GHz is shown in Figure 26, and the IIP3 is −4∼−9.2 dBm.

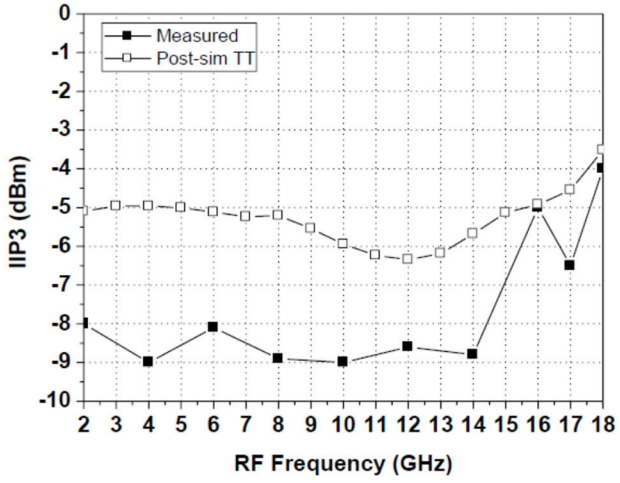


FIGURE 26. Simulated and measured IIP3 versus RF frequency.

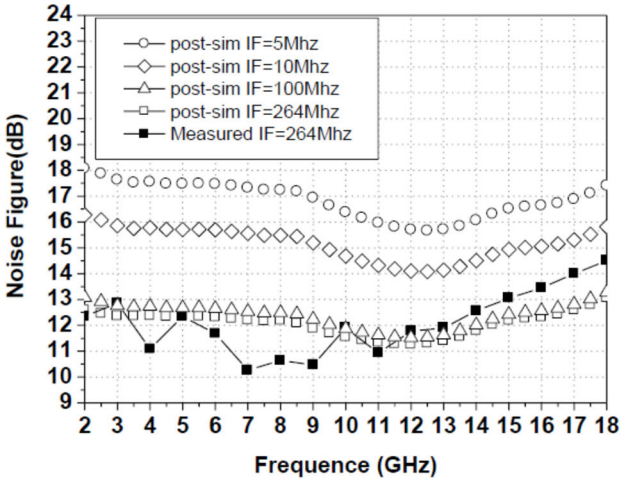


FIGURE 27. Simulated and measured double-sideband noise figure versus RF frequency.

Compare simulated and measured results for linearity. The linearity is inversely proportional to conversion gain. Therefore, as the conversion gain measurement increases, the linearity of the measurement decreases. Figure 27 shows that the measured double-sideband (DSB) noise of 10.3–14.5 dB from 2 to 18 GHz. Compare simulated and measured results for noise. The return loss of the RF port shifts forward, causing the sweet spot for noise measurements to move forward. The flicker noise is inversely proportional to the IF frequency. Therefore, noise increases at low IF frequencies. A photomicrograph of the fabricated circuit with a die area of 0.917 × 1.1 mm^{2}including the pad frame is shown in Figure 28. Table 2 lists the measured results and compares them with those of the existing mixers. The gains of the mixers in [5], [6], [16], [17], [18], and [19] were extremely small for the frequency band above 10 GHz when the supply voltage was less than 1.2 V. The gain was attenuated owing to the transconductance stage of the MOS element as it operates at high frequencies. Therefore, a high supply voltage was required to achieve high conversion gain [12], [19], [20], [21], [22], [23]. The mixer in [12] provides a high gain; however, its bandwidth response was only 23–25 GHz, and this linearity measurement was not provided. This linearity was inversely

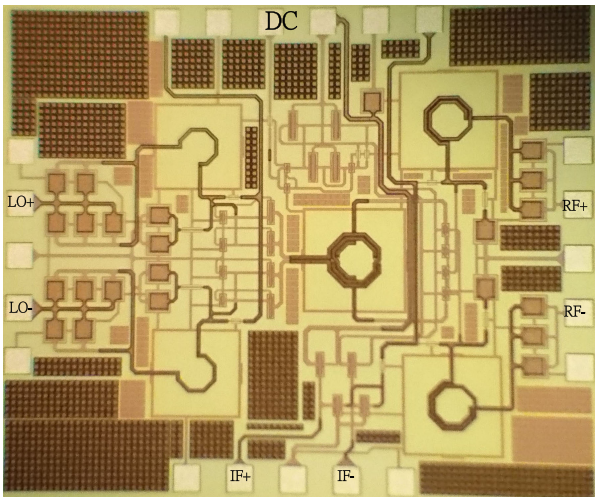


FIGURE 28. Chip microphotograph (chip area of 0.917 × 1.1 mm^2 including the pad frames).

TABLE 2. The performance of existing L to Ku Wideband Mixers.

Ref.	CMOS (μm)	Freq. (GHz)	LO (dBm)	Gain (dB)	IF (MHz)	IIP3 (dBm)	NF (dB)	V_{DD}	P_{DC} (mW)	Die Area (mm^2)
[5]	0.18	3.4-8.4	0	6.5~9.5	10	-5	12.4-13.3 [a]	1	3.18	1.14 x1.08
[6]	0.18	3.4-6.8	0	4.3~7.2	10	2~3	13.9-14.4[a]	1	2.9	1.145x1.08
[12]	0.13	23-25	-3	24.8~26.1	100	N/A	7.1-7.8[a]	1.5	16.8	0.8x1.2
[16]	0.18	2.1-12	5	6.9~9.9	264	-10	11.8-14[a]	0.8	*0.88	0.62x0.58 [c]
[17]	0.18	1-6	8.7	4~7	100	0	13.5~17[a]	1	*0.63	0.36
[18]	0.065	4-8.8	0	8~10.7	200	-4	3.8~5.8[a]	1	11.5	0.81x0.66[c]
[19]	0.13	1-10	0	3~8	100	-7	11.3-15[b]	1.2	8.4	0.7x0.4
[20]	0.18	11-20	-5	10.1~13.6	100	−5	8.6 -11.2[a]	1.8	8.3	0.77 x 0.75
[21]	0.18	0.2-16	-2	5.3~8.3	528	N/A	N/A	1.8	15	0.68x0.65
[22]	0.18	1-6	7	10~13	170	-4.5	12-18 [a]	1.8	*3.45	0.819 x0.655
[23]	0.18	2-27	3	11.5~13.5	10	0	14.3-17[b]	2	40	0.87x0.82
[24]	SiGe 0.18	3-11	0	9.8~10.6	264	-8	12.2-14.1[a]	1	4.3	0.84x0.85[c]
[25]	SiGe 0.18	3-11	7	8.8~17.1	264	-10~0	12.8~16.56[b]	1	3.45	0.875x0.89[c]
This Work	0.18	1-18	0	10.1~15.9	264	-9.2~-4	10.3~14.5[a]	1	6.8	0.917 x 1.1[c]

*excluding buffers [a]:DSB [b]:SSB [c]: Including DC and RF pads. The double side band (DSB) noise is calculated as the single-sideband noise minus 3dB.

proportional to the gain. References [24] and [25] used a 0.18-μm SiGe BiCMOS process with a gain of more than 10 dB when the supply voltage is less than 1 V. The gain is greater than 10 dB at 3.1–10.6 GHz. The primary reason for this is the low-voltage folded-switch mixer topology that combines the advantages of the BJT (HBT) and CMOS. The gain was boosted by the transconductance stage of the BJT element as it operated at a high frequency. When the supply voltage was lower than 1 V, the proposed mixer had a higher bandwidth and gain and a lower noise figure than the existing mixers.

IV. CONCLUSION

A 1–18 GHz down-conversion mixer was designed and fabricated using a TSMC 0.18-μm CMOS process. The proposed mixer offers a measured conversion gain of 10.1–15.9 dB, third-order input intercept point of −4∼−9.2 dBm, and noise figure of 10.3–14.5 dB over 1–18 GHz. The total power consumption, including the output buffer, was only 6 mW when the power supply voltage was 1 V. This mixer adopts an inductor parallel-series switched-stage technology, which can effectively increase the switching current above a high frequency and improve the conversion gain when the power supply voltage is less than 1 V. The measurement results showed excellent bandwidth and gain performance.

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