IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 16 September 2023, accepted 14 October 2023, date of publication 23 October 2023,
date of current version 14 November 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3326818

RESEARCH ARTICLE

A Ka-Band 3-Bit GaN Digital Step Attenuator Using Phase Compensation Method

SEONHYE JANG[1], (Student Member, IEEE), JUNHYUK YANG[1], (Student Member, IEEE), JAEYONG LEE[1], (Student Member, IEEE), AND CHANGKUN PARK[1,2], (Member, IEEE)

[1]Department of Electronic Engineering, College of Information Technology, Soongsil University, Seoul 06978, Republic of Korea
[2]Department of Intelligent Semiconductors, College of Information Technology, Soongsil University, Seoul 06978, Republic of Korea

Corresponding author: Changkun Park (pck77@ssu.ac.kr)

This work was supported in part by the National Research Foundation of Korea (NRF) through the Korean Government [Ministry of Science and ICT (MSIT)] under Grant NRF-2021R1A2C1013666, and in part by the Development of Civil-Military Technology Project from the Institute of Civil-Military Technology Cooperation (ICMTC) under Grant 21-CM-RA-02.

ABSTRACT In this study, a 3-bit digital step attenuator (DSA) based on the GaN HEMT process was designed. A distributed structure was adopted to secure stable RF characteristics within a given operating frequency band. To suppress the phase variation according to the attenuation level in the distributed structure, a technique that utilizes a tail capacitor connected in series with a switch transistor has been proposed. The theoretical functionality of the proposed technique has been verified with a numerical analysis. For experimental feasibility verification of the proposed structure, a 3-bit DSA was designed using a 150-nm GaN HEMT process providing two metal layers. The chip size of the designed attenuator was 0.95 mm^2. The measured total attenuation range was 7 dB with 1 dB step. It was confirmed that the measured insertion loss was suppressed to less than 1.7 dB in the range of 26.5 to 40.0 GHz. The RMS amplitude and phase errors were measured to be less than 0.16 dB and 4.87°, respectively.

INDEX TERMS Attenuator, distributed structure, GaN switch, Ka-band, wideband.

I. INTRODUCTION

Along with the commercialization of 5G mobile communication, research on integrated circuits (ICs) constituting 5G mobile communication systems has been actively conducted. However, while the frequency band below 6 GHz for 5G mobile communication has been commercialized, the mm-wave band has technical difficulties for commercialization such as large path loss and atmospheric attenuation. Nevertheless, it is essential to secure circuit design technology in the mm-wave band to provide true 5G communication services over wide bandwidth.

In order to solve the problem of the mm-wave band for such 5G applications, a beamforming system and a small cell technology have been introduced [1], [2]. When implementing a beamforming system by arranging communication modules into multi-channels, the roles of phase shifters, variable gain amplifiers, and attenuators become important [3]. Among them, attenuators are used for various purposes, such as controlling the side lobe of the antenna beam pattern and correcting the channel signal of the array system. Thus, attenuation range, attenuation step, bandwidth, insertion loss, amplitude and phase errors, and high linearity are important parameters of the attenuator. In particular, it is important to suppress the RMS amplitude and phase errors of the attenuator in order to successfully secure the required beam characteristics of the beamforming system [4], [5]. In addition, the errors should be suppressed to avoid complex phase calibration [6], [7].

In previous studies, attenuators were designed primarily in T- and π-type structures considering attenuation level [7], [8], [9], [10]. However, in these structures, since a switch composed of a transistor is located on an RF signal line, RF characteristics vary greatly depending on an operating frequency [11], [12].

In addition, in order to support small cell technology, IC design technology with high power handling capability is essential. From the perspective of power handling capability,

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

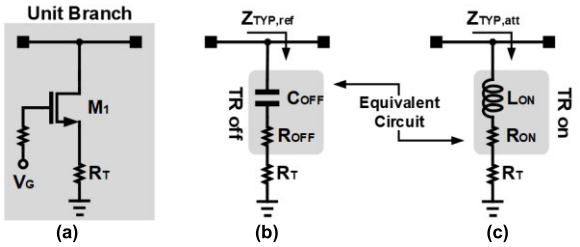

FIGURE 1. Typical distributed structure: (a) unit branch and equivalent circuits of (b) reference and (c) attenuation modes.

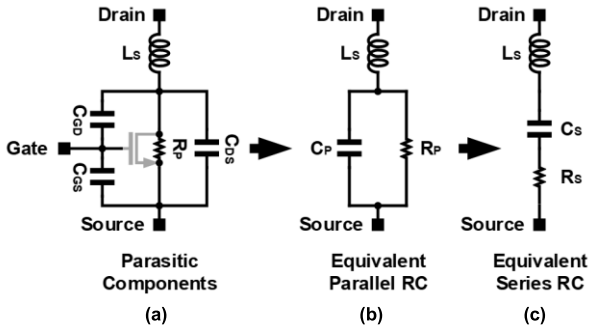

FIGURE 2. Equivalent circuits of the transistor: (a) transistor with parasitic components, (a) equivalent parallel RC circuit and (c) equivalent series RC circuit.

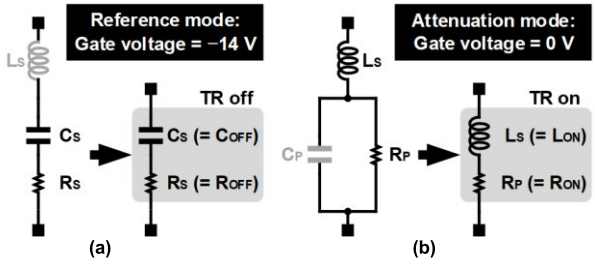

FIGURE 3. Simplified equivalent circuits of the transistor for (a) off- and (b) on-states.

GaN-based ICs for mm-wave band communication systems are actively attracting attention [13]. Compared to Si, GaAs, and SiC, GaN has the largest energy band gap and may ensure linearity even at high power. In addition, GaN is suitable as an element for the mm-wave band circuit because of its high electron mobility and fast switching characteristics at high frequencies [14], [15], [16].

In this study, we aimed to design a wideband GaN attenuator with low insertion loss and stable frequency characteristics. Distributed structure was used to secure the wideband characteristics. We also proposed an attenuator that minimizes RMS phase error by attaching tail capacitors to the distributed structure.

In Section II-A, we described the equivalent circuits of the designed attenuator. The conceptual structure of the proposed attenuator was provided in Section II-B. The proposed phase compensation technique using the tail capacitor was theoretically verified in Section II-C. In Section II-D, we showed distributed matching networks for wideband characteristics. In Section III, simulation and measurement results were compared.

II. DESIGN OF THE PROPOSED GaN ATTENUATOR

In this study, a digital step attenuator was designed by applying a distributed structure to secure wideband characteristics [7], [11]. In addition, a tail capacitor technique was proposed to suppress phase error. For the analysis, first, the typical unit branch constituting the distributed structure was considered as shown in Fig. 1. From the analysis of the equivalent circuits, the cause of the phase error is identified and the proposed design technique is described to mitigate the phase error.

A. EQUIVALENT CIRCUITS FOR THE GaN HEMT ATTENUATOR

Fig. 1 shows the unit branch of the typical attenuator with distributed structure. When the transistor of the unit branch is turned off and on, the attenuator operates in the reference and attenuation modes, respectively.

Fig. 1(b) and Fig. 1(c) are equivalent circuits in the reference and attenuation modes, respectively. Here, the process of configuring the equivalent circuits is shown in more detail in Fig. 2. The transistor can be represented by parasitic capacitances C_{GD}, C_{DS}, and C_{GS}, the parasitic resistance R_P, and the parasitic inductance L_S. The L_S includes metal lines connected to source and drain of the unit transistor. The C_P in Fig. 2(b) can be expressed as C_{GD}, C_{DS}, and C_{GS} as follows.

$$C_P = \frac{C_{GD}\,C_{GS}}{C_{GD} + C_{GS}} + C_{DS} \tag{1}$$

Furthermore, the equivalent parallel RC circuit of Fig. 2(b) can be converted into an equivalent series RC circuit as shown in Fig. 2(c) through the following equation.

$$R_S = \frac{R_P}{1 + (\omega\, R_P C_P)^2}$$
$$C_S = \left(1 + \frac{1}{(\omega\, R_P C_P)^2}\right) C_P \tag{2}$$

As illustrated in Fig. 3, these equivalent series and parallel RC circuits were used as simplified transistor models under reference and attenuation mode conditions, respectively. In particular, the reason for using the equivalent series RC circuit in the reference mode is to ensure the convenience of analysis by considering the passive devices connected in series with the source of the transistor in the next design process.

As shown in Fig. 3, parasitic components of actually used transistor were investigated to further simplify equivalent series and parallel RC circuits. In this study, the size of GaN HEMT was set to a gate width of 25 μm under the 150-nm gate length condition through transistor optimization process. The used transistor is centered-gate optimized structure for switching. Here, the transistor size was selected so that the transistor can act as a switch and the on-resistance (R_{ON})

TABLE 1. Parasitic components of the transistor (gate width = 25 μm, gate length = 150 nm).

Parasitic components	Range (Freq.: 26.5–40.0 GHz)
R_S (= R_{OFF}) with V_G = −14 V	16.86–7.61 Ω
R_P (= R_{ON}) with V_G = 0 V	74.9–74.3 Ω
C_S (= C_{OFF})	12.06–13.37 fF
L_S (= L_{ON})	200.8–207.2 pH

of the transistor along with the R_T can act as an attenuator. In particular, when the size of the transistor increases, the R_{ON} of the transistor decreases, so the required R_T increases, and parasitic inductance and capacitances increase, thereby reducing the bandwidth of the entire attenuator.

In Table 1, the ranges of parasitic components of the used transistor in the range of operating frequencies 26.5 GHz to 40.0 GHz are summarized. In the case of the reference mode of Fig. 3(a), as the impedance by L_S is negligible compared to the impedance by C_S, the transistor can be simplified into C_S (= C_{OFF}) and R_S (= R_{OFF}) connected in series. On the other hand, in the case of the attenuation mode of Fig. 3(b), the impedance by C_P is negligibly larger than that of R_P in parallel connection, so the transistor can be simplified to L_S (= L_{ON}) and R_P (= R_{ON})connected in series.

As a result, as shown in Fig. 1(b), in the reference mode, since the transistor is turned off, the transistor may be equivalently modeled with a resistance, R_{OFF} and capacitance, C_{OFF}. Similarly, Fig. 1(c) is equivalent circuit in the attenuation mode of the unit branch. In the attenuation mode, since the transistor is turned on, the transistor may be equivalently modeled with an inductance, L_{ON} and a resistance, R_{ON}.

B. PROPOSED STRUCTURE OF ATTENUATOR WITH TAIL CAPACITOR

Fig. 4 shows a more simplified versions of the equivalent circuits shown in Fig. 1 for convenience of analysis. Here, the C_{OFF} in the reference mode was regarded as open circuit. Assuming that the load of the unit branch is the resistor, R_{LOAD}, the equivalent circuits of the ideal reference and attenuation modes are shown in Fig. 4(a) and Fig. 4(b), respectively. In such an ideal case, there is no phase imbalance between reference and attenuation modes.

However, in the actual situation of the attenuation mode, as shown in Fig. 1(c), there is parasitic inductance, L_{ON} of transistor. The L_{ON} in Fig. 1(c) is indicated as L_A in Fig. 4(c). The L_A causes a phase error in the attenuation mode. In this study, tail capacitor, C_T was added as shown in Fig. 4(d) to offset the effect of L_A. In the proposed attenuator structure with C_T, the Z_{PRO} of Fig. 4(d) can be conversed to ideal resistive impedance, Z_{IDE} of Fig. 4(b) through an appropriate C_T value according to the L_A value in consideration of the operating frequency. As a result, the use of C_T is a technique that can mitigate phase imbalance between reference and attenuation modes in actual situations.

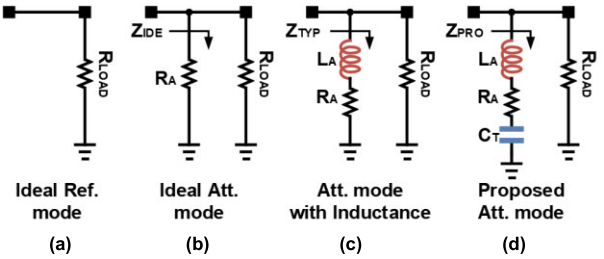

FIGURE 4. Conceptual equivalent circuits for (a) ideal reference mode, (b) ideal attenuation mode, (c) attenuation mode with parasitic inductance, and (d) proposed attenuation mode with tail capacitor.

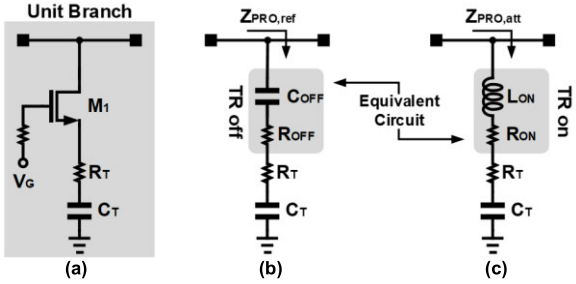

FIGURE 5. Proposed distributed structure with a tail capacitor: (a) unit branch and equivalent circuits of (b) reference and (c) attenuation modes.

C. NUMERICAL ANALYSIS OF THE PROPOSED ATTENUATOR WITH USING TAIL CAPACITOR

Based on the concept of the proposed attenuator structure with C_T shown in Fig. 4, the phases of the typical and proposed structures were numerically analyzed. The unit branch of the proposed attenuator using C_T and its equivalent circuits were shown in Fig. 5.

In the typical unit branch of the distributed attenuator shown in Fig. 1, the equivalent impedance and phase can be calculated as the following equations.

$$Z_{TYP,ref} = \frac{1 + j\omega C_{OFF} R_{OFF,t}}{j\omega C_{OFF}} \Big\| \frac{1}{2} Z_0 \tag{3}$$

$$\tan\left(\theta_{TYP,ref}\right) = \frac{-\omega C_{OFF} Z_0}{2 + \omega^2 C_{OFF}^2 R_{OFF,t}\left(2R_{OFF,t} + Z_0\right)} \tag{4}$$

$$Z_{TYP,att} = \left(j\omega L_{ON} + R_{ON,t}\right) \| \frac{1}{2} Z_0 \tag{5}$$

$$\tan\left(\theta_{TYP,att}\right) = \frac{\omega L_{ON} Z_0 \left(R_{ON,t} + Z_0\right)}{2\omega^2 L_{ON}^2 Z_0 + Z_0 R_{ON,t}\left(R_{ON,t} + \frac{1}{2} Z_0\right)} \tag{6}$$

where, $Z_{TYP,ref}$, and $Z_{TYP,att}$ are equivalent impedances in the reference and attenuation modes of the typical distributed structure, respectively. $\theta_{TYP,ref}$ and $\theta_{TYP,att}$ are equivalent phases in the reference and attenuation modes, respectively. $R_{OFF,t}$ and $R_{ON,t}$ are $R_{OFF} + R_T$ and $R_{ON} + R_T$, respectively.

Similarly, in the proposed unit branch shown in Fig. 5, the equivalent impedance and phase can be calculated as the

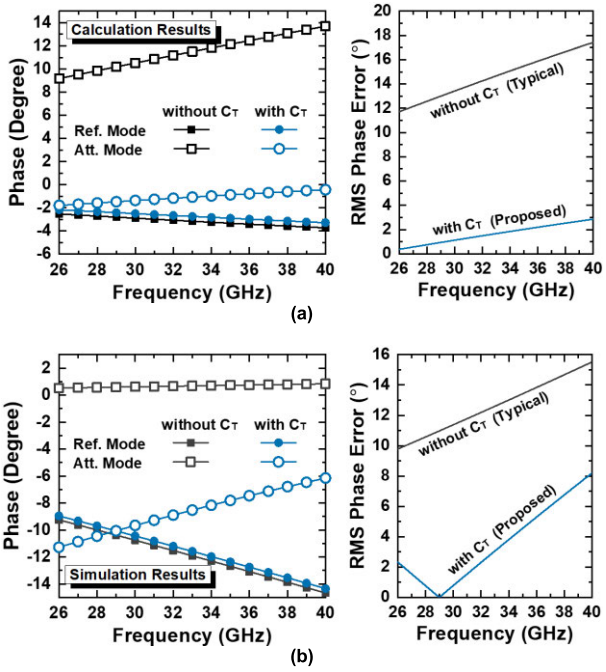

FIGURE 6. Phase of S_{21} and RMS phase error according to transistor on/off: (a) calculation and (b) simulation results.

following equations.

$$Z_{PRO,ref} = \frac{\omega C_T C_{OFF} R_{OFF,t} - j\left(C_T + C_{OFF}\right)}{\omega C_T C_{OFF}} \Big\| \frac{1}{2} Z_0 \tag{7}$$

$$\tan\left(\theta_{PRO,ref}\right) = \frac{-\omega C_{OFF} C_T \left(C_{OFF} + C_T\right) Z_0}{\omega^2 C_{OFF}^2 C_T^2 R_{OFF,t} \left(2R_{OFF,t} + Z_0\right) + 2\left(C_{OFF} + C_T\right)^2} \tag{8}$$

$$Z_{PRO,att} = \frac{j\omega^2 C_T L_{ON} - j + \omega C_T R_{ON,t}}{-\omega C_T} \Big\| \frac{1}{2} Z_0 \tag{9}$$

$$\tan\left(\theta_{PRO,att}\right) = \frac{\omega C_T \left(\omega^2 C_T L_{ON} - 1\right) Z_0}{\omega^2 C_T^2 R_{ON,t} \left(2R_{ON,t} + Z_0\right) + 2\left(\omega^2 C_T L_{ON} - 1\right)^2} \tag{10}$$

where, $Z_{PRO,ref}$, $Z_{PRO,att}$, $\theta_{PRO,ref}$, and $\theta_{PRO,att}$ are equivalent impedance and phase in the reference and attenuation modes of the proposed distributed structure, respectively.

The equivalent impedance and phase of the unit branch of the attenuator can be calculated through the extracted R_{OFF}, R_{ON}, C_{OFF}, L_{ON}, R_T, and C_T. In the calculation, C_T was set to 75 fF, taking into account the other extracted parasitic values. If the input and output impedance are matched to Z_0 and the R_T is 140 Ω, from the Eqs. (4) and (6), the output phases of the typical distributed attenuator at the operating frequency of 28 GHz can be calculated as −2.69° and 9.83° in the reference and attenuation modes, respectively. Therefore, the difference in output phase between each mode is approximately 13°.

For the proposed distributed attenuator case, the output phases at the operating frequency of 28 GHz can be calculated as −2.39° and −1.09° in the reference and attenuation modes, respectively. Therefore, the difference in output phase between each mode is approximately 1.3°.

This analysis shows that the tail capacitor, C_T is effective in suppressing the output phase variation due to bit regulation in the attenuator. Fig. 6 shows the calculation and simulation results of the output phase according to reference and attenuation modes of the typical and proposed unit branch according to the frequency. Simulation results also show that the tail capacitor, C_T successfully suppresses the variations in the output phase.

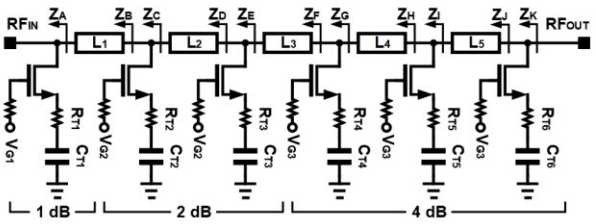

FIGURE 7. Schematic of the designed Ka-band GaN attenuator.

TABLE 2. Parameters of the used components.

Device	Value	Device	Value	Device	Value
R_{T1}	140 Ω	C_{T1}	75 fF	L_1	257.4–362.4 pH
R_{T2}	140 Ω	C_{T2}	75 fF	L_2	257.4–362.4 pH
R_{T3}	140 Ω	C_{T3}	75 fF	L_3	119.1–128.5 pH
R_{T4}	90 Ω	C_{T4}	67 fF	L_4	352.8–709.5 pH
R_{T5}	90 Ω	C_{T5}	67 fF	L_5	352.8–709.5 pH
R_{T6}	90 Ω	C_{T6}	67 fF	-	-

D. SECURING WIDEBAND USING DISTRIBUTED STRUCTURE

A schematic of the designed attenuator is shown in Fig. 7. The attenuator controlled by a 3-bit digital signal was designed using a 150-nm GaN HEMT process that provides two metal layers. The values of the main devices used in the proposed attenuator are shown in Table 2. In the schematic, all gate bias resistors were designed to be 11 kΩ. The gate bais resistor serves to remove undesired effects from impedance by bonding-wire for bias voltage.

In order to secure a wideband, a distributed structure in which a series inductor and a shunt capacitor are repeated was used. At this time, the inductor was implemented as a transmission line, and the shunt capacitor was implemented as a parasitic capacitance, C_{OFF} of off-state transistor and a tail capacitor C_T. As a result, the impedance at the nodes of "A" to "K", which are the main nodes of Fig. 7, was designed to be located around 50 Ω. From the impedances of Smith

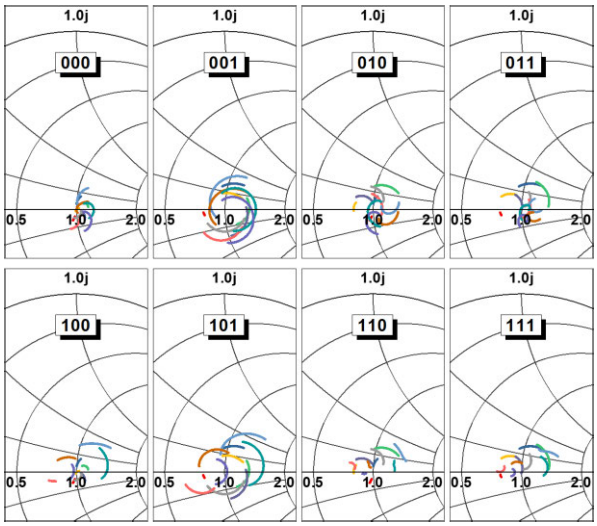

FIGURE 8. Simulated S-parameters from *A* to *K* nodes according to the control bits (frequency range: 26.5 – 40.0 GHz).

chart for each node in 000- and 111-bits shown in Fig. 8, it was confirmed that the proposed attenuator has wideband characteristics in Ka-band.

III. SIMULATION AND MEASUREMENT RESULTS

In this section, the simulation and measurement results are provided. Additionally, the comparison between proposed and previously reported attenuators is provided.

A. SIMULATION RESULTS

Fig. 9 shows the simulation results of the designed attenuator. Simulated S_{11} and S_{22} are -15.13 dB and -14.26 dB or less in the Ka-band, respectively. As shown in Fig. 9(b), the insertion loss is lower than 1.82 dB. Fig. 9(c) is a result of simulated attenuation level of other bits based on S_{21} of 000-bit. Fig. 9(d) is a graph of calculated output phase difference for each bit based on a simulated phase of S_{21} of 000-bit. As the C_T decreases, the crossing point is formed at a higher frequency. However, due to the minimum capacitance limit of the capacitor provided by the used foundry, the crossing point was slightly lower than the center frequency. The minimum available capacitor is 67 fF, the C_{T4}, C_{T5}, and C_{T6} are the minimum values of 67 fF. On the other hand, C_{T1}, C_{T2}, and C_{T3} were initially set to 67 fF, but were finally designed to 75 fF through optimization considering bandwidth, S_{11}, and amplitude and phase errors.

Fig. 10(a) is a graph of RMS amplitude and phase errors. The simulated RMS amplitude and phase errors were lower than 0.267 dB and 8.77°, respectively. Simulated RMS amplitude and phase errors were the lowest at 28.9 GHz and 30.4 GHz, respectively, with 0.026 dB and 0.55°. As shown in Fig. 10(b), the simulated maximum magnitude of the difference of the group delay was 0.56 psec. Here, the difference in the group delay was based on a group delay of 000-bit.

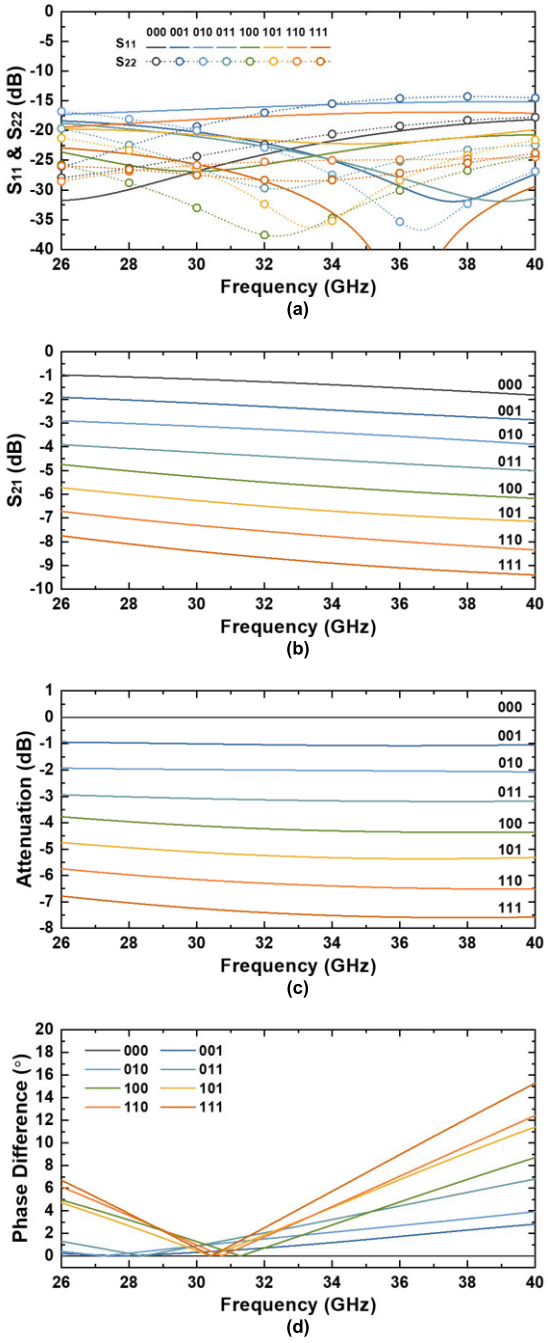

FIGURE 9. Simulation results: (a) S_{11} and S_{22}, (b) S_{21}, (c) attenuation, and (d) output phase difference.

B. MEASUREMENT RESULTS

Fig. 11 shows the chip photograph of the designed Ka-band GaN distributed attenuator. The chip size including test pads is 1.33×0.71 mm^2. The gate voltages of each transistor were 0 V and -14 V, respectively, for the on- and off-states of the transistor constituting the attenuator. DC voltages are applied through bonding-wire. On the other hand, input and output signals were measured through on-wafer probes.

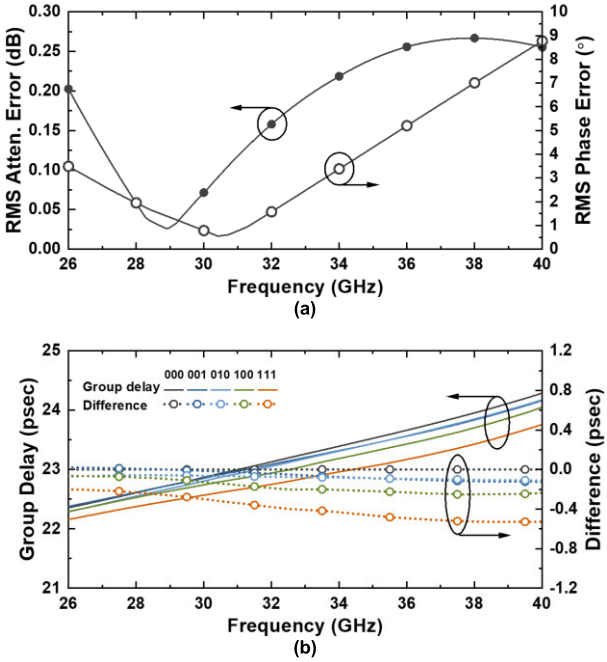

FIGURE 10. Simulation results: (a) RMS amplitude and phase errors and (b) group delay.

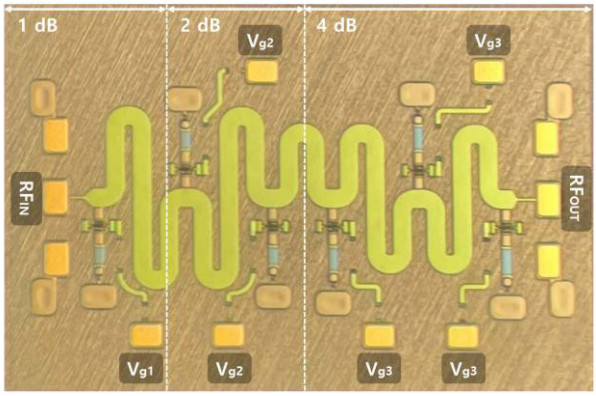

FIGURE 11. Chip photograph of the designed GaN attenuator (1.33 × 0.71 mm^2).

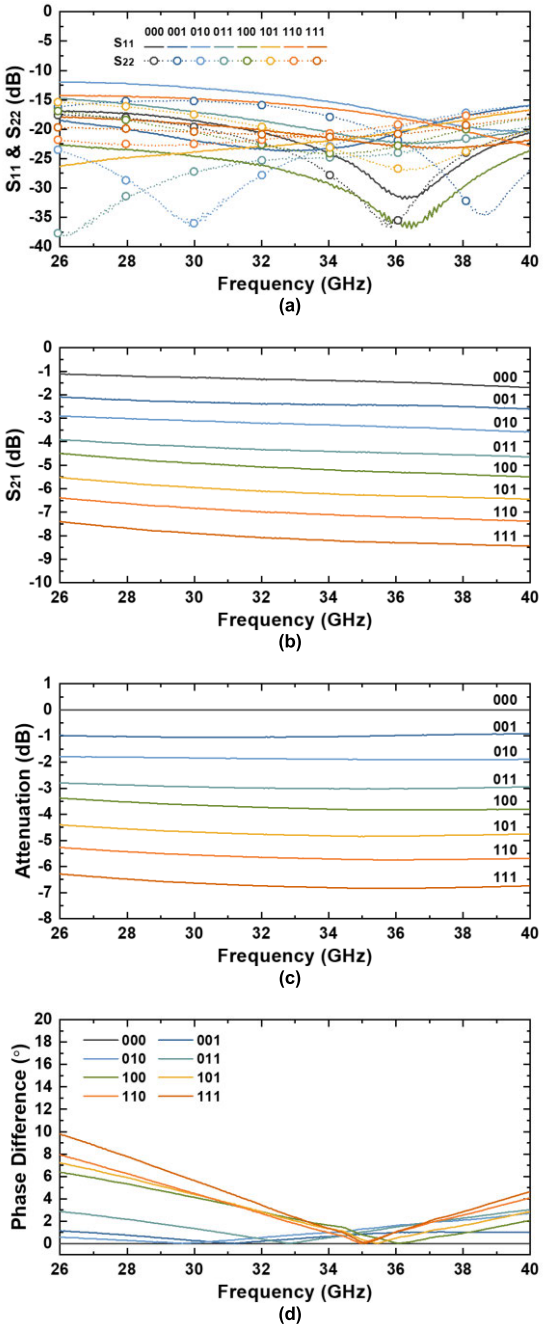

FIGURE 12. Measurement results: (a) S_{11} and S_{22}, (b) S_{21}, (c) attenuation, and (d) output phase difference.

In the small signal measurement, an input power of −30 dBm was used. In addition, even when the input power of 20 dBm, which is the maximum output power of the used network analyzer to measure the small signal characteristics, was used, the same results were obtained as when the input power of −30 dBm was used. In the large signal measurements, a commercial power amplifier was additionally used for measurements such as input 1dB gain compression point (P_{1dB}).

Fig. 12 shows the measurement results of the designed attenuator. The measured S_{11} and S_{22} are lower than −12 dB and −15.1 dB in the Ka-band, respectively. The measured insertion losses were 1.1 dB and 1.7 dB at 26.0 GHz and 40.0 GHz, respectively. Overall, the measured insertion loss was lower than 1.7 dB. Fig. 12(c) is a graph of the calculated attenuation level based on S_{21} of 000-bit which is an insertion loss. As shown in Fig. 12(d), the measurement results of the frequency at which the phase difference is minimized was moved slightly upward compared to the simulation result.

Fig. 13(a) is the measured RMS amplitude and phase errors. The measured RMS amplitude and phase errors were lower than 0.17 dB and 4.87°, respectively. Simulated RMS amplitude and phase errors were the lowest at 29.5 GHz and 35.1 GHz, respectively, with 0.074 dB and 0.62°. As shown in Fig. 13(b), the measured maximum magnitude of the difference of the group delay was 4.8 psec. Here, the difference in the group delay was based on a group delay of 000-bit.

TABLE 3. Performance comparison with various RF attenuators.

Ref.	Process	Freq. (GHz)	Atten. range (dB)	Control bits	Insertion loss (dB)	Return loss (dB)	RMS amplitude error (dB)	RMS phase error (°)	IP_{1dB} (dBm)	Topology	Chip Size (mm^2)
T-CAS I '20 [4]	65-nm CMOS	37–40	31	5	7	> 12	< 0.27	< 3.7	12	Bridged-T/π-type with C_T	0.21
MWCL '18 [10]	130-nm SiGe BiCMOS	19–24	31.5	6	N/A	> 10	< 0.5	< 4.1	N/A	Switched T/π-type	0.51
T-MTT '20 [11]	65-nm CMOS	15–43	15	4	2.9–4.3	> 8.8	0.3–2.2	1–6	14 @ 35 GHz	DS	0.29
MWCL '21 [12]	130-nm SiGe BiCMOS	28–40	31	5	< 9.1	> 10	< 0.43	< 5.4	15.7 @ 35 GHz	DS & T/π-type	0.21
MWCL '15 [17]	180-nm BiCMOS	36–52	8	3	4.4–5.9	> 9.7	0.8–1.4	1.9–6.7	20 @ 44 GHz	Switched T/π-type	0.33
T-MTT '17 [18]	150-nm GaAs pHEMT	1.5–45	26	Analog	< 5.5	> 5	N/A	N/A	30	DS with stacked-FET	0.84
T-MTT '16 [19]	180-nm SiGe BiCMOS	22–29	13.7–14.5	4	5.4–7.9	> 9.9	< 0.51	< 4.7	14	Integrated diplexer attenuator	0.94
T-MTT '18 [20]	250-nm GaAs pHEMT	6–18	31.75	7	< 9	> 12	< 0.6	<5	N/A	Bridged-T type	5.4
IMS '19 [21]	100-nm GaN HEMT	30–40	18	5	N/A	N/A	< 1.5	< 10[1)]	N/A	Loaded line & π-resistive type	N/A
Analog Devices '20 [22]	GaAs	0.1–40	31	5	6.4	13 @ 40 GHz	N/A	N/A	N/A	ADH939S[3)]	2.176
Analog Devices '16 [23]	GaAs	0.1–40	31	5	7	> 10	N/A	N/A	24[2)]	HMC939A[3)]	2.34
This work	150-nm GaN HEMT	26.5–40.0	7	3	< 1.7	> 12	< 0.16	< 4.87	> 30.3	DS & C_T	0.947

* DS: distributed structure, ** C_T: tail capacitor, [1)] graphically estimated, [2)] input power for 0.1 dB compression, [3)] part number.

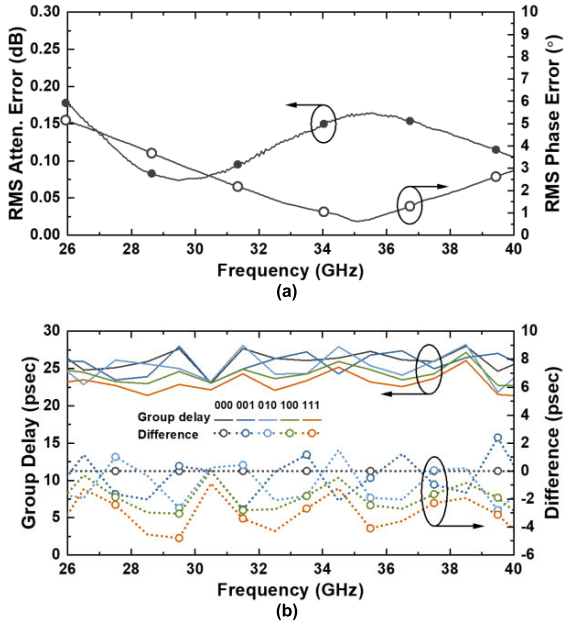

FIGURE 13. Measurement results: (a) RMS amplitude and phase errors and (b) group delay.

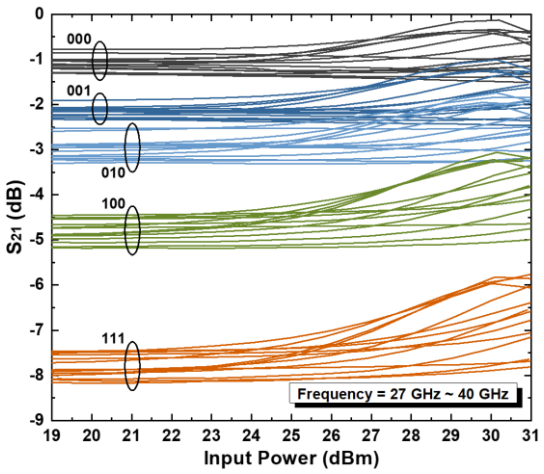

FIGURE 14. Measured S_{21} according to the input power.

Fig. 14 shows the measured power characteristic of the designed attenuator. Here, S_{21} according to the input power is shown in a 1 GHz step from an operating frequency of 27 GHz to 40 GHz for each attenuation bit. The measured input P_{1dB} was higher than 30.3 dBm. In Fig. 14, 000-bit indicates that the gate voltage of all transistors is −14 V, and all transistors are off-state. Conversely, 111-bit is a case where the gate voltage of all transistors is 0 V, and all transistors are on-state. As can be seen from the measurement results of Fig. 14, compared to a case where the gate voltage of the transistors

is high at 0 V, a case where the gate voltage is low at −14 V showed high linearity. That is, the power handling capability increased from 111- to 000-bits.

C. PERFORMANCE COMPARISON

The comparison of RF performances of proposed and previously reported attenuators are shown in Table 3. The insertion loss of the proposed attenuator is noticeably low compared to all other attenuators referenced. The RMS amplitude error is similar to the reference [17] with the same number of bits, and the RMS phase error is also the lowest among attenuators with bandwidth of 7 GHz or more. For attenuator with the better RMS phase error than this work, the bandwidths are 3 GHz, 7 GHz, and 5 GHz, respectively. The bandwidth of the designed attenuator is nearly twice as wide as that of the attenuator with the most similar RMS phase error.

In this study, although we designed a 3-bit attenuator, the proposed design technique is easily scalable to a higher attenuation range.

IV. DISCUSSIONS

In this study, in order to confirm the feasibility of the proposed design technique, C_T, a tail capacitor, was connected to the source of the transistor through R_T, a resistor. Accordingly, the source of the transistor is connected to the ground through C_T and R_T connected in series. Therefore, the voltage between the gate and the source changes according to the change in the source voltage caused by the voltage drop in C_T and R_T connected in series. However, in this study, performance degradation due to the voltage change between the gate and the source was not observed. Nevertheless, in some cases, there may be situations in which such voltage changes between the gate and the source should be removed.

Such stabilization of the voltage between the gate and the source can be secured by simple deformation of the circuit. As a variant of the proposed structure, C_T can also be connected to the drain of the transistor. In this case, a voltage between the gate and the source of the transistor in the on-state may be relatively stably secured. In particular, when both CT and RT are connected to the drain of the transistor, the source of the transistor is directely connected to the ground. In this case, the voltage between the gate and source of the transistor is most stabilized.

V. CONCLUSION

This paper presents the design of a Ka-band 3-bit digital step attenuator using 150-nm GaN HEMT process. The distributed structure was used for low insertion loss and wideband characteristics, and the distributed matching network was designed by implementing series inductance as a transmission line. It was proved through the numerical analysis that phase variation can be suppressed by compensating incorrect phases for each control bit using the tail capacitor. The total attenuation range was 7 dB with a step of 1dB. The maximum measured insertion loss is 1.7 dB and measured return loss is under −12 dB. The maximum measured RMS amplitude and phase errors were 0.16 dB and 4.87°, respectively over Ka-band.

REFERENCES

[1] M. G. S. Sriyananda, X. Wang, and R. K. Rao, "Crowdsensing-assisted path loss estimation and management of dynamic coverage in 3D wireless networks with dense small cells," *IEEE Access*, vol. 9, pp. 112670–112685, 2021, doi: 10.1109/ACCESS.2021.3100085.

[2] M. R. Akdeniz, Y. Liu, M. K. Samimi, S. Sun, S. Rangan, T. S. Rappaport, and E. Erkip, "Millimeter wave channel modeling and cellular capacity evaluation," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 6, pp. 1164–1179, Jun. 2014, doi: 10.1109/JSAC.2014.2328154.

[3] N. Peng, P. Gu, and D. Zhao, "A Ka-band balanced four-beam phased-array receiver with symmetrical beam-distribution network in 65-nm CMOS," *IEEE Access*, vol. 9, pp. 110026–110038, 2021, doi: 10.1109/ACCESS.2021.3100129.

[4] C. Zhao, X. Zeng, L. Zhang, H. Liu, Y. Yu, Y. Wu, and K. Kang, "A 37–40-GHz low-phase-imbalance CMOS attenuator with tail-capacitor compensation technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 10, pp. 3400–3409, Oct. 2020, doi: 10.1109/TCSI.2020.2990705.

[5] L. Zhang, C. Zhao, X. Zhang, Y. Wu, and K. Kang, "A CMOS K-band 6-bit attenuator with low phase imbalance for phased array applications," *IEEE Access*, vol. 5, pp. 19657–19661, 2017, doi: 10.1109/ACCESS.2017.2750203.

[6] S. Walker, "A low phase shift attenuator," *IEEE Trans. Microw. Theory Techn.*, vol. 42, no. 2, pp. 182–185, Feb. 1994, doi: 10.1109/22.275244.

[7] B.-W. Min and G. M. Rebeiz, "A 10–50-GHz CMOS distributed step attenuator with low loss and low phase imbalance," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2547–2554, Nov. 2007, doi: 10.1109/JSSC.2007.907205.

[8] H. Dogan, R. G. Meyer, and A. M. Niknejad, "Analysis and design of RF CMOS attenuators," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2269–2283, Oct. 2008.

[9] Z. Hao, W. Chuanchuan, and Z. Dezheng, "A high linearity digital attenuator with low phase variations for X-band phased array systems," in *Proc. IEEE Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, vol. 1, Beijing, China, Jun. 2016, pp. 173–175, doi: 10.1109/ICMMT.2016.7761714.

[10] Y. Yuan, S.-X. Mu, and Y.-X. Guo, "6-bit step attenuators for phased-array system with temperature compensation technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 8, pp. 690–692, Aug. 2018, doi: 10.1109/LMWC.2018.2849224.

[11] K. Park, S. Lee, and S. Jeon, "A new compact CMOS distributed digital attenuator," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 11, pp. 4631–4640, Nov. 2020, doi: 10.1109/TMTT.2020.3017820.

[12] K. Wang, T. Zhou, H. Zhang, and L. Qiu, "A 28–40-GHz digital step attenuator with low amplitude and phase variations," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 1, pp. 64–67, Jan. 2021, doi: 10.1109/LMWC.2020.3039914.

[13] T. Kim, H. Im, S.-H. Lee, K.-J. Kim, and C. Park, "Highly linear K-/Ka-band SPDT switch based on traveling-wave concept in a 150-nm GaN pHEMT process," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 8, pp. 987–990, Aug. 2022, doi: 10.1109/LMWC.2022.3161498.

[14] R.-J. Liu, X.-W. Zhu, J. Xia, Z.-M. Zhao, Q. Dong, P. Chen, L. Zhang, X. Jiang, C. Yu, and W. Hong, "A 24–28-GHz GaN MMIC synchronous Doherty power amplifier with enhanced load modulation for 5G mm-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 8, pp. 3910–3922, Aug. 2022, doi: 10.1109/TMTT.2022.3176818.

[15] A. Piacibello, R. Giofrè, R. Quaglia, R. Figueiredo, N. Carvalho, P. Colantonio, V. Valenta, and V. Camarchia, "A 5-W GaN Doherty amplifier for Ka-band satellite downlink with 4-GHz bandwidth and 17-dB NPR," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 8, pp. 964–967, Aug. 2022, doi: 10.1109/LMWC.2022.3160227.

[16] P. Chen, X.-W. Zhu, R.-J. Liu, Z. Zhao, L. Zhang, C. Yu, and W. Hong, "Harmonic suppression of a three-stage 25–31-GHz GaN MMIC power amplifier using elliptic low-pass filtering matching network," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 6, pp. 551–554, Jun. 2022, doi: 10.1109/LMWC.2022.3148793.

[17] J. Bae and C. Nguyen, "A 44 GHz CMOS RFIC dual-function attenuator with band-pass-filter response," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 4, pp. 241–243, Apr. 2015, doi: 10.1109/LMWC.2015.2403574.

[18] D. P. Nguyen, B. L. Pham, and A.-V. Pham, "A 1.5–45-GHz high-power 2-D distributed voltage-controlled attenuator," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4208–4217, Nov. 2017, doi: 10.1109/TMTT.2017.2706692.
[19] J. Bae and C. Nguyen, "A novel concurrent 22–29/57–64-GHz dual-band CMOS step attenuator with low phase variations," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 6, pp. 1867–1875, Jun. 2016, doi: 10.1109/TMTT.2016.2546256.
[20] J.-C. Jeong, I.-B. Yom, J.-D. Kim, W.-Y. Lee, and C.-H. Lee, "A 6–18-GHz GaAs multifunction chip with 8-bit true time delay and 7-bit amplitude control," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 5, pp. 2220–2230, May 2018, doi: 10.1109/TMTT.2017.2786698.
[21] B. Berthelot, J.-G. Tartarin, C. Viallon, R. Leblanc, H. Maher, and F. Boone, "GaN MMIC differential multi-function chip for Ka-band applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, Jun. 2019, pp. 1399–1402, doi: 10.1109/MWSYM.2019.8701085.
[22] Analog Devices. *ADH939S Aerospace 0.1 GHz to 40 GHz, GaAs, MMIC, 5-Bit 1.0 dB LSB, Digital Attenuator*. Accessed: Apr. 15, 2020. [Online]. Available: https://www.analog.com/en/products/adh939s.html
[23] Analog Devices. *HMC939A-Die 1.0 dB LSB GaAs MMIC 5-Bit Digital Attenuator, 0.1–40 GHz*. Accessed: Jan. 22, 2016. [Online]. Available: https://www.analog.com/en/products/hmc939a-die.html

SEONHYE JANG (Student Member, IEEE) received the B.S. and M.S. degrees in electronic engineering from Soongsil University, Seoul, South Korea, in 2021 and 2023, respectively.

His current research interests include wireless power transfer and millimeter wave integrated circuits.

JUNHYUK YANG (Student Member, IEEE) received the B.S. and M.S. degrees in electronic engineering from Soongsil University, Seoul, South Korea, in 2019 and 2021, respectively.

His current research interests include wireless power transfer and millimeter wave integrated circuits.

JAEYONG LEE (Student Member, IEEE) received the B.S. and M.S. degrees in electronic engineering from Soongsil University, Seoul, South Korea, in 2017 and 2019, respectively, where he is currently pursuing the Ph.D. degree.

His current research interest includes millimeter-wave integrated circuits.

CHANGKUN PARK (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2001, 2003, and 2007, respectively.

From 2007 to 2009, he was with the Advanced Design Team, DRAM Development Division, Hynix Semiconductor Inc., Icheon, South Korea, where he was involved in the development of high-speed I/O interfaces of DRAM. In September 2009, he joined the Faculty of the School of Electronic Engineering, Soongsil University, Seoul, South Korea. His current research interests include RF and millimeter-wave circuits, wireless chip-to-chip communications, and power transfers.