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RESEARCH ARTICLE

A Walsh-Based Arbitrary Waveform Generator for 5G Applications in 28nm FD-SOI CMOS Technology

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ABSTRACT This paper presents the first Arbitrary Waveform Generator (AWG) based on Walsh's theory for wideband radio frequency (RF) conversion. The architecture is dedicated to 5G-FR1 applications (sub-6GHz) to perform a direct and large bandwidth conversion while achieving the highest energy efficiency. The circuit generates Walsh sequences weighted by Walsh coefficients thanks to dedicated Digital-to-Analog Converters (DACs). It embeds an internal memory to feed the data to be converted for measurement purposes. The sum of the weighted Walsh sequences carries out RF signals made of intrinsically synchronous aggregated channels over a frequency range between 600 MHz and 4 GHz. A high-level simulation study is performed as well as transistor-level simulation including post-layout and Monte-Carlo analysis. The circuit is designed in 28nm FD-SOI CMOS technology from STMicroelectronics. The power consumption is 44 mW depicting an energy per bit of 0.34 pJ/bit, the lowest of the state of the art to the authors' knowledge.

INDEX TERMS 5G, broadband, carrier aggregation, Hadamard, sub-6GHz, Walsh transform, wideband, RF DAC, frequency interleaving.

I. INTRODUCTION

The 5G sub-6GHz standard (5G-FR1) uses spectrum resources in a wide band between 600 MHz and 5 GHz. It aggregates carriers using high-order modulations such as 64-QAM. Current radio frequency (RF) architectures cannot achieve highly efficient direct conversion of several aggregated carriers over such a wide spectrum. They are limited by their RF Front End (RFFE) which can only operate at specific frequencies, reducing the carrier component bandwidth to hundreds of MHz [1]. Also, wideband converters generally use dedicated filters for each RF band, as well as programmable Phase Locked Loops (PLL) which generate a variable Local Oscillator (LO) for RF mixers, increasing the complexity, the die area, and the power consumption while reducing the spectral purity [2]. Digital-to-Analog Conversion (DAC) architectures need to be reviewed to generate direct RF signals throughout the 5G-FR1 band.

The literature displays two main architectures to challenge this technical bottleneck:

- Time interleaving (TI) introduced in [3], [4], and [5] is a technique used in converters to increase the data rate, where DACs are used in parallel, each one of them having an allocated time slot, and multiplexers merging each DAC value. This technique allows high data rate conversion, but is greatly sensitive to mismatches between converters and has poor energy efficiency.
- Frequency Interleaving (FI) is a similar technique that allocates a frequency slot to each DAC reducing the bandwidth that needs to be processed per DAC, improving overall spectral purity. FI allows the generation of wideband signals, enabling carrier aggregation in

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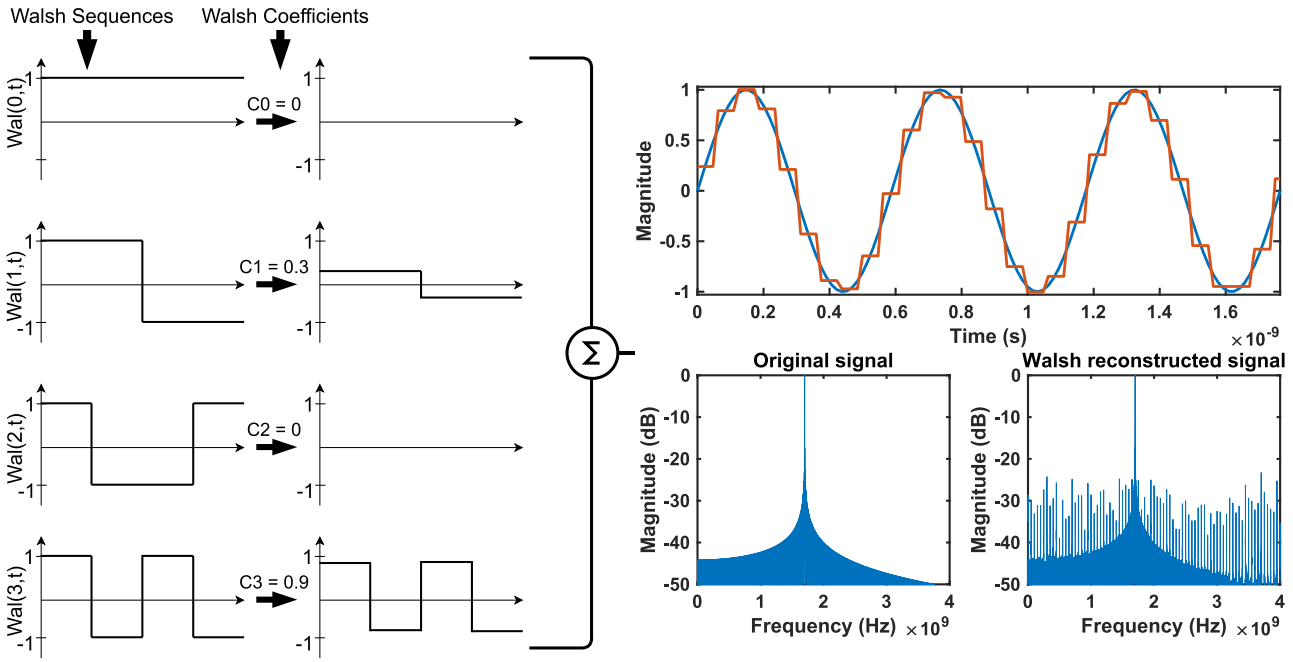

FIGURE 1. Walsh conversion principle - A sum of weighted Walsh sequences by Walsh coefficient carries out a sinewave.

all 5G-FR1 bands simultaneously. Most FI architectures use narrow bandpass filters to split the signal spectrum [6].

Fig. 2 depicts a survey of architectures operating in the 5G-FR1 frequency bands, targeting sub-pJ/bit energy efficiency and multi-carrier generation. This study benchmarks their energy efficiency, but extends its scope to large-bandwidth operations. Reference [7] describes a 6-bit 20 GS/s two-channel time-interleaved current-steering DAC with optimized transition timings and analysis of leakage current effects. Reference [5] presents a four-channel time-interleaved high-speed current-steering DAC with a proposed two-stage analog multiplexer. Reference [8] introduces a multimode delta-sigma RF digital-to-analog converter (RF-DAC) with on-chip second-order DSM and analog interleaving. Reference [9] presents a 12-bit 2.9 GS/s current-steering DAC with triple cascading to address nonlinearities and achieve improved performance. Reference [3] features a 13-bit current-steering DAC-based transmitter prototype with a focus on low noise and distortion. Reference [10] presents an RF DAC with a modified switch output structure and current source calibration scheme. Finally, [11] focuses on wideband RF-sampling D/A converters for multi-band software-defined-radio applications. It should be mentioned that while [5] achieved similar performance, it exhibited a low output power of −22 dBm, which is below average for this particular application. State-of-the-art RF-DACs typically generate an output power greater than -10 dBm.

This paper proposes a direct converter for the 5G-FR1 frequency bands using the sequential domain. It counteracts the complexity of RFFE by avoiding any analog apparatus

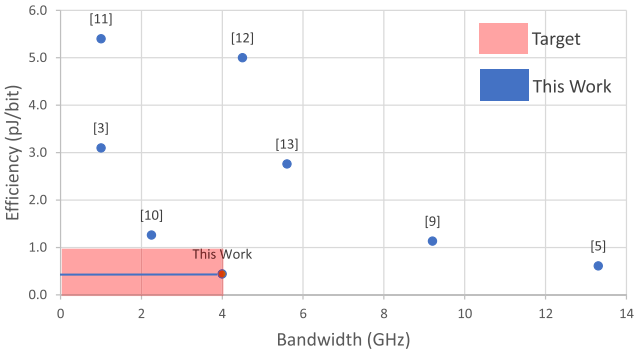

FIGURE 2. Efficiency vs Bandwidth RF-DAC survey.

such as filters or mixers to perform carrier aggregation over wide bands. The Walsh Transform (WT) performs conversion from the time domain to the sequential domain. It uses square sequences to build any signal rather than continuous waves (CW), which makes it the most suitable for monolithic integration. Also, it has properties similar to the Fourier Transform (FT). Thus, the sequential domain gathers the benefits from the time domain with a low-complex architecture and from the frequency domain with a reduced number of operations. The design of an Arbitrary Waveform Generator (AWG) in 28 nm FDSOI CMOS technology from STMicroelectronic is presented. It brings into play the WT as initiated in [12] with high-level Matlab and partial schematic-level simulations with single tone limitation, and as demonstrated in [13] at 8.33 MHz with COTs implementation and limited frequencies. This paper presents the first fully Post-Layout Simulated (PLS) Walsh-based

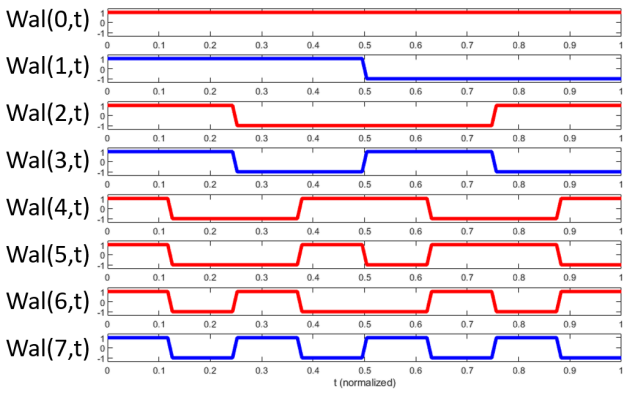

FIGURE 3. First 8 Walsh sequences.

AWG at RF frequencies. It is organized as follows: the WT is explained in full in Section II. Then, the Walsh-based RF AWG is described in Section III. The simulation results are presented in Section IV. Finally, Section V concludes the paper and provides a comparison with the state-of-the-art.

II. THE WALSH TRANSFORM

The WT is a sequential transform with properties similar to the FT. It uses a basis of orthogonal square waves called Walsh sequences to generate arbitrary signals as depicted in Fig. 1. They are weighted by Walsh coefficients and summed to directly generate the RF signal. Eq. 1 shows the WT [14] with $x(t)$ the original signal, $Wal(n,t)$ the n^{th} Walsh sequence, C_n the n^{th} Walsh coefficient, M the number of Walsh coefficients and T the Walsh period.

$$x(t) = c_0 Wal(0,t) + \sum_{n=1}^{M} c_n Wal(n,t)$$
$$c_n = \frac{1}{T}\int_{t=0}^{T} x(t) Wal(n,t) dt \quad (1)$$

The Walsh sequences are described as follows:

$$Wal(n,t) = \Pi_i Rad(i,t)^{g_i}$$
$$Rad(i,t) = sgn(sin(2^i \pi t)) \quad (2)$$

where $Rad(i,t)$ is the Rademacher function. g_i is the gray coding of the Walsh sequence. Fig. 3 exhibits the first 8 Walsh sequences.

The Walsh coefficients are processed by the Walsh matrix $H_w(n)$ and the original signal as described in Eq. 3. The Walsh matrix is built by permutation of the rows of the Hadamard matrix $H_h(k)$ according to the number of sign changes per row [15].

$$C_x(n) = \frac{1}{N} H_w(n) X(n)$$
$$H_h(k) = \begin{bmatrix} H_h(k-1) & H_h(k-1) \\ H_h(k-1) & -H_h(k-1) \end{bmatrix} \quad (3)$$

Main WT parameters are defined as follows:

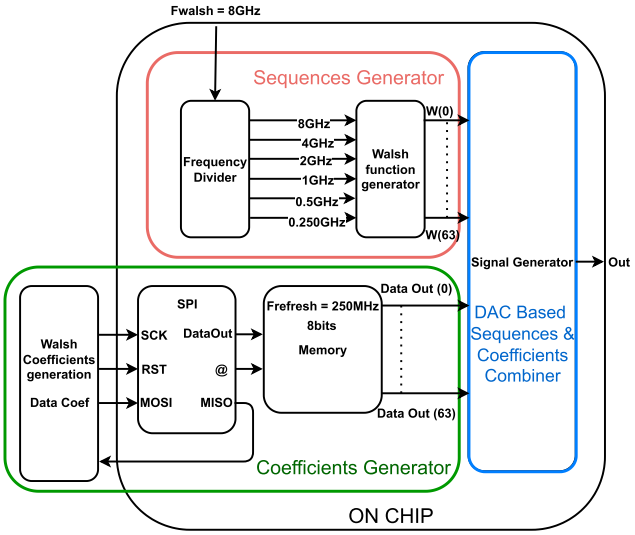

FIGURE 4. Architecture of the Walsh-based AWG.

- F_{Walsh} corresponds to the maximal Walsh sequence frequency. It determines the maximum frequency of the reconstructed signal $F_{max} = \frac{F_{walsh}}{2}$.
- The Walsh order $walsh\_order$ defines the number of Walsh sequences and coefficients M per period of refreshment of the Walsh coefficients $M = 2^{walsh\_order}$.
- $F_{refresh} = \frac{F_{Walsh}}{2^{walsh\_order-1}}$ represents the frequency of Walsh coefficients refreshment.

F_{Walsh} = 8 GHz is chosen to cover the 0 − 4 GHz band as a demonstration and for ease of understanding as 8 GHz is a multiple of a power of 2. A $walsh\_order$ of 6 leads to $F_{refresh}$ = 250 MHz. A high $walsh\_order$ reduces $F_{refresh}$ but increases the number of sequences. $F_{refresh}$ is optimum to refresh Walsh coefficients by DAC while maintaining a limited number of sequences, here 64.

The architecture of a Proof-of-Concept (PoC) circuit is presented in Fig. 4. It is composed of:

- a Walsh sequences generator with a frequency divider and a Walsh function generator,
- a Walsh coefficients generator with a Serial Peripheral Interface (SPI) to interface Walsh coefficients processed from an external device with embedded memory,
- a DAC-based sequences and coefficients combiner to carry out the RF signal.

III. WALSH-BASED ARBITRARY WAVEFORM GENERATOR

A. WALSH SEQUENCES GENERATOR

There are 2 kinds of Walsh sequences:

- The primary sequences are square signals with a duty cycle of 50%. They are generated by the division of F_{Walsh}. D flip-flops are wired as frequency dividers. The architecture detailed in Fig. 5 uses 6 primary sequences with frequencies between 250 MHz and 8 GHz (W(1,t), W(3,t), W(7,t), W(15,t), W(31,t), W(63,t)).

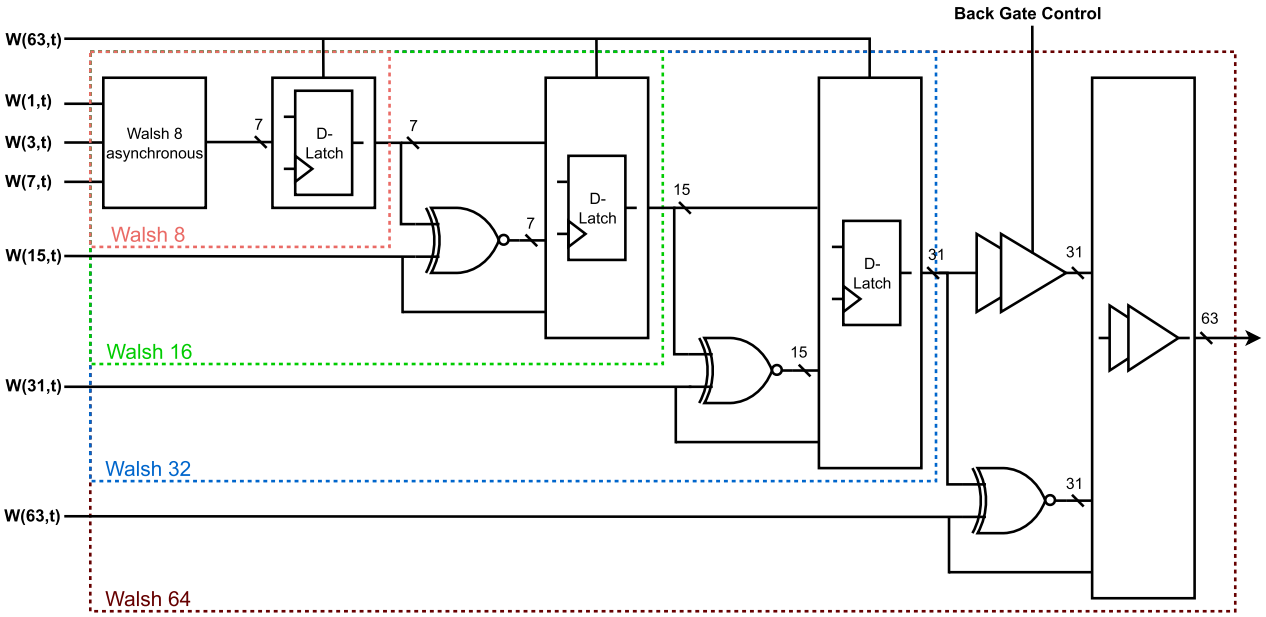

FIGURE 5. Walsh sequences generator architecture.

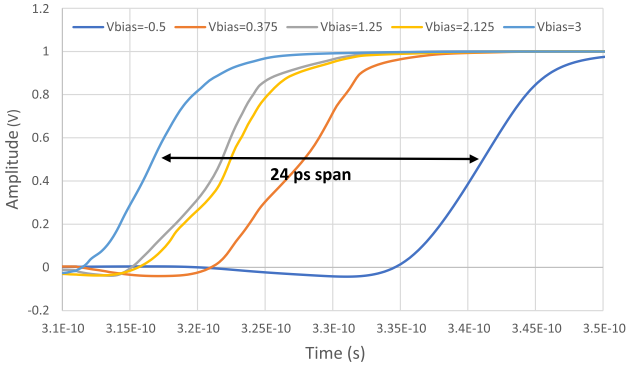

FIGURE 6. Buffer delay variation with different back-gate voltage control.

- The secondary sequences are generated by combining the primary and secondary sequences of the previous Walsh orders with logic gates. D flip-flops synchronize all the sequences from one to another. The last stage of synchronization of the sequences uses buffers because the last 32 sequences are too close in frequency to the clock signal to be synchronized with D flip-flops. The synchronization buffers are sized to compensate for the delay between the first 32 sequences and the last 32 sequences. Moreover, the back-gates of the transistors of buffers are used to adjust delays to compensate for the process variations (PVT) as shown in Fig. 6.

The layout is designed to ensure balanced propagation times between each stage by keeping similar connection distances between blocs.

B. WALSH COEFFICIENTS GENERATOR

The Walsh coefficients are quantified on 8 bits including one signed bit and are refreshed at $F_{refresh} = 250$ MHz. The Walsh coefficients are calculated with MatLab and stored in an embedded memory accessible with an SPI. The memory has a size of 1.28 Mbits to be able to generate modulated signals with respect to the 5G-FR1 standard with a duration of 10 ms.

C. DAC-BASED SEQUENCES AND COEFFICIENTS COMBINER

The weighting of the 64 sequences is performed by modified DACs based on current-summed differential pairs. The DAC output value is controlled by the commutation of its current sources and not by the differential pair transistor. The modified DACs detailed in Fig. 7 have a dynamic range of 7 bits. The 8^{th} bit monitors the sequence inversion for signing. The weighting of the differential pairs is hybrid: the 3 Least Significant Bits (LSB) use a binary coding, and the 4 Most Significant Bits (MSB) use a thermometer coding. This trade-off allows ensuring a good accuracy of the DAC while having a reduced footprint, as detailed in [16]. The circuit is composed of 64 DACs, composed of 127 current unit pairs. The unit current of each pair was chosen to ensure measurable output power while limiting the total power consumption of the circuit. The current of a current unit pair is $I_0 = 10\ \mu$A, giving a maximum total output current of 81.28 mA.

The current unit pair is detailed in Fig. 8. The M_{cs} transistors form a current mirror that copies the unitary current I_0. The M_{sw} transistors form the differential pair which are commuted by the Walsh sequences. They are

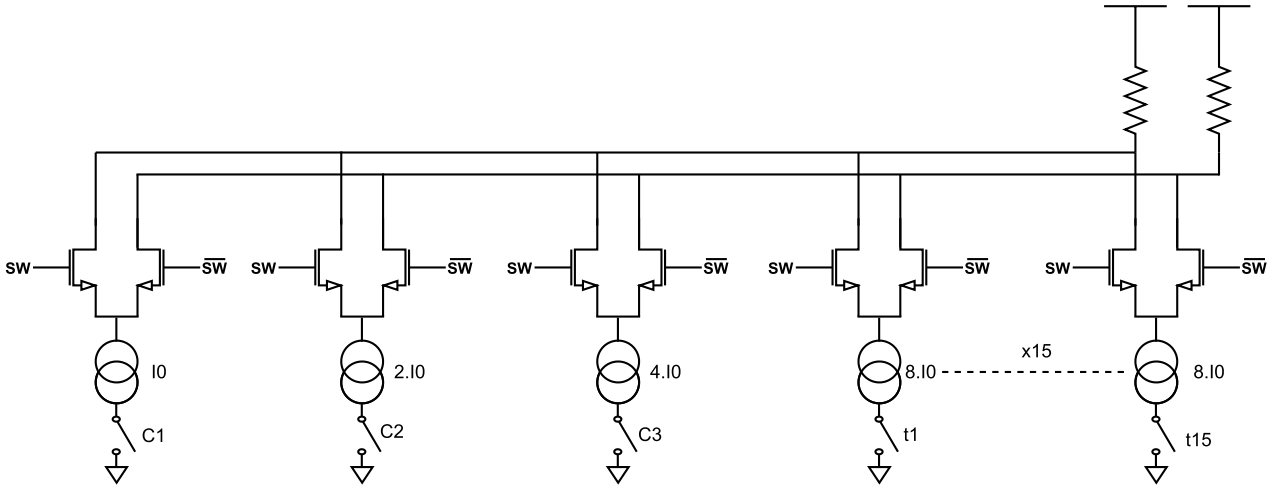

FIGURE 7. 7-bit DAC.

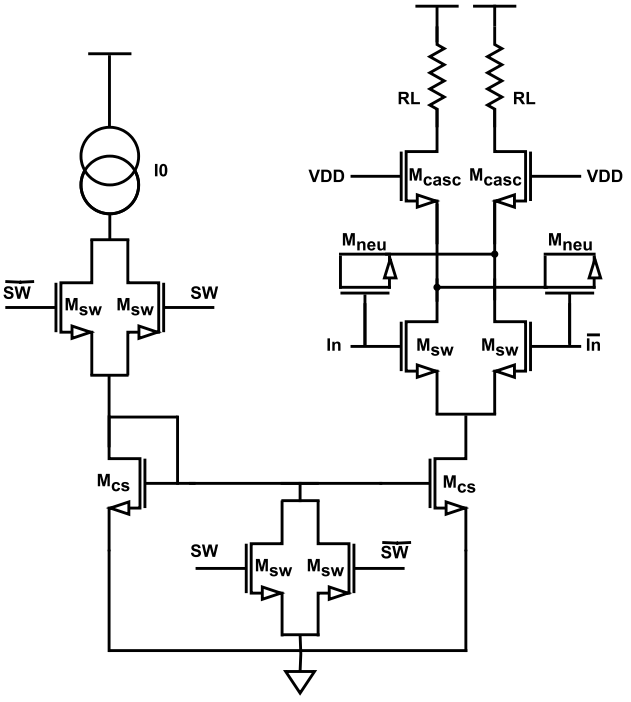

FIGURE 8. DAC current unit pair.

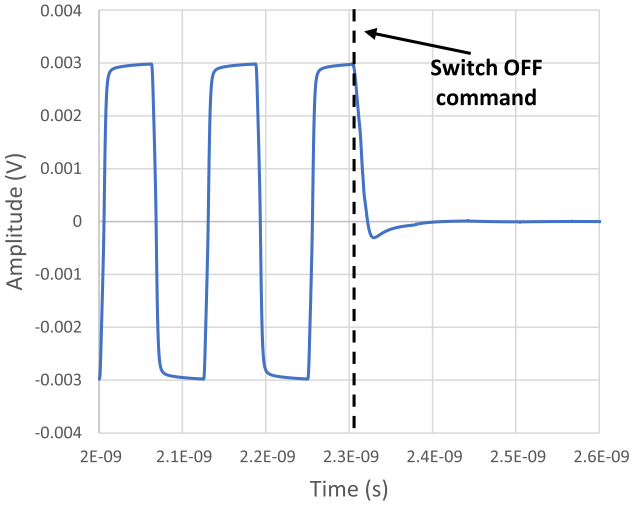

FIGURE 9. Unary current source switch off transition.

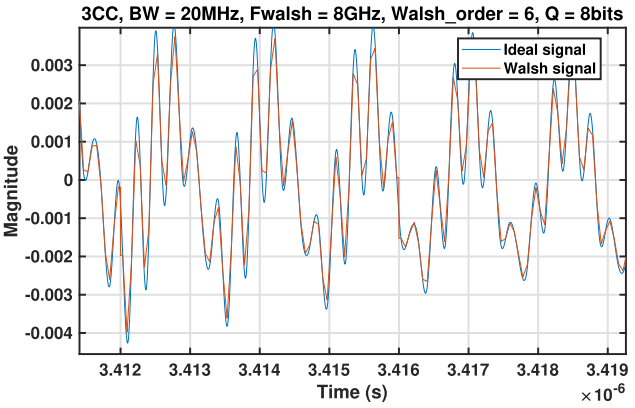

FIGURE 10. Time domain multi-carrier 64-QAM signal (MatLab).

cascaded by two NMOS M_{casc} transistors to reduce the charge injection phenomenon. The M_{neu} transistors act as neutralizing capacitors. Their role is to reduce the charge injection brought by the C_{gd} capacitors of the M_{sw} transistors. Finally, the M_s transistors are driven by the coefficients through the SW differential input to turn off the pair. The M_{s2} transistors short-circuit the current mirror transistor, allowing a fast switching of the pair. The M_{s1} transistors open the circuit so that the current mirror does not consume power when it is turned off. Enhancing this design is to preserve the square characteristics of the Walsh sequences by reducing the commutation delay. Additionally, it is crucial to ensure that each current pair exhibits minimal current glitches and leakage current, due to their massive parallelization

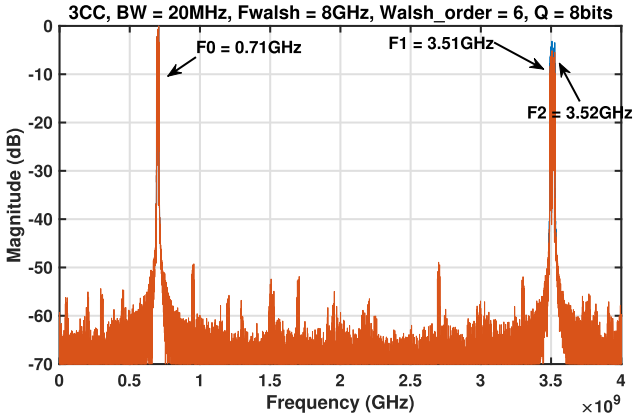

FIGURE 11. Frequency domain multi-carrier 64-QAM signal (MatLab).

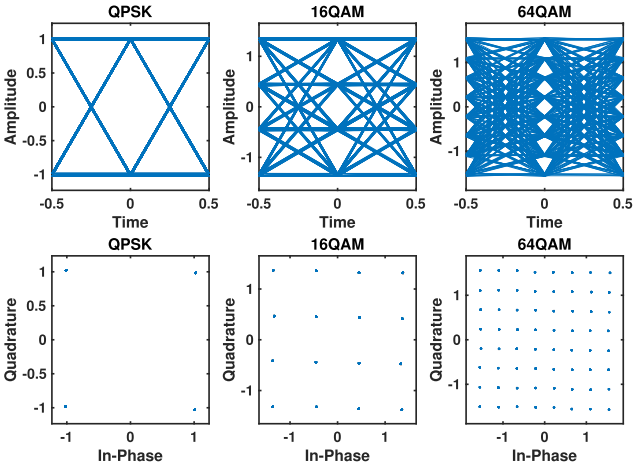

FIGURE 12. Eye diagram and EVM constellation of QPSK, 16-QAM, 64-QAM aggregated carriers (MatLab).

(64 DACs). Any glitches or leaks would accumulate and result in significant errors, jeopardizing the integrity and accuracy of the overall system. In Fig. 9, a square signal at 8 GHz is depicted passing through a unary current pair, along with the corresponding switch-off signal for that pair. The commutation time for this operation is measured at 250 ps, accounting for approximately 6.5% of the coefficient period.

IV. SIMULATION RESULTS

A. MATLAB SIMULATIONS

High-level simulations are performed in MatLab to validate the architecture with a test scenario composed of 3 aggregated 64-QAM modulated carriers, each having a bandwidth of 20 MHz. Those carriers follow the 5G-FR1 test model E-TM3.1 from [17].

Fig. 10 and 11 shows a carrier at 700 MHz and two neighbor carriers at 3.51 GHz and 3.53 GHz. We evaluate a Spurious Free Dynamic Range (SFDR) of 45.85 dBc, an Adjacent Channel Leakage Ratio (ACLR) of 51.04 dBc, and an Error Vector Magnitude (EVM) of 2.06% which results in a high-quality eye diagram exhibited in Fig. 12.

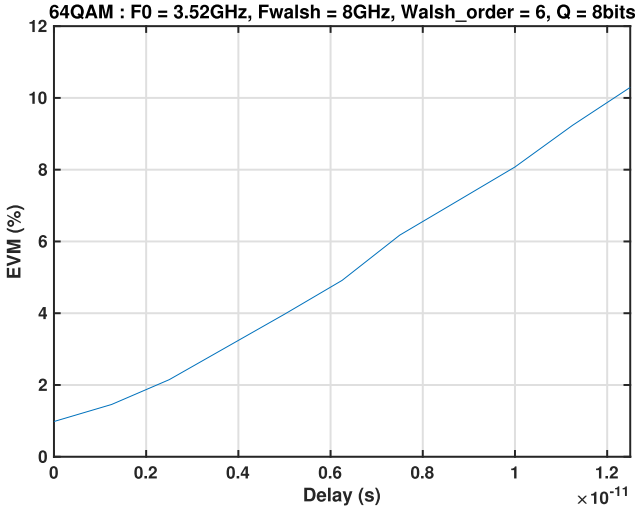

FIGURE 13. Impact on the EVM of the delay between the first 32 sequences and the last 32 sequences (MatLab).

The impact of the delay between the first 32 sequences and the last 32 sequences is simulated in Fig. 13 to size the synchronization buffer detailed in Fig. 5. The 5G-FR1 EVM standard (EVM $<$ 9% for 64-QAM) is met as long as the delay between the first 32 sequences and the last 32 sequences is lower than 12 ps. Monte Carlo simulations have demonstrated that Process, Voltage, and Temperature (PVT) variations can shift the buffers by up to 4 ps. This is mitigated with back-gate voltage tuning thanks to the FD-SOI technology. The back-gate control can compensate for PVT delay shift up to 7 ps.

The jitter effect on the Walsh sequences is shown in Fig. 14, simulated by a normal distribution with a mean value of 0 and a standard deviation as a percentage of the maximum frequency (8 GHz). The 5G-FR1 EVM standard is met if the jitter standard deviation is lower than 10 ps (8% of F_{walsh}). Each stage is synchronized with D-latches to reduce sequence mismatches.

B. POST LAYOUT SIMULATION

To evaluate the performance of the circuit depicted in Fig. 15, three Post Layout Simulations (PLS) were conducted:

- Fig. 16 with a single continuous wave signal at 4 GHz. It depicts a Spurious-Free Dynamic Range (SFDR) of 15.01 dBc, an output power of −4.40 dBm, and a power consumption of 39.95 mW.
- Fig. 17 with a two-tone continuous wave spaced of 100 MHz to investigate the effect of intermodulations. It depicts an SFDR of 13.35 dBc, an output power of −7.11 dBm, and a power consumption of 40.68 mW.
- Fig. 18 with three continuous wave signals at frequencies of 0.7 GHz, 2.4 GHz, and 4 GHz, demonstrating the wideband capabilities of the architecture. It depicts an SFDR of 15.14 dBc, an output power of −6.20 dBm, and a power consumption of 44 mW.

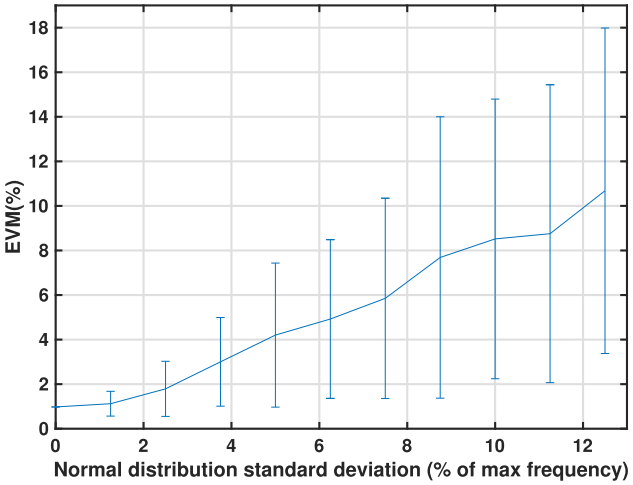

FIGURE 14. Impact on the EVM of the clock jitter (MatLab).

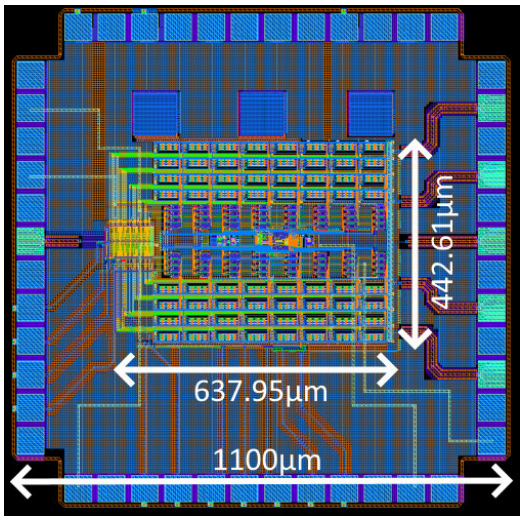

FIGURE 15. Chip Layout.

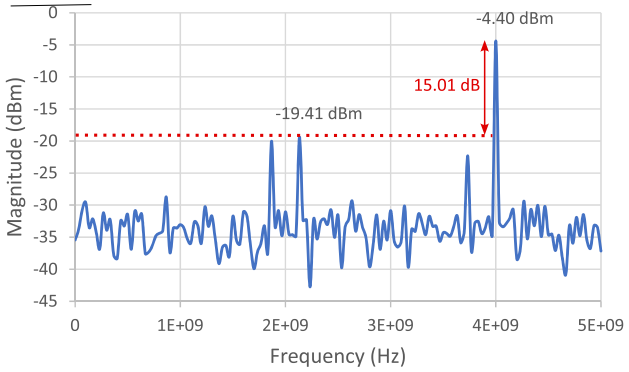

FIGURE 16. Spectrum PLS of single tone signal.

Furthermore, IM3 simulations were also carried as shown in Fig. 19 to evaluate the performance of the circuit with interfering signals. The test signals used for IM3 simulation were 2-ton continuous waves with 100 MHz frequency spacing. The worst simulated IM3 is −16.06 dBc at 2.5 GHz.

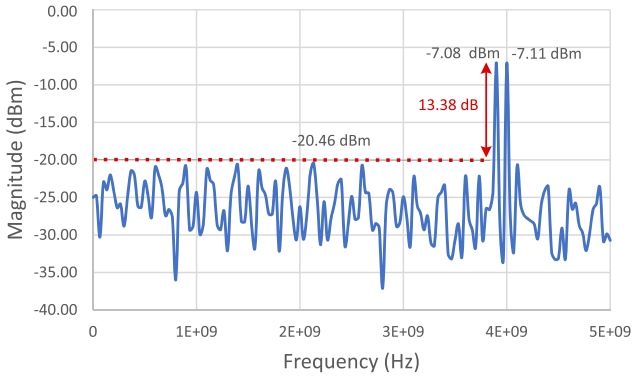

FIGURE 17. Spectrum PLS of a two-tone signal.

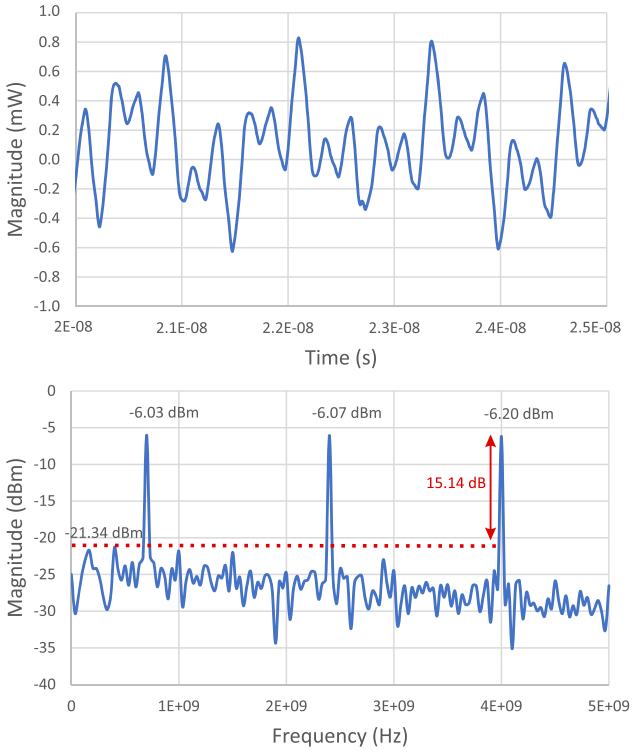

FIGURE 18. Time domain and spectrum PLS of 3 CW (0.7 GHz, 2.4 GHz, 4 GHz).

C. CALIBRATION AND STATIC ERROR CORRECTION

The circuit is prone to static errors caused by design imperfections, PVT variations, and packaging. Static design errors primarily result from buffer mismatch due to layout issues, while package-related errors primarily stem from wire bonding-induced inductance. Both of these errors lead to nonlinearity across the bandwidth. Static errors were reduced by calibrating the architecture. A test signal consisting of continuous waves spaced 100 MHz apart across the entire bandwidth was used to map amplitude non-linearities. A correction function was then applied to the coefficients. This calibration improved the circuit performance and amplitude linearity. Fig. 20 shows results illustrating an improvement in amplitude linearity, with a decrease in the drop from

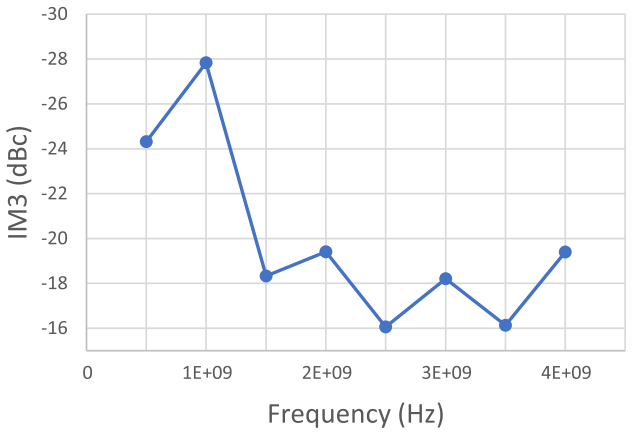

FIGURE 19. IM3 vs Frequency.

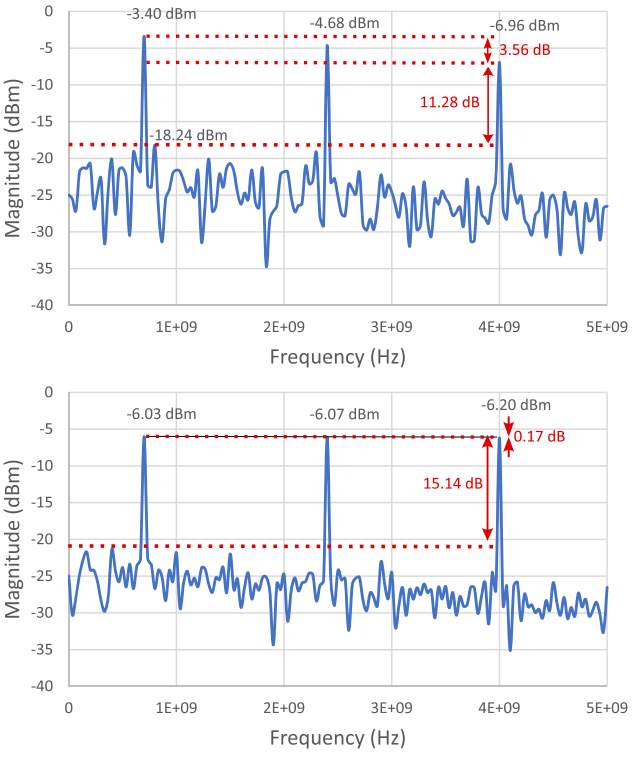

FIGURE 20. Before and after coefficients calibration.

3.56 dB to 0.17 dB across the entire bandwidth. It showcases a reduction of 3.39 dB in nonlinearity. The calibration process effectively addressed the initial discrepancies, resulting in a better linear response. It validates the successful mitigation of static errors and highlights the improved performance achieved through the corrective measures implemented.

D. STATE OF THE ART

Tab. 1 displays a comparison with the state-of-the-art. The instantaneous bandwidth was chosen rather than the maximum operating frequency to evaluate the circuit bandwidth. It refers to the ability of the circuit to handle the entire bandwidth simultaneously. Most architectures can only address a maximum frequency and lack the ability to generate signals with a bandwidth equal to their maximum frequency. Most papers do not provide instantaneous bandwidth and RF DACs are limited to hundreds of MHz [1]. The circuit carries out a bandwidth equal to the maximum operating frequency of the circuit and thus, contributes significantly to the overall effectiveness and relevance of the architecture for 5G-FR1 applications. The circuit occupies a pad-limited surface of 1.25 mm^2 and an active area of 0.282 mm^2. The conversion efficiency of the circuit is 0.34 pJ/bit, which is the lowest reported value to the authors' knowledge while having one of the highest output power.

TABLE 1. State of the Art of RF DACs.

Paper	[3]	[4]	[5]	[11]	[18]	[19]	This Work
Cmos node (nm)	28	65	40	16	16	130	**28**
Maximum operating frequency (GHz)	4.4	4.1	13.34	5.2	3.9	20	**4**
Instantaneous bandwidth (GHz)	-	0.875	-	-	-	-	**4**
Consumption (mW)	360	380	103	530	350	1910	**44**
Output power @max freq (dBm)	≈ 0	-8	≈ -22	-15.66	-	-18	**-4.4**
Quantization bits	13	16	16	12	16	10	**8**
Sample Rate (GS/s)	9	1.75	28	16	6	3.35	**16**
IM3 (dBc)	-45	-62	-35.6	-72	-80	-46	**-16.06**
Efficiency (pJ/bit)	3.10	13.5	0.61	2.71	3.65	57.01	**0.34**

V. CONCLUSION

The first AWG using the Walsh Transform has been designed in 28nm FD-SOI technology to generate 5G-FR1 signals. The architecture was validated by high-level and PLS simulations demonstrating the ability of the WT to perform direct RF conversion and carrier aggregation over a wide bandwidth. The simulation results highlight critical aspects mitigated by the design and the technology features and show preliminary performances with a bandwidth of 4 GHz, a power consumption of 44 mW, and a conversion efficiency of 0.34 pJ/bit, the best of the state of the art to the authors' knowledge.

REFERENCES

[1] B. Jann, G. Chance, A. G. Roy, A. Balakrishnan, N. Karandikar, T. Brown, X. Li, B. Davis, J. L. Ceballos, N. Tanzi, K. Hausmann, H. Yoon, Y.-L. Huang, A. Freiman, B. Geren, P. Pawliuk, and W. Ballantyne, "A 5G sub-6 GHz zero-IF and mm-wave IF transceiver with MIMO and carrier aggregation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 352–354.

[2] D. J. McLaurin, K. G. Gard, R. P. Schubert, M. J. Manglani, H. Zhu, D. Alldred, Z. Li, S. R. Bal, J. Fan, O. E. Gysel, C. M. Mayer, and T. Montalvo, "A highly reconfigurable 65 nm CMOS RF-to-bits transceiver for full-band multicarrier TDD/FDD 2G/3G/4G/5G macro basestations," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 162–164.

[3] J. Xiao, B. Chen, T. Y. Kim, N.-Y. Wang, X. Chen, T.-H. Chih, K. Raviprakash, H.-F. Chen, R. Gomez, and J. Y. C. Chang, "A 13-bit 9 GS/s RF DAC-based broadband transmitter in 28 nm CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. C262–C263.

[4] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "A 5.3 GHz 16b 1.75 GS/S wideband RF mixing-DAC achieving IM<−82 dBc up to 1.9 GHz," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[5] W.-C. Kim, D.-S. Jo, Y.-J. Roh, Y.-D. Kim, and S.-T. Ryu, "A 6b 28 GS/s four-channel time-interleaved current-steering DAC with background clock phase calibration," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. C138–C139.
[6] G. Ding, C. Dehollain, M. Declercq, and K. Azadet, "Frequency-interleaving technique for high-speed A/D conversion," in *Proc. Int. Symp. Circuits Syst. (ISCAS)*, vol. 1, 2003, p. 1.
[7] S.-N. Kim, W.-C. Kim, M.-J. Seo, and S.-T. Ryu, "A 65-nm CMOS 6-bit 20 GS/s time-interleaved DAC with full-binary sub-DACs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 9, pp. 1154–1158, Sep. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8303762/
[8] J. J. McCue, B. Dupaix, L. Duncan, V. J. Patel, T. Quach, and W. Khalil, "A time-interleaved multi-mode $\Delta\Sigma$ RF-DAC for direct digital-to-RF synthesis," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Phoenix, AZ, USA, May 2015, pp. 103–106. [Online]. Available: http://ieeexplore.ieee.org/document/7337715/
[9] C.-H. Lin, F. van der Goes, J. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, "A 12b 2.9 GS/s DAC with IM3 $\ll -60$ dBc beyond 1GHz in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 74–75.
[10] G. Engel, M. Clara, H. Zhu, and P. Wilkins, "A 16-bit 10 Gsps current steering RF DAC in 65 nm CMOS achieving 65 dBc ACLR multi-carrier performance at 4.5 GHz fout," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Kyoto, Japan, Jun. 2015, pp. C166–C167. [Online]. Available: http://ieeexplore.ieee.org/document/7231252/
[11] D. Gruber, M. Clara, R. Sanchez, Y.-S. Wang, C. Duller, G. Rauter, P. Torta, and K. Azadet, "A 12b 16 GS/s RF-sampling capacitive DAC for multi-band soft-radio base-station applications with on-chip transmission-line matching network in 16 nm FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 174–176.
[12] N. Bouassida, F. Rivet, Y. Deval, D. Duperray, and A. Cathelin, "A concurrent transmitter in CMOS 28 nm FDSOI technology based on Walsh sequences generator," in *Proc. 14th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2016, pp. 1–4.
[13] R. Quéheille, F. Rivet, N. Deltimple, Y. Deval, and E. Kerhervé, "Demonstration of a Walsh-based arbitrary waveform generator using components off-the-shelf," in *Proc. 28th IEEE Int. Conf. Electron., Circuits, Syst. (ICECS)*, Nov. 2021, pp. 1–4.
[14] J. L. Walsh, "A closed set of normal orthogonal functions," *Amer. J. Math.*, vol. 45, no. 1, p. 5, Jan. 1923.
[15] J. Johnson and M. Puschel, "In search of the optimal Walsh–Hadamard transform," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process.*, vol. 6, Jun. 2000, pp. 3347–3350.
[16] B. Razavi, "The current-steering DAC [a circuit for all seasons]," *IEEE Solid-State Circuits Mag.*, vol. 10, no. 1, pp. 11–15, Winter 2018.
[17] *LTE, Evolved Universal Terrestrial Radio Access (E-UTRA), Base Station (BS) Conformance Testing*, document 3GPP TS 36.141, Version 14.3.0, Apr. 2017. [Online]. Available: https://www.etsi.org/deliver/etsi_ts/136100_136199/136141/14.03.00_60/ts_136141v140300p.pdf
[18] C.-H. Lin, K. L. J. Wong, T.-Y. Kim, G. R. Xie, D. Major, G. Unruh, S. R. Dommaraju, H. Eberhart, and A. Venes, "A 16b 6GS/S Nyquist DAC with IMD < -90 dBc up to 1.9 GHz in 16 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 360–362.
[19] L. Duncan, B. Dupaix, J. J. McCue, B. Mathieu, M. LaRue, V. J. Patel, M. Teshome, M.-J. Choe, and W. Khalil, "A 10-bit DC-20-GHz multiple-return-to-zero DAC with >48-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3262–3275, Dec. 2017.

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