IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 26 September 2023, accepted 17 October 2023, date of publication 19 October 2023, date of current version 26 October 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3325938

RESEARCH ARTICLE

Analysis of Quarter Method Applied ROM-Based DDFS Architecture

JAE-YUN PARK, SU-HYEON KIM, HYUNYOUNG YOO, AND JAE-WON NAM, (Member, IEEE)
Department of Electronic Engineering, Seoul National University of Science and Technology, Seoul 01811, Republic of Korea

Corresponding author: Jae-Won Nam (jaewon.nam@seoultech.ac.kr)

This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education under Grant 2022R1A4A3029433; and in part by the Ministry of Science and Information Communication Technology (MSIT), South Korea, under the Information Technology Research Center (ITRC) Support Program supervised by the Institute for Information and Communications Technology Planning and Evaluation (IITP) under Grant IITP-2023-RS-2022-00156295.

ABSTRACT This paper compares various performance metrics of the conventional direct digital frequency synthesis (DDFS) with DDFS introducing the quarter method, which is most commonly used among ROM-based DDFS. The evaluation is implemented at the register-transfer level (RTL) in the low-power and general-purpose 65 nm CMOS technologies, and 180 nm CMOS technology. We have observed that phase-to-amplitude converter (PAC) becomes a key building block that mainly determines the performance of DDFS. At a 12-bit resolution, the PAC of the conventional DDFS occupies about 97% of the total cell area and accounts for approximately 83% of the total power consumption. On the other hand, the PAC of DDFS with the quarter method applied occupies about 80% of the total cell area and uses about 45% of the total power consumption. In addition, because the quarter method requires additional decoding logic to map the phase to the corresponding amplitude, this method has area and power consumption disadvantages at relatively small resolution targets below 10-bit. However, at relatively high-resolution targets beyond 11-bit, the quarter method has significant benefits in terms of various performance metrics (e.g., area, power consumption, and speed). Then, the quarter method has advantages at resolutions exceeding 7 bits based on figure of merit (FoM). Based on FoM, a similar pattern is evaluated despite changing the CMOS technology. As a result, the quarter method is the crucial structure in DDFS architecture. The designed DDFS is verified in implementation results using a field programmable gate array (FPGA) in 65 nm CMOS technology.

INDEX TERMS Direct digital frequency synthesis, ROM-based direct digital frequency synthesis, quarter method, benchmark.

I. INTRODUCTION

The scaling down of technology significantly contributes to reducing both power consumption and silicon area requirements. Specifically, digital integrated circuits enhance the operating speed, thus triggering more research opportunities in the field of high-performance processor systems (e.g., hardware accelerators, in-memory computing, and edge computing engines). Also, a design strategy that is robust to process, voltage, and temperature (PVT) variations is highly desired, and a methodology that reduces some analog circuits and adopts more digital circuits has become a preferred solution.

Direct digital frequency synthesis (DDFS), which is used as a frequency synthesizer, has an appropriate structure for the scaling-down of technology, as a significant part including the core driving block is in the digital domain. Additionally, DDFS has the advantages of frequency switching and good accuracy, because, unlike a phase-looked loop (PLL) in which the reference frequency is stabilized through a feedback loop, the output frequency is immediately converted, and the accuracy of DDFS is mainly determined by the resolution that is easy to manipulate [1], [2]. Therefore, DDFS is adopted in high-performance applications [3], [4], [5], [6].

The associate editor coordinating the review of this manuscript and approving it for publication was Christian Pilato.

There have been multiple studies of DDFS to highlight the structural benefits. Various approaches have utilized a digital-to-analog converter (DAC) [7], [8], [9], [10], [11], [12], [13] as well as a phase-to-amplitude converter (PAC). Specifically, ROM-based DDFS, which uses ROM as a look-up table (LUT) to store all phase and amplitude data of the sine waveform, has been greatly improved in studies involving the use of PACs. Although ROM-based DDFS has been adopted due to its simple structure, this type of DDFS has a significant limit due to the size of the LUT. Also, a large size of the LUT results in significant power consumption. Therefore, various approaches using mathematical methods (e.g., trigonometric function and polynomial approximation) have been introduced to reduce the size of the LUT [14], [15], [16], [17], [18], [19], [20]. In another case, an angular rotation based method that utilizes the CORDIC (coordinate rotation digital computer) algorithm is introduced to realize a high spurious-free dynamic range (SFDR) [21], [22], [23], [24], [25], [26].

Circuit designs without guidelines are challenging and time-consuming. In particular, circuit designers have difficulty determining the power consumption, area, and speeds. In detail, the heat generated due to high power consumption can trigger unwanted side effects, as one characteristic of a MOSFET is its dependency on the temperature [27]. Active area limits can be another issue. Also, the priorities of the performance metrics can differ depending on the purpose of the system. Accordingly, benchmark is required because this can provide designers the guidelines that quantitatively take into account specifications and constraints.

The main contribution of this brief is to benchmark the performance of DDFS in a wide range by comparing the conventional architecture with an architecture that applies the quarter method, which is commonly used as a ROM-based DDFS architecture. In other words, this research provides benchmarks through a quantitative analysis of the area, power consumption, and speeds. To definitely compare the benefits of DDFS with the quarter method applied, the figure of merit (FoM) is introduced. The performance metrics are evaluated at the register-transfer level (RTL) based on the 65 nm CMOS technology. We also check the physical design level and verify the implementation results using a field programmable gate array (FPGA).

The rest of the paper is organized as follows. The conventional DDFS and DDFS with the quarter method applied are summarized in Section II. Section III analyzes the cell area, power consumption, time constraints, and FoM according to the resolution on the conventional DDFS and DDFS with the quarter method applied, and compares performance metrics between the two described DDFS architectures. Section IV verifies the design and the evaluation of the conventional DDFS and DDFS with the quarter method applied, followed by the conclusion in Section V.

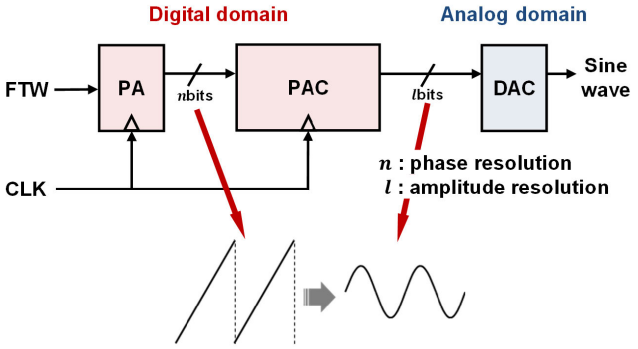

FIGURE 1. Architecture of the conventional DDFS.

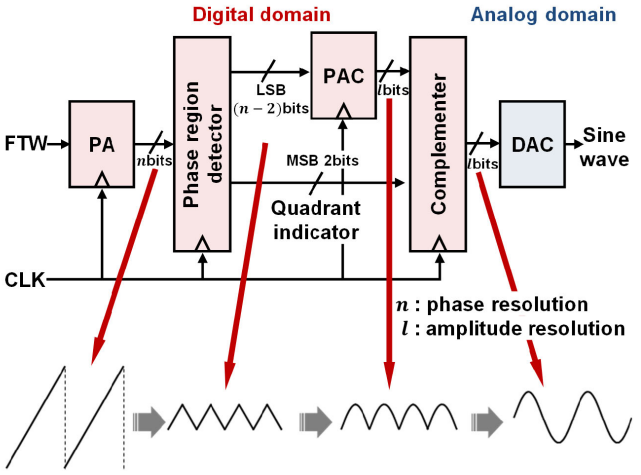

FIGURE 2. Architecture of DDFS with the quarter method applied.

II. DIRECT DIGITAL FREQUENCY SYNTHESIS

A. CONVENTIONAL DDFS

The architecture of DDFS as proposed by Tierney et al. [28] (shown in Fig. 1) consists of a phase accumulator (PA), PAC, and DAC, where n is the phase resolution and l is the amplitude resolution. The conventional DDFS can be divided into two parts: a digital part consisting of PA and PAC, and an analog part consisting of DAC. First, the PA serves to accumulate the phase by means of frequency tuning word (FTW) units and generates the n-bit phase. Next, the PAC is used to translate appropriately the phase to the corresponding amplitude on the sine waveform and to generate the l-bit amplitude. The DAC is employed to change the output of the digital block to an analog sine waveform. The converted sine waveform frequency can be formulated as

$$f_{\mathrm{OUT}} = \frac{\mathrm{FTW} \times f_{\mathrm{CLK}}}{2^n}, \tag{1}$$

where f_{OUT} is the output frequency, and f_{CLK} is clock frequency [29]. The output frequency can be bounded as

$$0 \leq f_{\mathrm{OUT}} \leq \frac{f_{\mathrm{CLK}}}{2}. \tag{2}$$

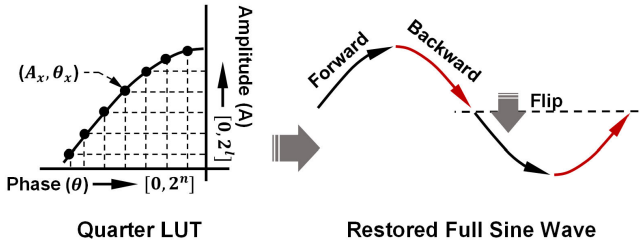

FIGURE 3. Waveform-restoring sequence in the quarter method.

The output frequency is limited by half of the clock frequency due to the discrete-time characteristics of the DDFS [30].

The PAC adopted from the ROM-based DDFS memorizes all relevant phase and amplitude pairs of a full-cycle sine waveform. The number of the phase and amplitude pairs increases when increasing the resolution of the phase and amplitude. Therefore, the PAC strongly depends on the resolutions of the phase and amplitude. The size of the LUT is mathematically determined by the resolutions of phase and amplitude, and the phase and amplitude resolutions regulate the size of the LUT in different manners. In the case of the phase resolution, increase of one bit resolution generates exponential changes on the size of the LUT, specifically doubling per bit. However, increase of one bit amplitude resolution generates linear changes on the size of the LUT. Therefore, especially in terms of the area, the exponential increase of the size due to the phase resolution becomes a large burden. To mitigate the challenge, the quarter method, which is implemented with simple digital decoding logic, is widely applied to the ROM-based DDFS architecture [13], [14], [15], [16], [17], [18].

B. QUARTER METHOD

The quarter method is a quite effective ROM-based DDFS architecture that reduces the LUT size by a quarter, using the characteristics of the sinusoidal waveform (e.g., symmetry and periodicity) [22]. As shown in Fig. 2, DDFS with the quarter method applied consists of PA, PAC, DAC, and the additional logic. The PA and DAC have the same role and structure as the conventional DDFS. Different from the conventional DDFS, the PAC only stores the phase and amplitude pairs corresponding to a quarter cycle of the sine wave. Accordingly, the additional logic is utilized to decode the reduced the LUT.

The waveform-restoring sequence is implemented by flipping the first quadrant of the sine waveform vertically or horizontally, as shown in Fig. 3. In other words, the waveform-restoring sequence is closely related to the reading order of the LUT. The second quadrant is reconstructed by reading backward, the third quadrant is reconstructed by reading forward before flipping the amplitude, and the fourth quadrant is reconstructed by reading backward before flipping the amplitude. The flipping process is performed by

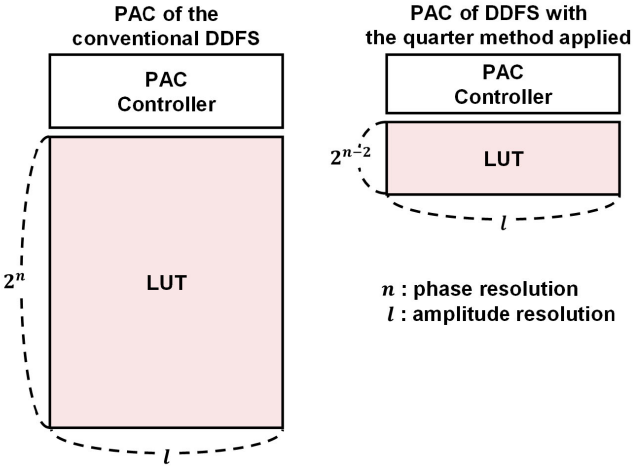

FIGURE 4. Architectures of the PAC on the conventional DDFS and DDFS with the quarter method applied.

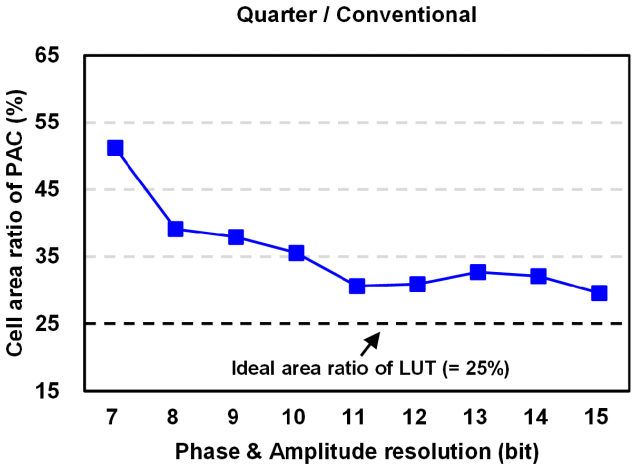

FIGURE 5. Cell area ratio of the PAC.

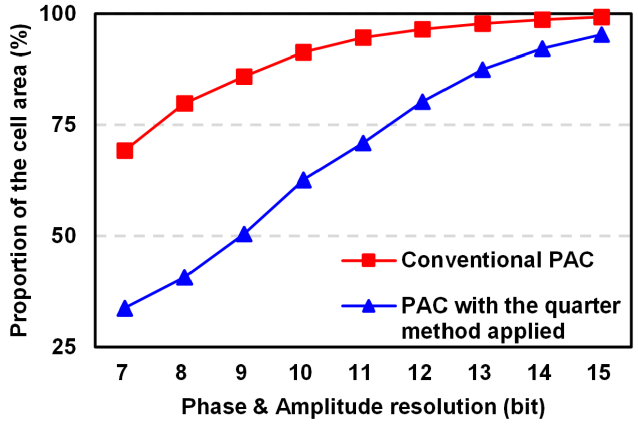

FIGURE 6. Proportion of the PAC cell area.

the complementer. As a result, DDFS with the quarter method applied has a significant advantage on the size of the LUT without any functional constraints.

A phase region detector (PRD) is employed to resolve the data size discrepancy between the PA and the PAC.

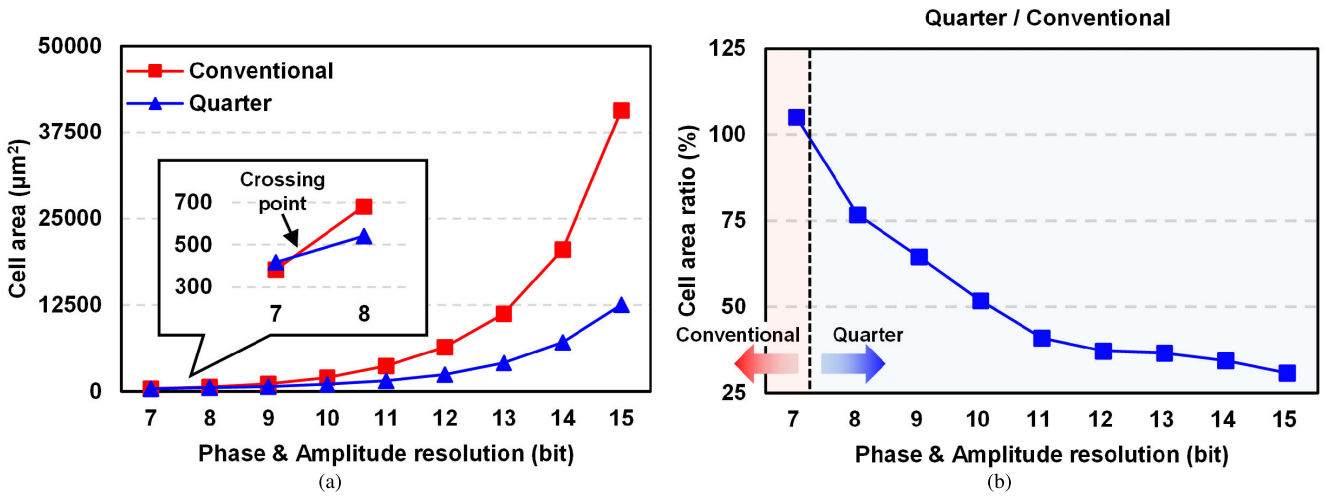

FIGURE 7. (a) Cell area, and (b) cell area ratio of the conventional DDFS and DDFS with the quarter method applied.

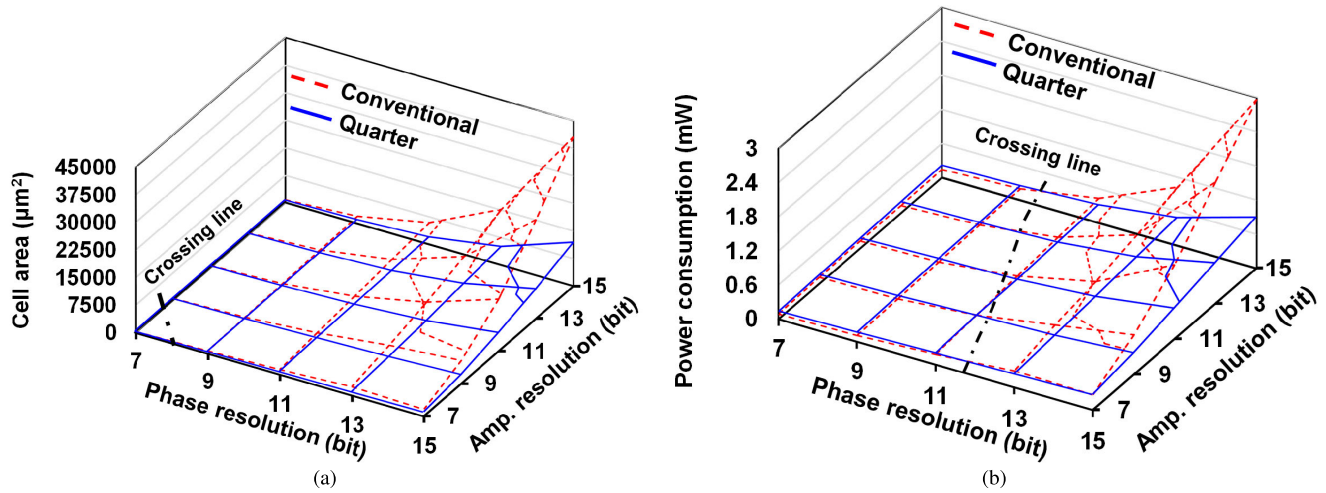

FIGURE 8. Distribution of (a) the cell area, and (b) the power consumption.

The PRD generates an indicator (referred to in Fig. 2 as a quadrant indicator) that signals which part corresponds to the point where the sine wave is equally divided into four parts. The quadrant indicator is made by using the 2-bit most-significant bits (MSB). Also, the PRD manipulates the phase to reconstruct appropriately by using the quadrant indicator, and it is implemented by flipping the phase on the second and fourth parts divided. To reconstruct the sine waveform, a complementer flips the amplitude by using the quadrant indicator when the quadrant indicator represents the third and fourth parts. The flipping process in the PRD and the complementer is performed by a bitwise not operator.

III. ANALYSIS

We analyze the constraints and advantages of DDFS with the quarter method applied in terms of performance metrics in this section. Additionally, we target the amplitude resolution region from 7 bits to 15 bits, a commonly used [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16]. The evaluation is performed at the RTL based on the low-power 65 nm CMOS technology.

A. CELL AREA

The digital design starts with a standard cell library. Thus, the cell area derives the overall area. Fig. 4 presents the architecture of the PAC block. Both the conventional DDFS and DDFS with the quarter method applied consist of a PAC controller and a LUT. The PAC controller serves to access the LUT appropriately. Also, the area of the LUT for DDFS with the quarter method applied is just a quarter compared to that of the conventional DDFS. On the other hand, it is hard to figure out the size of the PAC controller, unlike the size of the LUT. Accordingly, the area of the PAC controller is

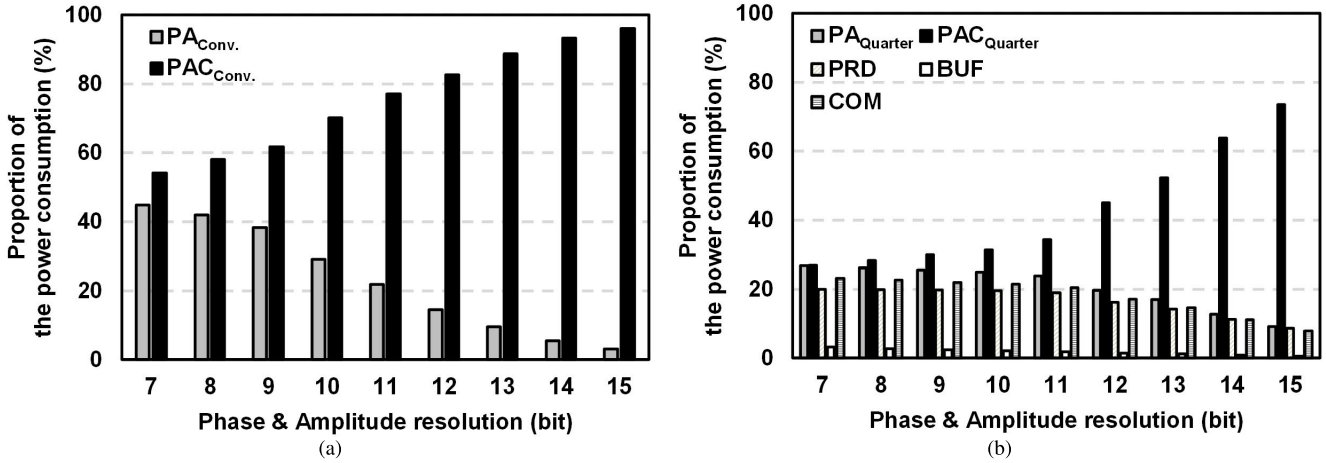

FIGURE 9. The power consumption proportion of the sub-blocks on (a) the conventional DDFS, and (b) DDFS with the quarter method applied.

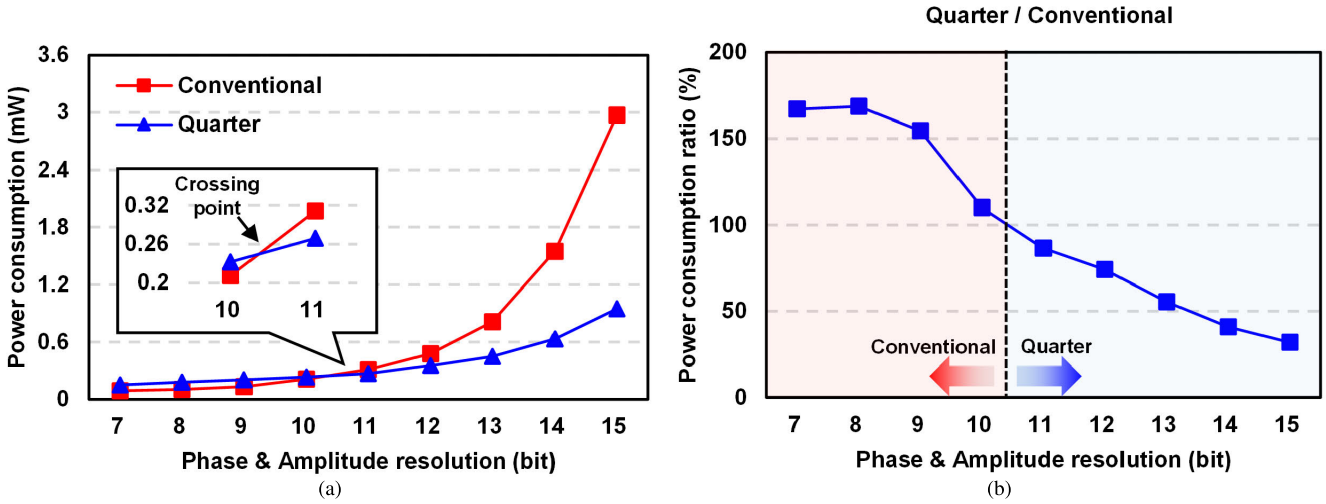

FIGURE 10. (a) Power consumption, and (b) power consumption ratio of the conventional DDFS and DDFS with the quarter method applied.

indirectly estimated using the cell area ratio of the PAC block. In Fig. 5, the cell area of the PAC of the conventional DDFS is compared with that of DDFS with the quarter method applied. The cell area ratio of PAC is over 50% at the 7-bit resolution, and the ideal area ratio of the LUT is 25%. In other words, the cell area ratio of PAC controller of the conventional DDFS and DDFS with the quarter method applied is over 75%. Also, the cell area ratio of PAC controller is maintained because the size of the PAC controllers of the conventional DDFS and DDFS with the quarter method applied depends only on the phase resolution. The cell area ratio of the PAC block is not reduced by a quarter, though the ratio becomes closer to 25% as the resolution increases. Therefore, below the 7-bit resolution, the PAC controller is the dominant block in the PAC. Conversely, at a relatively high-resolution above 8-bit, the cell area ratio is under 50%, indicating that the area of the LUT is dominant. Therefore, as the resolution increases, the area of the LUT becomes a constraint in the PAC block.

Fig. 6 presents the proportion of the PAC cell area within the area of the entire block. Here, the PAC area on the conventional DDFS always exceeds 50%. Also, the PAC area of DDFS with the quarter method applied is above 50% at a relatively high resolution (9 bits or more). Accordingly, we can consider the phase resolution generates the area changes, although not only the phase and the amplitude resolution are swept simultaneously but also the sub-blocks of the DDFS have the different relationship between the phase and amplitude resolution.

Fig. 7(a) and (b) represent the special case of Fig. 8(a), which is introduced to estimate the overall area changes according to the phase and amplitude resolution. As shown in Fig. 8(a), a wide range of the cell area distribution is evaluated, when considering the phase and amplitude resolutions. First of all, we discuss the overall changes by analyzing the special case for both the phase and amplitude resolutions before considering each resolution. In Fig. 7(b),

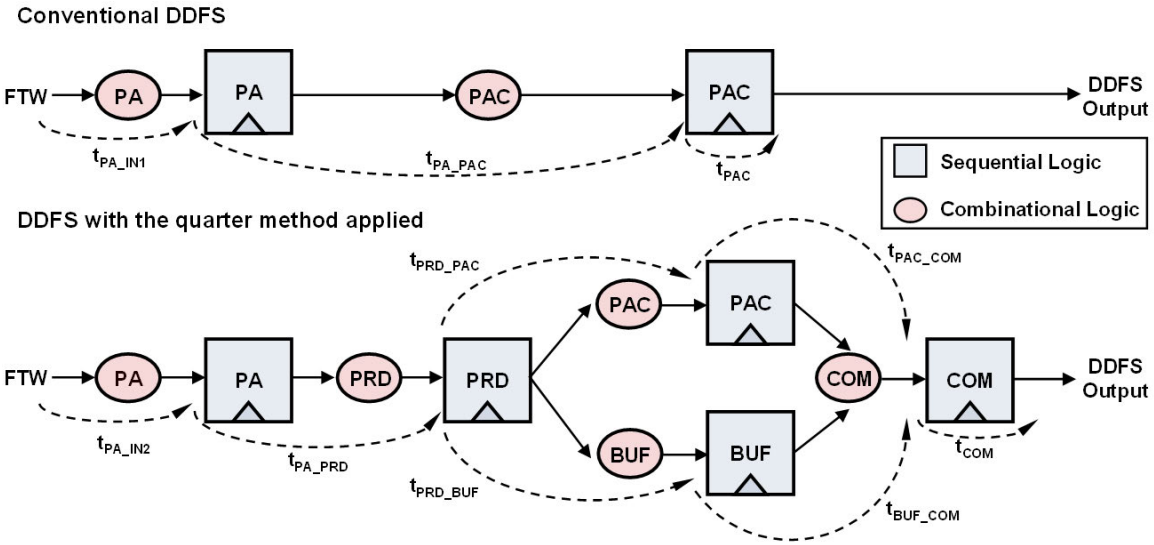

FIGURE 11. Timing constraint paths of DDFS architectures.

TABLE 1. Maximum timing constraints.

Architecture	Timing constraints	Phase and amplitude resolution (bit)								
		7	8	9	10	11	12	13	14	15
Conventional DDFS	t_{PA_IN1} (ns)	0.37	0.44	0.48	0.53	0.56	0.64	0.74	0.70	0.77
	t_{PA_PAC} (ns)	**0.52**	**0.79**	**0.89**	**1.02**	**1.15**	**1.25**	**1.39**	**1.56**	**1.79**
	t_{PAC} (ns)	0.12	0.12	0.12	0.12	0.12	0.13	0.14	0.13	0.14
DDFS with the quarter method applied	t_{PA_IN2} (ns)	0.30	0.36	0.42	0.47	0.51	0.55	0.63	0.63	0.69
	t_{PA_PRD} (ns)	0.18	0.19	0.18	0.19	0.21	0.19	0.20	0.22	0.23
	t_{PRD_PAC} (ns)	**0.35**	**0.41**	**0.64**	**0.78**	**0.87**	**1.07**	**1.12**	**1.31**	**1.36**
	t_{PRD_BUF} (ns)	0.12	0.12	0.13	0.13	0.12	0.14	0.15	0.12	0.13
	t_{PAC_COM} (ns)	0.18	0.18	0.19	0.19	0.20	0.21	0.21	0.21	0.21
	t_{BUF_COM} (ns)	0.24	0.25	0.29	0.30	0.31	0.41	0.43	0.41	0.40
	t_{COM} (ns)	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.13	0.12

the area ratio of the conventional DDFS and DDFS with the quarter method applied becomes closer to 25%, which is the ratio of the LUT size. Thus, the PAC becomes a dominant block out of the total block, and the size of the PAC becomes a limit in the total block according to increase of the phase and amplitude resolution.

Fig. 7(a) and (b) compare the cell area of the conventional DDFS and DDFS with the quarter method applied. As shown in Fig. 7(a), the cell area of both architectures increase exponentially, as the phase and amplitude resolution increases. For example, DDFS with the quarter method applied at the phase and amplitude resolution of 15-bit shows a reduced area by about 70% compared to the conventional DDFS. Moreover, the cell area difference between the conventional DDFS and the DDFS with the quarter method applied increases gradually above an 8-bit resolution of the phase and amplitude, and the crossing point is between the 7-bit and 8-bit phase and amplitude resolution. As a result, the conventional DDFS has an advantage below the 7-bit resolution of the phase and amplitude. Conversely, the conventional DDFS has a disadvantage when the phase and amplitude resolution exceed 8-bit.

The changes of the amplitude resolution result in the linear change on the area, as shown in Fig. 8(a). On the contrary, the changes of the phase resolution result in the exponential change on the area. The crossing line means the intersection point group in Fig. 8(a) between the conventional DDFS and DDFS with the quarter method applied. The crossing line also represents which DDFS architectures have an area advantage of the corresponding resolution. When comparing the case of sweeping both phase and amplitude resolution to the case of sweeping each resolution, the overall changes on area is similar to the changes sweeping the only phase resolution. Therefore, the phase resolution accounts for the significant portion of the overall changes of the area. Also, excluding the small region which is divided to the crossing line, DDFS with the quarter method applied has advantages on area at every region that is mostly used.

B. POWER CONSUMPTION

In the case of the higher voltage, we can get the considerable power consumption difference between the comparative group. Accordingly, we need to utilize the higher voltage for comparison. The analysis of the power consumption by digital circuits includes the best and worst conditions. In the best condition, the supply voltage is set at 1.1 V, which is 10% higher than the nominal supply voltage, and the temperature is maintained at −40 °C. Conversely, the worst condition features a supply voltage of 0.9 V and a temperature of 125 °C. Thus, we employ the best condition due to evaluating the notable results. In other words, we apply a 1.1 V supply voltage to evaluate. Also, in the same manner as the area analysis, we first track the overall changes by sweeping both phase and amplitude resolutions.

Fig. 9 compares the power consumption of the sub-blocks of DDFS, where BUF is the buffer utilized to match the appropriate timing between the inputs, $PA_{Conv.}$ and $PAC_{Conv.}$ are respectively the power consumption of the PA and PAC of the conventional DDFS, and $PA_{Quarter}$ and $PAC_{Quarter}$ are respectively the power consumption of the PA and PAC on DDFS with the quarter method applied. In digital integrated circuits, the power consumption is mainly estimated from the number of the digital logics, and the area increases in proportion to the number of digital logics. Therefore, the PAC blocks similarly account for the largest portion of the total power consumption. However, there is only a slight difference between the PAC blocks and the other sub-blocks at relatively low phase and amplitude resolutions. In the case of the conventional DDFS, although the difference between PAC and sub-blocks goes exponentially high as the resolution increases, there is only slight difference, 0.25% at 7-bit resolution. Similarly, in the case of the quarter method, the difference increases as the phase and amplitude resolution increases, $PAC_{Quarter}$ accounts for less than 50% below the 13-bit phase and amplitude resolution. Therefore, the area changes are not fully reflected in the power consumption changes, although the power changes stem from the area changes.

The specifications are represented in Fig. 10(a) and (b). The power consumption of both the conventional DDFS and DDFS with the quarter method applied also increase exponentially, as the phase and amplitude resolution increase. In Fig. 10(b), DDFS with the quarter method applied has an advantage of about 70% at the 15-bit phase and amplitude resolution, whereas, DDFS with the quarter method applied has a disadvantage of about 67% at the 7-bit phase and amplitude resolution. Furthermore, the conventional DDFS has benefits below 10 bits resolution. Conversely, the conventional DDFS has a disadvantage above the 11-bit phase and amplitude resolution. As a result, different with the area metric, the power consumption of the sub-blocks have the higher default value, though the power consumption have a lower sensitivity to the phase and amplitude resolution. Accordingly, the crossing point exists in the higher phase and amplitude resolution comparing to the area.

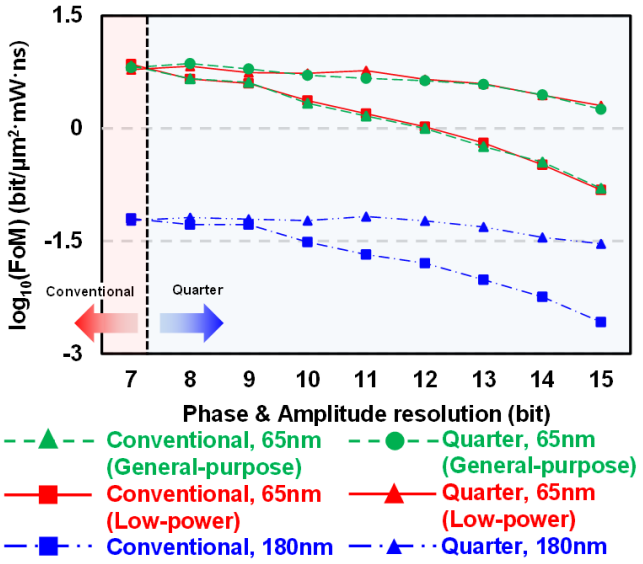

FIGURE 12. FoM of the conventional DDFS and DDFS with the quarter method applied on the CMOS technologies.

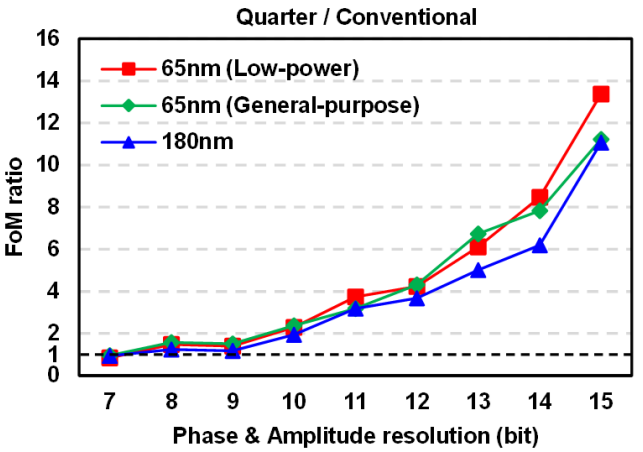

FIGURE 13. FoM ratio of the conventional DDFS and DDFS with the quarter method applied on the CMOS technologies.

The changes of the amplitude resolution, likewise, result in the linear change on the power consumption, as shown in Fig. 8(b). On the contrary, the changes of the phase resolution results in the exponential change on the power consumption. For the same reason with the area, the overall changes of the power consumption mainly depend on the phase resolution. Based on the characteristic of the power consumption changes, the crossing line, the intersection point between the power consumption of the conventional DDFS and DDFS with the quarter method applied, is spread more widely when comparing with the crossing line of the area.

C. TIMING CONSTRAINT

The depth of the combinational logic has deepened with the development of integrated circuits, and the maximum combinational logic has become the most burdensome factor when designing digital integrated circuits for the higher

throughput [31]. In other words, the timing constraints from the register to register, which consist of the combinational logics, are the important factor in determining the operating speed. Therefore, here we discuss the combinational logics, not the sequential logics. The results below are evaluated at a 100 MHz clock frequency with a 50% duty cycle. Also, the other conditions (e.g., input delay, output delay, clock uncertainty, transition, and latency) are fixed for the precise comparison.

Fig. 11 show the main timing constraints of the conventional DDFS and DDFS with the quarter method applied, and each timing constraint, expressed as t, includes seqeuntial logics or combinational logics. In Fig. 11, the following terms are employed: BUF indicates buffer, COM represent the complementer. Both architectures have the same PAC structures, the only difference is the size of the phase resolution applied to PAC. Accordingly, the t_{PA_PAC} and t_{PRD_PAC} have the similar components. As shown in Fig. 11 and Table. 1, the burdensome timing constraints are t_{PA_PAC} and t_{PRD_PAC} on each DDFS architecture. In addition, the timing constraints of the other paths have the small portion. For example, the smallest difference between the most burdensome timing constraint and the second burdensome timing constraint is about 15% at the 7-bit DDFS with the quarter method applied and is about 57% at the 15-bit conventional DDFS. Consequently, as same with the case of the area and power consumption, the PAC blocks result in the speed limit. Especially, as the PAC block gets complicated, the main constraint of the speed is the combinational logics of the PAC.

t_{PA_PAC} is always more time constrained than t_{PRD_PAC} at the target phase and amplitude resolutions from 7-bit to 15-bit. Unlike the area and power consumption, t_{PA_PAC} and t_{PRD_PAC} change linearly according to the phase and amplitude resolution. Furthermore, an additional design margin of the operating speed is ensured with the quarter method when performed at a 100 MHz clock frequency. As a result, the DDFS with the quarter method applied has the advantage over the target resolution.

D. FIGURE OF MERIT

The performance metrics of DDFS commonly consists of the clock frequency, SFDR, area, and power consumption [3], [32]. Thus the FoM can be expressed as

$$\text{FoM} = \frac{2^n}{\text{Area} \cdot \text{Power} \cdot \text{T}_{\text{max}}}. \tag{3}$$

Here, Area, Power, and T_{max} respectively represents the cell area, the power consumption, and the worst timing constraint of the DDFS. The phase resolution is introduced instead of the SFDR because the SFDR strongly depends on the phase resolution [30], [33]. The FoM of the digital domain design on DDFS is evaluated at the RTL only the quantization noise exists. In this section, the FoM is evaluated at the low-power and the general-purpose 65 nm CMOS technologies and

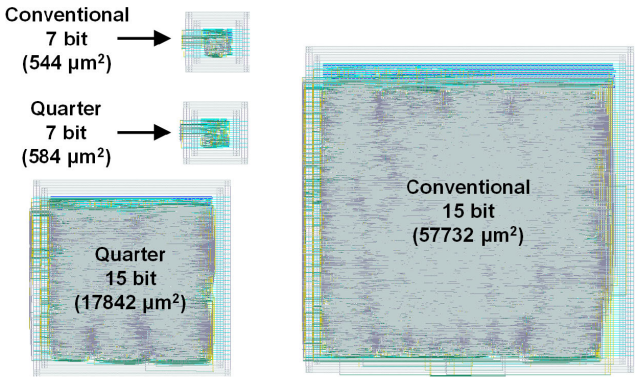

FIGURE 14. Area of the conventional DDFS and DDFS with the quarter method applied (65 nm CMOS technology).

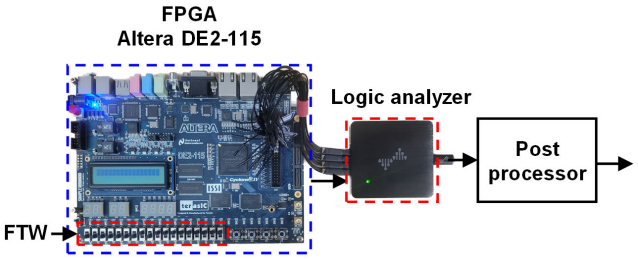

FIGURE 15. Measurement setup.

180 nm CMOS technology to verify the quarter method according to the CMOS technology.

Similar characteristics are observed in the FoMs across the three distinct CMOS technologies (low-power and general-purpose 65 nm CMOS technologies, and 180 nm CMOS technology). As shown in Fig. 12, DDFS with the quarter method applied consistently outperforms the conventional DDFS beyond the 7-bit phase and amplitude resolution in the introduced CMOS technologies. Furthermore, the FoM difference between the conventional DDFS and DDFS with the quarter method applied increases as the phase and amplitude resolution increase, and it is precisely presented in Fig. 13. Fig. 13 represents the benefits of DDFS with the quarter method applied more accurately by comparing the FoM ratio. The exponentially increasing advantages of DDFS with the quarter method applied emerge in the same pattern in the introduced 65 nm and 180 nm CMOS technologies. Consequently, the advantages of the quarter method could be applied consistently across different CMOS technologies.

In the analysis section, we pinpoint specific phase and amplitude resolution thresholds where the structural advantages shift. Regarding power consumption, this transition occurs between 10-bit and 11-bit phase and amplitude resolution. In terms of area and figure of merit, it happens within the 7-bit to 8-bit phase and amplitude resolution range. These transition points are situated in relatively low-resolution regions. However, when considering the differences in structural advantages, there is little difference in the relatively low-resolution regions. Therefore, DDFS

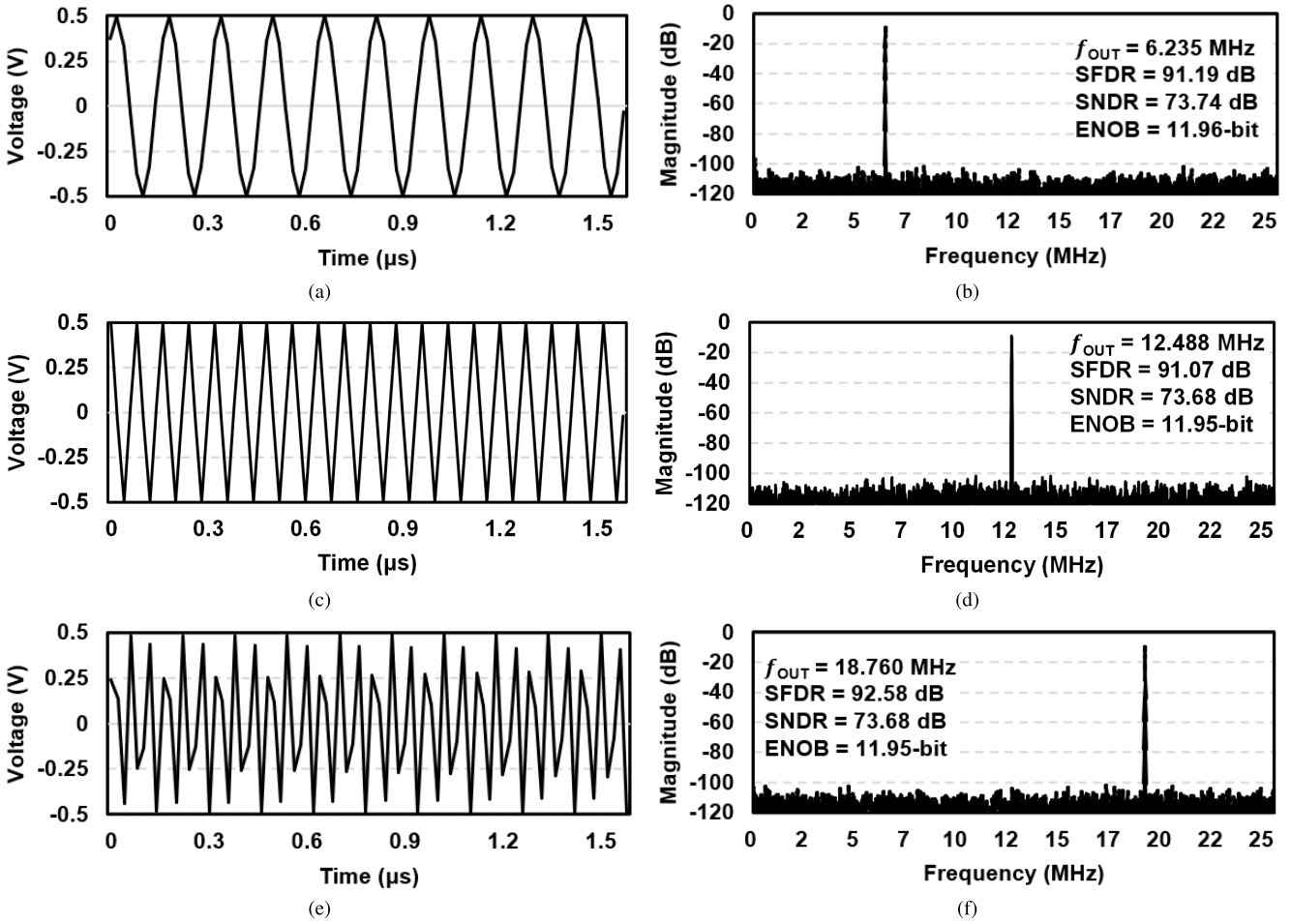

FIGURE 16. Measured transient responses and FFT spectrums of low, medium, and high DDFS output frequencies.

with the quarter method applied offers significant advantages compared to the conventional DDFS.

IV. MEASUREMENT RESULTS

A. PHYSICAL DESIGN RESULTS

The core area is evaluated in terms of the digital place and route (PNR) results, as shown in Fig. 14. In order to increase the reliability of the evaluation, the cell utilization rate is maintained at about 70% and the evaluation is conducted at 7-bit and 15-bit resolution. The core area in Fig. 14 is respectively 544 μm^2, 584 μm^2, 17842 μm^2, and 57732 μm^2. Also, the core area ratio of the conventional DDFS and DDFS with the quarter method applied is approximately 107% at 7 bits resolution and 31% at 15 bits resolution. These area ratios are nearly identical to the cell area ratio, which is evaluated according to the RTL, of the conventional DDFS and DDFS with the quarter method applied (105% at 7 bits resolution and 31% at 15 bits resolution). Therefore, the cell area at the RTL is effective in terms of the area.

B. IMPLEMENTATION RESULTS

The block diagram of the measurement setup is shown in Fig. 15. DDFS architectures are built on FPGA (Altera DE2-115 with Cyclone IV E EP4CE115F29C7N device). In addition, the general-purpose input/output (GPIO) switch embedded in the FPGA is used to supply FTW, which is the digital input of DDFS architecture, and the clock is also supplied by the FPGA board. A logic analyzer (Dreamsourcelab DSLogic Plus) is introduced to receive up to 16 channels of digital data, which is the output of the digital domain on DDFS. The outputs of the logic analyzer are captured and converted to the analog sinusoidal waveform by using a post-processor instead of the DAC. The FPGA is also fabricated using 65 nm CMOS technology which is the same as the RTL foundry, although the operating voltage is higher. Accordingly, the reliability of the evaluated data from the RTL is enhanced.

The output frequency of DDFS with the quarter method applied is measured at low, medium, and high FTW inputs (FTW is respectively 511, 1023, and 1537). Here, f_{CLK} is 50 MHz with a 50% duty cycle and the phase resolution is 12 bits. In addition, an ideal DAC is used to exclude any other effects except for digital parts of the DDFS design. According to (1), we can estimate that the output frequencies are respectively 6.237 MHz, 12.488 MHz, and 18.763 MHz when the FTW size is 511, 1023, and 1537. As shown in

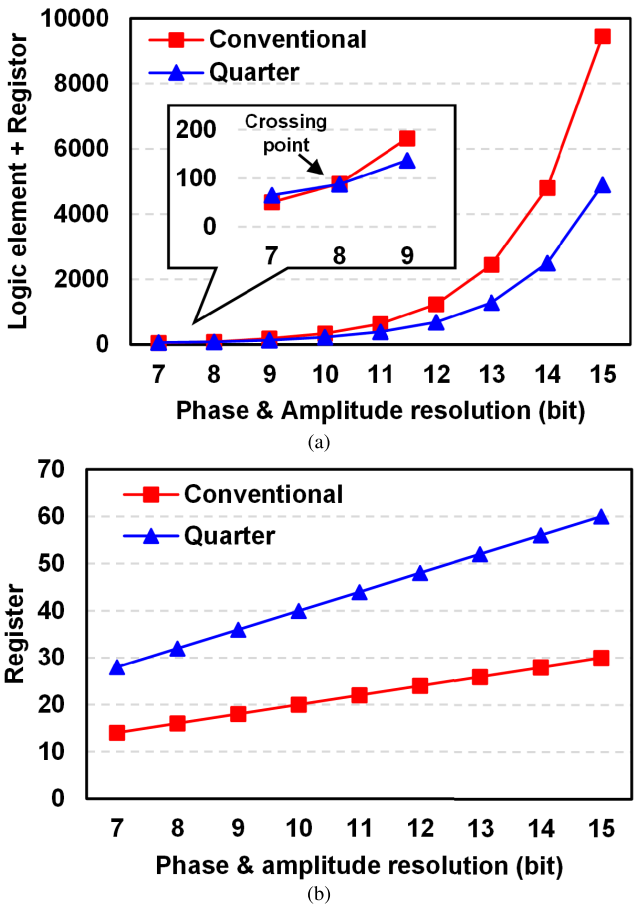

FIGURE 17. (a) Measured logic elements and registers, and (b) measured registers in FPGA.

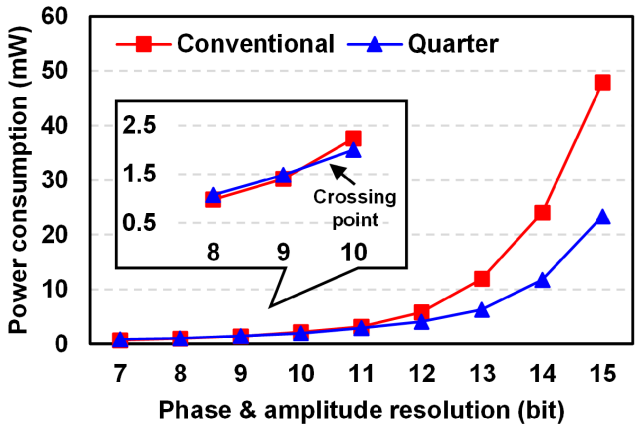

FIGURE 18. Measured power consumption in FPGA.

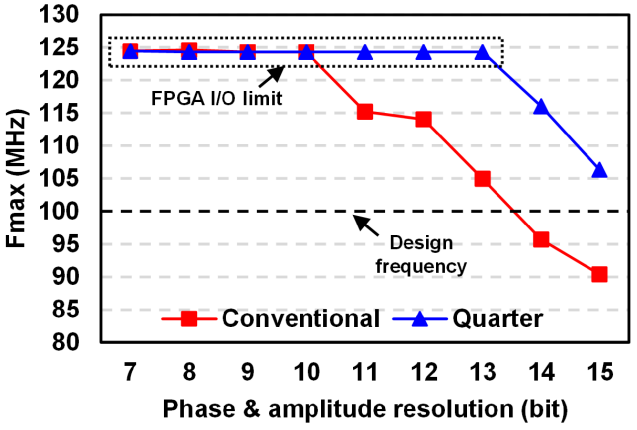

FIGURE 19. Measured synthesizable maximum clock frequency in FPGA.

Fig. 16, the output frequency increases as the size of the FTW increases. Fast-fourier transform (FFT) proceeds with 5120 samples after windowing. The only a 0.05% difference in the output frequency between the measured results and the estimation. The signal-to-noise-and-distortion ratio (SNDR) and an effective number of bits (ENOB) also have negligible differences compared to those when only the quantization error exists (74 dB and 12 ENOB). Accordingly, a spurious-free dynamic range (SFDR) is dominantly deteriorated by an only noise floor of the quantization error. As a result, the functionality of DDFS with the quarter method is totally verified.

Logic elements and registers consist of the implemented design in the FPGA. The area is induced by evaluating the number of the logic elements and the registers. As shown in Fig. 17(a), similar to the RTL evaluation, the number of logic element and register increase exponentially in both the conventional DDFS and DDFS with the quarter method applied, although the increase rate is different to the evaluation of the RTL; the difference is derived from the reason that each logic element and register occupies different areas. In addition, DDFS with the quarter method applied has an area advantage, when exceeds 8-bit resolution. In Fig. 17(b) however, the number of registers of the conventional DDFS consists of fewer registers because DDFS with the quarter method applied is more complicated than the conventional DDFS; DDFS with the quarter method stores more intermediate results, data inputs, or control signals within the digital logic circuit. Furthermore, the LUT which performs a simple function mostly consists of logic elements, and the number of registers increases linearly as the resolution increases due to a negligible effect of the LUT.

Similar to the RTL evaluation, the measured power consumption increases exponentially, as shown in Fig. 18. The crossing point also exists and appears between 9 bits and 10 bits resolution in measured data. A slight difference with the RTL evaluation is derived from the operating voltage. MOSFET is greatly dependent on the operating voltage and the change of the operating voltage generates an exponential increase in power consumption, not a linear increase. Therefore, digital logics of the DDFS which are implemented in FPGA have more power consumption and the crossing point appears at a lower resolution than the evaluation of the RTL.

Fig. 19 represents the advantage of DDFS with the quarter method applied in terms of the operating speed, where Fmax

indicates the maximum synthesizable clock frequency. At the resolution of 13 bits to 15 bits, the maximum synthesizable frequency of DDFS with the quarter method applied is approximately 20% faster than the conventional DDFS, though there is a flat region in both the conventional DDFS and DDFS with the quarter method applied due to the limit of the FPGA evaluating process. In other words, a complexity of DDFS architecture is tolerable below 10 bits resolution in the conventional DDFS and below 13 bits resolution in DDFS with the quarter method applied. As the time constraints increase linearly when the resolution increases, the maximum synthesizable clock frequency decreases linearly except for the flat region, and even deteriorate below the design frequency in the case of the conventional DDFS.

V. CONCLUSION

In this paper, we provide a wide range of benchmarks according to the resolution for the conventional DDFS and DDFS with the quarter method applied. The most burdensome factor is analyzed as PAC in terms of area, power consumption, and timing constraint. The quarter method has advantages in area, power consumption, and FoM when the phase and amplitude resolution exceed 7-bit, 10-bit, and 7-bit, respectively. In the case of the timing constraint, it always outperforms comparing to the conventional DDFS when the quarter method is applied. Furthermore, DDFS with the quarter method applied offers significant advantages compared to the conventional DDFS. Because the crossing points that the structural advantages change are in the relatively low-resolution regions where the only slight differences between the conventional DDFS and DDFS with the quarter method applied exist. Also, the architecture and area are demonstrated by physical design results and FPGA verification. In this study, therefore, we obtain a broad range of the specification benchmarks for both DDFS architectures.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

REFERENCES

[1] X. Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "24-bit 5.0 GHz direct digital synthesizer RFIC with direct digital modulations in 0.13 μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 944–954, May 2010.

[2] A. M. Alonso, M. Miyahara, and A. Matsuzawa, "A 7GS/s direct digital frequency synthesizer with a two-times interleaved RDAC in 65 nm CMOS," in *Proc. ESSCIRC*, Sep. 2017, pp. 151–154.

[3] A. M. Alonso, M. Miyahara, and A. Matsuzawa, "A 12.8-ns-latency DDFS MMIC with frequency, phase, and amplitude modulations in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2840–2849, Oct. 2018.

[4] J. P. G. van Dijk, B. Patra, S. Pellerano, E. Charbon, F. Sebastiano, and M. Babaie, "Designing a DDS-based SoC for high-fidelity multi-qubit control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5380–5393, Dec. 2020.

[5] A. Tang, Y. Kim, T. J. Reck, G. Chattopadhyay, I. Mehdi, B. J. Drouin, K. B. Cooper, N. J. Livesey, and M. F. Chang, "DDFS and $\Sigma\Delta$ approaches for fractional frequency synthesis in terahertz instruments," *IEEE Trans. THz Sci. Technol.*, vol. 8, no. 4, pp. 410–417, Jul. 2018.

[6] S. D'Souza, F. Hsiao, A. Tang, S.-W. Tam, R. Berenguer, and M. F. Chang, "A 10-bit 2-GS/s DAC-DDFS-IQ-controller baseband enabling a self-healing 60-GHz radio-on-chip," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 8, pp. 457–461, Aug. 2013.

[7] T. Yoo, H. C. Yeoh, Y.-H. Jung, S.-J. Cho, Y. S. Kim, S.-M. Kang, and K.-H. Baek, "A 2 GHz 130 mW direct-digital frequency synthesizer with a nonlinear DAC in 55 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2976–2989, Dec. 2014.

[8] H. C. Yeoh, J.-H. Jung, Y.-H. Jung, and K.-H. Baek, "A 1.3-GHz 350-mW hybrid direct digital frequency synthesizer in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1845–1855, Sep. 2010.

[9] X. Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "An 11-bit 8.6 GHz direct digital synthesizer MMIC with 10-bit segmented sine-weighted DAC," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 300–313, Feb. 2010.

[10] Z. Zhou and G. S. La Rue, "A 12-bit nonlinear DAC for direct digital frequency synthesis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2459–2468, Oct. 2008.

[11] J. Lindeberg, J. Vankka, J. Sommarek, and K. Halonen, "A 1.5-V direct digital synthesizer with tunable delta-sigma modulator in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1978–1982, Sep. 2005.

[12] S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with sine-weighted DAC at 32-GHz clock frequency in InP DHBT technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2284–2290, Oct. 2006.

[13] S. Mortezapour and E. K. F. Lee, "Design of low-power ROM-less direct digital frequency synthesizer using nonlinear digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1350–1359, Oct. 1999.

[14] C.-C. Wang, J.-M. Huang, Y.-L. Tseng, W.-J. Lin, and R. Hu, "Phase-adjustable pipelining ROM-less direct digital frequency synthesizer with a 41.66-MHz output frequency," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 10, pp. 1143–1147, Oct. 2006.

[15] D. De Caro, N. Petra, and A. Strollo, "Reducing lookup-table size in direct digital frequency synthesizers using optimized multipartite table method," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 2116–2127, Aug. 2008.

[16] A. Ashrafi, R. Adhami, and A. Milenkovic, "A direct digital frequency synthesizer based on the quasi-linear interpolation method," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp. 863–872, Apr. 2010.

[17] M. J. Schulte and J. E. Stine, "Approximating elementary functions with symmetric bipartite tables," *IEEE Trans. Comput.*, vol. 48, no. 8, pp. 842–847, Aug. 1999.

[18] X. Li, L. Lai, A. Lei, and Z. Lai, "A memory-reduced direct digital frequency synthesizer for OFDM receiver systems," *IEEE Trans. Consum. Electron.*, vol. 54, no. 4, pp. 1564–1568, Nov. 2008.

[19] Y. Song and B. Kim, "Quadrature direct digital frequency synthesizers using interpolation-based angle rotation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 7, pp. 701–710, Jul. 2004.

[20] S.-S. Jeng, H.-C. Lin, and C.-Y. Wu, "High-performance DDFS design using the equi-section division method," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 57, no. 12, pp. 2616–2626, Dec. 2010.

[21] C. Y. Kang and E. E. Swartzlander, "Digit-pipelined direct digital frequency synthesis based on differential CORDIC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 5, pp. 1035–1044, May 2006.

[22] J. M. P. Langlois and D. Al-Khalili, "Phase to sinusoid amplitude conversion techniques for direct digital frequency synthesis," *IEE Proc., Circuits Devices Syst.*, vol. 151, no. 6, pp. 519–528, Dec. 2004.

[23] D. De Caro, N. Petra, and A. G. M. Strollo, "A 380 MHz direct digital synthesizer/mixer with hybrid CORDIC architecture in 0.25 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 151–160, Jan. 2007.

[24] A. Madisetti, A. Y. Kwentus, and A. N. Willson, "A 100-MHz, 16-b, direct digital frequency synthesizer with a 100-dBc spurious-free dynamic range," *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp. 1034–1043, Aug. 1999.

[25] D. De Caro, E. Napoli, and A. G. M. Strollo, "Direct digital frequency synthesizers with polynomial hyperfolding technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 7, pp. 337–344, Jul. 2004.

[26] D. De Caro, N. Petra, and A. Strollo, "Digital synthesizer/mixer with hybrid CORDIC–multiplier architecture: Error analysis and optimization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 364–373, Feb. 2009.

[27] A. -J. Annema, "Analog circuit performance and process scaling," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 711–725, Jun. 1999.

[28] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Trans. Audio Electroacoust.*, vol. AU-19, no. 1, pp. 48–57, Mar. 1971.
[29] J. Vankka, "Methods of mapping from phase to sine amplitude in direct digital synthesis," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 44, no. 2, pp. 526–534, Mar. 1997.
[30] H. T. Nicholas and H. Samueli, "An analysis of the output spectrum of direct digital frequency synthesizers in the presence of phase-accumulator truncation," in *Proc. 41st Annu. Symp. Freq. Control*, May 1987, pp. 495–502.
[31] M. Sivaraman and A. J. Strojwas, "Primitive path delay faults: Identification and their use in timing analysis," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 19, no. 11, pp. 1347–1362, Nov. 2000.
[32] D. Yoon, K. Baek, and T. T. Kim, "A 2.5 GHz 104 mW 57.35 dBc SFDR non-linear DAC-based direct-digital frequency synthesizer in 65 nm CMOS process," in *Proc. ESSCIRC*, Sep. 2022, pp. 241–244.
[33] P. O'Leary and F. Maloberti, "A direct-digital synthesizer with improved spectral performance," *IEEE Trans. Commun.*, vol. 39, no. 7, pp. 1046–1048, Jul. 1991.

JAE-YUN PARK received the B.S. degree in electronic and IT media engineering from the Seoul National University of Science and Technology (SeoulTech), Seoul, in 2021, where he is currently pursuing the M.S. degree in electronic engineering. His research interest includes low-power high-speed high-resolution analog-to-digital and digital-to-analog data converters.

SU-HYEON KIM is currently pursuing the B.S. degree in electronic engineering with the Seoul National University of Science and Technology (SeoulTech), Seoul. Her research interests include CMOS based analog and mixed-signal integrated circuit and signal processing circuit design.

HYUNYOUNG YOO received the B.S. degree in electronic engineering from the Seoul National University of Science and Technology (SeoulTech), Seoul, South Korea, in 2023, where she is currently pursuing the M.S. degree in electronic engineering. Her research interests include mixed-signal integrated circuits and CMOS sensor readout circuit design.

JAE-WON NAM (Member, IEEE) received the B.S. and M.S. degrees from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2006 and 2008, respectively, and the Ph.D. degree in electrical engineering from the University of Southern California (USC), Los Angeles, CA, USA, in 2019. From 2008 to 2012, he was a full-time Researcher with the Electronics and Telecommunications Research Institute (ETRI), Daejeon. Since Fall 2017, he has been a Graduate Intern with the Data Center Group, Intel Corporation, Santa Clara, CA, USA, involving on next-generation high-speed I/O architectures. From July 2019 to July 2020, he was an Analog Engineer with Intel Corporation Ltd., I/O Circuit Technology Team. He is currently an Assistant Professor with the Department of Electronic Engineering, Seoul National University of Science and Technology (SeoulTech). His research interests include designing cryogenic low-power high-speed high-resolution analog-to-digital data converters and high-speed I/O interface circuits.