RESEARCH ARTICLE

Design of a Double-Half-Bridge Rectifier With Single-Stage and Power Decoupling

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ABSTRACT Several power decoupling techniques have been studied in the specialized literature to reduce or eliminate the ripple at 120 Hz intrinsic to the nature of single-phase AC-DC converters. Among these techniques are the active decoupling circuits, which insert new switches and passive elements in the circuit to increase costs and losses in the converters. The complete single stage (CSS) of power decoupling is defined in this study. The switches responsible for controlling the power factor in the proposed converter also control the output voltage and the ripple at 120 Hz using the phase-shift technique. Thus, lower-value capacitors can be used, allowing the replacement of the widely used electrolytic capacitors with film capacitors, which have a long useful life compared to the former. In addition, the proposed converter is isolated and has high efficiency. Simulation and experimental results are presented for a 1 kW prototype with an efficiency of up to 93%, showing that power decoupling is obtained, and the CSS topology definition can be incorporated into the literature.

INDEX TERMS Single-phase AC–DC converter, power factor correction, integrated power decoupling, single-stage converter, ripple power, phase-shift control.

I. INTRODUCTION

AC-DC converters are used in all sectors of the economy, whether in industrial and commercial industries or household equipment. For instance, they have been used in lighting drivers LED (light emitting diode) [1], [2], [3], energy storage systems (ESS) [4], uninterruptible power supplies (UPS) [5], [6], sources for charging laptops [7], converters for controlling the speed of engines [8], interfaces with renewable energy sources such as wind and solar photovoltaic energy, process technology as electroplating and welding units [9], and application in electric vehicles (EV) [10].

Current single-phase AC-DC converters have Power Factor Correction (PFC), and for processing powers above 1kW, half-bridge and full-bridge topologies are the most used. These can reach yields of 96% to 98% when not isolated [11], [12] and from 90% to 95% when isolated [13], [14].

Output voltage ripple at 120 Hz, commonly called power coupling or ripple, is inherent in single-phase AC-DC converters. Decreasing this ripple with output filtering capacitors

is costly, resulting in high-capacitance capacitors, and electrolytic capacitors are often used for this purpose. Still, they have a short useful life compared to film capacitors [15], [16]. Thus, several topologies have been presented over the years to minimize output voltage ripple, being initially introduced in AC-DC converters as pre-regulator circuits [17] with active filters.

The circuit of Fig. 1(a) shows the typical configuration of an AC-DC converter. The converter in this figure is composed of two stages. The first stage is used for rectification and PFC control. The output of the first stage has a ripple that is minimized but not eliminated with the use of capacitor C (central bus).

In the second stage, the converter output voltage V_0 is controlled, and the ripple is reduced. Usually, the second stage uses active circuits with command switches and passive elements (capacitors and inductors), which provide energy storage from the input power ripple. Several topologies can be verified in [18], [20], [21], and [22].

New circuit elements are inserted in the second stage, and efficiency decreases and costs increase. Due to this inconvenience, the so-called single-stage topologies have been
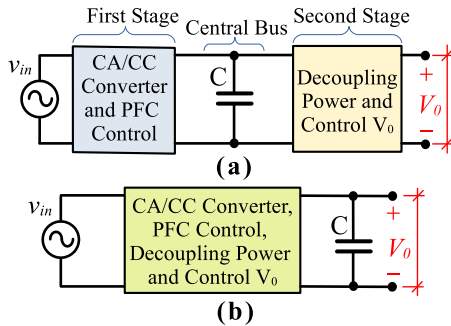
FIGURE 1. (a) Topology of two-stage converters. (b) CSS topological configuration of the proposed converter.

studied and have as their main characteristic the use of the same set of switches, which performs the rectification and the PFC control to eliminate or minimize the ripple at 120 Hz and regulate the output voltage.

The topology by [19] is presented as a single-stage with current input and not isolated. The authors present a full-bridge structure with four command switches, an AC-DC diode rectifier bridge at the input, and two other diodes inserted in the topology together with two capacitors that operate with high ripples and absorb the ripple at 120 Hz of the output, promoting power decoupling. Compared to isolated converter topologies, the converter efficiency is low due to the input rectifier bridge and the two diodes inserted in the topology.

A full-bridge isolated topology with two input inductors that help to control PFC and two other diodes in parallel with the DC bus capacitor where the reference of the alternating input source is connected is presented by [23]. The circuit needs a small inductor and capacitor in series with the transformer's primary to operate resonantly. According to the authors, it allows the operation of all the command switches in a zero-voltage switching (ZVS) and zero-current switching (ZCS) for the diode rectifier stage on the secondary side of the transformer. The DC bus capacitor has a low value, allowing its use in film capacitors. Still, the output filter capacitor on the secondary side is exceptionally high for the processed power of the converter (1 kW). The converter presented by [24] is a full-bridge based on the AC-DC half-bridge converter. The correct switching of command switches causes the output voltage ripple to be stored in the capacitor below the half-bridge output. This capacitor can work with a high ripple, which allows its size to be reduced. The load is connected in parallel with the upper capacitor, which is exempt from ripple and hence can also be reduced. The prototype has an efficiency slightly higher than 92%, with a 1 kW power, but it is not isolated. The drawback of the topology is the complex way of switching the command keys.

The study by [25] shows that some active decoupling circuits and circuits using the half-bridge topology with the technique called interleaving are suitable for processing powers higher than 0.5 kW and may form full-bridge topologies with power decoupling and single-stage output

voltage control. Topologies based on half-bridge interleaving and isolated topologies have as main characteristics the reduction of input current ripples, as it is a function of the number of switching arms to be used, directly impacting the removal of current flowing in command switches [26]. The study by [27] uses a topology derived from the interleaved half-bridge converter to be isolated bi-directionally, and the power transfer occurs through the phase-shift delay between the primary and secondary arms of the converter. Although the study's main objective is not a reduction in ripple in the structure of [27], it was analyzed by [28], who changed the topology so that it could be used in EV battery charging systems, which are bidirectional and isolated. This topology, also presented by [29], seeks to obtain power decoupling and output voltage control through phase-shift control. Results obtained with a 1 kW prototype showed that the output ripple is reduced, and the converter efficiency reaches approximately 90% when operating at nominal power.

Another isolated topology that uses phase-shift control may be obtained by integrating the interleaved differential boost AC-DC converters and the bidirectional DC-DC converter. The combination of the two converters is shown by [33] and is also used for charging EV batteries. The topology has as its main features that it is isolated, has smooth commutation for almost all command switches, and uses only film capacitors due to the power decoupling obtained with the converter control system. The power of the prototype presented by the authors is 6.6 kW; the efficiency is not shown, and the topology uses two isolating transformers and a high number of command switches and power diodes.

Single-stage topologies often use auxiliary circuits to reduce or minimize the output ripple, as in [22] and [23], and others specifically for LED lighting applications [30], requiring non-switched rectifiers for AC-DC conversion. Therefore, the definition of a complete single-stage (CSS) topological structure is to be presented and set, as shown in Fig. 1(b). The interleaved half-bridge topology is used with the phase-shift control system in this structure. The AC-DC converter proposed in this study with the CSS definition has the following advantages:

1) Unitary PFC and high-frequency isolation;
2) Division of the input current equally between switches, which allows applications at high powers;
3) Complete single-stage, with no other new active or passive element inserted in the circuit, which increases the topology efficiency even when isolated;
4) Power decoupling through phase-shift control and
5) The possibility of using film capacitors and, consequently, increases the useful life of the converter.

II. PROPOSED TOPOLOGY AND CONVERTER OPERATION
The topology of the proposed converter is obtained by connecting two half-bridge converters with PFC, which are identical and denoted HB1 and HB2 in Fig. 2(a). In this figure, HB1 and HB2 are delineated by the gray and red polygons, respectively, using the same source v_{in} and
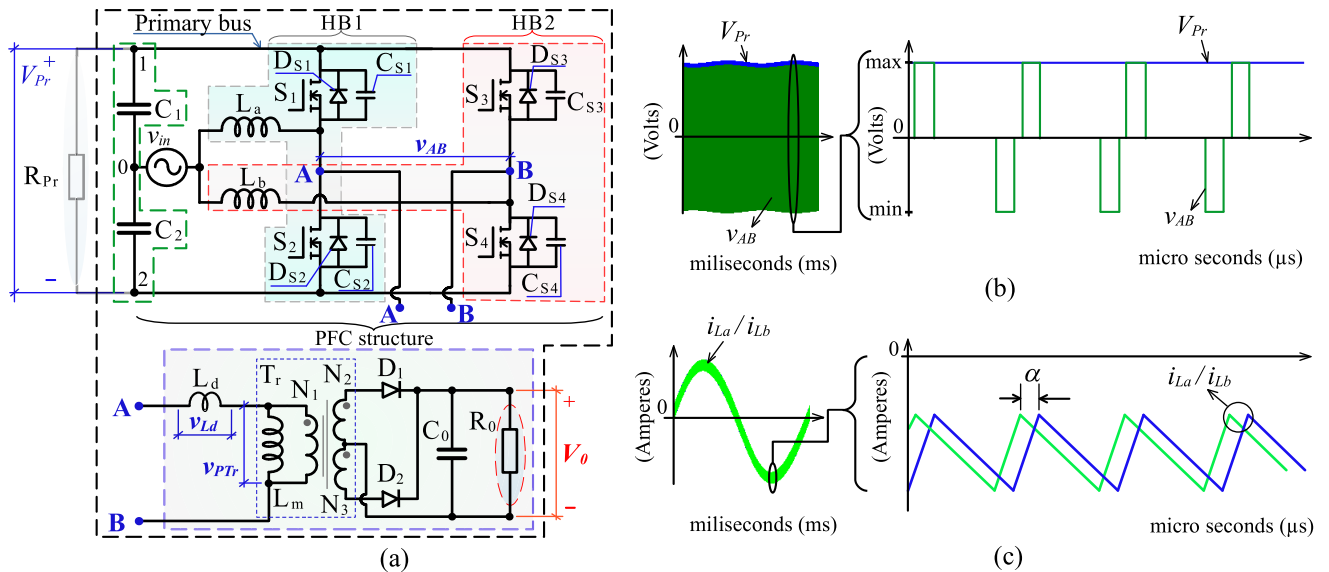
FIGURE 2. (a) Complete topology of the proposed AC-DC converter. (b) Typical waveforms of voltages between points AB and V_{Pr}. (c) Waveform of currents in inductors L_a and L_b at low frequency (left) and high frequency (right).

capacitors C_1 and C_2, outlined by the green polygon. Switches S_1 and S_2 and inductor L_a form commutation arm 1, and switches S_3 and S_4 and inductor L_b form commutation arm 2. The entire top circuit in Fig. 2(a) is referred to as the PFC structure, and all commanded switches, their diodes, and intrinsic capacitances are represented by D_S and C_S and follow this nomenclature along with their respective switch numbers.

When switching arms 1 and 2 have the same duty cycle, the circuit continues to operate as a single half-bridge, and the voltage between points AB (v_{AB}) of the circuit in Fig. 2(a) is zero. However, when the duty cycle between the switching arms is shifted by an angle D_α, the voltage v_{AB} has three levels, as shown in Fig. 2(b) on the right. The voltage between points 1 and 2 of the structure PFC is called the primary bus voltage V_{Pr} and still has a ripple of 120 Hz, as shown in the graph in Fig. 2(b) on the left. Although this ripple is present, it can be significantly reduced, as shown in Section VI of this paper. Fig. 2(c), on the left, are the waveforms of the currents i_{La} and i_{Lb} at low frequency and on the right at high frequency, showing the delay D_α between the cyclic ratios of switching arms 1 and 2.

The complete topology of the converter is obtained by inserting an isolation transformer T_r with a center tap and the rectifier circuit on the secondary/tertiary side of the same. The rectifier circuit consists of D_1, D_2, and C_0. The load R_{Pr} connected to the primary bus in Fig. 2(a) is redrawn on the secondary side of the transformer and replaced by R_0. Although the configuration also allows different loads on both the primary and secondary of the transformer, in this study, the load R_0 will be on the secondary side of T_r only. In transformer T_r, L_m is the magnetizing inductance of the transformer, which also has a leakage inductance L_{disp}. The energy transfer between the primary and secondary sides of

the transformer can be achieved only through the leakage inductance and is suitably achieved by the fabrication process, as proposed in [36]. Still, in practice, a small series inductance L_s is used with the primary side of T_r such that $L_d = L_{disp} + L_s$. Fig. 2(a), bounded by the black dashed rectangle, shows the complete topology of the converter, with the output voltage V_0 and voltages v_{Ld} and v_{PTr} highlighted to help understand the operation of the converter.

III. OPERATION STAGES
The converter operation analysis is obtained from the circuits in Fig. 3. The transformation ratio of the isolation transformer is called

$$a = \frac{N_1}{N_2} = \frac{N_1}{N_3}, \qquad (1)$$

where N_1, N_2, and N_3 are the number of turns of the primary, secondary, and tertiary of the T_r, where $N_2 = N_3$. Nine operation steps occur for each half-cycle of the network, and the input voltage v_{in} in a switching cycle is considered constant and is equal to V_{in} for the positive half-cycle. The voltages at C_1 (v_{C1}) and C_2 (v_{C2}) are considered constant and result in the primary bus voltage when added together,

$$V_{Pr} = v_{C1} + v_{C2}. \qquad (2)$$

The operating stage shown below considers the positive half cycle of v_{in} and a fixed D_α phase shift without eliminating the ripple in V_{Pr}. Fig. 4 shows the main waveforms of the converter.

A. STAGE 1 (t_0 TO t_1)
This operating stage occurs between t_0 and t_1 when S_1 and S_4 are closed. The resulting circuit is represented in Fig. 3(a). At t_0, i_{La} has reached its peak value, and between t_0 and t_1,
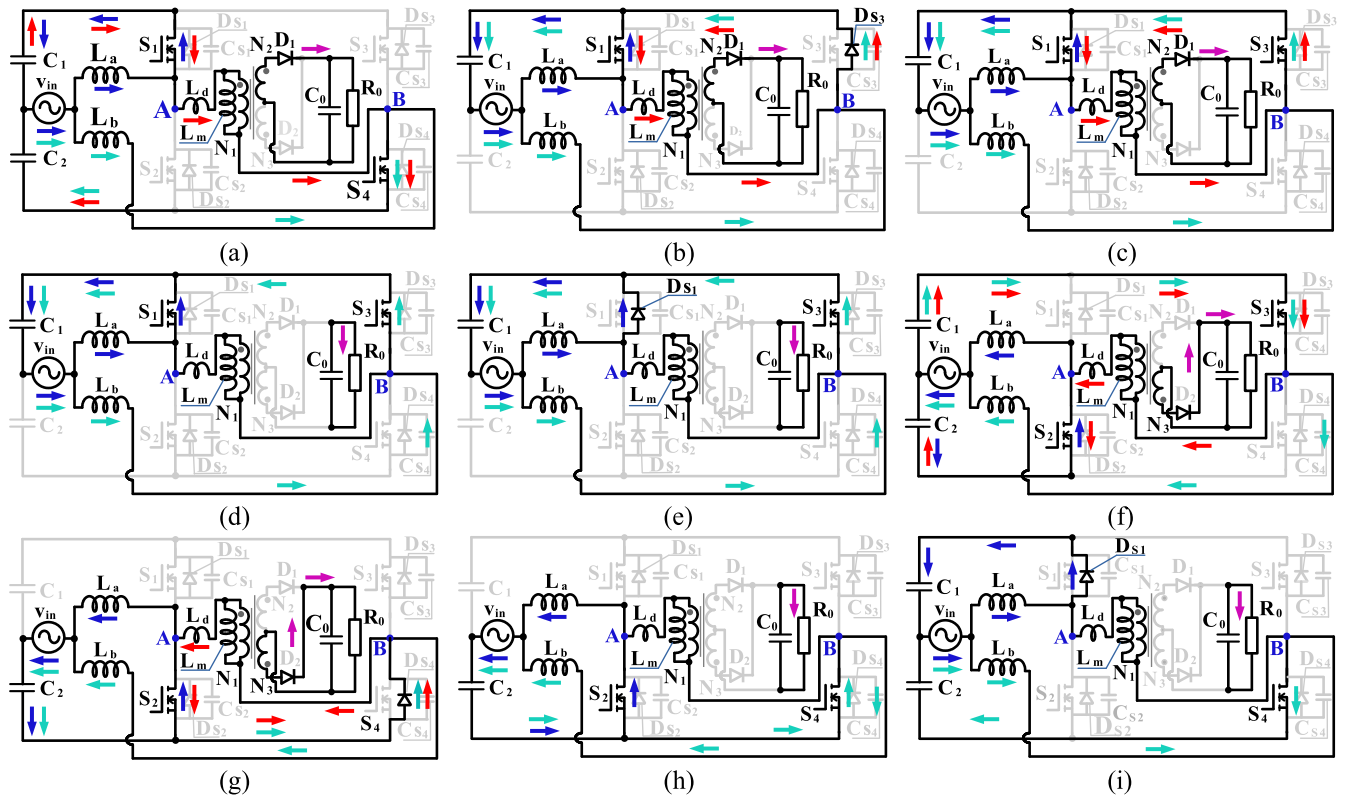
FIGURE 3. Operation stages of the proposed converter (positive half-cycle of v_{in}).

i_{La} decreases, and i_{Lb} increases linearly until it reaches its maximum value. In the same time interval, i_{Ld} increases from zero (t_0) to its peak value i_{Ldp} in t_1, as shown in the plot of Fig. 4. Currents i_{La} and i_{Lb} are equal in the module at the end of this stage, when S_4 is commanded to open at time t_1.

B. STAGE 2 (t_1 TO t_2)
This operating stage (Fig. 3(b)) occurs between the dead time instant t_{m12} (t_1 and t_2). The intrinsic diode D_{S3} enters conduction when S_4 opens at t_1 and remains conducting until S_3 closes in t_2. The current i_{Ld} decreases linearly according to the plot in Fig. 4.

C. STAGE 3 (t_2 TO t_3)
Switches S_1 and S_3 are closed in this operating stage, and the circuit configuration differs from the circuit of stage 2 only because i_{Lb} and i_{Ld} now circulate in S_3 instead of circulating in D_{S3}. The current i_{Ld} decreases linearly as in stage 2 until it reaches the zero value at t_3. Fig. 3(c) shows the equivalent circuit for this stage.

D. STAGE 4 (t_3 TO t_4)
The equivalent circuit for this operating stage is shown in Fig. 3(d) and occurs between t_3 and t_4. During this time interval, the current in capacitor C_1 remains in the same direction, indicating that it continues to receive the energy accumulated in the L_a and L_b. As the i_{Ld} is zero, the output rectifier bridge is open, and the load voltage is applied using C_0.
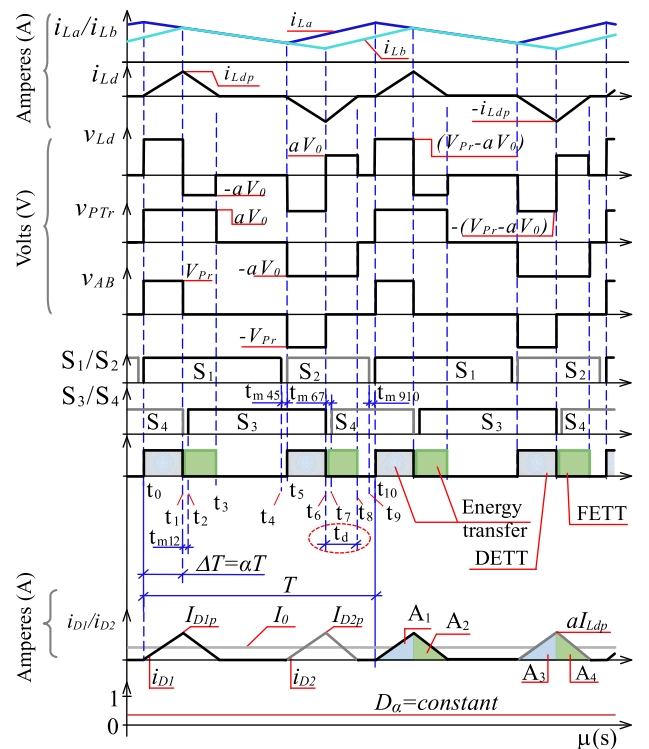

FIGURE 4. Main waveforms of the proposed AC-DC converter.

E. STAGE 5 (t_4 TO t_5)
At the instant of time t_4, when S_1 is commanded to open, the i_{La} that circulates in S_1 starts to circulate in D_{S1} and has its

minimum value reached at t_5. Capacitor C_1 continues to store energy from L_a and L_b. Fig. 3(e) shows the equivalent circuit.

F. STAGE 6 (t_5 TO t_6)

Switch S_2 closes at time t_5. Fig. 3(f) shows the equivalent circuit. The i_{La} starts to increase, and i_{Lb} decreases linearly until t_6. The inductance L_d is subjected to the voltage

$$v_{Ld} = -(V_{Pr} - aV_0). \tag{3}$$

Thus, i_{Ld} begins to decrease, reversing its direction, which leads to the conduction of D_2.

The current i_{La} increases from when S_2 is commanded to close (t_5), and i_{Lb} continues to decrease. Thus, L_a begins to store energy with the current circulating along the path indicated by the blue arrows in Fig. 3(f). The current in the L_b continues to decrease and supplies energy to capacitor C_1. This operating stage is completed at time t_6 when S_3 is commanded to open.

G. STAGE 7 (t_6 TO t_7)

This operating stage occurs between the moment of dead time t_{67} when only S_2 is closed, and i_{Lb} and i_{Ld} circulate in D_{S4}. The current i_{Ld} reaches its minimum value $-I_{Ldp}$ at t_6 and increases until t_7. Fig. 3(g) shows the equivalent circuit.

H. STEP 8 (t_7 TO t_8)

This operating stage occurs between t_7 and t_8 when L_d is completely discharged. Fig. 3(h) shows the equivalent circuit for this stage.

I. STAGE 9 (t_8 TO t_9)

This operating stage occurs between t_8 and t_9 when S_2 is commanded to open. In this stage, i_{Ld} is zero, and only i_{La} and i_{Lb} circulate, as shown in Fig. 3(i) with blue and cyan arrows, respectively. The voltage on the load is maintained with C_0. Switch S_1 is commanded to close at time t_{10}, indicating the beginning of the first stage again.

IV. ENERGY TRANSFER, STATIC GAIN, AND GLOBAL DUTY CYCLE

Fig. 4 shows the converter's switching for a certain instant of time included in a switching period T. The duty cycle of the two switches that make up each switching arm does not control the transfer of power but the phase shift between the commands of the two arms of the converter. Thus, the control of I_0 and V_0 is performed by decreasing or increasing this angle called α. This operating characteristic implies a converter with double modulation, the first coming from the PF correction of the two half-bridge converters operating together and the second referring to energy transfer and power decoupling.

At the bottom of Fig. 4, it is possible to verify the high-frequency waveforms of currents i_{D1} and i_{D2}, whose mean value is I_0. From the analysis of the stages, it is observed that i_{D1} and i_{D2} increase linearly in module from the time

instants t_0 to t_1 and t_5 to t_6. For these time intervals, i_{D1} is given by

$$i_{D1}(t) = \frac{V_{Ld}(t)}{L_d}\Delta T. \tag{4}$$

Substituting (3) into (4), results in

$$i_{D1}(t) = \frac{a(V_{Pr} - aV_0)}{L_d}\Delta T. \tag{5}$$

The time interval ΔT in (5) can be obtained with

$$\Delta T = \alpha T = D_\alpha. \tag{6}$$

Two complete energy transfers occur in a single period T. Therefore, ΔT is a time interval that depends only on D_α, as the switching frequency (F_S) is constant. The D_α value is between 0 and 1, and the value in degrees can be obtained by

$$D_\alpha(degress) = \frac{D_\alpha}{360^0}. \tag{7}$$

The plot at the bottom of Fig. 4 shows that D_α is represented with a constant value $D_\alpha = constant$, which makes the green and blue rectangles in the previous plot of the same figure with a fixed width over the period.

The time interval D_α is called direct energy transfer time (DETT), and the maximum value of i_{Ld}, i_{D2}, and i_{D2} occurs at the end of this time. The peak currents of i_{D1} and i_{D2} result in

$$I_{D1p} = I_{D2p} = \frac{a(V_{Pr} - aV_0)}{L_d}D_\alpha T. \tag{8}$$

The voltage v_{Ld} in stages 2, 3, 7, and 8 is equal, in module, to aV_0, and the decay time t_d highlighted in Fig. 4 with red ellipses is defined as free-energy transfer time (FETT) and is obtained by

$$t_d = \frac{L_d I_{D1p}}{a^2 V_0}. \tag{9}$$

Substituting (8) into (9), results in

$$t_d = \frac{(V_{Pr} - aV_0)}{aV_0}D_\alpha T. \tag{10}$$

The areas A_1/A_3 and A_2/A_4 in Fig. 4 are equal. Thus, the mean values of i_{D1} and i_{D2} result in the output current

$$I_0 = \frac{2(A_1 + A_2)}{T}. \tag{11}$$

Areas A_1 and A_2 can be obtained with (12) and (13).

$$A_1 = I_{D1p}D_\alpha T \tag{12}$$
$$A_2 = I_{D2p}t_d \tag{13}$$

Substituting (10), (12), and (13) into (11) and performing some mathematical manipulations

$$I_0 = \frac{2\left\{I_{D1p}D_\alpha \frac{T}{2} + I_{D2p}\left[\frac{(V_{Pr}-V_0).D_\alpha T}{2aV_0}\right]\right\}}{T}. \tag{14}$$

Equation (8), when substituted into (14), results in

$$I_0 = \frac{D_\alpha^2(V_{Pr}^2 - V_{Pr}V_0 a)}{F_S L_d V_0}. \tag{15}$$

Equation (15) can be rewritten in terms of the output power

$$P_0 = \frac{D_\alpha^2(V_{Pr}^2 - V_{Pr}V_0 a)}{F_S L_d}, \tag{16}$$

or rearranged to obtain the output voltage

$$V_0 = \frac{V_{Pr}}{a} - \frac{P_0 F_S L_d}{a D_\alpha^2 V_{Pr}}. \tag{17}$$

If $a = 1$ in (17), the maximum output voltage V_0 cannot reach the primary bus voltage V_{Pr} because there is a voltage drop for $0 < D_\alpha \le 1$ given by

$$\Delta V = \frac{P_0 F_S L_d}{a D_\alpha^2 V_{pr}}. \tag{18}$$

Dividing (17) by V_{Pr}, obtaining the static gain q_α defined by

$$q_\alpha = \frac{V_0}{V_{pr}} = \frac{1}{a} - \frac{P_0 F_S L_d}{a D_\alpha^2 V_{pr}^2}, \tag{19}$$

If $a = 1$ in (15) and using manipulation

$$\frac{(V_{Pr} - V_0)}{V_0} = \frac{(1 - q_\alpha)}{q_\alpha}, \tag{20}$$

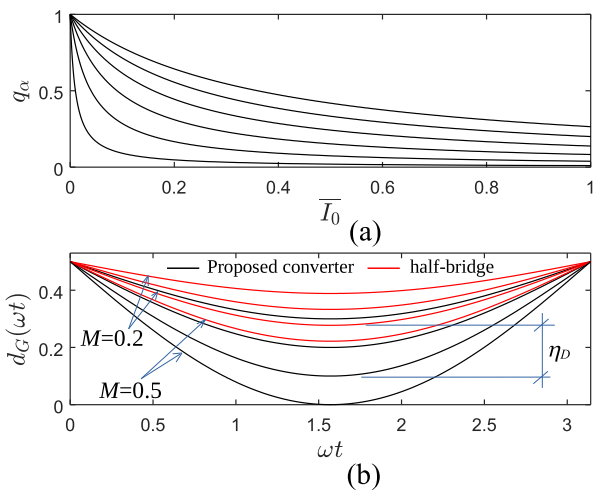the current I_0 can be rewritten in terms of q_α and results in

$$I_0 = \frac{(1 - q_\alpha)}{q_\alpha} \frac{D_\alpha^2 V_{pr}}{F_S L_d}. \tag{21}$$

The parameterized mean output current is defined as $\bar{I}_0$ (21), resulting in

$$\bar{I}_0 = I_0 \frac{F_S L_d}{V_{pr}} \Rightarrow \bar{I}_0 = D_\alpha^2 \frac{(1 - q_\alpha)}{q_\alpha}. \tag{22}$$

Fig. 5(a) shows the graphical result of (22).

(a)

(b)

FIGURE 5. (a) Parameterized mean output current for the proposed. (b) Differences between the duty cycles of the proposed converter ($a=1$, D_α = constant, and $D_\alpha \ne 0$) and the half-bridge converter.

The static gain between the input source v_{in} of the converter and the primary bus given by the voltage V_{Pr} is the static gain q_{H_B} of the half-bridge PFC converter and given by

$$q_{H\_B} = \frac{V_{pr}}{v_{in}} = \frac{2}{1 - 2D_{H\_B}}. \tag{23}$$

Isolating V_{Pr} from (23) and substituting in (17), we obtain

$$V_0 = \frac{2v_{in}}{(1 - 2D_{H\_B})a} - \frac{P_0 F_s L_d}{2v_{in} D_\alpha^2}(1 - 2D_{H_B}). \tag{24}$$

Dividing all terms of (24) by v_{in} and considering $P_0 = V_0^2/R_0$, the global static gain defined by q_G results in

$$q_G = \frac{V_0}{V_{in}} = \frac{2}{(1 - 2D_{H\_B})a} - \frac{P_0 F_s L_d}{2v_{in}^2 D_\alpha^2}(1 - 2D_{H\_B}), \tag{25}$$

which can be rewritten as

$$q_G = \left(\frac{2}{(1 - 2D_{H\_B})}\right)\left[\left(\sqrt{1 + \frac{4\gamma}{a D_\alpha^2}} - 1\right)\frac{D_\alpha^2}{2\gamma}\right], \tag{26}$$

where $\gamma = L_d F_s / R_0$. Equations (23) and (26) differ only due to the term in square brackets of (26).

Inserting v_{in} in the sinusoidal form in (26) allows the isolation of D_{H_B}, which results in the duty cycle of the proposed converter, named $d_G(\omega t)$.

$$d_G(\omega t) = 0.5 - M\sin(\omega t)\left\{\frac{D_\alpha^2}{2\gamma}\left(\sqrt{1 + \frac{4\gamma}{D_\alpha^2 a^2}} - 1\right)\right\}, \tag{27}$$

where $M = V_P/V_0$ is the modulation index, and V_P is the peak voltage of v_{in}. The duty cycle for the half-bridge converter given by $d_{H\_B} = 0.5 - M\sin(\omega t)$ differs from (27) due to the term between braces. This term is called the effective loss of duty cycle, designated by

$$\eta_D = \frac{D_\alpha^2}{2\gamma}\left(\sqrt{1 + \frac{4\gamma}{D_\alpha^2 a^2}} - 1\right). \tag{28}$$

The resulting curves for different values of M in (27) and $d_{H\_B} = 0.5 - M\sin(\omega t)$ can be seen in the plot of Fig. 5(b).

The curves in Fig. 6(b) show the behavior of the maximum and minimum values of $d_G(\omega t)$ as a function of η_D, D_α, and different M values. The peak-to-peak value of $d_G(\omega t)$ is reduced as M decreases.

The vertical distance difference between the curves of both converters for the same M value is the effective loss of the duty cycle defined in (28), whose graphical result is shown in Fig. 6(a).

An indetermination in (27) with $D_\alpha \to 0$ shows that the converter starts to operate as a half-bridge if there is no power transfer between the primary bus and the converter output. In practice, one possibility is to start the converter with a load on the primary bus, transfer power to the converter output, and remove the load from the primary bus, if necessary.
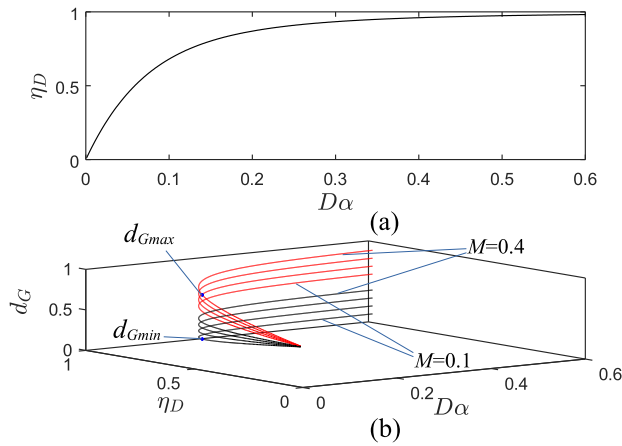
FIGURE 6. (a) Effective loss of the duty cycle. (b) Variation of the proposed converter duty cycle for different M values.

V. OPERATING LIMITS

To understand the operating limits of the converter, the following analyses considered the instantaneous value of $d_G(\omega t)$, and the lag between arms 1 and 2 of the converter was admitted as the value α $(0<\alpha<1)$. Figs. 7(a), (b), (d), and (e) are the currents i_{D1} and i_{D2} at four different points of $d_G(\omega t)$, the latter shown in Fig. 7(c).
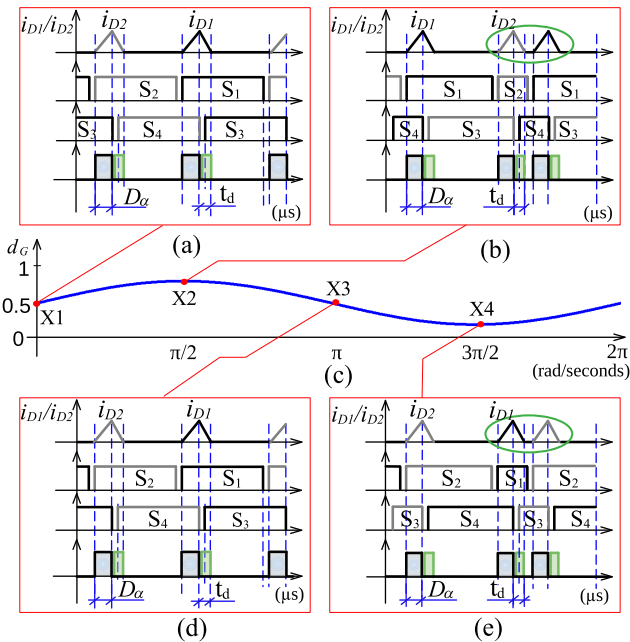

FIGURE 7. (a), (b), (d), (e) Current waveforms in diodes D$_1$ and D$_2$ and switching of S$_1$, S$_2$, S$_3$, and S$_4$ at high frequency. (c) Duty cycle waveform $d_G(\omega t)$.

The duty cycle of both switching arms is 0.5 at point X$_1$ of Fig. 7(c) when $\omega t=0$ but lagged of D_α. For this condition, i_{D1} and i_{D2} are far apart, as shown in Fig. 7(a). i_{D1} and i_{D2} approach each other when $d_G(\omega t)$ reaches its maximum value at point X$_2$, as highlighted in the green ellipse in Fig. 7(b). Currents in the diodes start moving away again at point X$_3$ of

$d_G(\omega t)$ (Fig. 7(d)), and again i_{D1} and i_{D2} approach each other when $d_G(\omega t)$ reach its minimum value at X$_4$, as highlighted in Fig. 7(e). The non-complete extinction of the i_{Ld} before a new transfer of energy causes the interference of energy transfer called by I$_{TE}$.

There are two ways for I$_{TE}$ to occur, the first resulting from an L$_d$ designed with a very high value so that the current in the device does not reach zero before a new energy transfer cycle. The second form of I$_{TE}$ occurs with an excessive increase in D_α, which causes the same effect mentioned earlier. Fig. 7(c) shows that it may happen for values close to $\omega t = \pi/2$ and $\omega t = 3\pi/2$ of $d_G(\omega t)$.

The two operating limits are presented as

$$\begin{cases} I_{TE1} \Rightarrow L_d > L_{dmax} \\ I_{TE2} \Rightarrow D_\alpha > D_{\alpha max}, \end{cases} \quad (29)$$

that is, there is a maximum value for L$_d$, and the converter cannot reach the $D_{\alpha max}$ value under operation.

A. I$_{TE1}$ DUE TO L$_d$ $_{max}$

The maximum inductance is obtained from the condition

$$d_G T > D_\alpha T + t_d, \quad (30)$$

considering V_{Pr}, V_0, and P_0 constant. Substituting (10) into (30), the maximum series inductance results in

$$L_d < \frac{V_{pr}^2 D_\alpha^2 (d_G - D_\alpha)}{P_0 F_S d_G}, \quad (31)$$

which can be rewritten as follows when parameterized

$$\overline{L_{dmax}} < L_d \frac{P_0 F_S}{V_{pr}^2} \frac{D_\alpha^2 (d_G - D_\alpha)}{d_G}. \quad (32)$$

The plot in Fig. 8(a) presents the parameterized series inductance values for different D_α values. For instance, the two red curves in this figure result from (32), considering the maximum and minimum value of (27), with D_α varying from 0 to 0.9. $D_\alpha=0.1$ is highlighted in the zoom of the figure and results in two inductance values, $\overline{L_{d1}}$ and $\overline{L_{d2}}$. Thus, $\overline{L_{dmax\_}}$ must be projected using $d_{Gmin}(\omega t)$ in (32).

B. I$_{TE2}$ DUE TO D$_\alpha$ $_{max}$

I$_{TE2}$ is obtained by replacing t_d in condition (30), which results in

$$D_\alpha < d_G a q_\alpha. \quad (33)$$

Equation (33), the smallest value of $d_G(\omega t)$. In the left graph of Fig. 8(d), a section of $d_G(\omega t)$ is shown. In the same figure on the left, it is possible to observe in a representative way and highlighted in the red ellipse, that a new transfer of energy caused in the closing of the switches S$_2$ and S$_3$ occurs with non-zero current in diode D$_1$ (Fig. 8(b)). This fact causes a voltage $V_{Ld} = - (V_{Pr} + aV_0)$ at the moment of energy transfer (Fig. 8(c)) that distorts i_{Ld} and v_{Ld} and causes different descent times t_d and called in Fig. 8(b) by t$_{d'}$ e t$_{d''}$. This causes distortion of I$_0$ and V$_0$ of the converter.
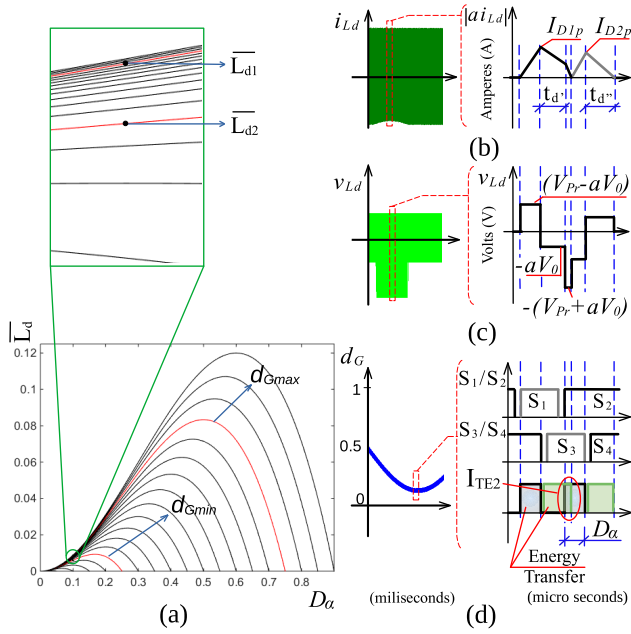
FIGURE 8. (a) I_{TE1} operating limit due to L_d inductance. (b), (c) and (d): I_{TE2} operating limit due to increased D_α.

The distortion in V_{Ld} (Figure 8(c) makes the average value of i_{Ld} no longer zero, which causes overheating in T_r, loss of efficiency, and damage to the converter.

VI. CONTROL STRATEGY

The control system is shown in Fig. 9 and comprises four control loops, three for voltage and one for current.

The signals i_{La}, i_{Lb}, v_{in}, V_{Pr}, V_0, and v_m are needed, the latter the average voltage at the central point between C_1 and C_2 (node 0 in Fig. 2). The entire control system is digital and signals of current and voltage are conditioned and filtered before going to the DSP (digital signal processor).

A. GENERAL OPERATION OF THE CONTROL SYSTEM

The Voltage Loop V_{Pr} is the primary bus voltage control loop responsible for generating the reference signal amplitude for i_{La} and i_{Lb}. The i_{in_ref} signal that comes out of the $C_{VPr}(s)$ controller can be added to a fixed value close to V_{Pr} and called by F_{d_VPr} (feedforward V_{Pr}), which makes the response of this control loop faster. Voltage control on C_1 and C_2 is performed with the control loop **Voltage Loop Balance v_{C1} and v_{C2}**. This loop controls possible voltage differences in C_1 and C_2. The $C_{VBL}(s)$ controller generates the B_L signal.

The signals from the $C_{iLa}(s)$ and $C_{iLb}(s)$) controllers can be added to the feedforward signals obtained in **Feedforward i_{La} and i_{Lb}**, which reduces the computational effort [31]. The V_{mod_La} and V_{mod_Lb} signals are compared with the Triangular Carrier 1 and Triangular Carrier 2, resulting in the switch activation signals (V_{gS1} to V_{gS4}).
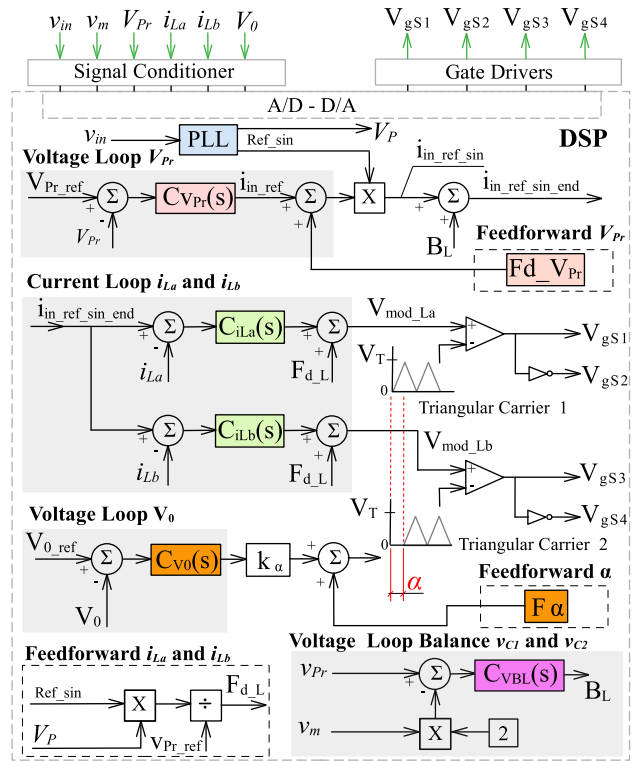

FIGURE 9. Control strategy of the proposed AC-DC converter.

B. OUTPUT VOLTAGE CONTROL AND POWER DECOUPLING

By replacing $P_0 = V_0^2/R_0$ in Equation (19), the static gain q_α results in

$$q_\alpha = \frac{D_\alpha^2}{2\gamma}\left(\sqrt{a^2 + \frac{4\gamma}{D_\alpha^2}} - a\right). \tag{34}$$

The power transfer between the primary bus and the converter output in (34) does not depend on the PFC duty cycle; that is, the power transfer to the converter output is a function only of D_α and $\gamma = constant$.

Fig. 10 shows the result of q_α as a function of D_α for typical values of γ and transformation ratio a. The plotted curve in Fig. 10 presents a saturation behavior with the increase of D_α.
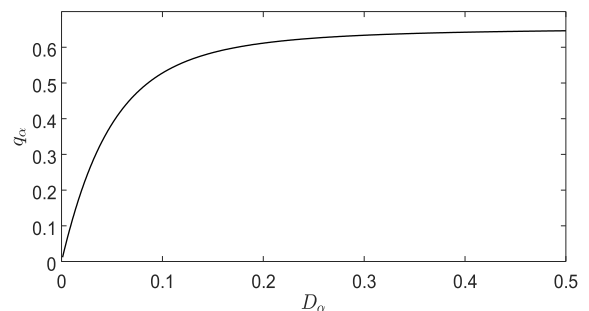

FIGURE 10. Static gain q_α between the primary bus and the output voltage of the proposed converter.
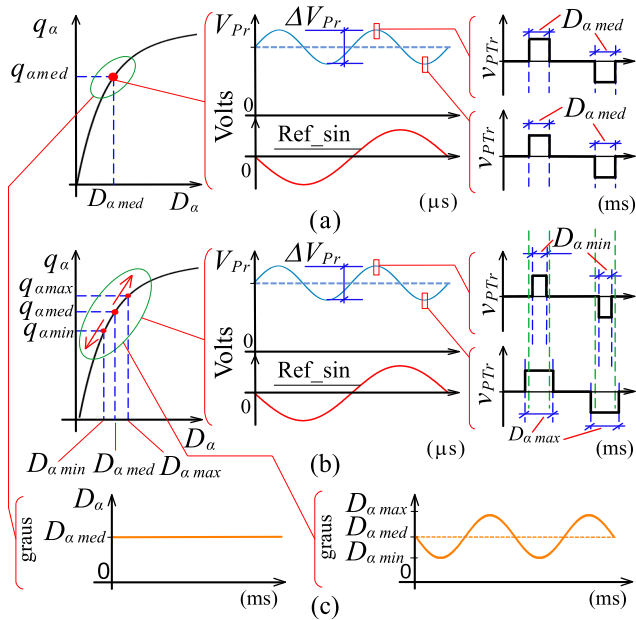
FIGURE 11. Operation of the output voltage control loop of the proposed converter.

Therefore, the converter needs to work with low D_α values to allow energy transfer to the converter output and not reach the I_{TE2} shown in Section V.

The input current control is independent of D_α, enabling the insertion of a second modulation to correct the V_0 ripple.

Fig. 9 shows that the **Voltage Loop V$_0$** control loop has a block called k_α, which converts the signal from the controller $C_{V0}(s)$ and shifts Triangular Carrier 2 relative to Triangular Carrier 1.

The central curves of Fig. 11(a) and (b) show the voltage waveforms in V_{Pr}, the ripple ΔV_{Pr}, and the input reference voltage v_{in}. The voltage on the primary of the transformer, which reflects its secondary, is given by

$$v_{PTr} = V_{Pr} - v_{Ld}. \qquad (35)$$

The voltage on the primary of the V_{PTr} transformer (Fig. 11(a)-right) has a fixed width $D_\alpha(t) = D_{\alpha\,med}$ over time regardless of the ΔV_{Pr} ripple reaching the maximum or minimum value. Therefore, if the converter is operated in this way, we will have a fixed q_α gain, the V_0 control loop will be deactivated, and the 120 Hz ripple of the primary bus will be transferred to the converter output.

On the other hand, if the $C_{V0}(s)$ controller starts to operate in the control system with $k_\alpha \neq 0$, the signal coming from it increases or decreases the angle D_α as variations in the output voltage occur. For instance, the controller decreases α if V_{Pr} reaches the maximum value and, consequently, v_{PTr} and V_0. D_α increases if V_{Pr} reaches its minimum value. Fig. 11(b) on the left shows the result of D_α variation for maximum and minimum points of V_{Pr}. Thus, $D_\alpha(t)$ now has a mean value $D_{\alpha\,med}$ added to a sinusoidal function and 180 degrees out of phase with the primary bus voltage ripple (see Fig. 11(c) on

the right), which results in

$$D_\alpha(t) = D_{\alpha\,med} - A\sin(2\omega t), \qquad (36)$$

where A is the amplitude of the sinusoidal function and (36) is the second modulation of the converter that starts to operate with the variable q_α, increasing and decreasing its value according to the indicative arrows in Fig. 11(b) on the left.

The operation of the converter with fixed and constant $D_{\alpha\,med}$ (Fig. 11(c) on the left) is the same as that conducted on the full-bridge DC-DC converter presented by [32]. The second modulation described in (36) does not change the issues of switching under zero voltage (ZVS) of the converter presented in [32]. Therefore, the proposed converter inherits characteristics regarding ZVS, but it is not addressed in this study.

VII. SIMULATION AND EXPERIMENTAL RESULTS
Simulation and experimental results obtained from a 1 kW prototype are shown below.

A. SIMULATION RESULTS
Table 1 shows the specifications of components used in the simulation and the developed prototype. The plots in Fig. 12 show the simulation results for the proposed converter. Fig.12(a) shows that FP is practically unitary, which implies the effective control of PFC. The maximum input current ripple is observed in this figure.

The voltage waveform V_{Pr} is shown in Fig. 12(b), and the output voltage V_0 and the signal $D_\alpha = constant$ are shown in Fig. 12(c) and Fig. 12(e). The V_0 ripple still exists for $D_\alpha = constant$. $D_\alpha(t)$ becomes the function described in (36) (Fig. 12(f)) and the ripple of V_0 is eliminated, as shown in

TABLE 1. Parameters for simulation and experimental prototypes.

Name	Description	Value	Unit
v_{in}	Input Voltage	100	Volts RMS
i_{in}	Input Current	10	Amperes RMS
f_r	Grid Frequency	60	Hz
f_s	Switching Frequency	43.2	kHz
V_{Pr}	Primary Bus Voltage	550	V
V_0	Output Voltage	250	V
P_0	Output Power	1,0	kW
R_0	Load Resistance	62.5	Ω
$L_a = L_b$[b]	Input Inductors	1.5	mH
$C_1 = C_2$[b]	Primary Bus Capacitors	940	μF
C_0[b]	Output Capacitor	66	μF
a[a]	Ratio Transformation of T_r	26/17	turns
L_m	Transformer Magnetization Inductance	1.47	mH
L_{disp}	Transformer Dispersion Inductance	10	μH
L_s	Series Inductance	5.7	μH
L_d	Total series Inductance ($L_{disp}+L_S$)	15.7	μH

[a] $a=(N_1/N_2)=(N_1/N_3)$, where N_1, N_2, N_3 are number of turns in the primary, secondary, and tertiary of the T_r.
[b] L_a, L_b, C_1, and C_2 obtained with: $\Delta_{in} = 30\%$; $\Delta V_{Pr} = 2\%$. ΔV obtained from [34] without power decoupling and $\Delta V_0 = 2\%$.
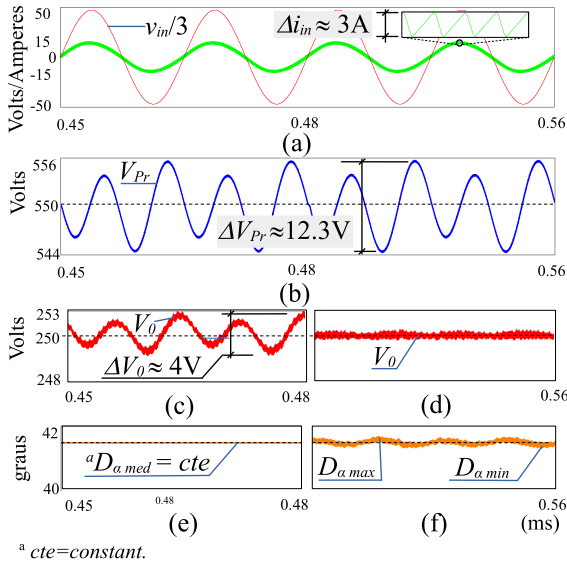
FIGURE 12. Simulation results for the proposed converter.

1: DSP
2: Switches S_1 to S_4
3/4: Capacitance C_1/C_2
5/6: Inductance L_a/L_b
7: Inductance L_d
8: Transformer T_r
9: Diodes D_1/D_2
10: Capacitance C_0

FIGURE 13. Prototype of the proposed converter.

Fig. 12(d), with the connection of the output voltage control loop.

B. EXPERIMENTAL RESULTS

Table 2 shows the specifications of the components used in the prototype, as shown in Fig. 13.

TABLE 2. Prototype component specifications.

Component	Specification
Switches S_1 to S_4	(SiC C2M0025120D)
Input Inductors L_a and L_b	1.5mH, Magnetic Cor EE65/33/26 Thorton, 2x(75 turns Litz 50x34AWG)
Transformer T_r	1kW, Magnetic Cor EE65/33/39 Thorton, Primary 2x(26 turns Litz 50x34AWG), Secondary and Tertiary 3x(17 turns Litz 50x34AWG)
Capacitors C_1 and C_2	B4345A9477M 470µF, 450V, Epcos
Output Capacitor C_0	(DC 450V 66uF 17-27X) Panasonic
Series Inductance L_s	5.7µH, Magnetic Cor EE42/21/15 Thorton, 3x(14 turns Litz 50x34AWG)
Rectifier diodes D_1 and D_2	(IDH16G65C5 Infineon)
Digital Signal Processor (DSP)	MC56F84763V Freescale

Fig. 14(a) shows the v_{in} and i_{in} waveforms for the converter operating at rated power. There is practically no delay between the waveforms, indicating a high PF. The waveforms i_{La} and i_{Lb} are shown in Fig. 14(b) and indicate the halving of i_{in} in the two arms of the converter.

If the converter operates with the control loop of the output voltage V_0 turned off, with a $D_{\alpha\,med} = constant$, the ripple in V_{Pr} is transferred to the primary of the transformer and consequently, to the output voltage V_0. Fig. 15(a) shows only the AC coupling of voltages V_{Pr} and V_0 for this case. The plot of Fig. 15(b) shows that the ripple at 120 Hz is eliminated when the V_0 voltage control system is activated.
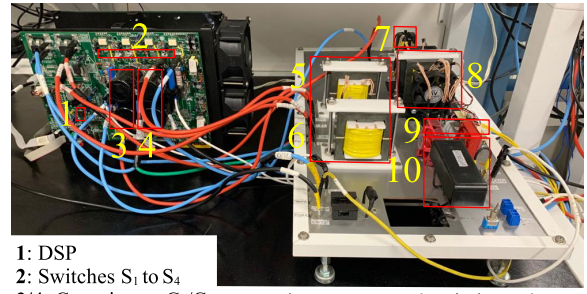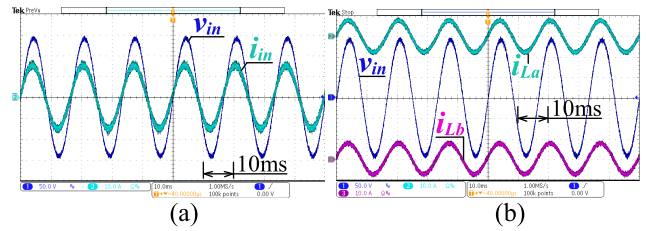

FIGURE 14. (a) v_{in} - 50V/div and i_{in} - 10A/div with the converter operating at rated power. (b) v_{in} - 50V/div and i_{La} and i_{Lb} - 10A/div with the converter operating at rated power.
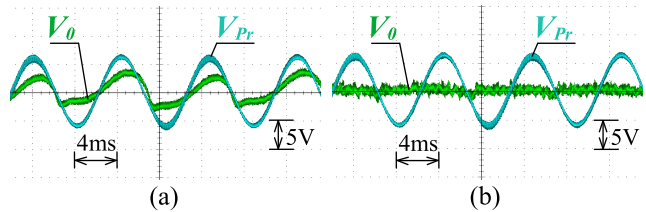

FIGURE 15. (a) V_{Pr} and V_0 with $D_{\alpha\,med} = constant$ with the V_0 control system deactivated. (b) V_{Pr} and V_0 with the V_0 control system activated.

The curves in Fig. 16(a) show the dynamic responses of the control systems with the converter initially processing 750 W and a step of 250 W. The primary bus voltage loop is slow, and this response was intentionally chosen because the system where DPS is located has filters to eliminate electromagnetic interference on the primary bus (maximum of 630 V).

The transient response is almost imperceptible because the V_0 output voltage loop can be fast enough to eliminate ripple at 120 Hz. Although the input current i_{in} amplitude comes from the voltage control loop V_{Pr}, the current i_{in} oscillates
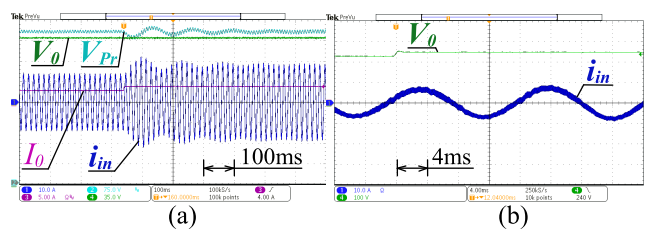

FIGURE 16. (a) Waveforms for a 25% load step (V_{Pr} - 75V/div; V_0 - 35V/div; i_{in} - 10A/div; I_0 - 5A/div). (b) Step from 225V to 250V at V_0 voltage reference (i_{in} - 10A/div; V_0 - 100V/d).

TABLE 3. Performance comparison table.

Converter	Nominal power v_{in}/V_0	Power Switches S/D/NT	Isolation	Sensor Current	Components CDCL / CR / C0 / LR	Soft commutation	Maximum efficiency (%)
Converter in [23]	1 kW 110 V_{rms} / 400 V	4/6/10	Y^{2W}	1	17 µF / 68 µF / 1500 µF / 37 µH	Y	94.8
Converter in [24]	1 kW 110 V_{rms} / 200 V	6/0/6	N	1	10 µF / N / N / N	N	92.5
Converter in [29]	6.6 kW 220 V_{rms} / 450 V	8/8/16	Y^{2W}	2	240 µF / N / 20 µF / 10 µH	N	-
Converter in [19]	0.45 kW 110 V_{rms} / 60 V	4/6/10	N	1	180 µF / N / N / 5mH	N	90
Converter in [35]	1 kW 120 V_{rms} / 350 V	6/0/6	N	1	180 µF / N / N / 1mH	N	95
Proposed Converter	1 kW 100 V_{rms} / 250 V	4/2/6	Y^{3W}	2	470 µF / N / 66 µF / 5µH	Y	93.2

S=Switch; D=Diode; CDCL= DC Link Capacitor; CR= Series Capacitor; LR= Series Inductor; C0=Output Capacitor; NT=Total Power Switches; 2W=2 windings; 3W=3 windings; Y=Yes; N=No.
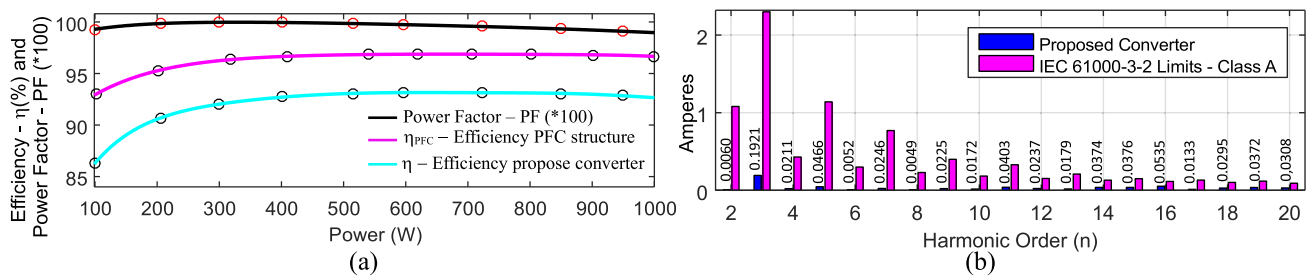

FIGURE 17. Efficiency and power factor of the proposed converter. (b) Nominal input current harmonic spectrum.

and goes into a steady state, keeping FP close to unity. Fig. 16(b) shows the actuation speed of the V_0 control loop for a step in the V_0 reference voltage with a load of 500 W.

Fig. 17(a) shows the efficiency and FP of the proposed converter. Fig. 17(b) shows the harmonic components of the nominal input current and their comparison with the IEC 61000-3-2 Limits – Class A standard. Table 3 compares the proposed converter topology and other topologies in the literature.

VIII. CONCLUSION

The converter topology proposed in this work is isolated and based on the half-bridge converter. The control system corrects the PF, allowing power decoupling and output voltage control without adding circuit components. The equation presents a detailed converter design, showing its practical operating limits. Simulation and experimental results with a 1 kW prototype are presented, highlighting the high efficiency (93%) and reduced number of components compared to other topologies in the literature. In addition, the converter also complies with the IEC 61000-3-2 Limits - Class A standard.

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