RESEARCH ARTICLE

Modified Discontinuous Pulsewidth Modulation Approach With Independent Phase Loss Adjustment for Voltage Source Converters

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ABSTRACT This paper presents an efficient independent phase switching loss reduction technique for 2-level 3-phase voltage source inverters. A modified carrier-based pulse-width modulation algorithm, named per-phase discontinuous pulse-width modulation, is used to generate various non-switching intervals for the phase leg having the worst aging state by injecting a proper zero-sequence voltage to reference voltages. The non-switching intervals result in keeping a specific phase leg from switching to decrease the switching frequency and corresponding loss. The careful determination of variable clamping intervals aims to achieve a desirable decrease in the per-phase switching frequency of 2-level 3-phase voltage source inverters while ensuring that the output performance is not much degraded. The decrease in switching frequency and corresponding switching loss exerts a positive impact on the thermal stress of power semiconductor devices, resulting in improving the reliability of voltage source inverters. To evaluate the performance of the proposed method, the conventional carrier-based space vector modulation, 3-phase generalized discontinuous pulse-width modulation, and a discontinuous pulse-width modulation using hybrid offset voltage are implemented along with the proposed method. The accuracy and efficiency of the proposed method are validated using both simulation and experimental data.

INDEX TERMS Lifetime, voltage source inverter, discontinuous pulse-width-modulation, loss reduction, reliability.

I. INTRODUCTION

It is quite unusual to come across an electrical energy system that does not make use of power electronics in today's world. High power density, high efficiency, low cost, and small size are the criteria used to evaluate commercial power electronics converters. However, maintaining reliability in these power converters can cause difficulty while attempting to achieve these characteristics because it has an impact on their price

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and lifetime [1], [2], [3]. This is especially true for a renewable energy system that works in harsh environments.

Because power devices are the most vulnerable components in power electronic systems, component reliability is a crucial factor in many failures or faults [4], [5]. Consequently, the lifetime of these components significantly influences the reliability and availability of power electronics systems. Temperature-related aging failure is one of the power switch failure mechanisms. Thermal stress accounts for 60% of the failures in a power semiconductor device, according to [6] and [7]. Thus, it can be shown that the temperature of power semiconductor devices, which is a result of energy loss during

operation, has a significant impact on the converter's lifetime and reliability. Bond-wire fatigue, for example, is one of the primary failure mechanisms in insulated-gate bipolar transistors (IGBTs) devices produced by cycling fluctuations in junction temperature (T_j) and temperature difference (ΔT_j) [8]. Improving component reliability by controlling the power loss of semiconductor devices is, hence, an indirect method of enhancing the reliability of power converters.

Switching loss of power semiconductor devices is primarily influenced by switching frequency, which is a loss-dependent characteristic. In general, the junction temperature of a converter is often adjusted using the switching frequency, but this approach can negatively impact the output performance in lower-level systems [9]. For a 2-level inverter used in an adjustable speed drive application, a switching frequency reduction strategy based on the junction temperature variation was proposed in [10]. The fundamental idea behind the well-known discontinuous pulse-width-modulation (DPWM) [11], [12], [13] strategy is to clamp the reference voltage to upper or lower dc-rail for a specific duration. By doing so, the corresponding power switch will not change its state, effectively reducing switching loss during that period. During clamping period, reduced power loss of device leads to a decrease in both the mean value and variance of junction temperature. In [14], a hybrid modulation controller selects between SVPWM and DPWM and reduces switching frequency according to the device degradation level to reduce the thermal stress of converter. Other output power-based thermal control techniques were investigated in [15] and [16]. These techniques lessen power loss by adjusting the output power in each power system cell in accordance with the state of aging. Although the goal of thermal control methods, such as reducing switching frequency, modifying the modulation strategies, and adjusting output power, is to increase the lifetime of power devices and corresponding systems, these methods should account for the associated costs and achieve a balance between them.

Potential failure sources for power semiconductor devices have been identified, including manufacturing methods [17]. It causes a typical distortion in the components' quality, which causes various aging situations. Additionally, this may be impacted by unequal stress or previous failures in one of them, such as the replacement of a defective component. Nevertheless, the previously mentioned active thermal control methods fail to consider the possibility that the converter's phase legs might experience different aging states, thus not fully enhancing the overall reliability of the converter. Another technique for controlling switching loss at the device level is existing gate control. Loss is influenced by gate voltage and driving resistance; the link between gate voltage, resistor, and power device lifetime has been determined based on a precise field mission profile [18]. The output current ripple of the converter is unaffected by gate control; however, gate control does necessitate an extra circuit. This increases the complexity of the system. Saturation voltage and switching loss are both influenced by the gate drive voltage. As a result, the loss of power devices can be regulated. The on-state resistance and power losses of power transistors tend to rise when their operating temperature rises. Hence, it is advised to compensate for this by increasing the amplitude of the applied driving level [19]. However, this technique's need for exact control of the voltage level makes it impractical. Additionally, the author in [20] proposed a control scheme for a 3-phase 4-wire converter. The objective of this approach is to regulate the output power of each phase leg based on its individual aging condition. However, that method is limited due to the converter structure. Recently, a DPWM technique using hybrid offset voltage to lower switching loss in the phase leg having the worst aging condition is proposed in [21]. In this DPWM hybrid offset method, the load output currents are used to determine the non-clamping and clamping regions, where both generated offset voltage of space vector PWM (SVPWM) and generalized DPWM (GDPWM) are respectively injected. However, due to using output currents to determine the non-clamping and clamping regions without considering the reference voltages, this method is not effective at large load angle conditions (low power factor). Another attempt in [22] develops a model predictive control (MPC) scheme with offset voltage injection in predicted reference voltage to generate a non-switching interval for the phase leg having the worst aging state. Although this per-phase MPC scheme can attain minimum switching loss for the phase leg having the worst aging state by generating a total of 240° clamping region, it increases switching frequency in remaining phases results in higher switching loss.

It can be seen that only limited research has been carried out to increase the reliability of converters with active thermal control, which aims at reducing the power loss and corresponding junction temperature of specific phase leg or semiconductor devices during operation while limiting the additional losses using a modified modulation control strategy. A per-phase DPWM strategy for precise control of individual phase switching frequency to reduce corresponding switching loss, which can be achieved as the proper zero-sequence voltage (ZSV) is added to the modulation signal while maintaining good output performance for 2-level 3-phase voltage source inverter (VSI). To address the reliability of the VSIs, each phase of the converter is expected to have a different aging state. This method reduces the switching loss of the phase leg having the worst aging state in the 2-level 3-phase VSI, which increases the corresponding lifetime in phase leg and entire VSI. The differences and advantages of the proposed method include:

(1) Control switching loss of the most aged leg instead of entire converter.

(2) Achieving minimum switching loss in the most aged leg by generating a total of 240° clamping interval (equal to a two-third fundamental cycle) instead of only 120° clamping interval as in conventional DPWM methods. Hence, the switching frequency reduction obtained by the proposed
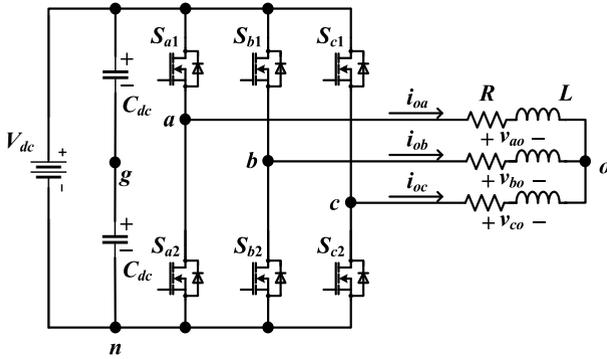
FIGURE 1. 2-level 3-phase VSI with RL load circuit diagram.

per-phase DPWM method in a particular phase leg can reach to about 67% instead of 33% in conventional DPWM methods. Additionally, this is effective at any load conditions.

(3) The proposed method guarantees the output performance of 2-level 3-phase VSI not too much degraded (i.e., total harmonic distortion (THD)) by combining both SVPWM and DPWM in ZSV generation. Meanwhile, the conventional 3-phase DPWM notably reduces the output performance of VSI.

(4) The proposed method does not require additional hardware and is straightforward to implement in a practical system.

The proposed per-phase DPWM approach is validated for its precision and effectiveness through both simulation and experimental tests. The evaluation and comparison of proposed per-phase DPWM method compared to conventional SVPWM, 3-phase GDPWM, and DPWM hybrid offset [21] techniques are included to verify the corresponding advantages of proposed approach.

II. CONVENTIONAL CBPWM FOR VSI

Fig. 1 depicts a 2-level 3-phase VSI in which the neutral point n is isolated, preventing the presence of a neutral current route. The inverter voltage, $v_{xn}(x = a, b, c)$, is the voltage at the phase x terminal with respect to the negative dc bus n. When the upper switch S_{a1} is ON, and the lower switch is OFF, leading to $v_{xn} = V_{dc}$. On the other hand, when the upper switch S_{a1} is OFF, and the lower switch is ON, leading to $v_{xn} = 0$. Hence, the inverter voltage can be described as

$$v_{xn} = S_{x1} \times V_{dc} \tag{1}$$

where S_{x1} equals to 1 or 0, which corresponds to ON-state and OFF-state of upper switch, respectively.

In terms of common-mode voltage, the common-mode voltage v_{CMV} is defined as the voltage v_{og} between the neutral point o of load and the middle-point g of the dc-link voltage in VSI. The common-mode voltage can be written with the terminal voltages with respect to the mid-point of the dc-link
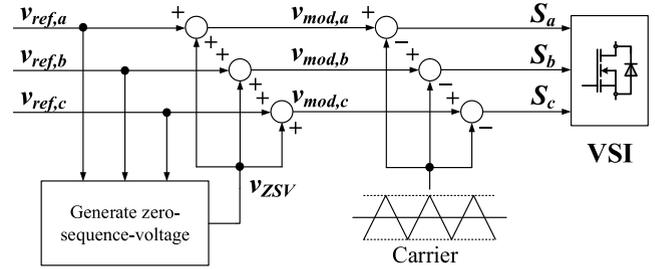
FIGURE 2. Block diagram of CBPWM.
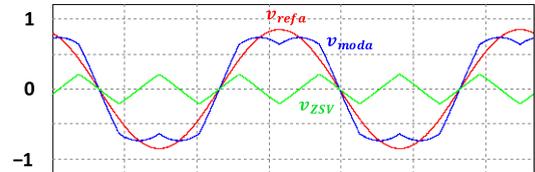
FIGURE 3. Waveforms of a normalized reference voltage, ZSV, and generated modulation signals of SVPWM.

voltage as

$$v_{\text{CMV}} = \frac{v_{ag} + v_{bg} + v_{cg}}{3} \tag{2}$$

As a result, in the case of CBPWM implementation, different types of ZSVs can be injected to the reference modulation waves, as shown in Fig. 2.

In the CBPWM methods, the non-sinusoidal modulation signal (v_{modx} ($x = a, b, c$)) can be expressed as follows:

$$\begin{cases} v_{moda} = v_{refa} + v_{ZSV} \\ v_{modb} = v_{refa} + v_{ZSV} \\ v_{modc} = v_{refa} + v_{ZSV} \end{cases} \tag{3}$$

where v_{refa}, v_{refb}, and v_{refc} are the sinusoidal reference signals and v_{ZVS} is the ZSV signal. The sinusoidal reference voltage signal can be expressed as follows:

$$\begin{cases} v_{refa} = V_{ref} \cos(2\pi f t) \\ v_{refb} = V_{ref} \cos(2\pi f t - 2\pi/3) \\ v_{refc} = V_{ref} \cos(2\pi f t + 2\pi/3) \end{cases} \tag{4}$$

where V_{ref} is the magnitude of the reference voltage signal, f is the fundamental frequency.

Sinusoidal PWM (SPWM) is the oldest and most popular PWM scheme for 3-phase VSIs. The SPWM approach compares three pure sinusoidal modulation signals with a triangular carrier waveform, and the result is a null ZSV signal.

$$v_{ZSV_{[\text{SPWM}]}} = 0 \tag{5}$$

However, a number of PWM techniques have been proposed in an effort to improve the under-utilization of dc-link voltage as a result of the issue. In this instance, the ZSV signal is altered to improve the voltage linearity of modulator.

The SVPWM approach is another popular modulation method [23]. As illustrated in Fig. 3, it is well known that for carrier-based modulation, the addition of ZSV, v_{ZSV} selected as (6) to the sinusoidal reference signals places the nonzero voltage vector (effective voltage vector) in the middle of a sampling period. When compared to the SPWM approach, it offers an optimal switching sequence, which has several benefits, including lower harmonic currents and a higher available modulation index.

$$v_{ZSV[SVPWM]} = -\frac{V_{max} + V_{min}}{2} \tag{6}$$

$$V_{max} = \max\left(v_{refa}, v_{refb}, v_{refc}\right) \tag{7}$$

$$V_{min} = \min\left(v_{refa}, v_{refb}, v_{refc}\right) \tag{8}$$

To reduce the switching loss of VSI, a carrier-based modulation named DPWM is widely used [11]. Only two phases are modulated in discontinuous modulation, while the third phase is clamped to either the positive $V_{dc}/2$ or negative $-V_{dc}/2$ rails. It is preferable to have the most current flowing through since the phase that is clamped has no switching losses. Thus, the GDPWM [12], [13] is based on both inverter reference voltage v_{refa}, v_{refb}, v_{refc} and the inverter output current i_{oa}, i_{ob}, i_{oc} to achieve optimal clamping intervals corresponding to the highest load current. Depending on whether the leg conducts a greater output current, the GDPWM will specify the maximum reference voltage V_{max} and minimum reference voltage V_{min}, which being clamped to positive or negative dc-rail. To avoid changing the state in the phase leg conducts the largest output current, modified modulation waves are generated by the reference voltage signal with injected ZSV. The ZSV is calculated as follows:

$$\begin{cases} v_{ZSV[GDPWM]} = \dfrac{V_{dc}}{2} - V_{max} & \text{if } |i_{max}| \geq |i_{min}| \\ v_{ZSV[GDPWM]} = -\dfrac{V_{dc}}{2} - V_{min} & \text{if } |i_{max}| < |i_{min}| \end{cases} \tag{9}$$

where i_{max} and i_{min} are the maximum and minimum values of reference output currents or measured output currents, respectively. As depicted in Fig. 4, the clamping region of modulation signal v_{moda} is corresponding to the highest value of phase a current.

III. PROPOSED PER-PHASE DPWM FOR INDEPENDENT SWITCHING LOSS REDUCTION METHOD

The previous sections show how various CBPWMs could be implemented through the addition of a ZSV signal in a VSI. Although the DPWM strategies significantly decrease the switching loss in converters, the output performance would be degraded because of switching frequency reduction. As indicated earlier, the producing techniques, uneven stress, and prior replacement might lead to different aging states among the legs of 3-phase VSIs. On the other hand, the useful lifetime of the VSI is detected based on the lifetime of most aged semiconductor devices. It means that when a semiconductor device is broken, the VSI will stop working. Therefore, in order to increase the lifetime of VSI or avoid
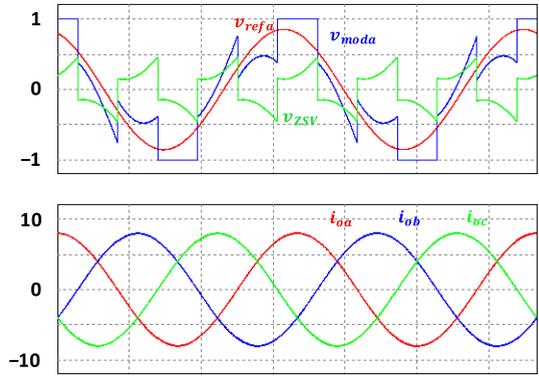
FIGURE 4. Waveforms of normalized reference voltage, ZSV, generated modulation signals, and output currents in GDPWM.
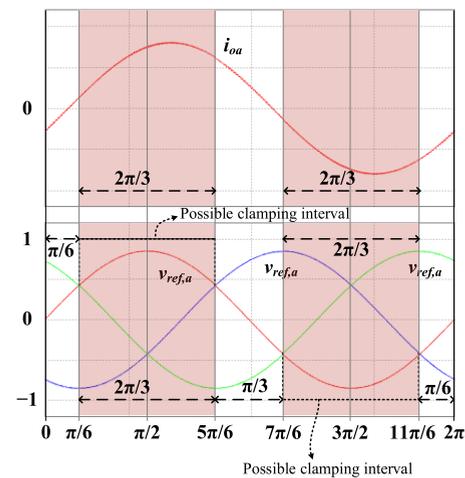
FIGURE 5. Possible clamping intervals in case phase a is phase leg having the worst aging state.

as much as failure in the most aged semiconductor devices, a modified CBPWM method based on DPWM for per-phase switching frequency control is proposed whereby the phase leg having the worst aging state is operated under lower switching frequency to improve its lifetime.

The basic idea of the proposed per-phase DPWM method is only generating non-switching intervals for the phase leg having the worst aging state, whereas the two remaining ones keep switching normally. This allows both to lower switching frequency of the phase leg having the worst aging state and not affect the output performance too much. To implement the proposed scheme, in the non-switching interval of the phase leg having the worst aging state, the ZSV signal related to the DPWM is injected into the reference voltages of both 3-phase legs of VSI. Meanwhile, in the switching interval, the ZSV signal calculated as in SVPWM is added to guarantee the output performance. It should be noted that the ZSV is injected during the non-switching interval of positive and negative dc-rail to ensure even loss distribution in the phase leg.

Assuming that phase a is phase leg having the worst aging state, Fig. 5 depicts the possible clamping intervals for phase a. Fig. 5 illustrates the phase a output current and

normalized reference voltages of 3-phase legs. The red parts indicate the possible clamping interval where the semiconductor devices are not switching or keeping the previous state of phase a, while the remaining parts indicate the impossible clamping intervals. As shown in Fig. 5, the maximum possible non-switching angle θ_{n_sw} is $120°(2\pi/3)$. During each clamping (non-switching) interval, the upper (lower) switch is clamped to the ON state. It results in the reduction of the corresponding switching frequency. Additionally, due to the clamping interval of 120° includes the time that phase a current with the largest magnitude is conducted, the corresponding switching loss of phase a is significantly reduced. The non-switching angle can be varied from 0° to 120°, where 0° is equivalent to continuous modulation. In this study, continuous modulation is considered as SVPWM. The variable clamping (non-switching) intervals can be calculated and determined by using the instantaneous value of phase reference voltage as follows:

$$\begin{cases} v_{refa} \geq V_{ref}\cos\left(\dfrac{\theta_{n\_sw}}{2}\right) \\ v_{refa} \leq -V_{ref}\cos\left(\dfrac{\theta_{n\_sw}}{2}\right) \end{cases} \quad (10)$$

By varying the value of the non-switching angle from 0° to 120°, the corresponding width of the non-switching interval will be changed consequently. Apparently, the highest θ_{n_sw} at 120° will decrease the most switching loss. This makes a critical difference between the proposed method and previous conventional 3-phase DPWM and recent per-phase DPWM methods, where the clamping interval is limited to 60°. From (8), the ZSV can be generated for per-phase control as follows:

$$\begin{cases} v_{ZSV[perphaseDPWM]} = \dfrac{V_{dc}}{2} - v_{refx} \text{ if } v_{refx} \geq V_{ref}\cos\left(\dfrac{\theta_{n\_sw}}{2}\right) \\ v_{ZSV[perphaseDPWM]} = -\dfrac{V_{dc}}{2} - v_{refx} \text{ if } v_{refx} \leq -V_{ref}\cos\left(\dfrac{\theta_{n\_sw}}{2}\right) \\ v_{ZSV[perphaseDPWM]} = -\dfrac{V_{max} + V_{min}}{2} \text{ other cases} \end{cases} \quad (11)$$

At the clamping (non-switching) interval, the ZSV is produced according to (11), whereas at the switching interval, the ZSV is calculated using SVPWM. For example, $\theta_{n\_sw} = 60°$, the phase a reference voltage v_{refa}, the generated ZSV v_{ZSV}, and the resulting modulation signal of phase av_{moda} are shown in Fig. 6. The red parts indicate the 60° clamping interval, whereas the white parts indicate the non-clamping interval.

Fig. 7 illustrates the flow diagram detailing the generation of the ZSV in the proposed approach. First, the maximum reference voltage and minimum voltage are determined at every sampling instant. The magnitude of the reference voltage is calculated for the determination of the non-switching interval by comparing the instantaneous value of reference voltage and the predefined value based on the desired non-switching angle. The determined conditions will specify the particular value of the ZSV. As indicated in (11), during the
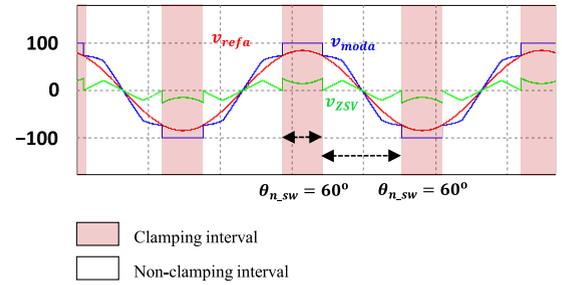
FIGURE 6. Waveforms of normalized reference voltage, ZSV, and generated modulation signals in proposed method with $\theta_{n\_sw} = 60°$.
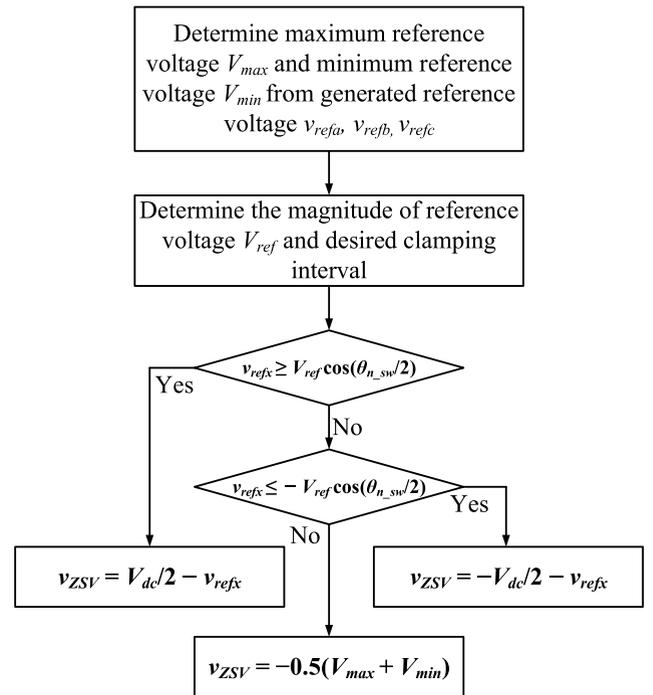
FIGURE 7. Flow chart of ZSV generation of the proposed method.

non-switching interval, the ZSV takes values of $(V_{dc}/2 - v_{refx})$ or $(-V_{dc}/2 - v_{refx})$. On the other hand, during the switching interval, the ZSV is determined using SVPWM and is calculated as $-0.5(V_{max} + V_{min})$.

Fig. 8 illustrates the block diagram of the proposed per-phase DPWM with ZSV generation. The differences between measured phase currents and corresponding reference currents are sent to proportional-integral (PI) controllers to produce the reference voltage. The generated ZSV v_{ZSV} is injected to reference voltages to produce modulation voltage signals, which will be compared with the carrier signal to produce a switching pattern for each phase.

IV. VERIFICATION RESULTS
A. SIMULATION RESULTS
Simulations were conducted in PSIM software to validate the proposed technique. As depicted in the previous section, the 2-level 3-phase VSI is connected to $R-L$ load, which is
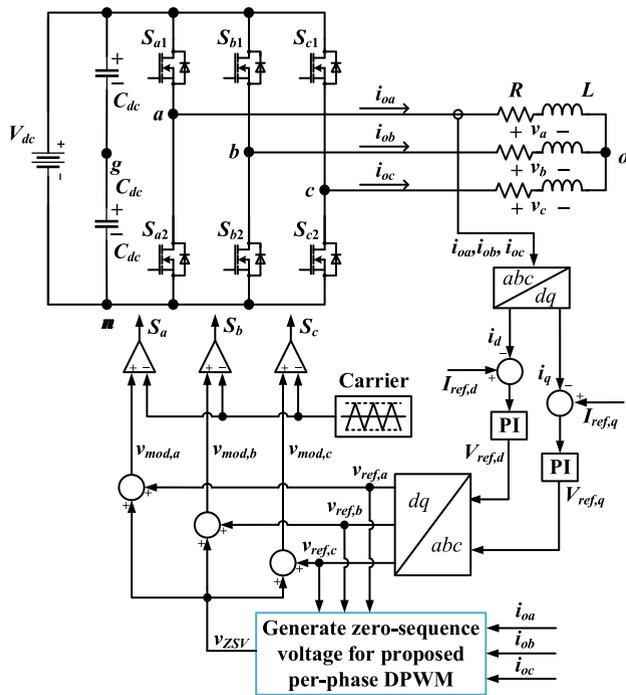
FIGURE 8. Proposed per-phase DPWM approach's control diagram.

TABLE 1. 2-level 3-phase VSI parameters.

Parameters	Value
dc input voltage V_{dc} (V)	200
dc-link capacitance (µF)	680
Load inductor L_f (mH)	10
Load resistor R (Ω)	10
Carrier frequency (kHz)	20

modeled in PSIM software. The parameters of 2-level 3-phase VSI are listed in Table 1.

Fig. 9(a) – (d) shows the simulated waveforms obtained by proposed approach at various non-switching angles, where the output currents, generated ZSV signal and modulation signals, and corresponding switching pattern waveforms in phase *a* are shown. Output current waveforms at various non-switching angles exhibit sinusoidal characteristics and accurately maintain the appropriate magnitude and phase. It can be seen from the switching signal in phase *a*, the proposed per-phase DPWM scheme prevents upper and lower switches of phase *a* from switching at different non-switching intervals thanks to the clamping period of modulation signal. Meanwhile, in phases *b* and *c*, the modulation signals do not contain clamping period. At switching intervals, switches are operated normally as in SVPWM scheme. The magnitude of the non-switching interval increases when the non-switching angle rises. Fig. 9(d) shows that the highest non-switching angle at 120° can keep the switches of phase *a* from switching for the longest time, resulting in a significant reduction of switching frequency and switching loss.

Fig. 10 shows the change in output performance following the increase of non-switching angle, ranging from 0°

to 120°. The non-switching angle at 0° is equivalent to the continuous modulation, which is SVPWM in this case. In Fig. 10(a), the change in phase *a* load current THD and average THD of VSI are shown as the non-switching angle increases. Regarding phase *a* load current THD, it increases from 0.37% at continuous modulation to 0.61% at 120° non-switching angle. The percentage increase is about 64%. In terms of average THD, at 0° non-switching angle or continuous modulation, both 3-phase legs are operated at the same switching frequency, which results in the same load current THD among three phases and average value. The average THD also increases following the rise of the non-switching angle but with a smaller amount due to the two remaining phases being operated with the same switching frequency as continuous modulation. It allows for reducing the degradation of VSI output performance. At 120° non-switching angle, the average THD increases by about 40% compared with continuous modulation. Fig. 10(b) and (c) show the change of power loss as the non-switching angle rises. Fig. 10(b) shows the conduction and switching losses in phase *a*. It can be seen that the conduction loss of phase *a* slightly increases when the non-switching angle increases. At 120° non-switching angle, the conduction loss of phase *a* is 7.42W, which is equivalent to about a 5% increase. Meanwhile, the switching loss sharply decreases as the non-switching angle increases. In continuous modulation, phase *a* switching loss is extremely high at 20.54W. However, at 120° non-switching angle, it decreases by approximately 80% at 4.24W. The total loss of VSI, as shown in Fig. 10(c), decreases by about 20% at 120° non-switching angle compared with the continuous modulation.

To evaluate the correct operation of the proposed per-phase DPWM approach, it will be compared to conventional SVPWM method and DPWM hybrid offset method [21] in terms of output performance and switching loss reduction capability. Fig. 11 shows the simulation result of the SVPWM method, DPWM hybrid offset method, and the proposed method. For comparison purposes, the proposed approach will be applied with a maximum non-switching angle of 120° while it is 60° for DPWM hybrid offset scheme. Additionally, phase *a* is assumed to have the worst aging condition. The waveforms of output currents, modulation signal and ZSV, and corresponding switching patterns of both three phases are presented. In Fig. 11(a), the simulation waveforms of the continuous modulation scheme SVPWM method are presented. The output currents exhibit sinusoidal characteristics and accurately maintain the appropriate magnitude and phase. It can be seen that the switches of both 3-phase legs are continuously switching without a non-switching interval. Fig. 11(b) presents the simulation results of the DPWM hybrid offset method. The output currents exhibit sinusoidal characteristics and accurately maintain the appropriate magnitude and phase, as in the SVPWM method. As presented in Fig. 11(b), the modulation signal of phase *a* includes the clamping region because of the ZSV signal injection. It leads to the switches in phase *a* not changing its state during the non-switching interval. In Fig. 11(c), the
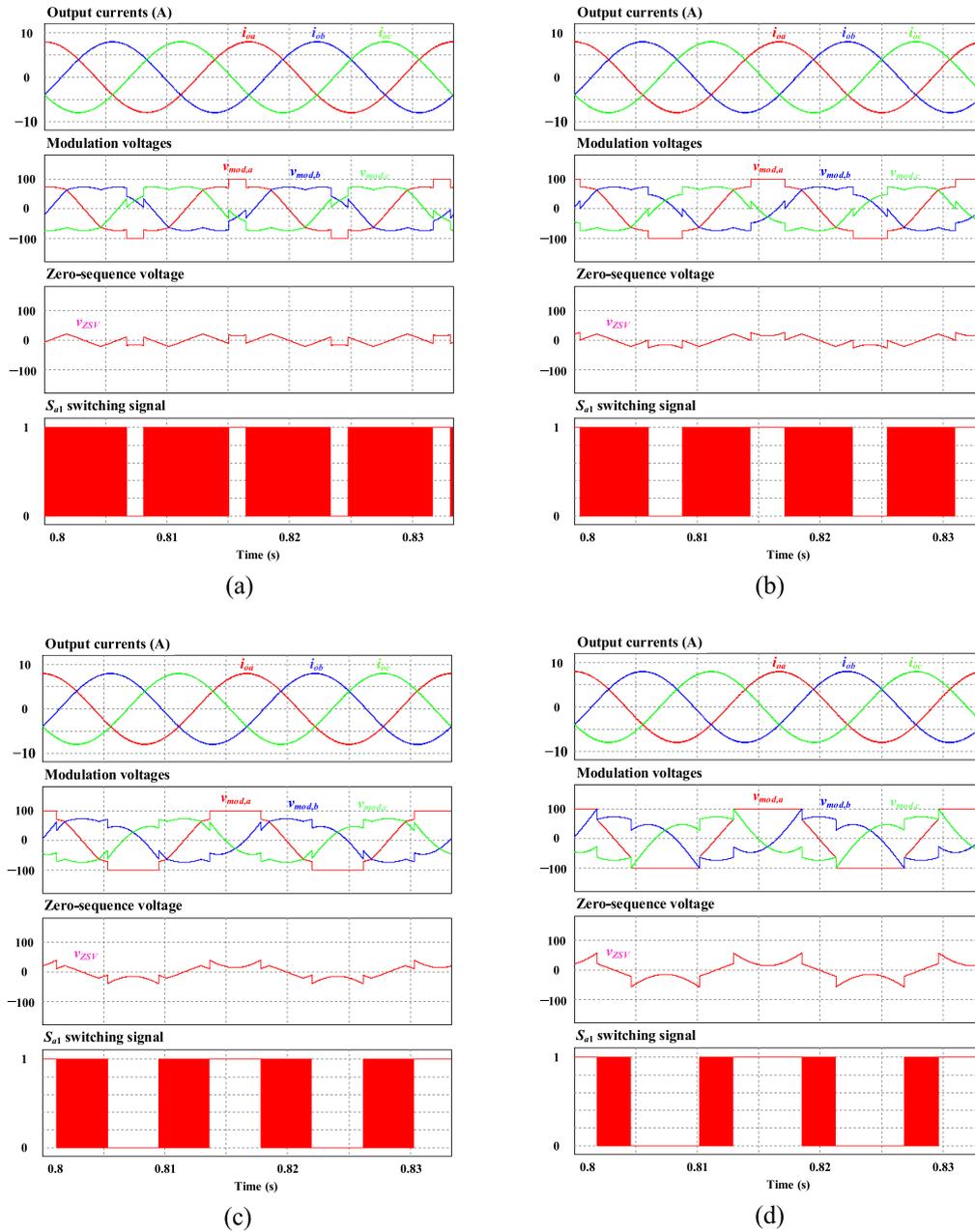
FIGURE 9. Simulation waveforms of output currents, reference voltage, modulation signal, ZSV signal, and switching pattern acquired by the proposed per-phase DPWM approach with different non-switching angles (a) $\theta_{n\_sw} = 30°$, (b) $\theta_{n\_sw} = 60°$, (c) $\theta_{n\_sw} = 90°$, (d) $\theta_{n\_sw} = 120°$.

simulation waveforms obtained by the proposed method are presented. The output currents exhibit sinusoidal characteristics and accurately maintain the appropriate magnitude and phase, which is similar to the two previous control schemes. Differently, thanks to using 120° non-switching angle, the proposed approach maintains phase a switching state for a longer time than the DPWM hybrid offset method. The switching signal of phase a matches the clamping region of the corresponding modulation signal. Meanwhile, the two remaining phases have continuous switching patterns, as in the SVPWM method. It can be seen that the proposed method

is working properly by generating the desired non-switching interval.

Fig. 12 shows the simulation waveforms of inverter voltages and line-to-line voltages. The obtained inverter voltages from both three control schemes have two levels correctly, V_{dc} and 0. However, due to the different switching patterns in phase a, the waveform of corresponding inverter voltage acquired by DPWM hybrid offset and proposed per-phase DPWM methods contains clamping regions, where the inverter voltage level is unchanged for a period of time. Regarding the line-to-line voltage, the obtained line-to-line

(a)

(b)

(c)
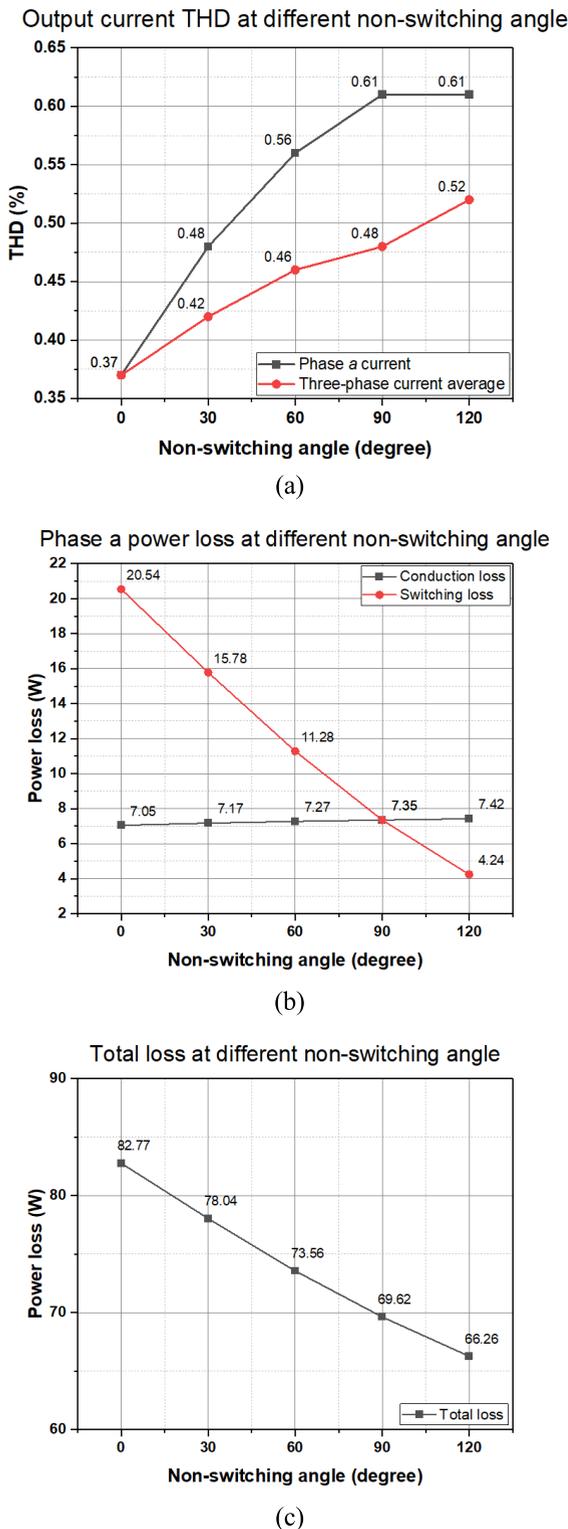
FIGURE 10. (a) Load current THD, (b) Phase *a* conduction and switching losses, (c) Total loss acquired by proposed per-phase DPWM approach at various non-switching angles.

voltages from both three control schemes correctly have three levels, V_{dc}, 0, and $-V_{dc}$.

The waveforms of common-mode voltage and corresponding spectrum obtained by three control schemes are given

in Fig. 13. As in Fig. 13(a), (b), and (c), the common-mode voltages obtained by three approaches have the same peak-to-peak magnitude, which equals to V_{dc}. As can be seen in the spectrums, the common-mode voltages from all these three methods contain both low-frequency and high-frequency harmonic components. The high-frequency components are centered around the integer multiples of the carrier frequency, whereas three methods have certain third harmonic components in the common-mode voltage waveforms.

B. EXPERIMENT RESULTS

The experiment was implemented to validate the proposed method in comparison with the SVPWM and DPWM hybrid offset methods. The picture of the experimental setup is shown in Fig. 14. The setup is realized with the same parameters as in the simulation section. The control algorithm is implemented and executed using a Texas Instrument TMS320F28335 digital signal processor (DSP).

The experiment results of output currents and modulation signal of phase *a* obtained by SVPWM, DPWM hybrid offset, and proposed per-phase DPWM method are presented in Fig. 15(a) – (c). The 120° non-switching angle is used to implement the proposed method. It can be seen that the experimental results are compatible with the simulation waveforms in the previous section. The output currents achieved through all three control schemes exhibit sinusoidal characteristics and accurately maintain the appropriate phase and magnitude.

Fig. 16 presents the output current, the modulation signal, and the corresponding switching pattern of phase *a* acquired by both three approaches. Similar to the simulation results, the switches of phase *a* are continuously switching in SVPWM method. The switching pattern of phase *a* is matched to the modulation signal in both DPWM hybrid offset and proposed per-phase DPWM method, as shown in Fig. 16(b) and (c), respectively. As observed, the non-switching interval generated by the proposed per-phase DPWM method is larger than that of the DPWM hybrid offset method, thanks to the use of 120° non-switching angle.

The experiment results validate the accuracy of the proposed per-phase DPWM technique, demonstrating its effective ability to lower switching frequency of a particular phase leg while maintaining the output performance not degraded.

C. PERFORMANCE EVALUATION

To verify the performance of the proposed per-phase DPWM method, this section compares and evaluates the calculated data from simulation by conduction SVPWM, 3-phase GDPWM, DPWM hybrid offset schemes along with the proposed per-phase DPWM approach.

The total harmonic distortion (THD) percentage is defined as

$$\%\text{THD} = \frac{\sum_{x=a,b,c}\sqrt{i_{ox2}^2 + i_{ox3}^2 + \dots + i_{oxn}^2}}{\sum_{x=a,b,c} i_{ox1}} \times 100 \quad (12)$$
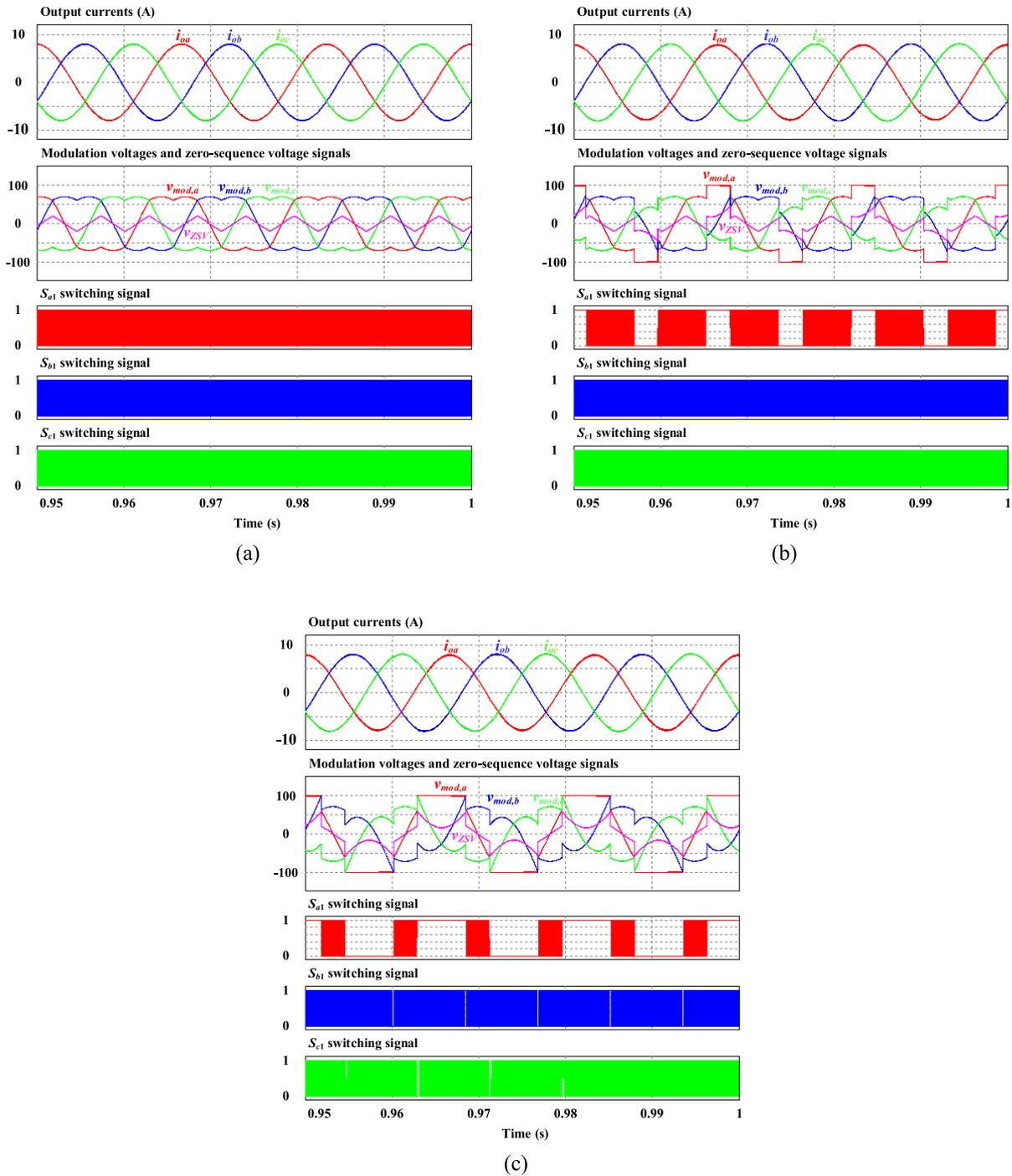
FIGURE 11. Simulation results of output currents, reference voltage, modulation signal, ZSV signal, and switching pattern obtained by (a) SVPWM, (b) DPWM hybrid offset, (c) proposed per-phase DPWM.

where i_{ox1} and i_{oxn} are the fundamental and n^{th}-harmonic components of the output current in phase x, respectively. The number n is set to 10000 in the simulation.

In terms of power losses of switching devices, the calculation of the losses in this study is based on previous work in [24]. The conduction loss, averaged over a switching period, can be calculated by

$$P_{\text{cond,IGBT}} = v_{ce}(i) \times i \times d_{\text{IGBT}} \qquad (13)$$

$$P_{\text{cond,Diode}} = v_f(i) \times i \times d_{\text{Diode}} \qquad (14)$$

where v_{ce} and v_f are the on-state voltage that is a function of the current and is estimated on the basis of datasheet curves, i is the current through the component, and d is the duty cycle.

The switching loss can be calculated by

$$P_{\text{sw,IGBT}} = \left(E_{\text{on,IGBT}} + E_{\text{off,IGBT}}\right) \times f_{sw} \qquad (15)$$

$$P_{\text{sw,Diode}} = \left(E_{\text{on,Diode}} + E_{\text{off,Diode}}\right) \times f_{sw} \qquad (16)$$
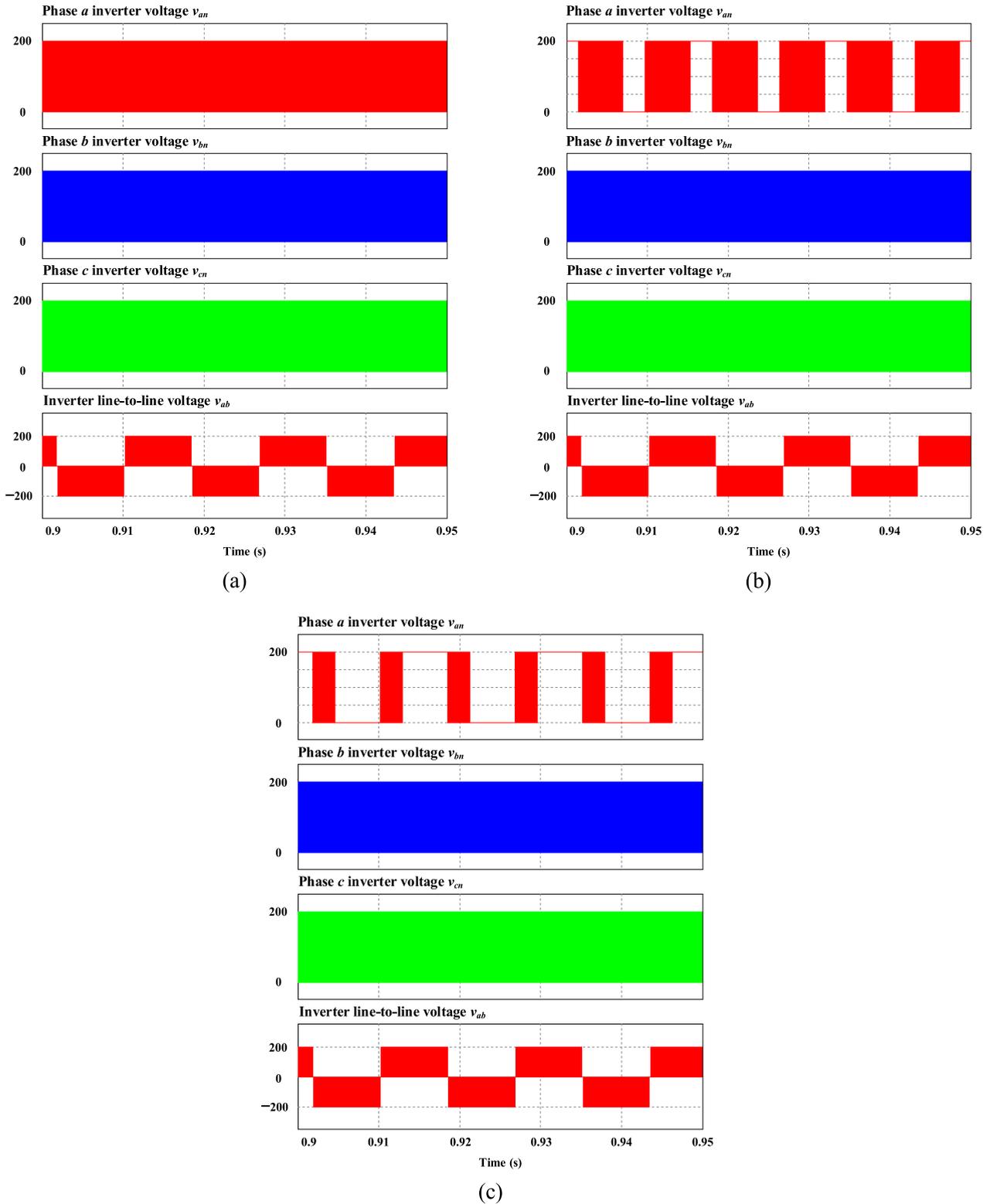
FIGURE 12. Simulation results of inverter voltages and line-to-line voltage obtained by (a) SVPWM, (b) DPWM hybrid offset, (c) proposed per-phase DPWM.

where E_{on} and E_{off} are the switching energies for the components that are a function of the current through the component and the switched voltage and are estimated using datasheet curves, and f_{sw} is the switching frequency of the component.
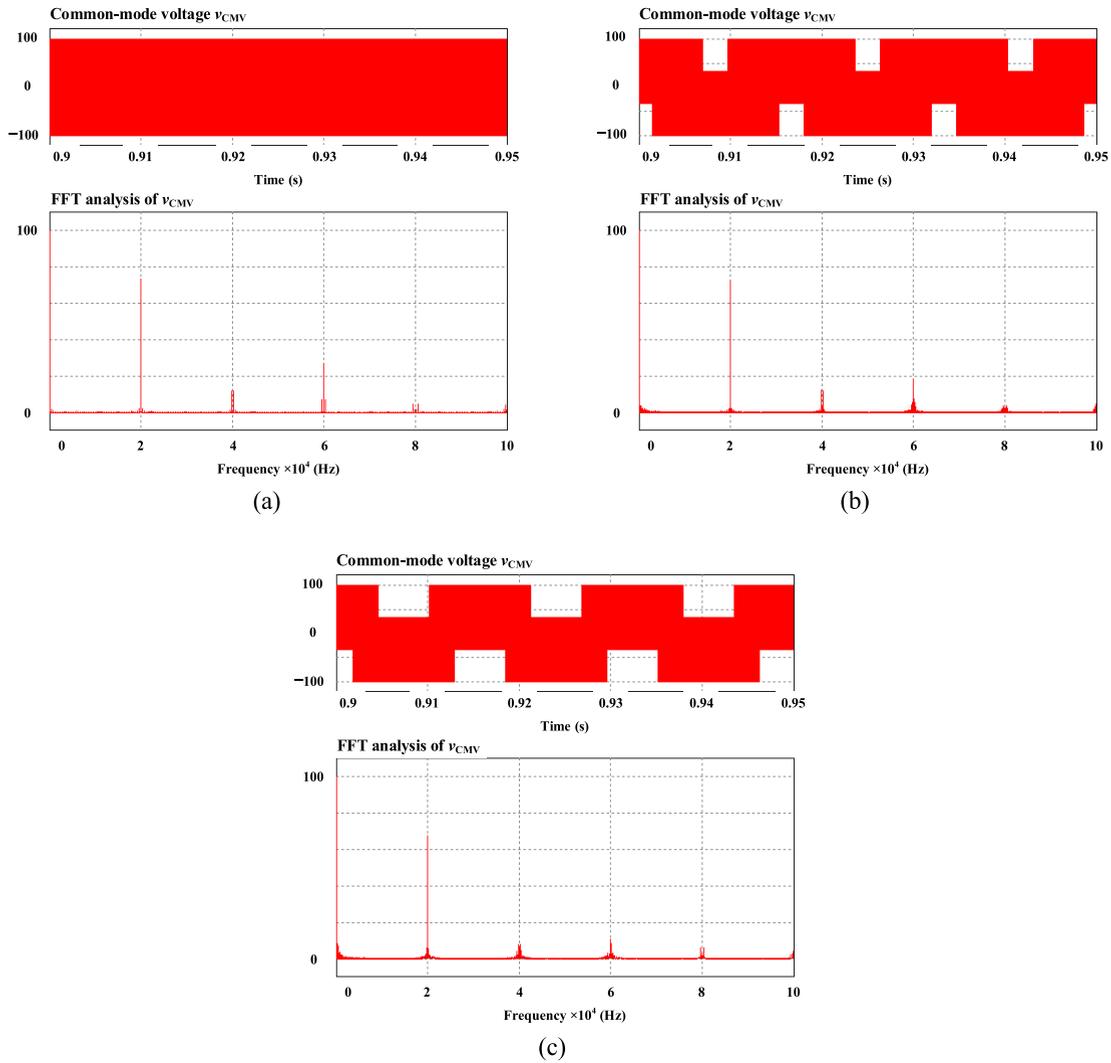
FIGURE 13. Simulation results of common-mode voltage and corresponding FFT analysis obtained by (a) SVPWM, (b) DPWM hybrid offset, (c) proposed per-phase DPWM.
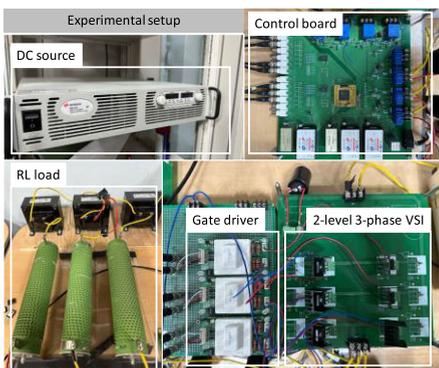
FIGURE 14. Experimental laboratory setup of 2-level 3-phase VSI.

A constant junction temperature $T_j = 25°C$ is used for the loss performance calculation.

The efficiency of the inverter is defined as

$$\eta = \frac{P_{out}}{P_{in}} \qquad (17)$$

where P_{out} and P_{in} are the output and input power of the inverter, respectively.

Fig. 17 shows the output performance comparison among four control schemes. As for the load current THD, the SVPWM has the lowest current THD due to continuous modulation. Meanwhile, the current THD of phase a increases following the rise of the non-switching interval. In Fig. 17(a), the proposed per-phase DPWM method produces the 120° non-switching interval, it results in the highest current THD in phase a. When comparing the 3-phase GDPWM method to the proposed per-phase DPWM control scheme, the latter shows approximately 16% reduction in the average current THD. In comparison with the DPWM hybrid offset method, the proposed per-phase DPWM control scheme has a higher average current THD by about 10%. As can be seen in Fig. 17(b), as assumed that phase a is the phase leg having the worst aging state, the switching frequency in phase a acquired by 3-phase GDPWM and DPWM hybrid offset method is lowered by approximately 33%. The 3-phase GDPWM method decreases the same amount of switching
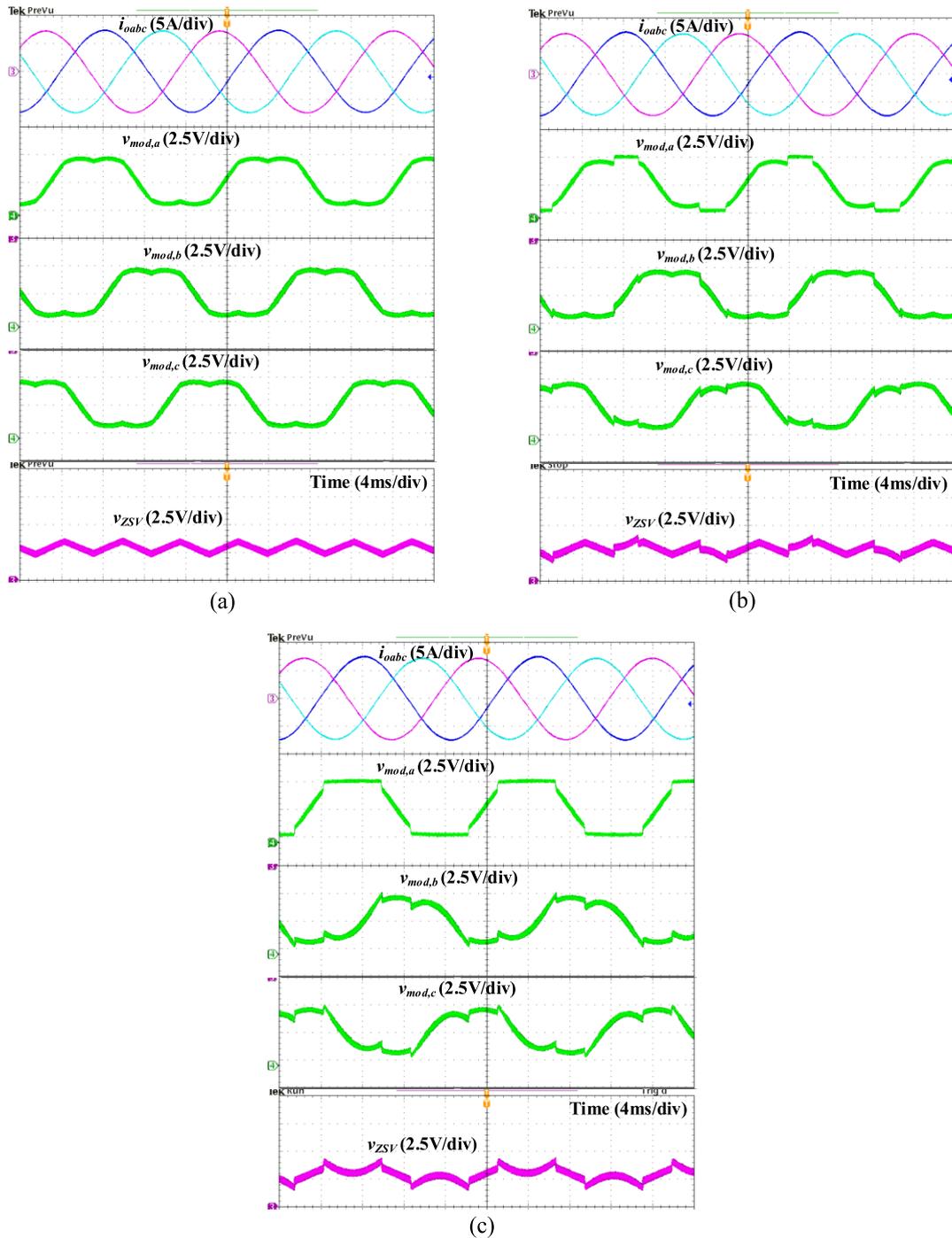
FIGURE 15. Experiment results of output currents, modulation signals, and ZSV signal obtained by (a) SVPWM, (b) DPWM hybrid offset, (c) Proposed per-phase DPWM method.

frequency in 3-phase legs by approximately 33%. Meanwhile, the proposed per-phase DPWM approach lowers the switching frequency in phase *a* by approximately 67%, and the remaining phase legs are operated with a similar switching frequency in SVPWM. Regarding power loss performance, Fig. 17(c) and (d) show the comparison of conduction and switching losses between four control schemes. As shown in Fig. 17(c), the conduction loss of phase *a* has a minor increase

as a result of the generated non-switching interval by 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods. Meanwhile, the switching loss decreases significantly, as shown in Fig. 17(d). 3-phase GDPWM and DPWM hybrid offset schemes lower the switching loss of phase *a* leg by approximately 47% reduction compared to SVPWM. The 3-phase GDPWM method decreases the same amount of switching loss in 3-phase legs by 47%. The
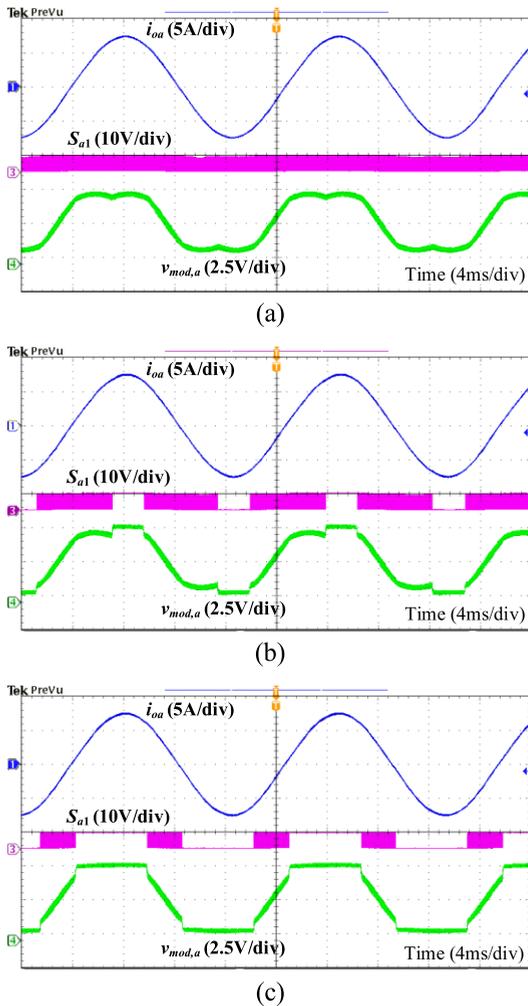
FIGURE 16. Experiment results of phase *a* output current, modulation signal, and corresponding switching pattern obtained by (a) SVPWM, (b) DPWM hybrid offset, (c) Proposed per-phase DPWM method.

proposed approach significantly lowers the switching loss of phase *a* by approximately 80%. Due to the reduction of the switching loss in 3-phase legs acquired by 3-phase GDPWM method, its total loss is the lowest, as shown in Fig. 17(e). The proposed per-phase DPWM method has lower total loss compared to SVPWM and DPWM hybrid offset by 20% and 10%, respectively. The calculated simulation results verify that the proposed method is working correctly.

To provide more apparent understanding of the performance of the proposed method, a detailed comparison is conducted among SVPWM, 3-phase GDPWM, DPWM hybrid offset [21], and proposed per-phase DPWM methods. This comparison is conducted under different conditions. Fig. 18 illustrates the behavior of load current THD following the variation of carrier frequency as analyzed using four approaches. As observed, the THD decreases as the carrier frequency is raised. Due to being the continuous PWM, SVPWM scheme has the lowest THD. The 3-phase GDPWM has the highest output current THD due to the reduction

of switching frequency in 3-phase legs. The DPWM hybrid offset and proposed per-phase DPWM approaches reduce the switching frequency of only phase *a*, so the phase and average current THD are still lower than that of 3-phase GDPWM by about 15 to 20% following the change of carrier frequency.

Switching frequency results acquired by SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods under various carrier frequency conditions are presented in Fig. 19. As carrier frequency rises, the 3-phase GDPWM approach leads to a reduction of approximately 33% in the switching frequency of 3-phase legs compared to SVPWM, while DPWM hybrid offset method decreases the switching frequency of only phase *a* with the same amount. The proposed per-phase DPWM approach lowers switching frequency of phase *a* by approximately 67% in comparison to SVPWM approach while maintaining similar switching frequencies for phases *b* and *c* as in SVPWM. The 3-phase GDPWM scheme has the lowest average switching frequency due to its reduced switching frequency in 3-phase legs compared to remaining approaches. Meanwhile, the average switching frequency of the proposed method is less than that of SVPWM and DPWM hybrid offset approaches.

The phase conduction loss obtained by SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches in Fig. 20(a) are similar following the change of carrier frequency. Due to the reduction of switching frequency, the conduction loss of 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods is slightly higher than that of SVPWM. As for switching loss in Fig. 20(b), proposed approach has the lowest switching loss in phase *a*. The proposed approach lowers the switching loss of phase *a* by approximately 80% at all carrier frequency conditions. The two remaining phase legs have similar switching loss as in SVPWM because they are operated with the same switching frequency. The 3-phase GDPWM method decreases the switching frequency in 3-phase legs, so the corresponding phase switching loss is decreased by about 50% compared to SVPWM. As for the DPWM hybrid offset method, the switching loss in phase *a* is decreased by about 50% compared to SVPWM, while two remaining phase legs have similar switching loss as in SVPWM and proposed per-phase DPWM schemes. Thus, 3-phase GDPWM has the lowest total switching loss and total loss, as shown in Fig. 20(c), whereas SVPWM has the highest ones. As can be seen in Fig. 20(d), the efficiency obtained by four techniques decreases when the carrier frequency increases. It is due to the increase of switching loss generated by the commutation in power devices. The SVPWM has the lowest efficiency, whereas the 3-phase GDPWM has the highest efficiency due to the reduction of switching loss in both three phase legs. The efficiency of VSI obtained by the proposed per-phase DPWM method is higher than that of SVPWM and DPWM hybrid offset approaches.

Fig. 21 depicts the behavior of THD following the variation of output power as analyzed using four approaches. Due to being the continuous PWM, SVPWM scheme has the lowest
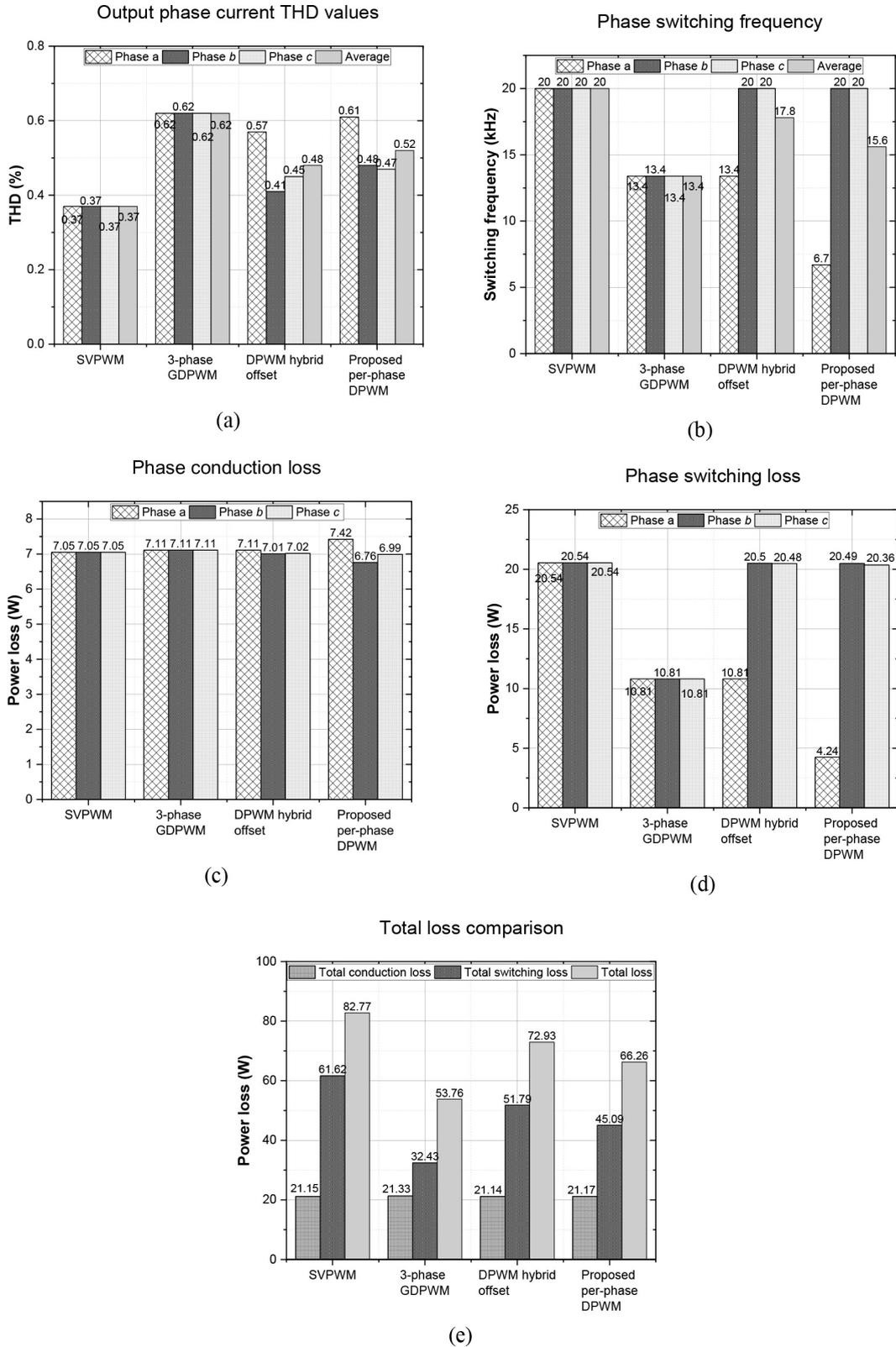
FIGURE 17. (a) Load current THD, (b) Phase leg switching frequency, (c) Phase conduction loss, (d) Phase switching loss, (e) Total loss comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods.
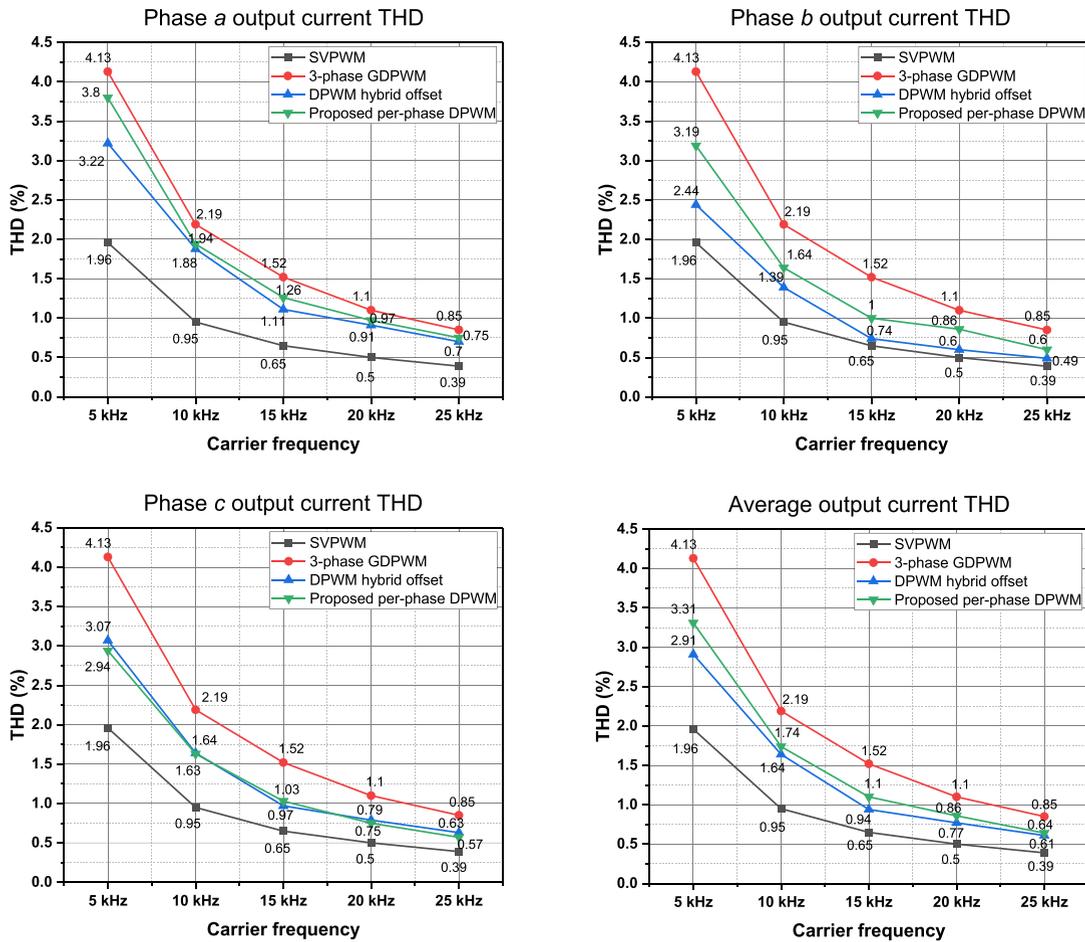
FIGURE 18. Phase load current THD comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of carrier frequency ($V_{dc} = 200V$, phase angle $\theta = 20°$ and $I^* = 5A$).

load current THD. In this comparison, the load current THD obtained by both 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods is significantly higher than that of SVPWM. The 3-phase GDPWM has the highest output current THD due to the reduction of switching frequency in 3-phase legs. The proposed per-phase DPWM approach decreases the switching frequency of only phase a, so the phase and average current THD are still lower than that of 3-phase GDPWM under different output power conditions. Meanwhile, the proposed per-phase DPWM method's average THD is slightly higher than DPWM hybrid offset.

Fig. 22 illustrates a comparison of phase switching frequencies among the SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods at different output powers. Under different output powers, the phase and average switching frequency of SVPWM are kept at 10 kHz as the carrier frequency. Similar to previous results, 3-phase GDPWM decreases the same amount of switching frequency by about 33% under different output powers, while the DPWM hybrid offset decreases the same amount of switching frequency by approximately 33% in phase a under different output powers. Simultaneously, the proposed

DPWM technique decreases the switching frequency of phase a by 67% across all output power variations.

The phase conduction loss obtained by SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM in Fig. 23(a) increases with the rise in output power. The conduction loss in phase a of the 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods is marginally greater than that of SVPWM as a result of the decrease in switching frequency. Meanwhile, the conduction loss of 3-phase GDPWM in the remaining phases is the highest. As shown in Fig. 23(b), the proposed per-phase DPWM approach exhibits the lowest switching loss in phase a. The switching loss of phase a is lowered by approximately 80% across all output power conditions. The remaining phase legs have similar switching loss as in SVPWM because they are operated with the same switching frequency. The 3-phase GDPWM method decreases the switching frequency in 3-phase legs, so the corresponding phase switching loss is decreased by about 48% compared to SVPWM. The DPWM hybrid offset method also decreases the switching frequency in only phase a, so the switching loss is decreased by about
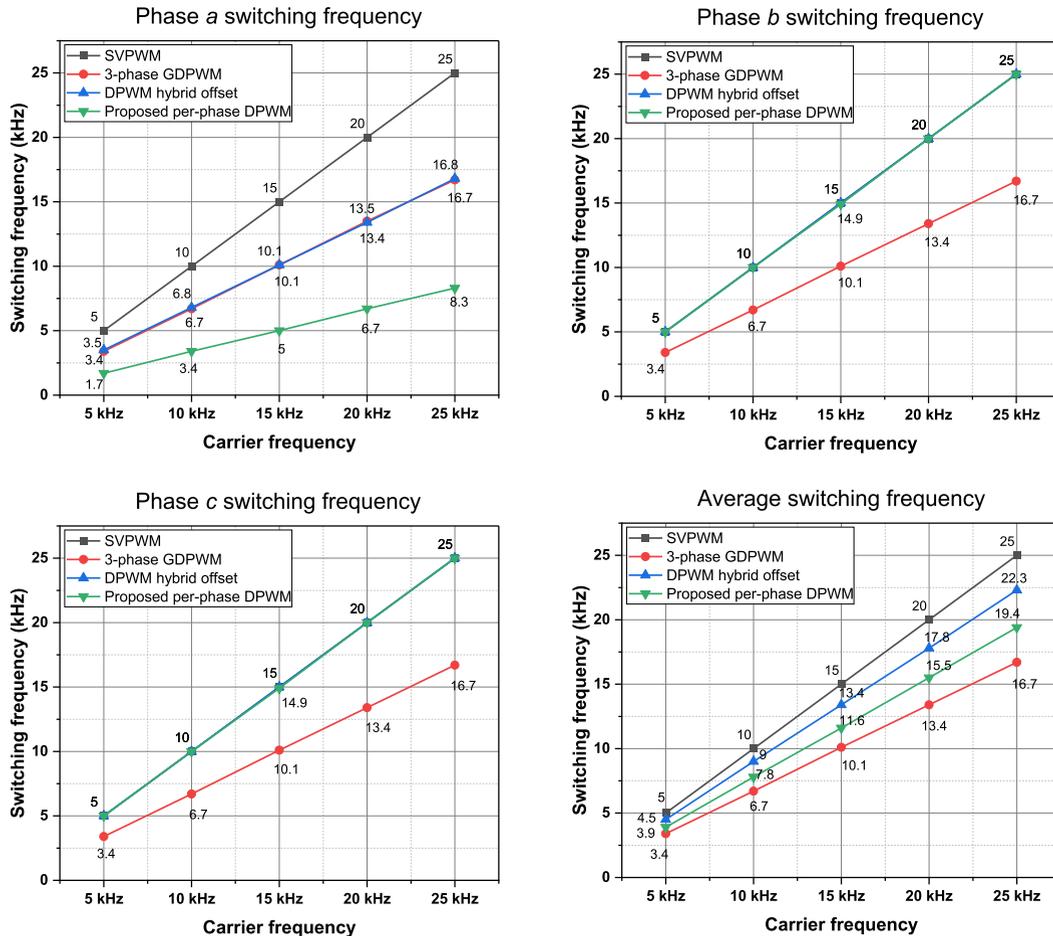
FIGURE 19. Switching frequency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of carrier frequency ($V_{dc} = 200V$, phase angle $\theta = 20°$ and $I^* = 5A$).

48% compared to SVPWM. As a result, the 3-phase GDPWM approach achieves the lowest total switching and total losses, as shown in Fig. 23(c), while SVPWM has the highest ones. Regarding the change of output power, the efficiency obtained by four techniques increases when the output power rises, as shown in Fig. 23(d). In this case, the efficiency of VSI obtained by the proposed per-phase DPWM method is higher than that of SVPWM and DPWM hybrid offset approaches but lower than 3-phase GDPWM method.

Fig. 24 displays the behavior of load current THD following the variation of load conditions as analyzed using four control schemes. In this case, the load phase angle is altered by increasing load inductance. The increased phase angle causes the load current THD to decrease. Due to the continuous PWM, SVPWM scheme has the lowest load current THD. Meanwhile, the 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods have higher load current THD than SVPWM because of the switching frequency reduction. Because of switching frequency reduction in 3-phase legs, the 3-phase GDPWM method has the highest output current THD. The phase and average current THD of proposed per-phase DPWM approach are still lower

than that of 3-phase GDPWM under different load conditions and slightly higher than that of DPWM hybrid offset scheme.

Fig. 25 displays a comparison of phase switching frequencies among the SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under various load conditions. Under different load conditions, the phase and average switching frequency of SVPWM are kept at 10 kHz as the carrier frequency. The 3-phase GDPWM decreases the same amount of switching frequency by about 33% under different output powers. The switching frequency of phase a is lowered by approximately 67% across all load conditions when conducting proposed per-phase DPWM approach. In Fig. 25, the switching frequency of phase a acquired by the DPWM hybrid offset is well reduced by about 30% at low load angle conditions. However, when the load phase angle is large, the efficiency of DPWM hybrid offset in reducing the switching frequency of phase a is lowered due to the use of output currents to locate the clamping regions without considering the load phase angle, as indicated earlier. Additionally, the generated offset voltage following output currents at large load phase angle results in unexpected clamping regions in other phases. As a result, the switching
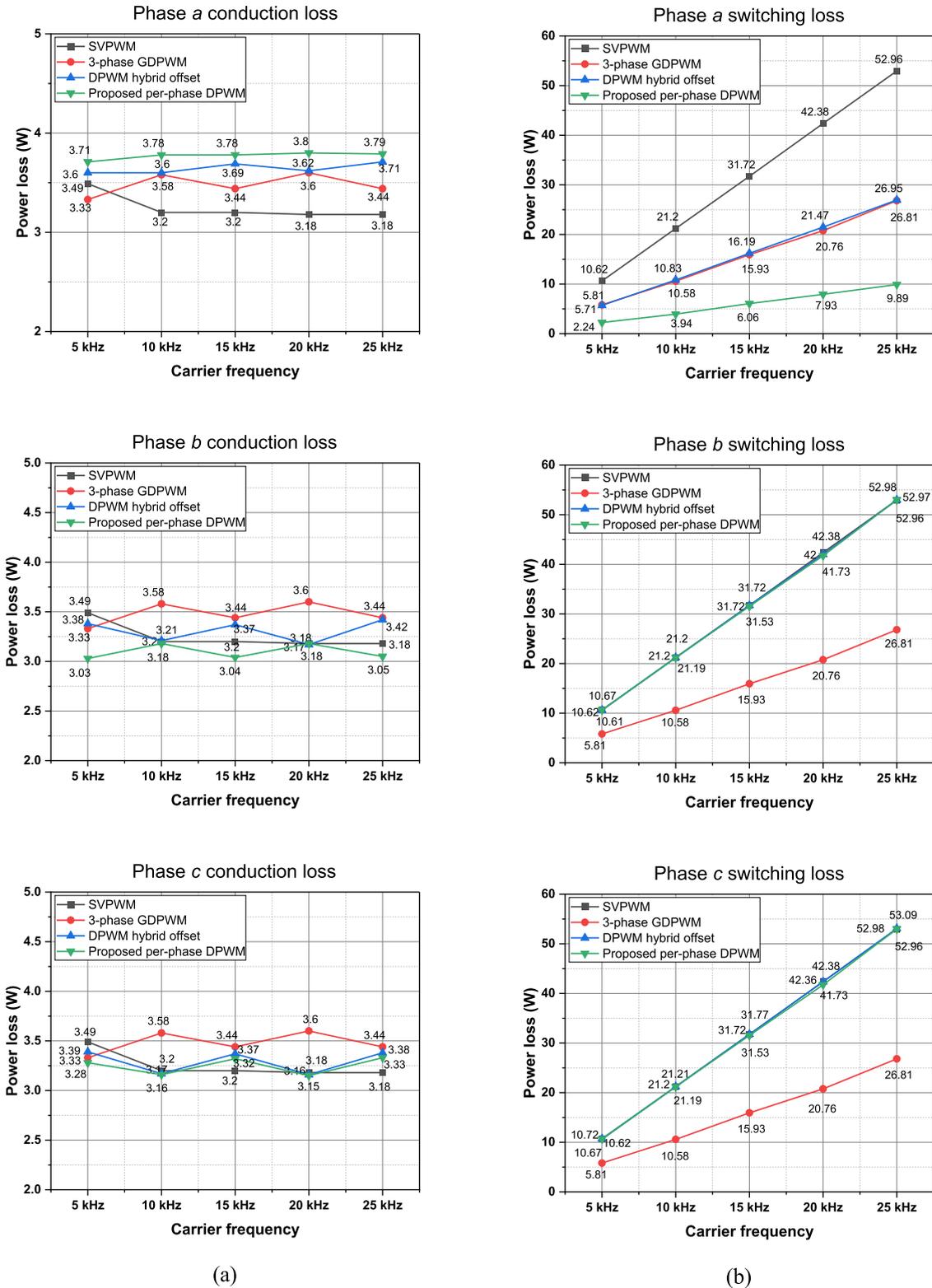
FIGURE 20. (a) Conduction loss, (b) switching loss, (c) total loss, and (d) efficiency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of carrier ($V_{dc} = 200V$, phase angle $\theta = 20°$ and $I^* = 5A$).

frequency of phase *b* decreases with the rise in the load phase angle when using the DPWM hybrid offset method.

The phase conduction loss depicted in Fig. 26(a) decreases with the increase in the load angle for both the 3-phase

Total conduction loss

Total switching loss

Total loss
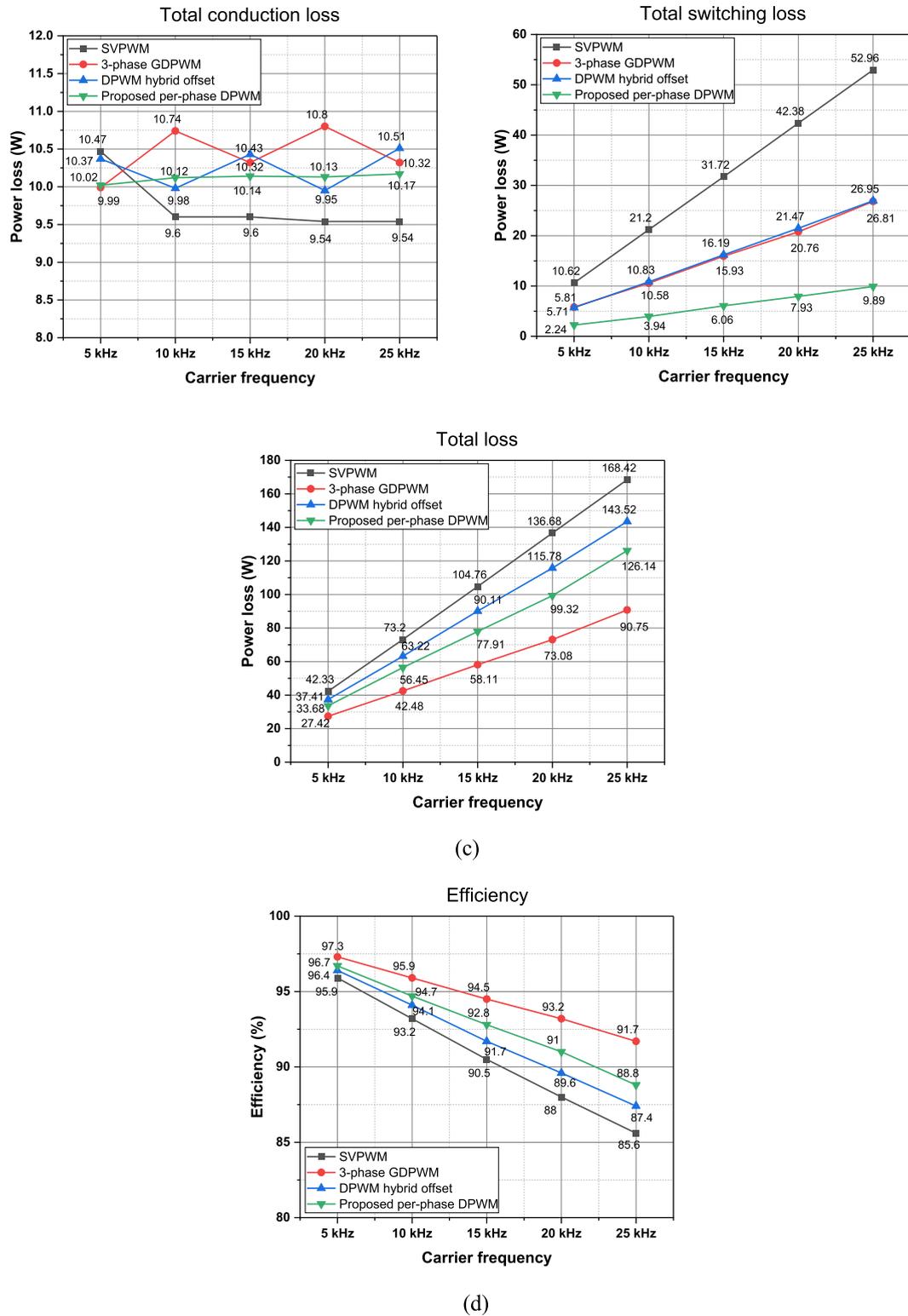
Efficiency

FIGURE 20. *(Continued.)* (a) Conduction loss, (b) switching loss, (c) total loss, and (d) efficiency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of carrier ($V_{dc} = 200V$, phase angle $\theta = 20°$ and $I* = 5A$).

GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods. Due to the unchanged switching frequency, the conduction and switching loss of SVPWM is maintained following the change of load conditions. The conduction
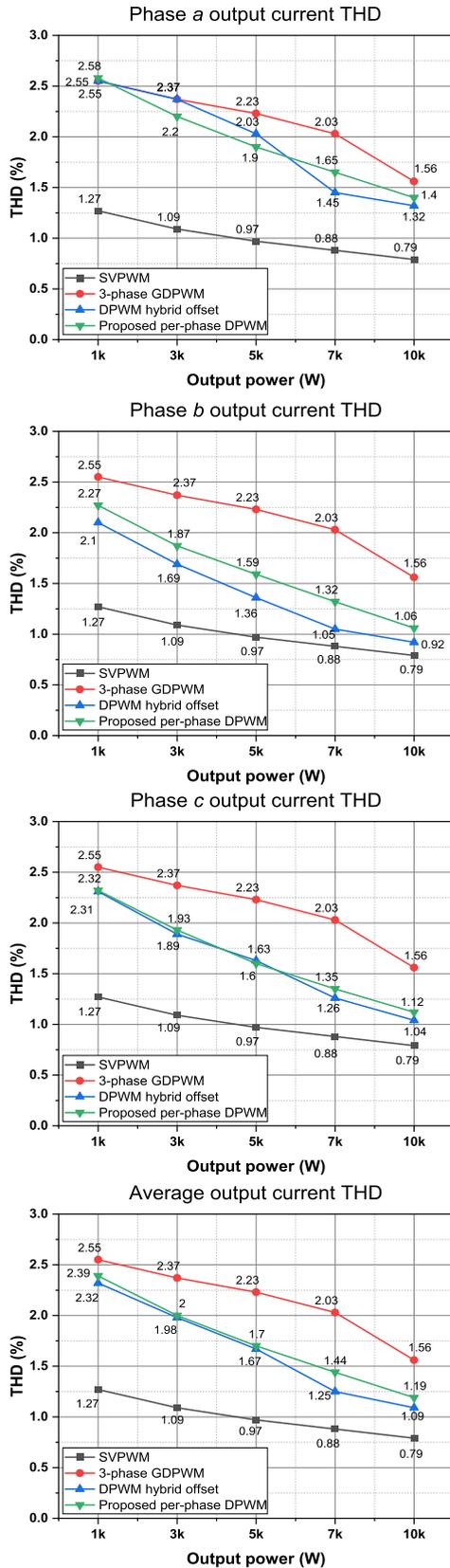
FIGURE 21. Phase load current THD comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of output power ($V_{dc} = 720V$, phase angle $\theta = 20°$ and carrier frequency $f_{cr} = 10kHz$).
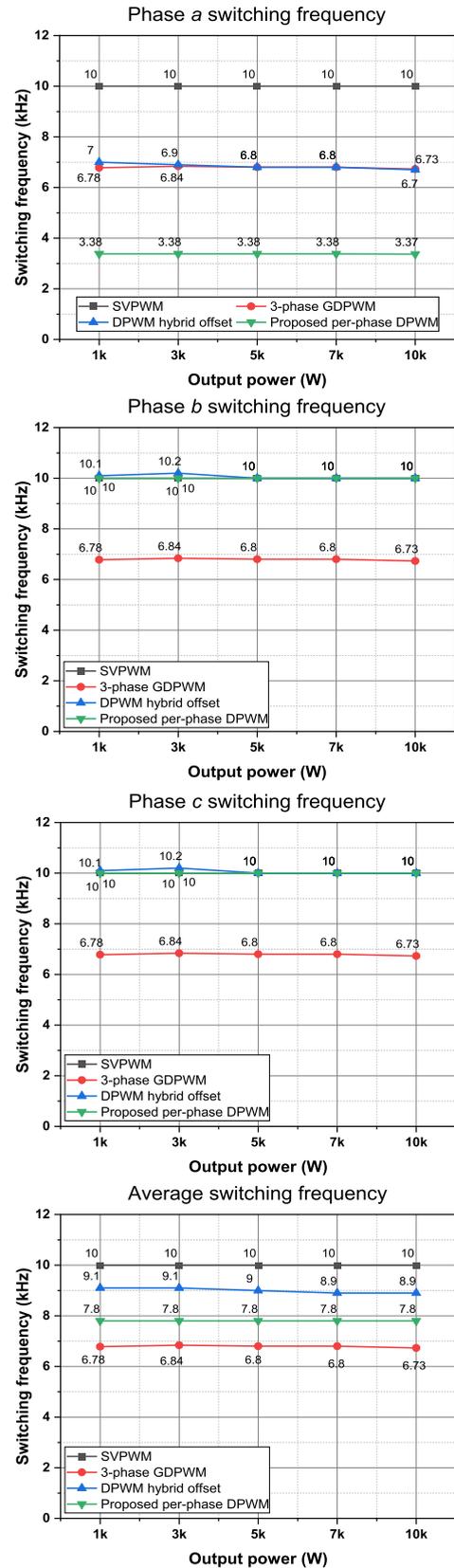
FIGURE 22. Phase switching frequency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of output power ($V_{dc} = 720V$, phase angle $\theta = 20°$ and carrier frequency $f_{cr} = 10kHz$).
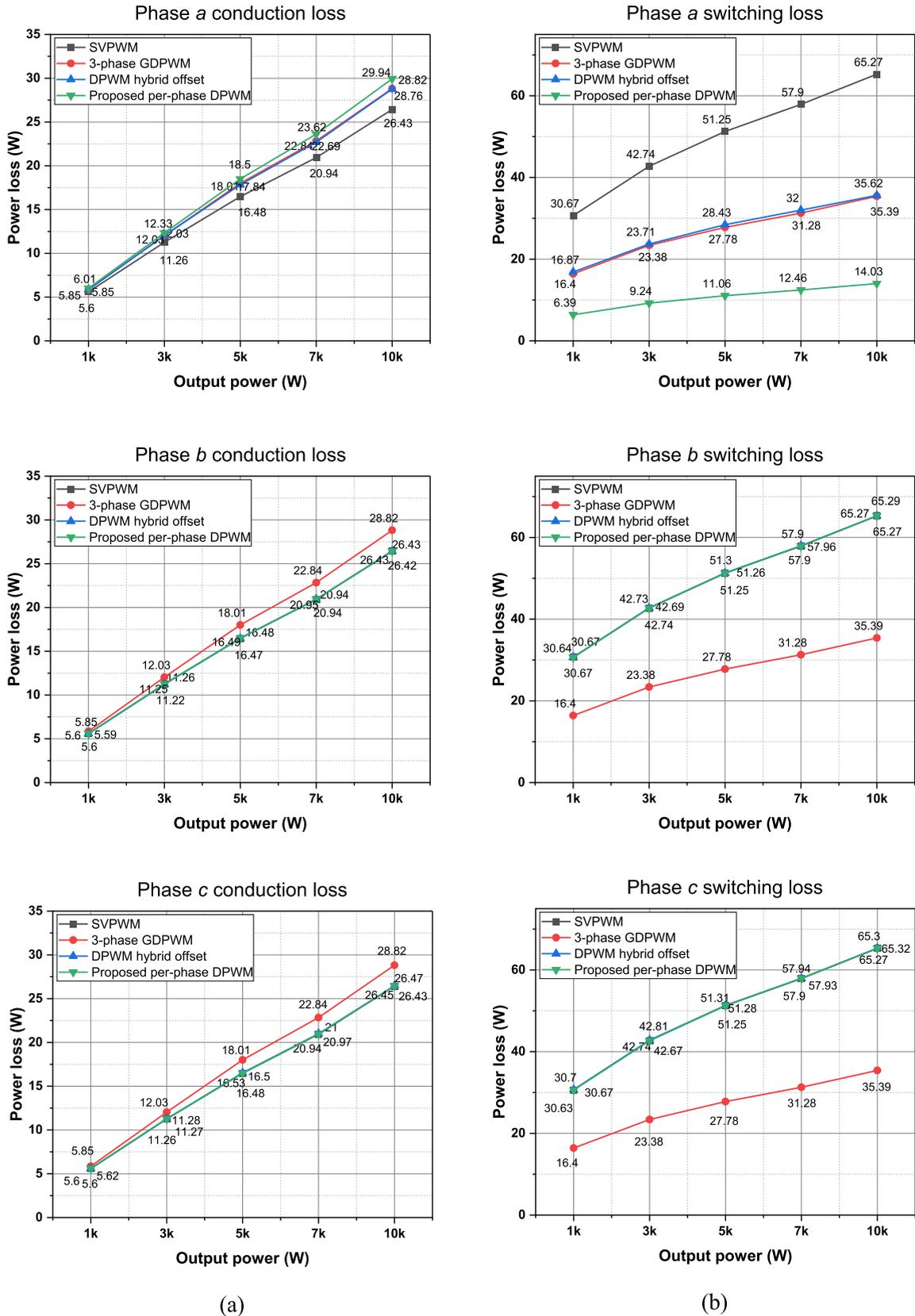
FIGURE 23. (a) Conduction loss, (b) switching loss, (c) total loss, and (d) efficiency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods under the variation of output power ($V_{dc} = 720V$, phase angle $\theta = 20°$ and carrier frequency $f_{cr} = 10kHz$).

(c)

(d)
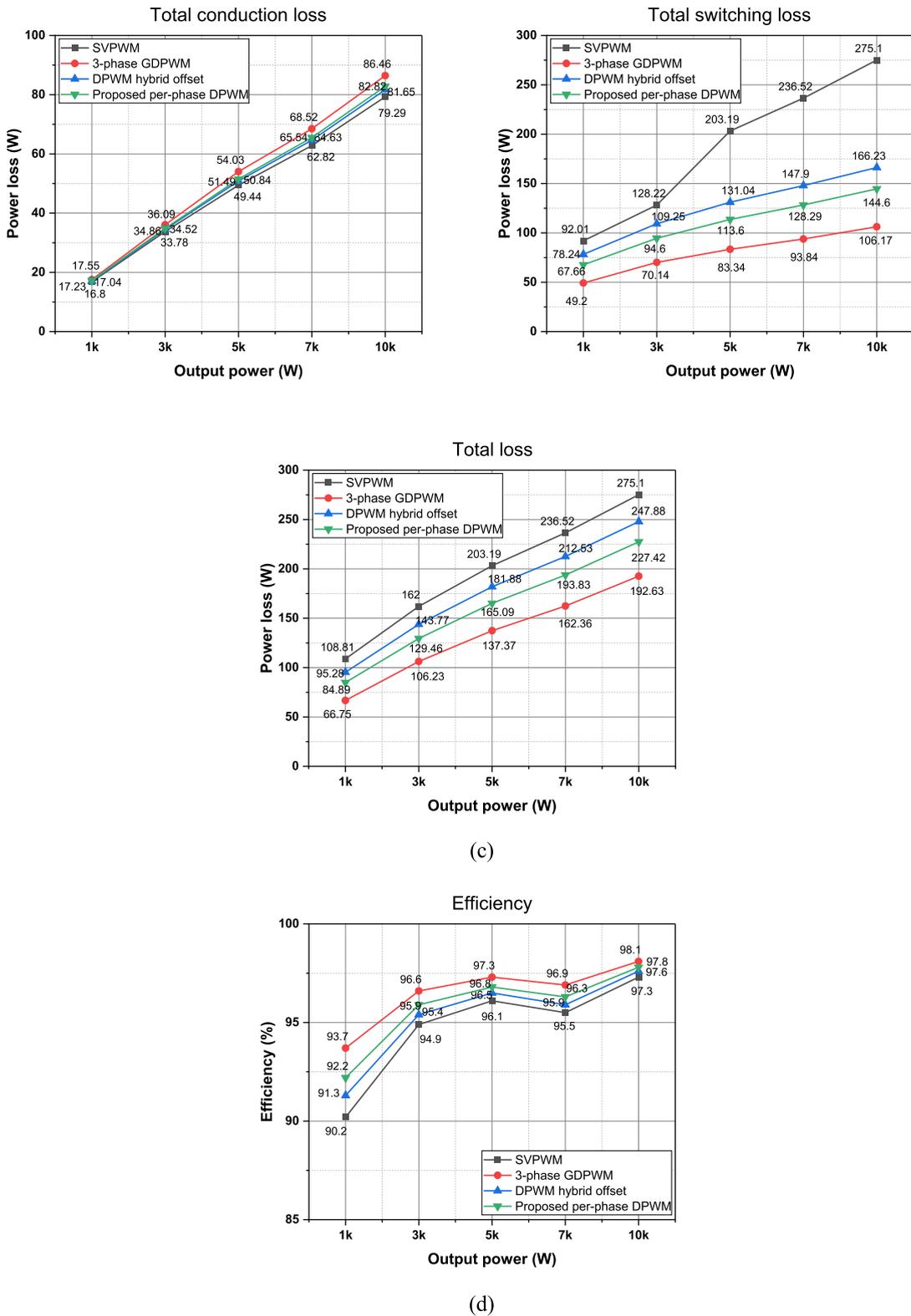
FIGURE 23. *(Continued.)* **(a) Conduction loss, (b) switching loss, (c) total loss, and (d) efficiency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods under the variation of output power ($V_{dc} = 720V$, phase angle $\theta = 20°$ and carrier frequency $f_{cr} = 10kHz$).**

loss acquired by 3-phase GDPWM scheme is the highest, attributed to the reduced switching frequency in 3-phase legs. Regarding the switching loss shown in Fig. 26(b), the proposed per-phase DPWM scheme achieves the lowest loss
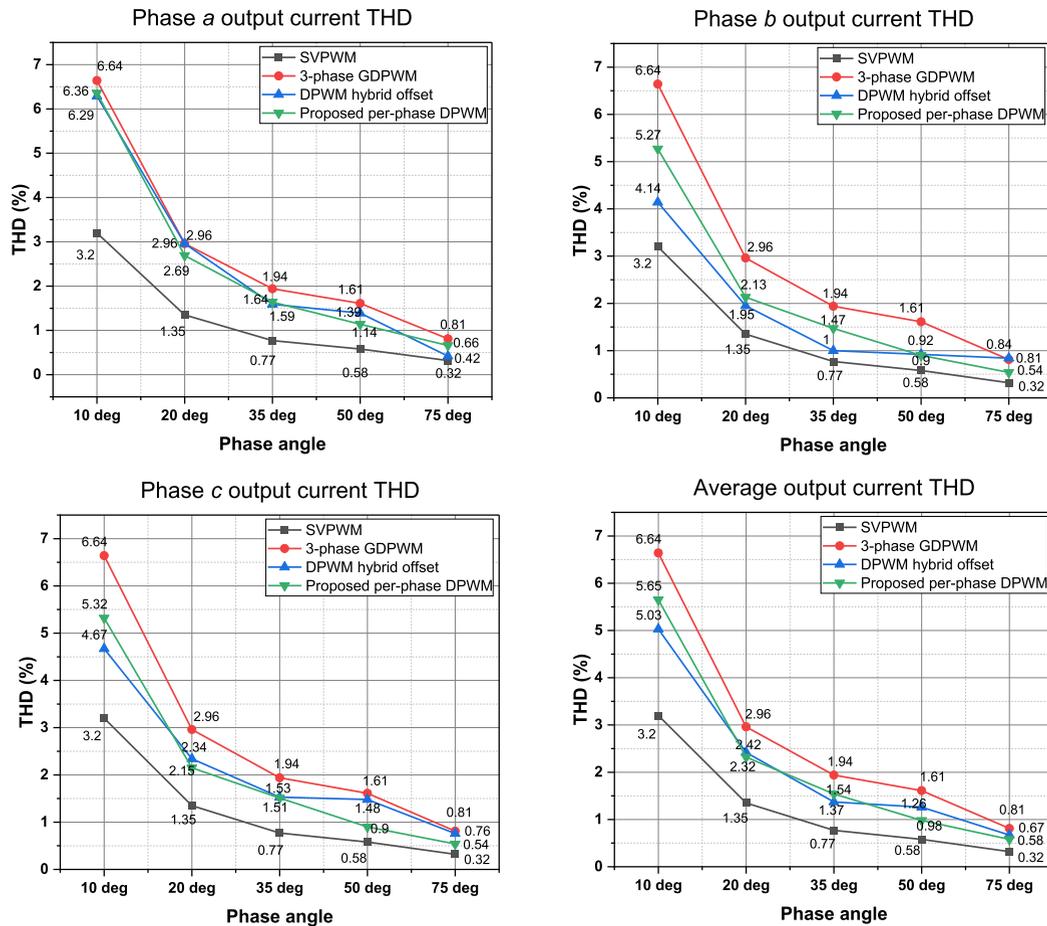
FIGURE 24. Phase load current THD comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of load condition ($V_{dc} = 720V$, $P_{out} = 1kW$ and carrier frequency $f_{cr} = 10kHz$).

in phase *a*. However, it is noticeable that the rate of reduction in switching loss for phase *a* decreases as the load phase angle increases. It is similar to in 3-phase GDPWM where its rate of reduction in switching loss slightly reduces as the load phase angle increases. This can be attributed to the fact that the increase in load phase angle causes a phase difference between the output converter voltage and output current. The two remaining phase legs in proposed per-phase DPWM approach have similar switching loss as in SVPWM because they are operated with the same switching frequency. At a large load phase angles of 50° and 75°, the reduction rate of switching loss obtained by the DPWM hybrid offset significantly decreases. However, thanks to the clamping region of 120°, the proposed per-phase DPWM method still has a higher reduction rate of switching loss in phase *a* than 3-phase GDPWM and DPWM hybrid offset schemes. The 3-phase GDPWM has the lowest total switching loss and total loss, as shown in Fig. 26(c), and SVPWM has the highest ones. In terms of variation of load conditions in Fig. 26(d), where the load phase angle increases, the efficiency of SVPWM method does not change. The efficiency obtained by 3-phase GDPWM, DPWM hybrid offset, and

TABLE 2. Junction temperature calculation following predefined mission profile.

	$T_{j,\text{high}}$	$T_{j,\text{low}}$	$T_{j,\text{mean}}$	ΔT_j
SVPWM	83.6 °C	58.6 °C	71.1 °C	25 °C
3-phase GDPWM	76 °C	57.2 °C	66.6 °C	18.8 °C
DPWM hybrid offset	76.1 °C	57.3 °C	66.7 °C	18.8 °C
Per-phase DPWM	75.6 °C	57.6 °C	66.6 °C	18 °C

proposed per-phase DPWM method slightly decreases when the load phase angle rises. Here, the efficiency obtained by the proposed per-phase DPWM method is slightly lower than that of 3-phase GDPWM method but higher than SVPWM and DPWM hybrid offset approaches.

As mentioned previously, thermal stress serves as the main factor leading to the failure of power semiconductor devices, thereby lowering the lifetime of power switches and entire converter. Therefore, it is required to assess the impact of implementing the proposed per-phase DPWM control scheme on the power semiconductor devices' lifetime.
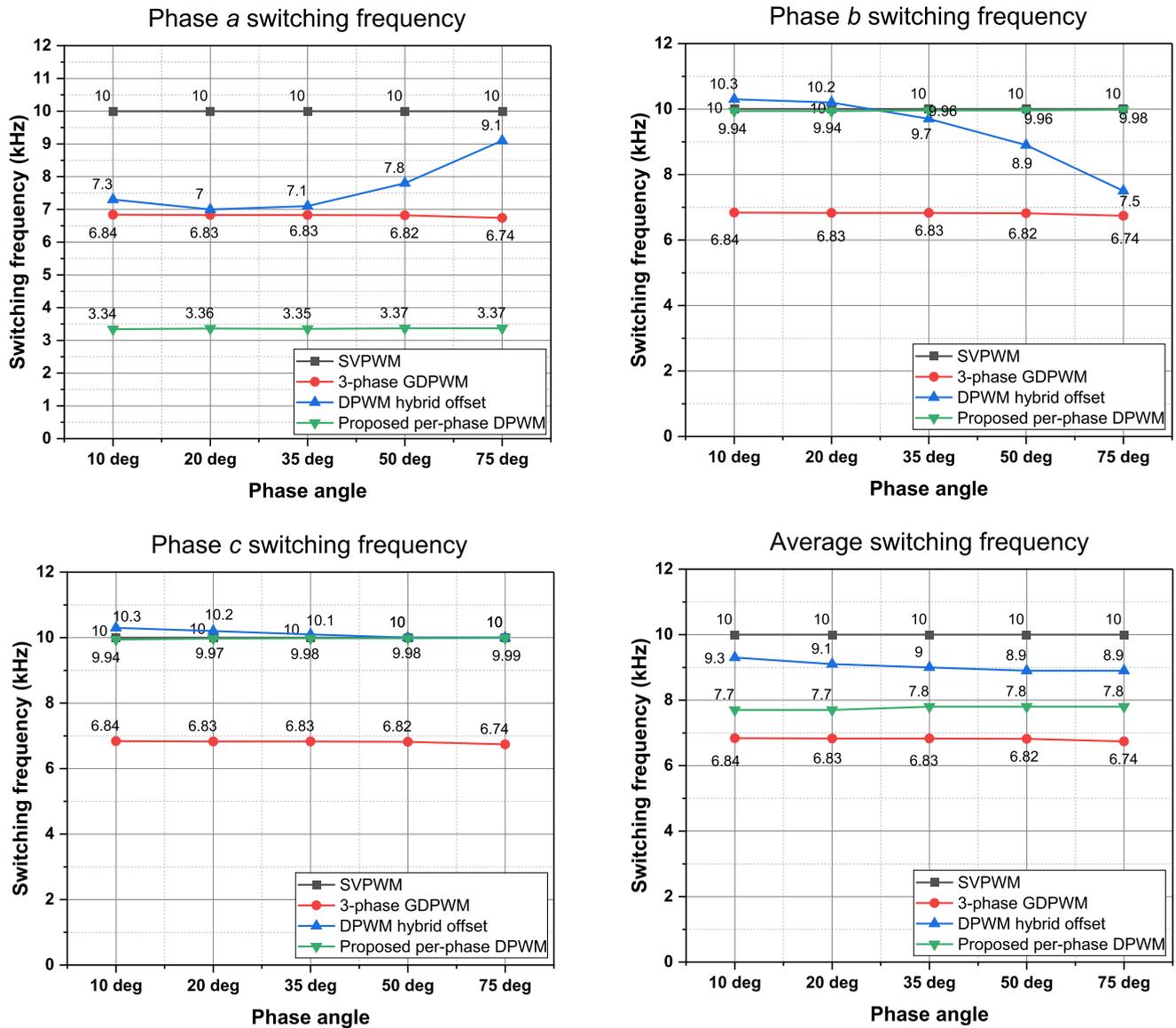
FIGURE 25. Phase switching frequency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed perphase DPWM approaches under the variation of load condition ($V_{dc} = 720\,V$, $P_{out} = 1kW$ and carrier frequency $f_{cr} = 10kHz$).

To estimate the lifetime of power switches, empirical models that describe the relationship between the number of cycles to failure N_f and temperature cycles will be employed. SKiM63 model in [25] will be applied to estimate lifetime of switching devices of the phase leg having the worst aging state after conducting the proposed control techniques in this study. It should be noted that the lifetime estimation models require knowledge of junction temperature. By employing thermal models and using calculated loss, it can determine the junction temperature of power switches. The switching device's losses can be computed by the thermal module in PSIM simulation program and the corresponding thermal characteristics of the selected device (IGBT from Semikron SKM75GB07E3). Therefore, the Foster-type thermal network shown in Fig. 27 is used to calculate the junction

temperature of power switches. In this context, T_j represents the junction temperature while T_c represents the case temperature, which is set as 50°C in this study. The thermal resistance and time constant values are obtained from the datasheet.

To assess the lifetime of power switches in VSI, a periodic mission profile is employed, with output power ranging from 2.5kW to 9kW. Fig. 28 depicts the junction temperature of phase a leg, which is assumed to be the phase leg having the worst aging state and magnitude of reference current following predefined mission profile, which has been calculated based on the variations in the output power within the mission profile obtained by four control schemes: SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM. In Fig. 28(a), the temperature variation ΔT_j
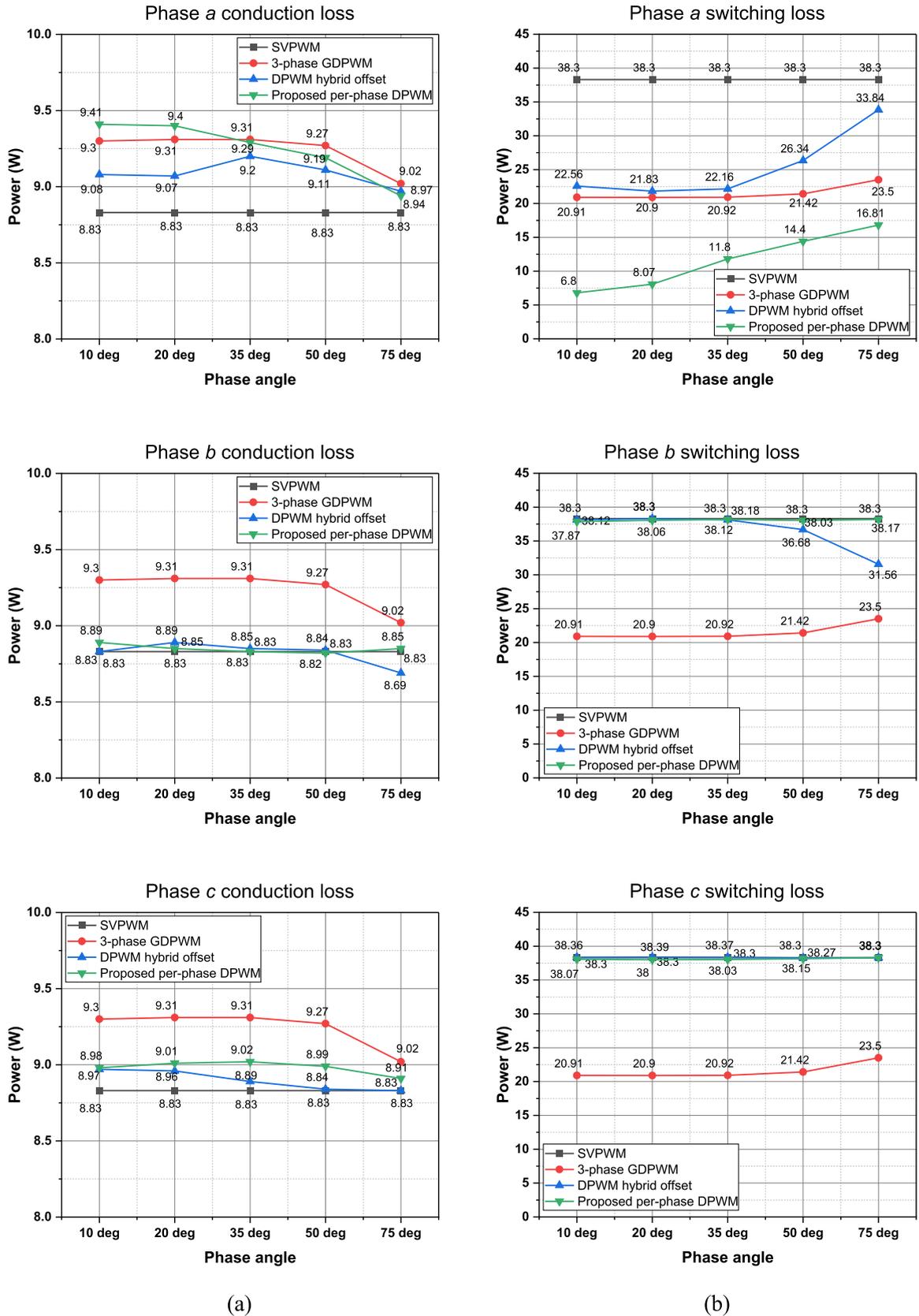
FIGURE 26. (a) Conduction loss, (b) switching loss, (c) total loss, and (d) efficiency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of load condition ($V_{dc} = 720V$, $P_{out} = 1kW$ and carrier frequency $f_{cr} = 10kHz$).
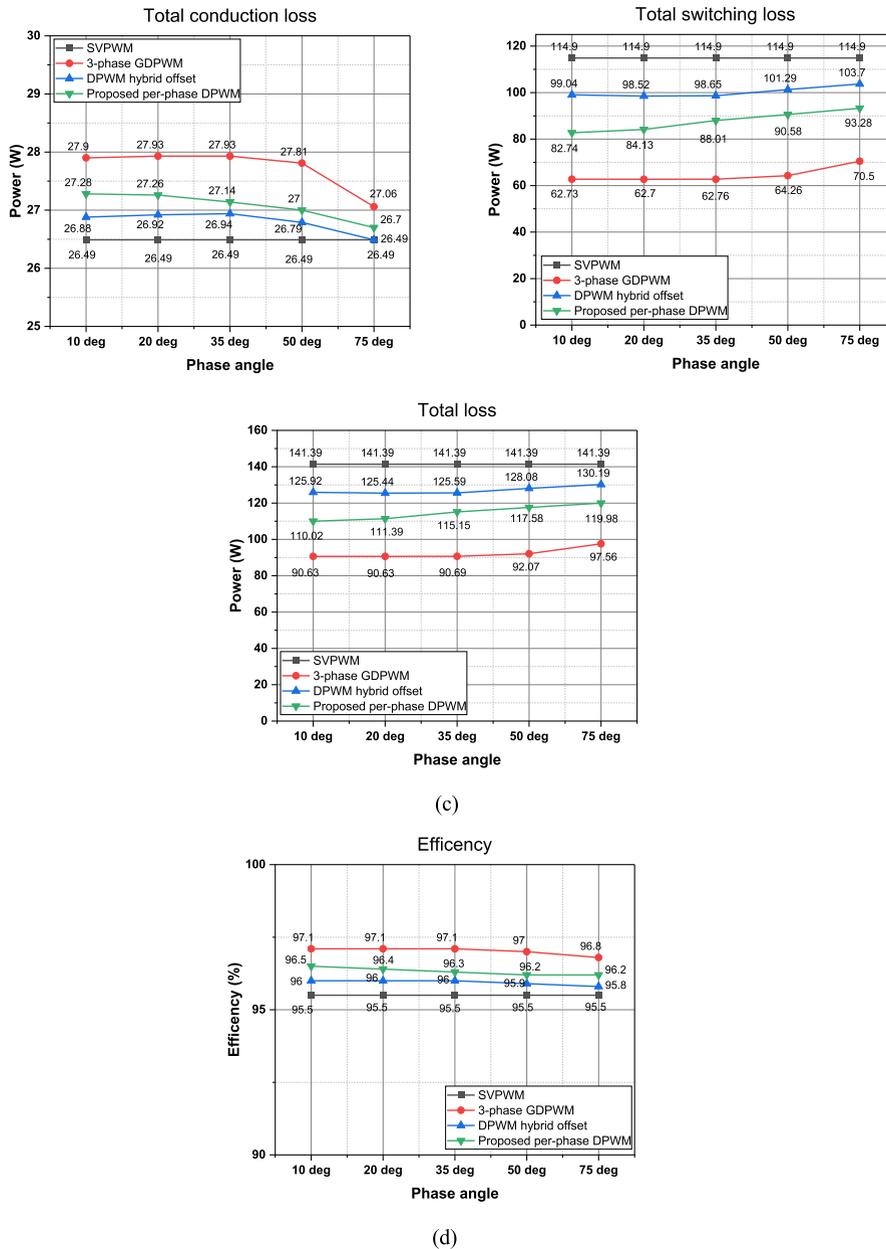
FIGURE 26. *(Continued.)* **(a) Conduction loss, (b) switching loss, (c) total loss, and (d) efficiency comparison among SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM approaches under the variation of load condition ($V_{dc} = 720V$, $P_{out} = 1kW$ and carrier frequency $f_{cr} = 10kHz$).**
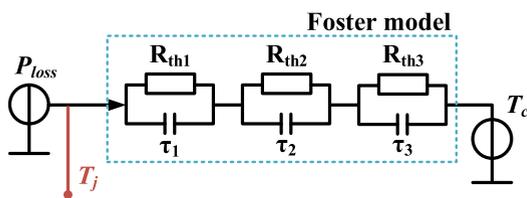
FIGURE 27. **Model of junction temperature calculation using Foster-type thermal network.**

amplitude of 25°C is acquired with SVPWM. The impact of 3-phase GDPWM and DPWM hybrid offset approaches is similar in the decrease of ΔT_j in phase a to 18.8°C,

as depicted in Fig. 28(b) and (c), respectively. Meanwhile, the proposed per-phase DPWM achieves the lowest temperature variation ΔT_j of 18°C, as shown in Fig. 28(d). Table 2 presents the estimated junction temperature obtained by SVPWM, 3-phase GDPWM, DPWM hybrid offset, and proposed per-phase DPWM methods.

Following the calculated junction temperature, the estimated number of cycles to failure N_f and the corresponding lifetime of the phase leg having the worst aging state calculated following different analytical lifetime models are shown in Fig. 29. The estimated lifetime obtained by SKiM63 models indicates that the proposed per-phase DPWM scheme
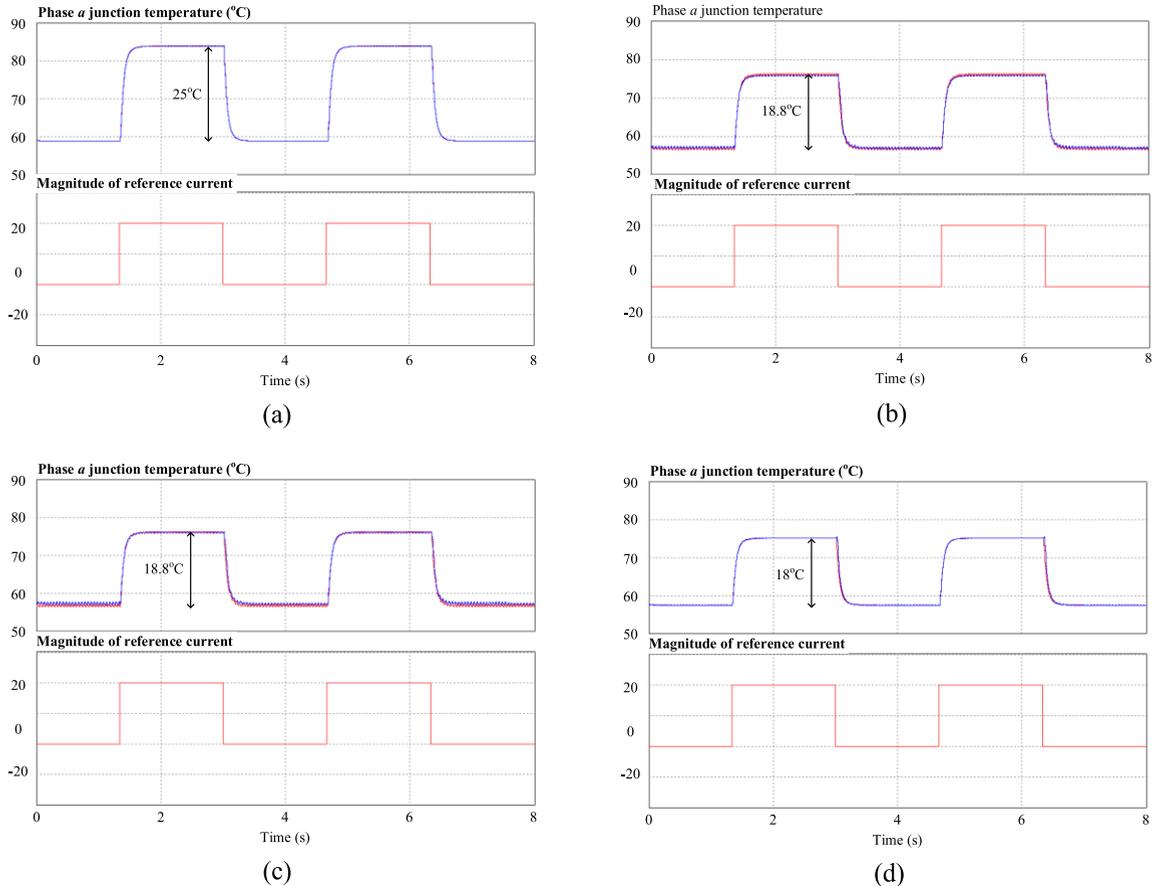
FIGURE 28. Junction temperature of power switches in phase *a* and magnitude of reference current (a) SVPWM, (b) 3-phase GDPWM, (c) DPWM hybrid offset, (d) Per-phase DPWM.
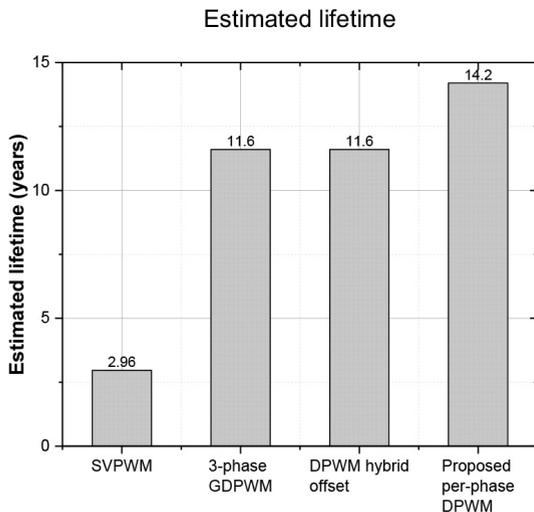
FIGURE 29. Estimated lifetime obtained by four control approaches.

increases the lifetime by about 4.8 times, compared to the SVPWM method. The proposed control scheme results in a lifetime that is approximately 20% longer than that of the 3-phase GDPWM and DPWM hybrid offset.

V. CONCLUSION

This paper proposed a modified CBPWM for independently reducing the switching loss of specific phases in 2-level 3-phase VSI. By injecting the proper ZSV signal to the reference voltage at both non-switching and switching intervals, this proposed per-phase DPWM significantly decreases the switching frequency of the phase leg having the worst aging state in the 2-level 3-phase VSI, which decreases corresponding power loss and increases the corresponding useful lifetime of that leg and VSI. Additionally, the output performance of the VSI is not degraded too much compared to the SVPWM, 3-phase GDPWM, and DPWM hybrid offset approaches. The slight increase of load current THD is a trade-off to the significant decrease of switching frequency and loss. The various non-switching angles can be used to achieve the desired non-switching interval and ease the rise of load current THD. The effectiveness and correctness of the proposed method were validated through the simulation and experimental results.

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