IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 19 September 2023, accepted 11 October 2023, date of publication 17 October 2023, date of current version 25 October 2023.
Digital Object Identifier 10.1109/ACCESS.2023.3325236

RESEARCH ARTICLE

Circuit-Specific and Technology-Independent Criterion for Selection of Power MOSFETs That Minimize Energy Dissipation

VIKAS JOSHI [1], UTKARSH JADLI [2], PEYUSH PANDE [1], (Member, IEEE), MAYANK CHATURVEDI [2], DANIEL HAASMANN [2], AND SIMA DIMITRIJEV [2], (Life Senior Member, IEEE)
[1]Department of Electronics and Communication Engineering, Graphic Era (Deemed to be University), Dehradun 248002, India
[2]Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, QLD 4111, Australia
Corresponding author: Mayank Chaturvedi (mayank.chaturvedi@griffithuni.edu.au)

This work was supported by the Australia National Fabrication Facility (ANFF), Queensland Node, QLD, Australia, a company established under the National Collaboration Research Infrastructure Strategy to Provide Nano- and Microfabrication Facilities to Australia's Researchers.

ABSTRACT We investigate the impact of power MOSFET channel width on the power efficiency of a switch-mode power supply. With this analysis, we derive a circuit-specific criterion that minimizes the power dissipated by a power MOSFET, which is based on the ratio between *on* resistance and output capacitance of the MOSFET and is independent of its technological parameters. The effect of channel width on the power dissipation is illustrated by simulation-based analysis, which also provide an example of a published non-optimum selection of a power MOSFET and demonstrate the advantage of the newly proposed method for MOSFET selection.

INDEX TERMS Channel width, conduction losses, power loss, power MOSFET, switching losses, SPICE MOSFET parameters.

I. INTRODUCTION

Switch-mode energy converters are utilized for power conversions, such as AC to DC, DC to AC, AC to AC, and DC to DC, because ideal switches do not dissipate power. Among several semiconductor implementations of power switches, the dominant device is the metal–oxide–semiconductor field-effect transistor (MOSFET). The resistance of a MOSFET when it acts as a switch in *on* mode is not zero, which results in undesired power dissipation. To minimize this conduction power loss, circuit designers tend to select MOSFETs with the smallest *on* resistance. However, the internal structure of MOSFETs creates parasitic capacitances, whose charging and discharging during device switching are responsible for dynamic power loss [1]. As the switching frequency is increased, in response to ever increasing demand for miniaturization of the power converters, the dynamic power dissipation becomes the dominant component of the total power loss. Therefore, the MOSFET with the lower *on* resistance is no longer the optimum selection for the highest conversion efficiency.

The recent development of SiC-based MOSFETs provides alternatives to both conventional and super-junction Si MOSFETs. SiC MOSFETs utilize the higher breakdown field of this material to offer devices for the design of circuits operating at higher switching frequencies. Several manufacturers offer families of power SiC MOSFETs with a wide range of *on* resistances.

Devices in a single family are fabricated by the same technology with the difference between them being the effective channel width (W). A MOSFET with a larger W has smaller *on* resistance, providing smaller conduction losses, but it increases the switching losses due to its larger parasitic capacitances. Therefore, the selection of a MOSFET

The associate editor coordinating the review of this manuscript and approving it for publication was Sneh Saurabh.

© 2023 The Authors. This work is licensed under a Creative Commons Attribution 4.0 License.
For more information, see https://creativecommons.org/licenses/by/4.0/

with the optimum channel width depends on specific circuit parameters and switching frequency. Because the circuit designers do not have information about channel width, we have developed and published an approach that selects the most suitable MOSFETs, determined by their *on* resistance alone [2]. We have also published a figure of merit for the selection of the best family of SiC MOSFETs in terms of device reliability [3]. However, the currently available SiC MOSFETs may or may not maximize the power-conversion efficiency in a specific circuit. Super-junction Si MOSFETs are competitive for many applications [4], and GaN-based high electron mobility transistors (HEMTs) are promising future devices for further increase in the switching frequency [5], [6], [7]. Therefore, we propose in this paper a general approach for the selection of power switches that will reduce the power loss in a specific switch-mode power converter. This method is based on a newly derived equation, which enables circuit designers to use desired circuit parameters for the calculation of the optimum ratio between *on* resistance and output capacitance of a MOSFET. The circuit designers can use this information in combination with other selection criteria, such as reliability [8], short-circuit capability [9], packaging for heat dissipation [10], price, availability, and so on, to decide on the most suitable power MOSFET for their specific applications.

II. THEORETICAL DERIVATION OF NEW CRITERION

In this section, we analyze the impact of a MOSFET's channel width on its power dissipation. Applying the condition for the channel width that minimizes the power dissipation, we derive a criterion for the optimum ratio between the *on* resistance and output capacitance. Irrespective of the MOSFET technology, this criterion presents an approach for choosing a power MOSFET that will reduce power loss in a specific circuit.

The total power dissipation by a MOSFET in a switch-mode power converter consists of two components: Conduction or static power loss due to the *on* resistance and switching or dynamic power loss due to the parasitic capacitances.

There are three parasitic capacitances in every MOSFET structure: gate–drain capacitance (C_{GD}), gate–source capacitance (C_{GS}), and drain–source capacitance (C_{DS}). To facilitate circuit analysis, manufacturer datasheets show the equivalent output (C_{OSS}) and input (C_{ISS}) capacitances:

$$C_{OSS} = C_{DS} + C'_{GD} \tag{1}$$

$$C_{ISS} = C_{GS} + C_{GD}. \tag{2}$$

Both C_{DS} and C_{GD}, as the constituting elements of C_{OSS}, are voltage-dependent capacitances due to the voltage dependence of the depletion layer in the n-type drift region. This voltage dependence is given by [11], [12], [13], [14], [15]:

$$C_{OSS}(V_{DS}) = C_{OSS}(0)\left(1 + V_{DS}/V_{bi}\right)^{-m} \tag{3}$$

where V_{DS} is the voltage between drain and source, $C_{OSS}(0)$ is defined as the output capacitance at $V_{DS} = 0$, V_{bi} is the built-in voltage at the drain-to-body n–p junction, and m is the junction grading coefficient whose value is between 1/2 for the case of an abrupt junction and 1/3 for the case of a linear junction. For high drain-to-source voltages, $V_{DS}/V_{bi} \gg 1$, (3) can be simplified to

$$C_{OSS}(V_{DS}) = C_{OSS}(0)\, V_{bi}^{m} V_{DS}^{-m} \tag{4}$$

It was recently shown that the power dissipation due to charging of this voltage-dependent capacitance to V_{DS} and its discharging to 0 is given by [11]:

$$P_{SW-OSS} = \gamma C_{OSS}(V_{DS})\, V_{DS}^{2} f \tag{5}$$

where f is the switching frequency and $\gamma = 1/(2-m)$. Since $1/3 \leq m \leq 1/2$, the value of γ is in the range between 0.60 and 0.67.

Both C_{DS} and C_{GD} are proportional to the effective channel width of the MOSFET (W): The area of the drain-to-source junction (A_{DS}) is proportional to W, and $C_{DS} = A_{DS}\left(\varepsilon_s/W_{depl}\right)$ where ε_s is the permittivity of semiconductor and W_{depl} is the depletion-layer width of the drain-to-source junction; likewise, the area of the gate-to-drain overlap (A_{GD}) is proportional to W and $C_{GD} = A_{GD}\left(\varepsilon_{ox}/t_{ox}\right)$ where ε_{ox} is the permittivity of gate-oxide and t_{ox} is the gate-oxide thickness. Therefore, (1) shows that C_{OSS} is also proportional to W. Defining $c_{oss/w}$ as the output capacitance per unit of channel width, (5) becomes:

$$P_{SW-OSS} = \gamma c_{oss/w}(V_{DS})\, V_{DS}^{2} f W \tag{6}$$

Regarding the power dissipation due to charging and discharging of the input capacitance, P_{SW-ISS}, we have shown in a recently published paper [2] that this power is independent of the channel width. It should be noted that the external gate resistance and the maximum output current of the driver IC limit the charging and discharging current of C_{ISS}. This impacts the charging and discharging times but not the energy that is stored or dissipated by the C_{ISS} during a switching cycle. Also, the voltage that dominates in the energy dissipation is the voltage between the drain and source terminals (V_{DS}), which is much higher than the gate-to-source voltage (V_{GS}). Consequently, the energy losses caused by V_{GS} are negligible in comparison to the energy losses due to V_{DS}.

Apart from the output and input capacitances, the body diode can contribute to the switching losses due to its reverse-recovery losses. In some circuit configurations, such as H-bridges, the reverse recovery losses can be significant. However, these losses are usually eliminated by connecting a Schottky diode in parallel with the body diode [16]. Therefore, this power loss can be neglected for the purpose of selecting a MOSFET that will minimize the power dissipation. With these considerations, the total switching power dissipation can be expressed as:

$$P_{SW} = \gamma c_{oss/w}(V_{DS})\, V_{DS}^{2} f W + P_{SW-ISS} \tag{7}$$

The conduction power dissipation is due to the *on* resistance, and is given by:

$$P_{CON} = D I^{2} R_{ON} \tag{8}$$

where R_{ON} is the *on* resistance, D is the duty cycle and I is the root-mean-square value of the drain current. The R_{ON} consists of several internal resistances in the MOSFET structure: the source contact resistance (R_{CS}), the source region resistance (R_{N+}), the channel resistance (R_{CH}), the accumulation resistance (R_A), the JFET resistance R_{JFET}, the drift region resistance (R_{drift}), the N^+ substrate resistance (R_{SUB}), and the drain contact resistance (R_{DS}) [14]. However, the contribution of R_{CH}, R_A, R_{JFET}, and R_{drift} is significantly higher than the other resistances, therefore, R_{ON} is approximately given by [14]:

$$R_{ON} = R_{CH} + R_A + R_{JFET} + R_{drift} \tag{9}$$

In (9), all resulting resistances are inversely proportional to the effective channel width, W [13], [14]. Defining r_{on-w} as the specific *on* resistance of a MOSFET with a unit of channel width, the total *on* resistance is given by:

$$R_{ON} = r_{on-w}/W \tag{10}$$

From (8) and (10), the conduction power dissipation can be expressed as:

$$P_{CON} = \frac{DI^2 r_{on-w}}{W} \tag{11}$$

Adding the switching power dissipation and the conduction power dissipation from (7) and (14), we obtain the following equation for the total power dissipation:

$$P_{TOT} = \frac{DI^2 r_{on-w}}{W} + \gamma c_{\frac{oss}{w}} (V_{DS}) V_{DS}^2 fW + P_{SW-ISS} \tag{12}$$

The first derivative of (12) is set to zero to minimize the overall power losses with reference to W,

$$\frac{dP_{TOT}}{dW} = \gamma c_{oss/w} (V_{DS}) V_{DS}^2 f - \frac{DI^2 r_{on-w}}{W^2} = 0 \tag{13}$$

which results in the following equation for the optimum channel width:

$$W_{opt} = \sqrt{DI^2 r_{on-w} \Big/ \gamma c_{oss/w} (V_{DS}) V_{DS}^2 f} \tag{14}$$

Given that the optimum output capacitance is $C_{OSS-opt} = c_{oss/w} W_{opt}$ and the optimum R_{ON} is $R_{ON-opt} = r_{on-w}/W_{opt}$, (14) can be written in terms of $C_{OSS-opt}$ and R_{ON-opt}:

$$W_{opt} = \sqrt{DI^2 R_{ON-opt} W_{opt}^2 \Big/ \gamma C_{OSS-opt} (V_{DS}) V_{DS}^2 f} \tag{15}$$

which leads to the following condition for the ratio between the optimum R_{ON} and the optimum output capacitance:

$$R_{ON-opt} \Big/ C_{OSS-opt} = \gamma V_{DS}^2 f \Big/ DI^2 \tag{16}$$

Equation (16) shows that the ratio of optimum R_{ON-opt} and $C_{OSS-opt}$ is determined by the circuit parameters V_{DS}, I, f, and D, since the value of the only non-circuit parameter (γ) is in the narrow range between 0.60 and 0.67. This means that, based on the specific circuit parameters, a circuit designer can use (16) to calculate the ratio between R_{ON-opt} and $C_{OSS-opt}$ of a MOSFET without the need to know the effective channel width or any other technological parameter. The designer can then use the values of R_{ON-opt} and $C_{OSS-opt}$, provided in manufacturers datasheets, to select a MOSFET that satisfies the condition in (16) knowing that such a MOSFET will minimize its power dissipation for the specific circuit parameters.

It is possible that MOSFETs fabricated in different technologies, such as SiC- and Si-based MOSFETs, result in the same optimum value of $R_{ON-opt}/C_{OSS-opt}$ while having different individual values of R_{ON-opt} and $C_{OSS-opt}$. Clearly, the MOSFET with the smaller R_{ON-opt} and $C_{OSS-opt}$ values will result in smaller power dissipation, whereas the optimum ratio $R_{ON-opt}/C_{OSS-opt}$ will ensure minimum power dissipation achievable by that specific family of MOSFETs.

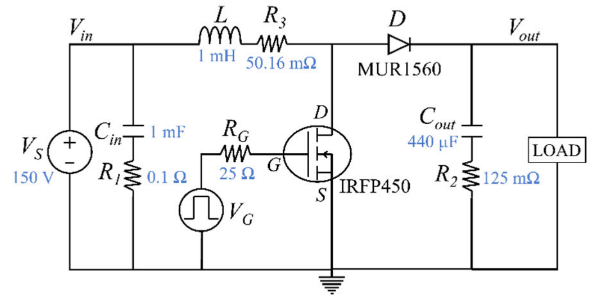


FIGURE 1. A standard boost converter circuit.

III. EXPERIMENTAL VERIFICATION

A conventional boost converter, shown in Fig.1, is utilized to demonstrate the effect of channel width on power dissipation and to show that a MOSFET selected according to the criterion in (16) minimizes the total power dissipation. This boost converter was presented in [17] with the following circuit parameters: input DC voltage $V_{IN} = 150$ V, output DC voltage $V_{OUT} = 300$ V, output power $P_{OUT} = 750$ W, maximum inductor current ripple $\Delta iL = 10$ A, and maximum voltage ripple $\Delta V_{OUT} = 3$ V.

It is important to note that the dependence of power dissipation on the channel width of a MOSFET cannot be demonstrated experimentally because the channel width of a fabricated MOSFET cannot be varied. However, this effect can be demonstrated by simulation, using adequately calibrated device model and parameters. Several studies examined how well SPICE models fit the characteristics of 4H-SiC power MOSFETs in both actual and simulated devices [18], [19]. A 10 kV DMOSFET was tested and simulated using a SPICE LEVEL 1 model that had been modified to account for temperature effects [19]. Tanner et al. [18] published a selection of SPICE LEVEL 3 parameters for SiC MOSFETs that provides an adequate match to measured characteristics.

In this section, we use SPICE LEVEL 3 MOSFET model, which is relatively simple, provides sufficient

TABLE 1. Static and dynamic parameters for spice level 3 model.

SPICE keyword (*LEVEL=3*)	NAME	Unit
W	Gate width	m
L	Gate length	m
KP	Transconductance parameter	A/V^2
Vto	Zero-bias threshold voltage	V
THETA	Mobility modulation constant	V^{-1}
NFS	Subthreshold-current fitting parameter	cm^{-2}V^{-1}
Tox	Gate oxide thickness	m
Cgso	Gate–source overlap capacitance per gate width	F/m
Cgdo	Gate–drain overlap capacitance per gate width	F/m
Cjo	Zero-bias capacitance	F
Mj	Grading coefficient	-
PB	Built-in potential	V

accuracy, and enables the model parameters to be set to match measured current–voltage and capacitance–voltage characteristics. In the first subsection, we show measured characteristics of a commercially available SiC power MOSFET (C3M0350120D) and the related extraction of SPICE parameters. In the second subsection, we show the dependence of power dissipation on the channel width to demonstrate that the minimum power dissipation corresponds to the newly proposed criterion by (16).

A. PARAMETER EXTRACTION FOR SPICE LEVEL 3 MOSFET MODEL

The SPICE parameters in MOSFET LEVEL 3 model, required for simulation of the boost converter shown in Fig. 1, are listed in Table 1.

SPICE uses these parameters in the following equations for the current–voltage characteristics:

For $V_{GS} \geq V_{TS}$

$$V_{TS} = \boldsymbol{Vto} + n_s V_t \tag{17}$$

$$n_s = 1 + \frac{q\boldsymbol{NFS} \cdot \boldsymbol{Tox}}{\varepsilon_{ox}} \tag{18}$$

$$I_D(V_{GS}) = \frac{\boldsymbol{KP}.\boldsymbol{W}}{\boldsymbol{L}\left[1 + \boldsymbol{THETA}\,(V_{GS} - \boldsymbol{Vto})\right]}\left(V_{GS} - \boldsymbol{Vto}\right) V_{DS} \tag{19}$$

For $V_{GS} < V_{TS}$

$$I_D = I_D \exp\left[\frac{-(V_{TS} - V_{GS})}{n_s V_t}\right] \tag{20}$$

In (17)–(20), q is the electron charge, I_D is the drain current, n_s is a coefficient analogous to the emission coefficient n of diodes, V_{TS} is the threshold voltage, ε_{ox} is the permittivity of gate oxide, V_t is the thermal voltage, V_{GS} is the gate-to-source voltage, and V_{DS} is the drain-to-source voltage. Power MOSFETs operate as switches, and the *on* mode of the device relates to high V_{GS} and small V_{DS}, whereas the *off* mode relates to sub-threshold V_{GS} (small current). The selected parameters correspond to the transfer characteristic for small V_{DS} values. The equation for sub-threshold current (I_D for $V_{GS} < V_{TS}$) takes into consideration the gradual and nonlinear rise in drain current with gate voltage. The default value of the parameter ***THETA*** in SPICE is ***THETA*** $= 0$, which can be used as the initial value for the nonlinear fitting. The parameter ***NFS***, on the other hand, can be determined to fit the sub-threshold current of the transfer characteristic. In the case of SiC power MOSFETs, a high ***NFS*** value corresponds to a high density of near interface-traps (NITs), causing the slow drain-current increase with gate voltage [18].

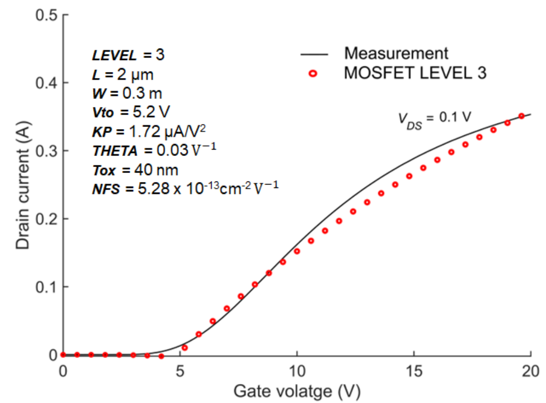


FIGURE 2. Transfer characteristics of SiC power MOSFET: measurements (line) and simulation with the extracted parameters (circles).

It is possible to get the MOSFET LEVEL 3 parameters by nonlinear fitting to experimental data. The transfer characteristic, shown by the solid line in Fig. 2, was measured using Agilent B1505A power device analyzer. The gate-oxide thickness was measured using Fowler-Nordheim tunneling method [21], and the value is ***Tox***$=$ 40 nm. After the nonlinear fitting, the parameter values are entered into SPICE and the simulated transfer characteristic for is compared with the experimental results shown in Fig. 2.

The channel width and length, ***W*** and ***L***, are technological parameters that are designed by the manufacturers and are usually not disclosed. However, the ratio of these parameters, $\boldsymbol{W}/\boldsymbol{L}$, can determined from the measured slope of the transfer characteristic. By assuming the typical channel length of $\boldsymbol{L} = 2\ \mu$m, the effective channel width for this MOSFET is $\boldsymbol{W} = 0.3$ m.

The MOSFET LEVEL 3 model additionally incorporates dynamic parameters, which consist of voltage independent gate-to-drain and gate-to-source overlap capacitances, ***Cgdo*** and ***Cgso*** respectively, which are defined as capacitances per unit channel-width.

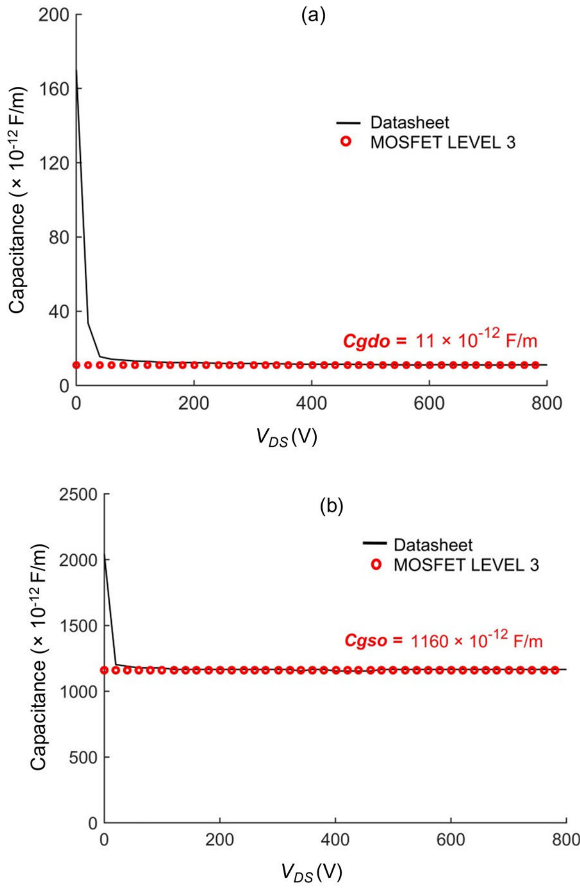


FIGURE 3. Verification of SiC MOSFET LEVEL 3 dynamic parameters (a) *Cgdo*, (b) *Cgso*.

It can be observed from datasheet that the C_{GS} and C_{GD} are essentially constant for most of the drain-voltage range. The energy dissipated by constant capacitance in SPICE is close to energy dissipated by the voltage-dependent capacitance because the capacitance change is limited to very small voltages. The data for C_{GS} and C_{GD} is taken from datasheet and subsequently divided by the effective channel-width to obtain the values of ***Cgdo*** and ***Cgso***. Figure 3 shows the extracted capacitance data from datasheet for SiC MOSFET.

Also, a diode model for the MOSFET P-N junction is also included in the MOSFET LEVEL 3 model [20], [22], and it may be used to simulate the non-linear C_{DS} for power MOSFETs with the SPICE parameters $\boldsymbol{C_{jo}}$, $\boldsymbol{PB}$, and $\boldsymbol{M_j}$. SPICE uses these parameters in the following equation:

$$C_{DS} = \boldsymbol{C_{jo}} \left[1 + \frac{V_{DS}}{\boldsymbol{PB}} \right]^{-\boldsymbol{Mj}} \tag{21}$$

These parameters can also be determined by non-linear fitting to the measured characteristic shown in Fig. 4 by the solid line. The initial value of $\boldsymbol{C_{jo}}$ should be the C_{DS} value from the datasheet at $V_{DS} = 0$ V. The initial value for $\boldsymbol{M_j}$ can be set to 0.5, and the initial value for $\boldsymbol{PB}$ can be set to 2 V.

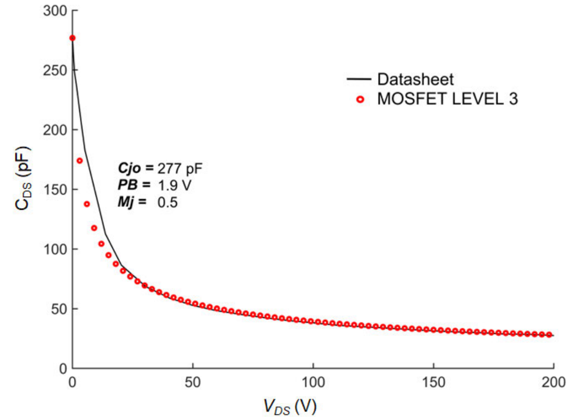


FIGURE 4. C_{DS}–V_{DS} **characteristic of SiC power MOSFET: measurements (line) and (21) with the extracted parameters (circles).**

The result of the non-linear fitting and the obtained values of these SPICE parameters are shown in Fig.4.

B. RESULTS

Based on the circuit parameters of the specific boost converter, shown in Fig. 1, the optimum $R_{ON-opt}/C_{OSS-opt}$ is

$$R_{ON-opt}/C_{oss-opt} = \gamma V_{DS}^2 f \Big/ DI^2 = \frac{0.65 \times 300^2 \times 10^5}{0.5 \times (5)^2} = 4.3 \times 10^8 \Omega/\mathrm{F} \tag{22}$$

This optimum value is 30.8 times smaller than the $R_{ON-opt}/C_{OSS-opt}$ value of the SiC power MOSFET used in this analysis. This result shows that the *on* resistance of the MOSFET is $\sqrt{30.8} = 5.5$ times larger and its capacitance is 5.55 times smaller than the optimum value, which means that a MOSFET with 5.5 larger effective channel width is required to minimize the power dissipation. This means a reduction of the *on* resistance from the actual 350 mΩ to around 60 mΩ and an increase in the output capacitance at $V_{DS} = 300$ V from the actual 26.4 pF to around 150 pF.

This conclusion is confirmed by the simulation results shown by the symbols in Fig. 5, which are in a good agreement with the theoretical equations (lines): (6) for the switching loss due to the output capacitance (P_{SW-OSS}), (8) for the conduction loss (P_{CON}), and (12) for the sum of these two losses ($P_{SW-OSS} + P_{CON} = P_{TOT} - P_{SW-ISS}$). As expected, the results shown in Fig. 5 illustrate that the conduction loss drops as the channel width is increased, due to proportional reduction in *on* resistance [(8) and (10)], whereas the switching loss increases proportionally with the channel width, due to the proportional increase in the output capacitance [(5) and (6)]. The minimum power dissipation corresponds to the channel-width scaling factor of 5.5, as determined from the newly proposed criterion.

Figure 5 also shows that the dependence of the total power dissipation on the channel-width scaling factor does not exhibit a sharp minimum at the value of 5.5. The implication

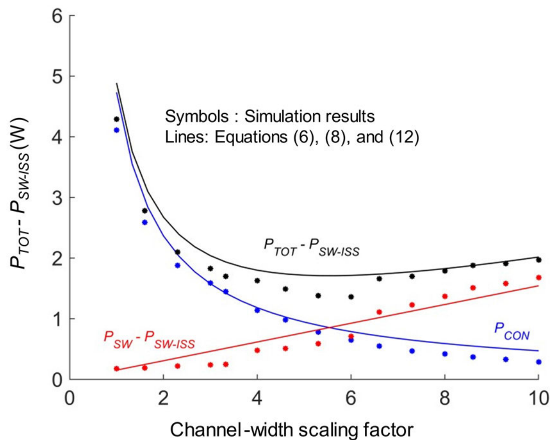


FIGURE 5. The simulation results (symbols) and (12) (the black line) demonstrate that C3M0350120D does not minimize the power dissipation. The selected MOSFET corresponds to the channel-width scaling factor of 1, whereas the minimum power dissipation is for a MOSFET with 5.5 times larger channel width (the scaling factor of around 5.5). The channel-width independent power dissipation is P_{SW-ISS} = 0.24 W.

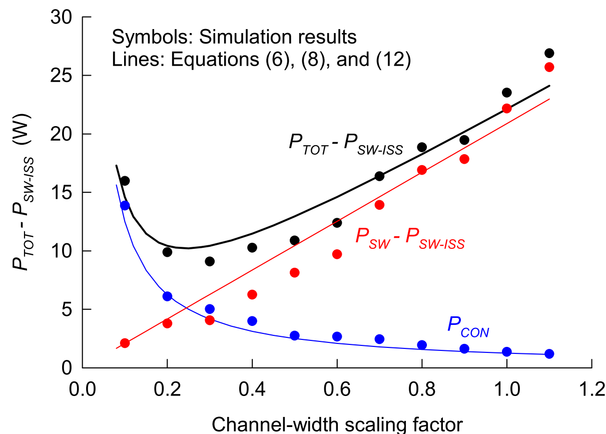


FIGURE 6. The simulation results (symbols) and (12) (the black line) demonstrate that IRFP450, which is the MOSFET selected in ref. [16] for the circuit shown in Fig. 1, does not minimize the power dissipation. The selected MOSFET corresponds to the channel-width scaling factor of 1, whereas the minimum power dissipation is for a MOSFET with three times smaller channel width (the scaling factor of around 0.3). The channel-width independent power dissipation is P_{SW-ISS} = 16 W.

is that a channel-width scaling factor as small as 4 is also acceptable, but this value is still much larger than the channel-width scaling factor of 1 for the MOSFET selected without the application of the newly proposed criterion. The practical implication is that either a larger MOSFET or four MOSFETs operating in parallel is required to minimize the power dissipation.

IV. APPLICATION OF NEW CRITERION: EXAMPLE

The MOSFET used by the authors of ref. [17] was IRFP450, and we will show in this section that this MOSFET does not minimize the power dissipation. To minimize the power dissipation, we need a MOSFET with $R_{ON-opt}/C_{OSS-opt}$ according to the criterion in (16). Based on the circuit parameters of the specific boost converter, shown in Fig. 1, the optimum $R_{ON-opt}/C_{OSS-opt}$ is:

$$R_{ON-opt}/C_{oss-opt} = \gamma V_{DS}^2 f / DI^2 = \frac{0.65 \times 300^2 \times 10^5}{0.5 \times (2.5)^2} = 1.9 \times 10^9 \Omega/\mathrm{F} \quad (23)$$

The MOSFET used in [17] is IRFP450, which also comes with a SPICE model provided by the manufacturer. The R_{ON} of this MOSFET is 0.4 Ω and C_{OSS} in the SPICE model is 3.57 nF. Hence, $R_{ON}/C_{OSS} = 0.112 \times 10^9 \Omega/\mathrm{F}$, which is much smaller than the optimum value of 1.6×10^9 Ω/F obtained by the criterion in (16). This means that the choice of the relatively small R_{ON} resulted in a too large C_{OSS}, and a power loss that will be higher than the minimum power dissipation due the switching losses by the output capacitance. The simulation results shown in Fig. 6 illustrates this scenario. The good agreement between the simulation results (the symbols in Fig. 6) and (12) (the black line in Fig. 6) confirms that the minimum power dissipation corresponds to a smaller channel width that is 0.3 times the channel width of IRFP450. The larger than optimum channel width and the corresponding smaller R_{ON} reduce the conduction losses, but the larger C_{OSS} due to the larger channel width causes a much larger dynamic power dissipation. This confirms that the smaller R_{ON}/C_{OSS} ratio than the derived optimum in (16) means that R_{ON} is too small and C_{OSS} is too large.

Searching through datasheets of available MOSFETs, we found a MOSFET with *on* resistance of 95mΩ and output capacitance at $V_{DS} = 300$ V of 58 pF, which has the ratio $R_{ON-opt}/C_{OSS-opt} = 1.6 \times 10^9$ Ω/F. This MOSFET is in the family of super-junction MOSFETs fabricated by Rohm, and its part number is R6035VNX. The channel width of this MOSFET is not provided by the manufacturer, but the criterion given by (17) should guarantee that this MOSFET minimizes the power dissipation.

The manufacturer provides LTSPICE model for R6035VNX to enable circuit designers to design their circuit using SPICE-based simulations. To demonstrate that the selected MOSFET minimizes the power dissipation, we performed simulations with scaled channel width above its nominal value (scaling factors larger than 1) and below its nominal value (scaling factors smaller than 1). We were able to do these simulations because the parameters of the provided MOSFET model could be changed in the "SPICE model editor." The provided LTSPICE model used the transconductance parameter, $\boldsymbol{KP}$, rather than the channel width, so we scaled $\boldsymbol{KP}$ knowing that:

$$\boldsymbol{KP} = \mu_n C_{ox}(\boldsymbol{W}/\boldsymbol{L}) \quad (24)$$

In (24), μ_n is the channel-carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and $\boldsymbol{L}$ is the channel length. As discussed in Section II, the R_{ON} of different MOSFETs (parts) in a family of MOSFETs is adjusted by varying the channel width, $\boldsymbol{W}$. This means that μ_n, C_{ox}, and $\boldsymbol{L}$, are

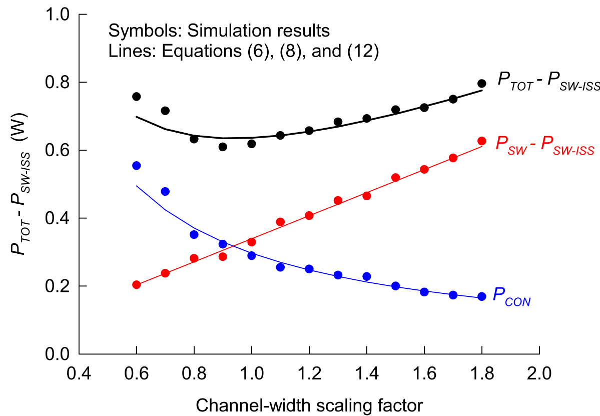


FIGURE 7. The simulation results (symbols) and (12) (the black line) demonstrate that the minimum power dissipation is for the channel-width scaling factor of 1, which corresponds to the nominal channel width of the selected MOSFET (R6035VNX). The channel-width independent power dissipation is P_{SW-ISS} = 25.2 W.

constant in a group of MOSFETs fabricated with similar technology. Therefore, scaling ***KP*** values above and below its nominal value was equivalent to scaling the channel width by the same factor.

Figure 7 shows that the minimum power dissipation is for the nominal channel width, corresponding to the channel-width scaling factor of 1. This verifies that a MOSFET can be chosen using (16) to reduce power dissipation, even when the channel-width values are not provided by the device manufacturers.

V. CONCLUSION

Power MOSFETs with larger effective channel widths (a large number of cells) exhibit small *on* resistances, but they may not provide the minimum power dissipation because the increased output capacitances result in increased dynamic power dissipation. There is an optimum channel width that minimizes power dissipation, but this parameter is not available to circuit designers. In this paper, we have derived a general criterion for the ratio of *on* resistance and output capacitance, $R_{ON-opt}/C_{OSS-opt}$, given by (16). The numerical value of the optimum $R_{ON-opt}/C_{OSS-opt}$ ratio depends on the circuit parameters (voltage, current, duty cycle, and frequency). Given that the *on*resistance and the output capacitance are provided by the MOSFET manufacturers in the device datasheets, the circuit designers can search for a MOSFET that satisfies the optimum $R_{ON-opt}/C_{OSS-opt}$ ratio, knowing that this will minimize the power dissipation irrespective of the specific technology, manufacturer, and device family. The proposed criterion is verified by using SiC MOSFET LEVEL 3 parameters through nonlinear fitting to experimental data and circuit simulation using LTSPICE MOSFET models provided by the device manufacturers. An example of a published typical boost converter was used to illustrate the power-minimization effect that can be achieved by applying the proposed criterion.

REFERENCES

[1] J. Wang, H. S. Chung, and R. T. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013, doi: 10.1109/TPEL.2012.2195332.

[2] U. Jadli, F. Mohd-Yasin, H. A. Moghadam, P. Pande, M. Chaturvedi, and S. Dimitrijev, "A method for selection of power MOSFETs to minimize power dissipation," *Electronics*, vol. 10, no. 17, p. 2150, Sep. 2021, doi: 10.3390/electronics10172150.

[3] M. Chaturvedi, S. Dimitrijev, D. Haasmann, H. A. Moghadam, P. Pande, and U. Jadli, "A figure of merit for selection of the best family of SiC power MOSFETs," *Electronics*, vol. 11, no. 9, p. 1433, Apr. 2022, doi: 10.3390/electronics11091433.

[4] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction power devices, history, development, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 713–727, Mar. 2017, doi: 10.1109/TED.2017.2658344.

[5] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[6] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices—Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015, doi: 10.1109/TED.2014.2368274.

[7] E. Santi, K. Peng, H. A. Mantooth, and J. L. Hudgins, "Modeling of wide-bandgap power semiconductor devices—Part II," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 434–442, Feb. 2015, doi: 10.1109/TED.2014.2373373.

[8] U. Jadli, F. Mohd-Yasin, H. A. Moghadam, J. R. Nicholls, P. Pande, and S. Dimitrijev, "A simple equation for the energy stored by voltage-dependent capacitances," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12629–12632, Dec. 2020, doi: 10.1109/TPEL.2020.2993639.

[9] J. Jordan, V. Esteve, R. Garcia-Gil, E. Sanchis, E. Maset, and E. Dede, "New power MOSFET selection method to avoid failures," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, Mar. 2004, pp. 1257–1261, doi: 10.1109/APEC.2004.1295984.

[10] A. Kanale and B. J. Baliga, "Selection methodology for Si power MOSFETs used to enhance SiC power MOSFET short-circuit capability with the BaSIC(EMM) topology," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8243–8252, Jul. 2021, doi: 10.1109/TPEL.2020.3043281.

[11] D. Kim, M. S. Won, J. Jang, S. Kim, and C. Oh, "Development of solderable layer on power MOSFET for double-side bonding," *Microelectron. Rel.*, vol. 129, Feb. 2022, Art. no. 114482, doi: 10.1016/j.microrel.2022.114482.

[12] R. W. Erickson and D. Maksimović, "Switch realization," in *Fundamentals of Power Electronics*. New York, NY, USA: Chapman & Hall, 2001, pp. 63–89, doi: 10.1007/978-3-030-43881-4_4.

[13] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985–995, Feb. 2015, doi: 10.1109/TPEL.2014.2313611.

[14] S. Dimitrijev, *Principles of Semiconductor Devices*. New York, NY, USA: Oxford Univ. Press, pp. 270–271, 2012.

[15] B. J. Baliga, "Power MOSFETs," in *fundaments of Power Semiconductor Devices*. Raleigh, NC, USA: Springer, 2019, pp. 413–449.

[16] A. Kumar, S. Bhattacharya, and J. Baliga, "Influence of the inverter dead-time on the reverse recovery characteristics of 3.3-kV SiC MOSFETs and JBSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, Oct. 2022, pp. 1–7, doi: 10.1109/ECCE50734.2022.9947390.

[17] Z. Ivanovic, B. Blanusa, and M. Knezic, "Analytical power losses model of boost rectifier," *IET Power Electron.*, vol. 7, no. 8, pp. 2093–2102, Aug. 2014, doi: 10.1049/iet-pel.2013.0422.

[18] P. Tanner, S. Dimitrijev, H. A. Moghadam, A. Aminbeidokhti, and J. S. Han, "Selection of SPICE parameters and equations for effective simulation of circuits with 4H-SiC power MOSFETs," *Mater. Sci. Forum*, vols. 778–780, pp. 997–1000, Feb. 2014, doi: 10.4028/www.scientific.net/msf.778-780.997.

[19] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "Characterization, modeling, and application of 10-kV SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008, doi: 10.1109/TED.2008.926650.

[20] U. Jadli, F. Mohd-Yasin, H. A. Moghadam, P. Pande, M. Chaturvedi, and S. Dimitrijev, "Modeling power GaN-HEMTs using standard MOSFET equations and parameters in SPICE," *Electronics*, vol. 10, no. 2, p. 130, Jan. 2021, doi: 10.3390/electronics10020130.

[21] M. Chaturvedi, S. Dimitrijev, D. Haasmann, H. A. Moghadam, P. Pande, and U. Jadli, "Comparison of commercial planar and trench SiC MOSFETs by electrical characterization of performance-degrading near-interface traps," *IEEE Trans. Electron Devices*, vol. 69, no. 11, pp. 6225–6230, Nov. 2022, doi: 10.1109/TED.2022.3206184.

[22] E. Bottaro, S. A. Rizzo, and N. Salerno, "Circuit models of power MOSFETs leading the way of GaN HEMT modelling—A review," *Energies*, vol. 15, no. 9, p. 3415, May 2022, doi: 10.3390/en15093415.

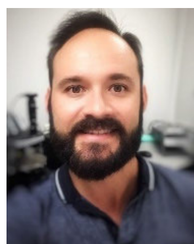
VIKAS JOSHI was born in Pithoragarh, Uttarakhand, India, in 1997. He received the B.Tech. degree in electrical engineering from Graphic Era (Deemed to be University), Dehradun, India, in 2021, where he is currently pursuing the M.Tech. degree in VLSI design and systems.

UTKARSH JADLI was born in Pauri, Pauri Garhwal, Uttarakhand, India, in 1994. He received the B.Tech. degree in electrical and electronics engineering and the M.Tech. degree in control systems from Graphic Era (Deemed to be University), Dehradun, India, in 2015 and 2017, respectively, and the Ph.D. degree from the Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, Australia, in 2021.

PEYUSH PANDE (Member, IEEE) received the B.Eng. degree in electronics and telecommunication engineering from Sant Gadge Baba Amravati University, Amravati, India, in 2002, the M.Eng. degree in VLSI system design from Griffith University, Australia, in 2004, and the Ph.D. degree from the Queensland Micro- and Nanotechnology Centre, Griffith University, in 2020. He is currently an Associate Professor with Graphic Era (Deemed to be University), Dehradun, India. His current research interests include the physics and engineering of metal-oxide-SiC device structures, design, and electrical characterization of wide bandgap power semiconductor (SiC and GaN) devices.

MAYANK CHATURVEDI received the B.Tech. degree in electrical and electronics engineering from H. N. B. Garhwal University, Srinagar, India, in 2008, the M.Tech. degree in control systems from Graphic Era (Deemed to be University), Dehradun, India, in 2014. He is currently pursuing the Ph.D. degree with the Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, Australia.

His current research interests include electrical characterization of power semiconductor devices and wide bandgap semiconductor materials.



DANIEL HAASMANN received the bachelor's degree (Hons.) in microelectronic engineering from Griffith University, Brisbane, Australia, in 2008, and the Ph.D. degree from the Queensland Micro- and Nanotechnology Centre, Griffith University, in 2015. He is currently a Lecturer with the School of Engineering and Built Environment, Griffith University, where he is also an active Researcher with the Queensland Micro- and Nanotechnology Centre. His current research interests include 4H-SiC gate-oxide growth and electrical characterization of SiC MOS devices.

SIMA DIMITRIJEV (Life Senior Member, IEEE) received the B.Eng., M.Sc., and Ph.D. degrees in electronic engineering from the University of Nis, Nis, Yugoslavia, in 1982, 1985, and 1989, respectively.

He is currently a Professor with the School of Engineering and Built Environment and the Deputy Director of the Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, Australia. He is the author of *Principles of Semiconductor Devices* (2nd edition) (New York: Oxford University Press, 2011).