IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 26 September 2023, accepted 13 October 2023, date of publication 17 October 2023, date of current version 30 October 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3325212

RESEARCH ARTICLE

A Seventeen-Level Step-Up Switched-Capacitor-Based Multilevel Inverter With Reduced Charging Current Stress on Capacitors for PV Applications

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This work was supported by Finnish Electronic Library (FinElib) and Aalto university, Finland, under the FinElib Consortium's Agreement with IEEE.

ABSTRACT Because of serious challenges such as air pollution, global warming, and fossil fuels limitations, renewable energy sources such as photovoltaic (PV) systems are increasingly being integrated into the power systems around the world. In this article, a new grid-tied system is proposed for PV applications which consists of an improved flyback DC-DC converter and a new switched-capacitor (SC) based multilevel inverter. Over previously introduced topologies in the same class, the proposed SC-based multilevel inverter has many advantages like reduced number of power switches and DC voltage sources, and also increased number of voltage levels produced at the output. In the proposed structure, one of the most important problems of the capacitive switching inverters, i.e. the occurrence of the impact currents during charging capacitors, is solved by using an inductor with a parallel diode in the capacitive charging current path. This increases the efficiency of the converter and reduces the charging current stress on the capacitors. To validate the performance of the proposed topology, comprehensive experiments and comparisons have been performed and presented. In the experiments, a current controller is used to control the amount of active and reactive power injected to the grid by the proposed grid-tied 17-levels inverter.

INDEX TERMS Switched capacitor, multilevel inverter, capacitor charging spike, solar energy, PV applications.

I. INTRODUCTION

Todays, global warming, increasing energy demand, increased carbon emissions, and fossil fuels limitations are definitely considered of the most important challenges around world [1], [2]. To solve and/or mitigate these concerns, different solutions and technologies have been introduced. Among these solutions, integration of renewable energy sources (RESs) into power systems can be named as one of the most popular and widely accepted solutions. At the large family of RESs, photovoltaic (PV) systems are one of the widely used members [3], [4]. However, to employ and integrate these sources into the power systems, power electronic based interfaces, i.e., power converters, are

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

required [5], [6], [7]. It is worth noting that besides RES applications, power converters are widely used in numerous modern applications [8], [9], [10]. Among these converters, multi-level inverters (MLI) are one of the most popular solutions to improve the performance of electric vehicles, renewable energy systems (RES) such as photovoltaic (PV) systems, and other power electronic devices in medium- and high-power applications [11], [12], [13], [14], [15]. Compared to other inverter topologies, these inverters benefit from many merits like producing a staircase voltage waveform of the output with lower total harmonic distortion (THD) and higher power quality [16], [17], [18]. The conventional MLIs are generally categorized into three configurations: flying capacitors, cascaded H-bridge (CHB), and diode clamped inverters [19], [20], [21]. Although these structures have a lot of benefits, they employ large numbers of power switches and power dc sources, and also large capacitor banks. In addition, a charge balancing control technique is needed in these inverters since the voltage of their capacitors will be discharged automatically. Up to now, several charge balancing methods along with their circuits have been introduced to control the DC link voltages of these structures [22], [23], [24]. In [22], [23], and [24], the duty cycle used for the flying capacitor of DC bus of MLIs was regulated by utilizing the existing redundancy switching state where the accuracy of the presented process depends on designing a closed-loop control method. In the recent years, numerous MLIs have been developed based on switched-capacitor (SC) circuits. Compared to other inverters, the SC-based MLIs can generate more voltage levels at the output and decrease the number of the needed DC supplies [25], [26]. Note that in these MLIs, an H-bridge inverter is generally employed to produce the negative output voltage levels causing the increased number of power elements for them which in turn will increase their overall power loss. In [27], two hybrid MLIs with an enhanced total standing voltage (TSV) of power switches have been introduced based on a new SC basic unit which includes two power switches, one diode, and one capacitor. Note that both of these MLIs need an H-bridge circuit to alternate their output voltages. Both MLIs of [9] and [13] have been analyzed for asymmetric DC source structure. These topologies are able to produce a large number of output voltage levels by using fewest power switches. In [28], a step-up MLI structure with multiple charging and discharging probabilities of the capacitors has been presented. This inverter needs a great number of bidirectional switches to enhance the charging possibilities which is undesirable. Another drawback of this inverter is that the more the level of its output voltage increases, the more its TSV increases. In [29], a high step-up MLI topology has been introduced tolerating high TSV in greater output voltage levels. In [30], symmetrical and asymmetrical SC-based MLI structures have been developed which employ fewer power switches and drivers. The basic unit of this inverter consists of one DC source, two capacitors, ten power switches, and one diode. Moreover, it can produce a 9-level output voltage. This MLI can stand higher values of TSV when the output voltage levels increase. One of the most challenging restrictions of SC-based MLIs is the high voltage stress across their switches and diodes while working in the step-up mode. This problem increases the overall cost of these kind of MLIs. A new Extended Multilevel Inverter topology with reduced switch count and voltage stress has been proposed in [31]. This multilevel inverter needs fewer elements, fewer input dc supplies, and gate drives. In addition, voltage stress is also low. So that, the overall costs and complexity are greatly reduced, especially for higher voltage levels. In [32] a new symmetric switched DC structure has been presented with a reduced elements compared to the traditional topologies. In [33], A new switched capacitor-based multilevel inverter with decreased power electronic elements count is introduced, which has the voltage boosting capability using switched capacitor units and applying an appropriate control system. This structure also has another advantage of a decreased voltage stress on power electronic switches. A modified self-balanced switched-capacitor thirteen-level structures with reduced Capacitors Count have been presented in [34]. In the mentioned paper, In, two simplified switched capacitors units are developed to replace the double-mode switched capacitor unit utilized in [35]. Also, a new seven-level switched capacitor-based multilevel inverter with reduced circuit components is presented in [36]. The needed of a voltage boosting feature for MLIs is necessary for the fuel cell, solar PV, and battery-based applications. In order to obtain to this aim, in [37], a new structure of MLIs with voltage boosting feature and reduced circuit elements has been presented. The suggested structure uses of eleven power semiconductor devices, one switched capacitor unit, and two input dc power supply.

In [25] and [38], a new kind of SC-based MLIs has been developed to obtain a large number of output voltage levels with minimum number of circuit elements such as switches. These MLIs utilize a series-parallel switching technique enabling them to enhance the system flexibility by switching between several capacitors in series or parallel modes. By using these topologies, the overall efficiency of the system can be successfully increased. In [27] and [39], new cascade and hybrid SC-based MLIs with modular structures have been presented which are able to generate more voltage levels at the output port by using the least number of power switches. However, these topologies need full H-bridge units and isolated DC supplies to change the polarity of output voltage, which in turn increases their overall conduction losses and the number of power switches and drivers. In [40], the authors have presented a 17-level SC MLI for renewable energy conversion systems. In [41], a square T-type module with fewer number of power components is presented for asymmetrical MLIs. In [42], Majumdar et al. developed an optimum decreased components multicell MLI for lower standing voltage. In [43], Barzegarkhoo et al. presented a generalized power conversion topology for a single-phase

SC MLI by utilizing a new multiple DC link producer with decreased number of switches. It is noteworthy that since one of the serious problems of the SC-based MLIs is their capacitors' current spikes, so far, several solutions have been introduced to overcome this drawback. Also, in [44], Zamiri et al. presented a new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components. This topology has the drawback of capacitor charging spike. For instance, in [45], a block, including an inductor in parallel with a diode, was used to solve the aforementioned problem.

Grid-connected photovoltaic (PV) topologies with a common-ground (CG) circuit architecture exhibit some excellent features in removing the leakage current challenge and enhance the overall efficiency [45], [46], [47], [48]. Recently, some single-phase multilevel inverters have been presented for PV applications [49], [50]. A new common grounded switched-capacitor based inverter is presented in [51]. In this topology the negative terminal of input dc source is tied to null of the power grid, directedly. Therefore, the proposed topology can provide common grounded strategy and can eliminate the leakage current, completely. A new Dual-Mode Switched-Capacitor Five-Level topology With Common-Ground feature has been presented in [52].

Here, a new system is presented which can be connected to the electric grid directly. This system consists of two-part: a flyback converter, and a new SC-based MLI. The modified MLI can produce multiple DC-link voltages. It should be noted that all capacitors are charged to the desirable values by using binary asymmetrical patterns without employing any additional circuits. Using the modified MLI, the performance of the proposed system is improved due to the inherent boosting ability and unipolar PWM technique. In this system, by using the SC module and the virtual DC connection method, the voltage boosting feature can be provided without using any additional boosting stage. In this topology, the DC-DC flyback converter is used not only to apply the maximum power point tracking (MPPT) algorithm but also to provide two independent DC voltages with a single input DC source. Also, due to control the amount of current injected to the power grid, a precise current controller (CC) along with a small inductor-based filter are employed. Generally, the modified topology provides a fast and robust dynamic response in regulating the amount of the active and reactive powers injected to the grid. The performance of the modified MLI is validated by comprehensive experimental and comparison results.

II. MODIFIED MULTILEVEL INVERTER

Fig. 1 (a) shows the basic circuit of the modified MLI. As seen, this basic unit consists of one DC voltage source, two diodes (D_1 and D_2), one capacitor (C_1), one small inductor (L_C), and two power switches (S_1 and S_2). Figs. 1(b) and 1(c) show the operating modes of the basic unit. As seen in Fig. 1(b), the output voltage of the unit is equal to the input voltage (V_{dc}). As seen, in the first mode, the switches S_2 and S_1 are respectively On and Off which force the diodes D_1 and D_2 to be On and Off. As a result, in mode 1, the capacitor C_1 is charged to V_{dc} through the power DC supply and inductor L_C. Due to using this inductor in the capacitor charging path, the current stress on the switches and the capacitor is decreased which in turn decreases the cost of these components and increases their lifetimes, especially that of the electrolytic capacitor. The capacitor is charged with decreased current spike. In this mode, the output voltage is equal to V_{dc} ($V_O = V_{dc}$). Fig. 1(c) shows the second operating mode of the basic unit where the switches S_2 and S_1 are in OFF- and ON-states. Besides, among the diodes, the diode D_2 is only conducting. As seen, the power supply, i.e. Photovoltaic (PV) panel, is placed in series with the capacitor C_1 which gives an output voltage which is twice of the input voltage (V_O=2V_{dc}). Obviously, the basic unit does not require any additional circuits and can be controlled with simple charging techniques.

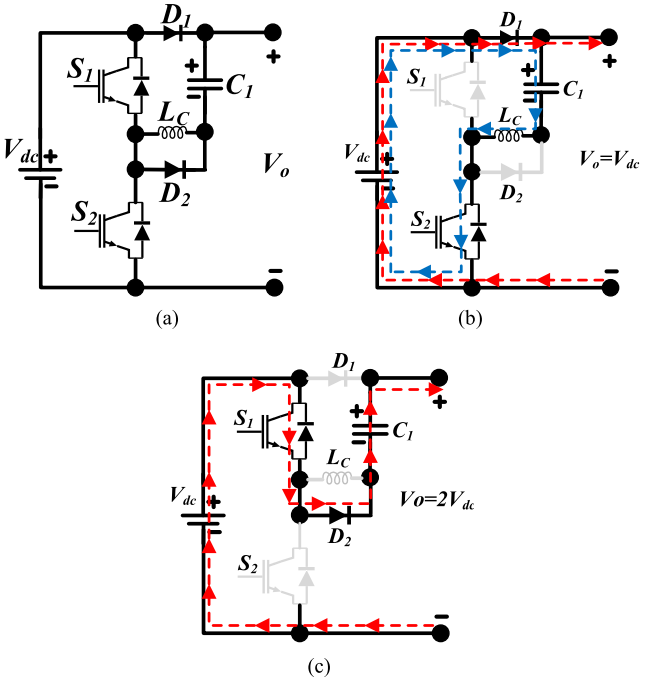


FIGURE 1. (a) Basic series/parallel unit; and its operating modes: (b) Mode 1 (charging mode) (c) Mode 2 (discharging mode).

As mentioned, in the modified inverter, Inductor L_C is used in this circuit in order to reduce the peak charging current of capacitor when the capacitor C_1 is charged by the input source. The presence of diode D_2 in parallel with inductor L_C causes no resonance by capacitor C_1 and inductor L_C. If the voltage across the L_C becomes negative, the resonance will occur which is not a case in this design, since the L_C voltage is always positive. The presence of the diode D_2 makes the voltage of the inductor L_C never have a negative value and therefore resonance does not occur in the circuit.

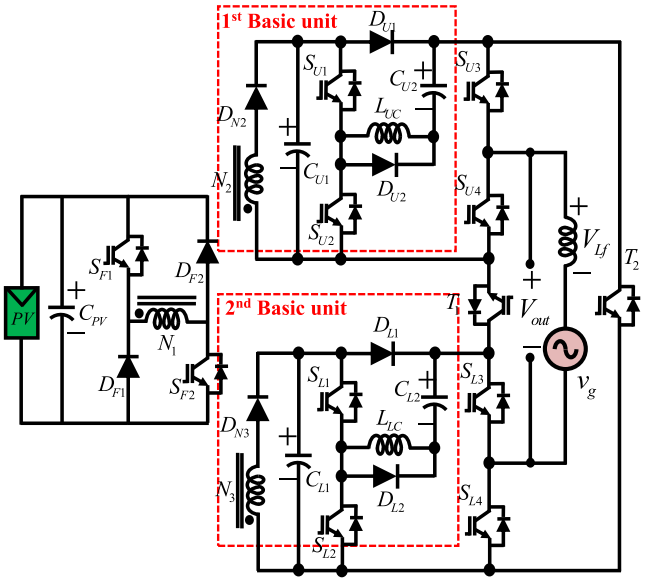


FIGURE 2. Configuration of the modified 17-level SC-based MLI.

TABLE 1. Switching states of the proposed 17-Level inverter.

Voltage levels	ON-state switches	V_{out}
1	S_{L2}, S_{U2}, S_{L4}, S_{U4}, T_1	V_{CL1}
2	S_{L1}, S_{U2}, S_{L4}, S_{U4}, T_1	$V_{CL1}+V_{CL2}$
3	S_{L2}, S_{U2}, S_{L3}, S_{U3}, T_1	V_{CU1}
4	S_{L2}, S_{U2}, $S_{U}3$, S_{L4}, T_1	$V_{CL1}+V_{CU1}$
5	S_{L1}, S_{U2}, S_{U3}, S_{L4}, T_1	$V_{CL1}+V_{CL2}+V_{Cu1}$
6	S_{L2}, S_{U1}, S_{L3}, S_{U3}, T_1	$V_{Cu1}+V_{CU2}$
7	S_{L2}, S_{U1}, S_{U3}, S_{L4}, T_1	$V_{CL1}+V_{Cu1}+V_{Cu2}$
8	S_{L1}, S_{U1}, S_{U3}, S_{L4}, T_1	$V_{CL1}+V_{CL2}+V_{CU1}$, V_{Cu2}
9	S_{L2}, S_{U2}, S_{L3}, S_{U4},T_1	0
	S_{L2}, S_{U2}, S_{L3}, S_{U4}, T_1	
10	S_{L2}, S_{U2}, S_{L3}, S_{U3}, T_2	$-V_{CL1}$
11	S_{L1}, S_{U2}, S_{L3}, S_{U3}, T_2	$-(V_{CL1}+V_{CL2})$
12	S_{L2}, S_{U2}, S_{L4}, S_{U4}, T_2	$-(V_{CL1}+V_{CL2})$
13	S_{L2}, S_{U2}, S_{L3}, S_{U4}, T_2	$-(V_{CL1}+V_{CU1})$
14	S_{L1}, S_{U2}, S_{L3}, S_{U4}, T_2	$-(V_{CL1}+V_{CL2}+V_{Cu1})$
15	S_{L2}, S_{U1}, S_{L4}, S_{U4}, T_2	$-(V_{Cu1}+V_{CU2})$
16	S_{L2}, S_{U1}, S_{L3}, S_{U4}, T_2	$-(V_{CL1}+V_{Cu1}+V_{Cu2})$
17	S_{L1}, S_{U1}, S_{L3}, S_{U4}, T_2	$-(V_{CL1}+V_{CL2}+V_{CU1}, V_{Cu2})$

In the experimental part, the value of capacitor C_{L2} C_{U2} is equal to 2200uF and the values of inductors L_{LC} and L_{UC} are equal to 50uH, the resonance frequency of this circuit is equal to 479.8Hz, while the switching frequency was much higher than this and equal to 20kHz is. The high switching frequency compared to the resonant frequency causes no resonance in the circuit.

$$f_r = \frac{1}{2\pi\sqrt{C_{L2} \times L_{LC}}} = \frac{1}{2\pi\sqrt{2200\mu \times 50\mu}} = 479.8Hz \tag{1}$$

In Fig. 2, the configuration of the modified SC-based MLI is shown providing a 17-level voltage at its output. Considering Fig. 2, the input voltage applied to the first basic unit is three times the PV voltage (V_{pv}) since the ratio of N_2 to N_1 is equal to 3 ($(N_2/N_1) = 3$). Also, the voltage applied to the second basic unit as its input voltage is the same as the input PV voltage ($(N_3/N_1) = 1$). Therefore, the capacitors C_{L1} and C_{U1} will be respectively charged to $V_{CL1} = V_{PV}$, and $V_{CU1} = 3V_{PV}$. In fact, these capacitors act as asymmetric DC-links or voltage sources needed for generating the desired voltage levels at the output port of the inverter. The switching pattern of the modified 17-level MLI are listed in Table 1. As seen, for generating any voltage level at the output, only five switches should be in On-state.

III. OPERATING MODES OF THE MODIFIED MLI

Figs. 3-5 show the operation modes of the proposed inverter only for the positive output voltage levels. In the following, these modes are discussed in detail. Since the operation modes of the negative half cycle are similar to the positive half cycle, the negative half cycle details are not presented in this section. In the mentioned figures, red dash line, blue dash line, and green dash line denote injected current to the grid path (active power), capacitor charging path, and reactive power path, respectively.

A. FIRST OPERATION MODE

The first operation mode of the proposed MLI is shown in Fig. 3(a) where the switches S_{L2}, S_{U2}, S_{L3}, S_{U4}, and T_1 are ON. Here, the zero level of the output voltage is achieved, i.e. $V_{out} = 0$.

B. SECOND OPERATION MODE

In Fig. 3(b), the second operation mode is presented in which at the output port of the inverter, a voltage with value of $(+V_{PV})$ is generated. As seen, here, the switches S_{L2}, S_{U2}, S_{L4}, S_{U4}, and T_1 are in ON-state. This makes the output voltage as the same as the voltage of capacitor C_{L1} ($V_{out} = V_{CL1} = +V_{PV}$).

C. THIRD OPERATION MODE

The equivalent circuit of third operation mode is presented in Fig. 3(c) where the switches S_{L1}, S_{U2}, S_{L4}, S_{U4}, and T_1 are conducting. As a result, the output voltage of the proposed inverter is equal to the sum of the capacitors C_{L1} and C_{L2} which gives $V_{out} = +2V_{PV}$.

D. FOURTH OPERATION MODE

Fig. 4(a) shows the fourth mode where the inverter generates $(+3V_{PV})$ at the output. As seen, in this mode, the switches S_{L2}, S_{U2}, S_{L3}, S_{U3}, and T_1 are ON which in turn leads to have an output voltage similar to the voltage of capacitor $C_{U1}(V_{out} = V_{CU1})$.

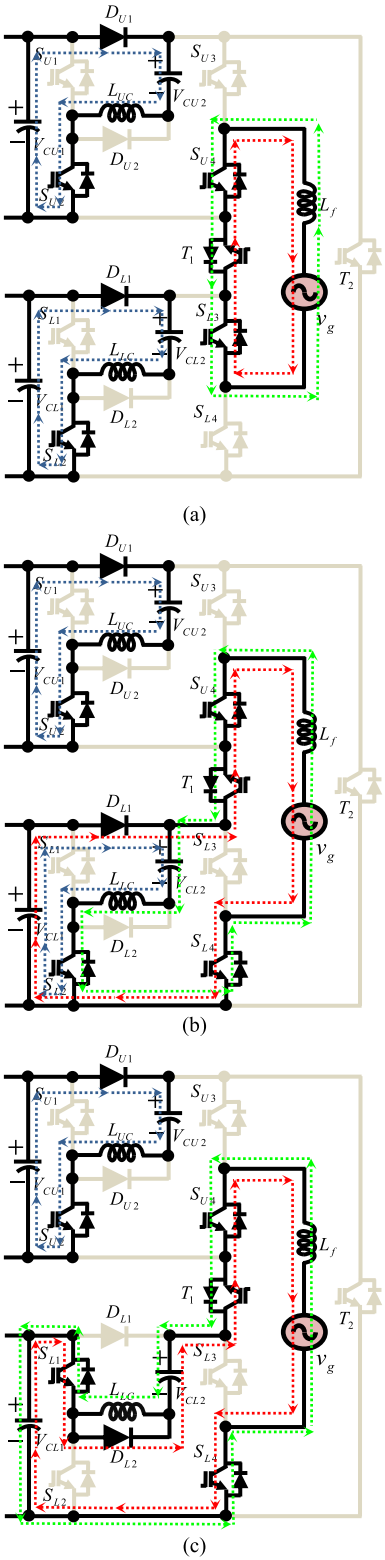


FIGURE 3. Operation modes: (a) Level (0), (b) Level ($+V_{PV}$), (c) Level ($+2V_{PV}$).

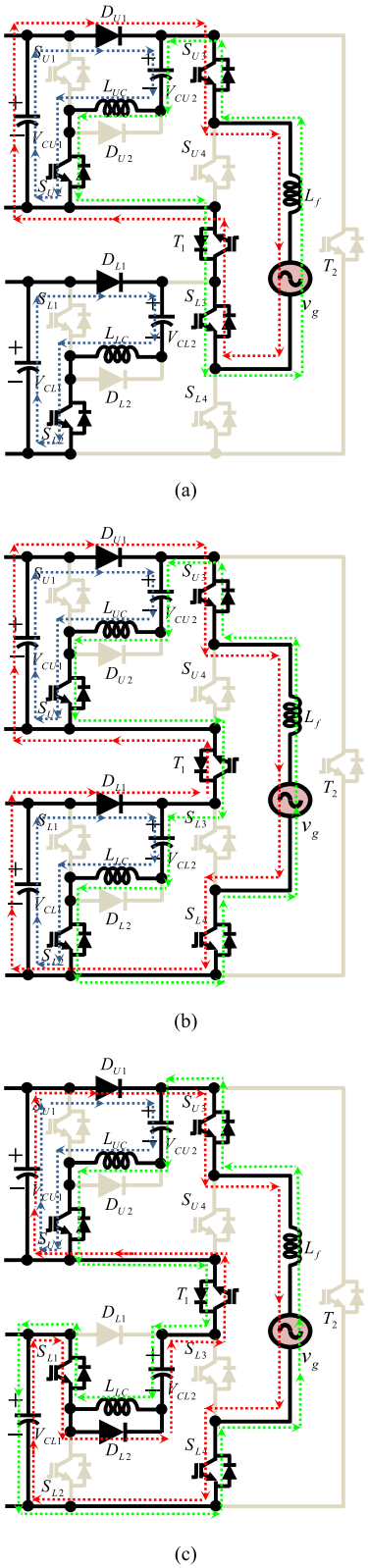


FIGURE 4. Operation modes: (a) Level ($+3V_{PV}$), (b) Level ($+4V_{PV}$), (c) Level ($+5V_{PV}$).

E. FIFTH OPERATION MODE

This operation mode is shown in Fig. 4(b) where to generate the output voltage equal to ($+4V_{PV}$), the switches S_{L2}, S_{U2}, S_{U3}, S_{L4}, and T_1 are turned on. Here, the output voltage is equal to the sum of voltages of capacitors C_{L1} and $C_{U1}(V_{out} = V_{CL1} + V_{CU1})$.

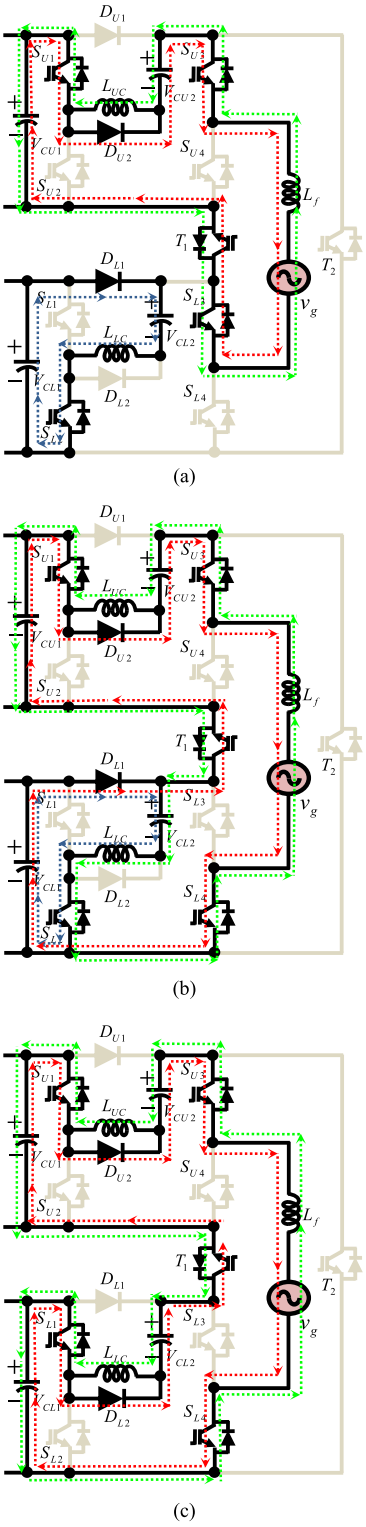


FIGURE 5. Operation modes: (a) Level ($+6V_{PV}$), (b) Level ($+7V_{PV}$), (c) Level ($+8V_{PV}$).

F. SIXTH OPERATION MODE

Fig. 4(c) shows the sixth operation mode of the proposed inverter in which the switches S_{L1}, S_{U2}, S_{U3}, S_{L4}, and T_1 are conducting in a way that the output voltage becomes equal to the sum of the voltages across the capacitors C_{L1}, C_{L2}, and $C_{U1}(V_{out} = +4V_{PV})$.

G. SEVENTH OPERATION MODE

Fig. 5(a) illustrates the seventh operation mode of the proposed MLI where the output voltage with value of $(+4V_{PV})$ is aimed to be provided. As seen, the switches S_{L2}, S_{U1}, S_{L3}, S_{U3}, and T_1 are ON. Under these conditions, the desired output voltage is obtained as the sum of the voltages of the capacitors C_{U1} and C_{U2}.

H. EIGHTH OPERATION MODE

The equivalent circuit of this mode is presented in Fig. 5(b) where to produce $(+4V_{PV})$ at the output, the switches S_{L2}, S_{U1}, S_{U3}, S_{L4}, and T_1 are turned on. As seen, the output voltage is equal to the sum of the voltages across the capacitors C_{L1}, C_{U1}, and C_{U2}.

I. NINTH OPERATION MODE

Fig. 5(c) shows the ninth operation mode where the output voltage of $(+8V_{PV})$ is generated. Here, the switches S_{L1}, S_{U1}, S_{U3}, S_{L4}, and T_1 are turned on leading to have a voltage equal to the sum of the voltages of the capacitors C_{L1}, C_{L2}, C_{U1}, and C_{U2} at the output.

IV. DESIGN GUIDELINES OF FLYBACK CONVERTER

The basic operation of the DC-DC flyback converter is similar to the bidirectional buck-boost converter. Energy is stored in magnetizing inductance (L_m) when the switch S_k is in ON state is transferred to the load when the switch is open. If the switch S_k is closed, the relationship between the voltage and current of magnetizing inductance (L_m) can be written as follow:

$$V_1 = V_{PV} = L_m \frac{di_{Lm}}{dt} \tag{2}$$

The duty cycle of switch S_k is D, being in ON state and off state for DT and $(1\text{-}D)T$ respectively, where T is switching period time of flyback converter.

With respect to (1), the ripple of the current through the magnetizing inductor can be written as follow:

$$I_{K,\max} = I_{PV} + \frac{V_{PV} DT}{2L_m} \tag{3}$$

By replacing $\Delta t_{ON} = DT$ into (2), it can be written:

$$(\Delta i_{Lm})_{ON} = \left(\frac{V_{PV}}{L_m}\right) DT \tag{4}$$

The accurate value of L_m can be obtained as following:

$$L_m = \left(\frac{V_{PV}}{(\Delta i_{Lm})_{ON}}\right) DT \tag{5}$$

The stress voltage of diode can be obtained as:

$$V_{DF1} = V_{DF2} = -V_1 - V_{PV}\left(\frac{N_2}{N_1}\right) \tag{6}$$

If the switches S_{F1} and S_{F2} are in off state, the ripple of current through the L_m can be calculated as:

$$V_{SF1} = V_{SF2} = V_{PV} - V_1 = V_{PV}\left(\frac{N_1}{N_2}\right) \tag{7}$$

where, the N_1 and N_i are turn number of primary winding and i^{th} secondary winding respectively.

Since over one period for steady-state condition, the net change in inductor current will be zero. So that, voltage of output capacitors ($V_{CU1} \sim V_{CLi}$) of flyback converter can be written as follow:

$$(\Delta i_{Lm})_{ON} + (\Delta i_{Lm})_{OFF} = 0 \tag{8}$$

$$V_{CU1} = V_{CL1} = V_{PV}\left(\frac{D}{D-1}\right)\left(\frac{N_2}{N_1}\right) \tag{9}$$

where, V_{Ci} represents the i^{th} capacitor voltage and Ni is turn number of ith secondary transformer winding.

The peak current and voltage stress of flyback switch (S_k), can be obtained as:

$$I_{SF1,\max} = I_{PV} + \frac{V_{PV}.DT}{2L_m}$$

$$I_{L,\max} = I_{Lm} + \frac{V_{PV}.DT}{2L_m} \tag{10}$$

$$I_{L,\min} = I_{Lm} - \frac{V_{PV}.DT}{2L_m} \tag{11}$$

Fig. 6 indicates the current of magnetizing inductance which is considered in equivalent circuit of transformer.

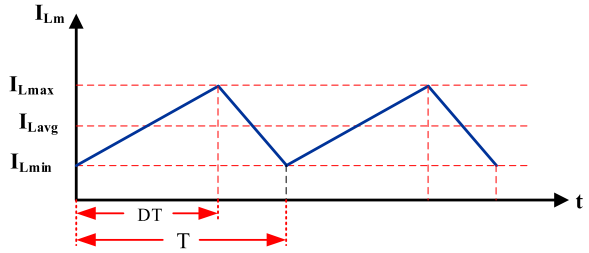


FIGURE 6. Waveform of magnetizing inductance current.

The maximum and minimum values of the magnetizing inductance current can be obtained as follow:

$$I_{L,\max} = I_{Lm} + \frac{V_{PV}DT}{2L_m}$$

$$I_{L,\min} = I_{Lm} - \frac{V_{PV}DT}{2L_m} \tag{12}$$

As well as, the equation of the maximum value of current through the i^{th} diode which is used in flyback converter can be indicated as:

$$I_{(DF1,\max)} = I_{Di} + \frac{V_{PV}DT}{2L_m}\left(\frac{N_1}{N_2}\right) \tag{13}$$

V. DESIGN GUIDELINES OF UTILIZED PASSIVE COMPONENTS

At this step, the sizes of the capacitors C_{L2} and C_{U2} are calculated. In the following, I_g and φ denote the amplitude of the injected grid current and the phase difference between the grid voltage and the injected grid current. Note that the output voltage is considered as a staircase waveform.

Thus, the maximum discharging value of each capacitor can be expressed in a half-cycle as follow:

$$Q_{Ci2} = \int_{t_k}^{(0.25T - t_k)} I_g \sin(\omega_s t - \varphi)\, dt \;\; ; \;\; i = L, U \tag{14}$$

where T, and ω_s are the periodic time of the grid voltage, and the fundamental angular frequency of the output voltage, respectively. Besides, $[t_k, 0.25T - t_k]$ is the time interval related to the longest discharging cycle (LDC) of each capacitor. This time interval will vary for C_{L2} and C_{U2} in the modified inverter. According to Table 1, the LDC for C_{L2} and C_{U2} is illustrated by Fig. 7. Thus, by considering the kV_{in} as maximum allowable voltage ripple, the size of the capacitors can be calculated by using (15).

$$C_{opt,i2} \geq \frac{Q_{C_{i2}}}{kV_{in}} \;\; ; \;\; i = L, U \tag{15}$$

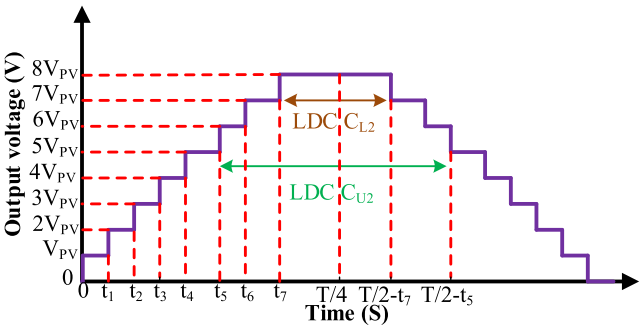


FIGURE 7. Typical output voltage waveform of the modified 17-level inverter for positive half-cycle.

Based on Fig. 1(b), the size of the inductor L_C should be obtained as follows:

$$L_c > \frac{R_{eq}^2.C_1}{4} \tag{16}$$

where, R_{eq} is equal to $[r_D + r_{ESR,C} + r_{L,c} + r_{DS} + r_{C1}]$ where r_D, $r_{ESR,C}$, $r_{L,c}$, r_{DS} and r_{C1} respectively present the internal resistances each of the diodes, capacitors, inductors and switches. In addition, the charging current of the capacitor can be calculated as follows:

$$i_{C1}(t) = \frac{V_{dc} - V_{C1}}{\sqrt{\frac{L_c}{C_1} - \frac{R_{eq}^2}{4}}} \times e^{-\frac{R_{eq}}{2L_c}t} \times \sin\left(\sqrt{\frac{1}{L_c C_1} - \frac{R_{eq}^2}{4L_c^2}}\right) t \tag{17}$$

During the time interval of t_P, this current reach to its maximum value obtained by the below equation:

$$t_P = \frac{\pi}{2 \times \sqrt{\frac{1}{L_c C} - \frac{R_{eq}^2}{4L_c^2}}} \tag{18}$$

Now, the maximum value (peak) of the charging current during t_P can be obtained as:

$$I_{C1,\max} = i_{C1}(t_p) = \frac{V_{dc} - V_{C1}}{\sqrt{\frac{L_c}{C_1} - \frac{R_{eq}^2}{4}}} \times e^{-\frac{R_{eq} \times \pi}{4L_c \times \sqrt{\frac{1}{L_c C} - \frac{R_{eq}^2}{4L_c^2}}}} \tag{19}$$

VI. APPLIED CLOSED LOOP CONTROL SYSTEM

In this paper, a CC-based approach is presented for the modified MLI structure to control injected active and reactive power to grid. In Fig. 8, the block diagram of this control approach is shown. As seen, since the PV panel is employed as the input source, the current controller block and the maximum power point tracking (MPPT) unit are considered in the control system. To synchronize the inverter to grid, a phase-locked loop (PLL) unit is embedded in the control system. Besides, to have a current injection with good dynamic characteristic, a filter based PLL system is used which includes the second order generalized integrator (SOGI) or enhance PLL (E-PLL) [12]. Here, the conventional perturb and observation (P&O) method is employed to track the MPPT of the PV panels. To track the maximum power of the PV source, its voltage and current are measured. Moreover, to calculate the amplitude and phase angle of the reference current (i_{ref}), the reference values of the injected active and reactive power are applied to the control system as the input parameters. This reference current is used as an input parameter of the current control loop. Based on Fig. 5, the instantaneous current slope passing through the inductor L_f, the L-type filter, should be measured.

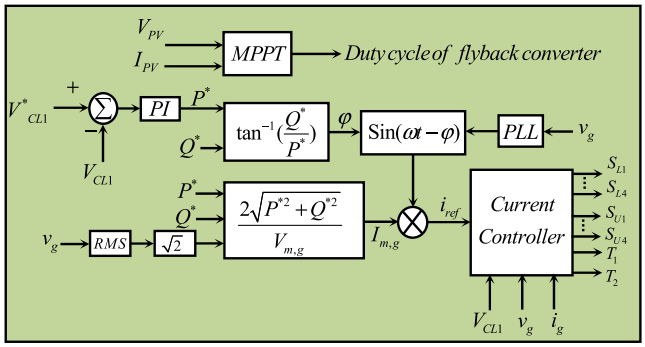


FIGURE 8. Block diagram of control method used for the modified MLI.

For generating the switching patterns, the reference current waveform (i_{ref}) is compared with the measured grid current (i_g). Here, the performance of the modified system is determined by the voltage polarity at the grid side (v_g). The sampling time (T_{smp}) is regulated to a specific value which is equal to ($1/2f_{sw}$) where f_{sw} denotes the maximum switching frequency. During the sampling time, the PLL and MPPT units produce the reference current (i_{ref}). Then, the reference current is compared with the measured grid current (i_g). The control technique assures that the output current of the inverter fits over the sinusoidal reference current perfectly.

VII. POWER LOSS AND EFFICIENCY ANALYSIS

In this section, the power loss analysis of the modified 17-level SC-based inverter are presented. It should be noted that the power losses of the switching devices, i.e. the switches, include two parts: Switching losses (P_{SW}) and conduction losses (P_{Con}). However, other components such as the capacitors only have conduction losses.

A. SWITCHING LOSSES

Generally, the switching losses can be calculated during the ON and OFF period of switching states. For simplification purposes, a linear approximation between the current and the voltage of switches is assumed during the switching states. Hence, the following statements can be written for the ith involved power switch.

$$\begin{aligned} P_{ON,sw_{ith}} &= \frac{1}{T_{SW}} \int_0^{t_{ON}} v_{ON,i}(t) i(t) dt \\ &= \frac{1}{6} (f_{SW} V_{ON,i} I_i) t_{ON} \end{aligned} \tag{20}$$

$$\begin{aligned} P_{OFF,sw_{ith}} &= \frac{1}{T_{SW}} \int_0^{t_{OFF}} v_{block,i}(t) i(t) dt \\ &= \frac{1}{6} (f_{SW} V_{block,i} I_i') t_{OFF} \end{aligned} \tag{21}$$

In (19) and (20), I_i and I_i' denote the currents which pass through ith power switch after turning ON state and before turning OFF state, respectively. Also, T_{SW} and f_{SW} respectively present the periodic time of switching frequency, and the switching frequency. Using (19) and (20), the total switching loss of all power switches are obtained as follows:

$$P_{SW} = \sum_{i=1}^{10} \left(\sum_{k=1}^{N_{ON}} P_{SW,ON,ik} + \sum_{k=1}^{N_{OFF}} P_{SW,OFF,ik} \right) \tag{22}$$

where N_{ON} and N_{OFF} are the numbers of switches which are in ON-state and OFF-state, respectively.

B. CONDUCTION LOSSES

To calculate the conduction losses of the components of the modified inverter, a clear and straightforward approach is provided based on the pure-resistive load. Based on Table 1, three operation states can be named for the capacitors C_{L2} and C_{U2}:

- Discharging states for each capacitor (states number 8 and 17)
- Charging states for each capacitor (states number 1, 3, 4, 10, 12 and 13)

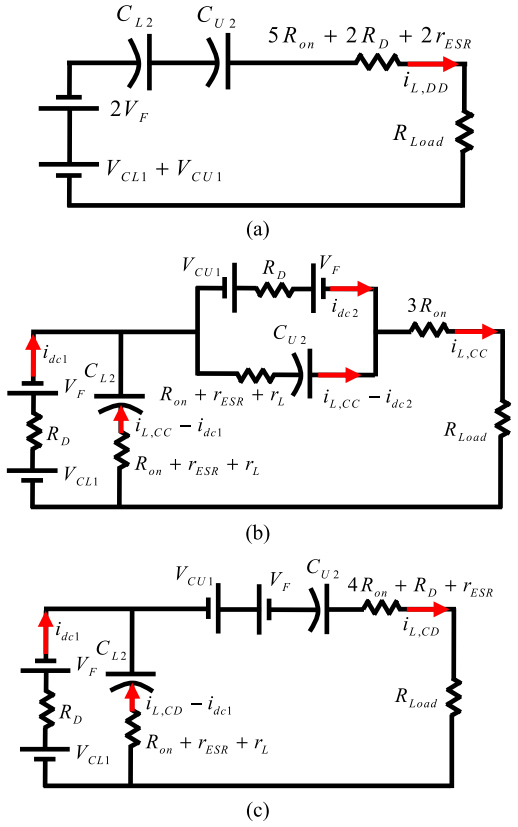


FIGURE 9. The equivalent circuit of the proposed 17-level grid-tied topology with a resistive load in (a) discharging modes, (b) charging modes, (c) charging and discharging modes together.

- Discharging states for one of the capacitors and charging states for the other capacitor or vice versa.

In Fig. 9, the equivalent circuits of the above-mentioned operation states are shown. In Fig. 9, V_F, R_{Load}, R_D, R_{on}, r_{ESR}, and r_L present the forward voltage decadence of each incurred diode, the load resistance, the internal resistance of each diode, the ON-state internal resistance of each switch, the equivalent series resistance (ESR) of both capacitors (C_{L2} and C_{U2}), and the internal resistance of each inductor (L_{LC} and L_{UC}), respectively. In Fig. 9(a), the equivalent circuit configuration of the modified inverter in discharging states for the capacitors is shown where the capacitors are in series with the corresponding voltage source. Thus, the injected current (the output current), can be obtained as:

$$i_{L,DD} = \frac{4V_{PV} + v_{CL2} + v_{CU2} - 2V_F}{5R_{on} + 2r_{ESR} + 2R_D + R_{Load}} \tag{23}$$

Now, by considering the time intervals presented in Fig. 7 and Table 1, the instantaneous conduction loss and the average conduction loss for one full-cycle of the discharging mode can be respectively written as given below:

$$P_{C,DD}(t) = (5R_{on} + 2R_D + 2r_{ESR})\, i^2_{L,DD} \tag{24}$$

$$P_{C,DD}(avg) = \frac{2f_S}{\pi}\left(\frac{\pi}{2} - t_8\right)P_{C,DD}(t) \tag{25}$$

According to Fig. 9(b) and the time intervals between the states 3 and 5, and also the states 1 and 2 shown in Fig. 7, the conduction losses of both capacitors in charging mode for instantaneous and average values are respectively obtained by (11) and (12).

$$\begin{aligned} P_{C,CC}(t) = {} & 3R_{ON} i^2_{L,CC}(t) + R_D(i^2_{dc,1} + i^2_{dc,2}) \\ & + [(i_{L,CC} - i_{dc,1})^2 + (i_{L,CC} - i_{dc,2})^2] \\ & \times (r_{ESR} + R_{ON} + r_L) \end{aligned} \tag{26}$$

$$P_{C,CC}(avg) = \frac{2f_S}{\pi}[(t_2 - t_1) + (t_5 - t_3)]P_{C,CC}(t) \tag{27}$$

Using the Kirchhoff Voltage Law (KVL), the equations of $i_{dc,1}$ and $i_{dc,2}$, charging currents of the capacitors C_{L2} and C_{U2}, can be derived as follow:

$$i_{dc1} = \frac{(R_{on} + r_{ESR} + r_L)\, .i_{L,CC} + V_{PV} - V_F - v_{CL2}}{R_D + R_{on} + r_{ESR} + r_L} \tag{28}$$

$$i_{dc2} = \frac{(R_{on} + r_{ESR} + r_L)\, .i_{L,CC} + 3V_{PV} - V_F - v_{CU2}}{R_D + R_{on} + r_{ESR} + r_L} \tag{29}$$

Similarly, based on Figs. 9(c) and 7, when the capacitor C_{L2} is charged (C_{U2} is discharged simultaneously) and C_{U2} is discharged (C_{L2} is charged simultaneously), instantaneous and average values of conduction losses can be given as follows:

$$\begin{aligned} P_{C,CD,i}(t) = {} & (4R_{ON} + r_{ESR} + R_D) i^2_{L,CD} + R_D .i^2_{dc,i} \\ & + (i_{L,CD} - i_{dc,i})^2 (R_{ON} + r_{ESR} + r_L) \\ & for \quad i = 1, 2 \end{aligned} \tag{30}$$

$$\begin{aligned} P_{C,CD}(ave) = {} & \frac{2f_S}{\pi}\left[[(t_8 - t_6)]\, .P_{C,CD,2}\right. \\ & \left. + [(t_6 - t_5) + (t_3 - t_2)]\, .P_{C,CD,1}\right] \end{aligned} \tag{31}$$

C. CONDUCTION LOSSES

In this subsection, the ripple losses of the used capacitors are calculated. The ripple losses are occurred when the capacitors are connected in parallel during charging mode. Under this condition, the capacitor ripple losses are created by difference between the related input dc power supply and voltage across of the implemented capacitors. In this case, the voltage ripple of the used capacitors of the modified inverter can be defined as follows:

$$\Delta V_{Cj} = \frac{1}{\omega}\int i_{Cj} d(\omega t) \quad ; \quad j = U_2, L_2 \tag{32}$$

Therefore, the capacitor ripple losses of used switched capacitor (C_{U2} and C_{L2}) the modified inverter can be obtained as follows:

$$P_{Cap} = \frac{2\pi}{\omega}\left(C_j \Delta V_{Cj}\right) \quad ; \quad j = U_2, L_2 \tag{33}$$

TABLE 2. Comparison between different multilevel inverters including the modified one.

Topology	Number of power components					N_{Level}	Reactive power supporting	Output power (W)	Total volume (mm^3)	Power density (W/mm^3)	Cost ($)	Ratio of Total Cost to Output Power (%)	Voltage boosting ability
	Switch	Diode	Cap.	Source	Total								
Proposed	10	2	2	2	16	17	Yes	777	44838.9	17.3×10^{-3}	98.1	12.6	Yes
[40]	18	0	2	1	21	17	No	500	356849.8	1.4×10^{-3}	252.9	50	Yes
[41]	12	12	0	4	28	17	Yes	432	15567.1	27×10^{-3}	227	53	No
[27]	9	4	2	2	17	17	No	250	58285.8	4.2×10^{-3}	58.7	24	Yes
[42]	9	0	0	3	12	15	No	113.75	23400	4.8×10^{-3}	117	103	No
MLI of [39]	24	4	4	4	36	17	No	500	696934.6	0.72×10^{-3}	372.6	75	Yes
[37]	13	0	2	2	17	13	Yes	180	347608.6	0.52×10^{-3}	232.24	129.1	Yes
[53]	12	0	4	3	19	13	Yes	500	661577.6	0.75×10^{-3}	307.64	61.5	Yes
[54]	12	2	3	1	18	17	Yes	777	598817.7	1.29×10^{-3}	154.11	19.8	Yes
[55]	18	2	6	2	28	17	Yes	260	334337.16	0.77×10^{-3}	254.16	97.5	Yes
[56]	10	5	5	1	21	17	Yes	217	186812.36	1.16×10^{-3}	105.38	49	Yes
[34]	10	4	6	1	21	17	No	210	552126.32	0.38	221.68	105	Yes
[57]	20	0	5	1	26	17	No	1200	459496.5	2.62×10^{-3}	560.99	46.7	Yes
[58]	10	1	1	3	15	15	No	200	698281.1	0.28×10^{-3}	323.71	161.85	No

TABLE 3. Summary of comparison results.

Parameter	Best structures
Total number of components	**Modified MLI**, [42]
Reactive power supporting	**Modified MLI**, [36], [37], [41], [53]-[55]
THD of output voltage	**Modified MLI,** [53], [56], [57]
Boosting capability	**Modified MLI,** [27], [34], [37], [39]-[41], [53]-[58]
Ratio of total cost to output power	**Modified MLI**

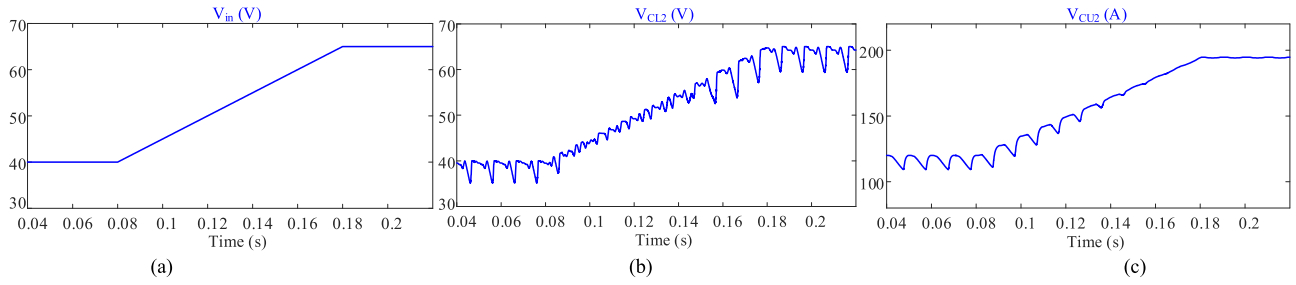


FIGURE 10. (a) Input voltage of converter during transition from 40 V to 65V (b) voltage of capacitor C_{L2}, and (c) voltage of capacitor C_{U2}.

VIII. COMPARISON RESULTS

In this section, comprehensive comparisons are presented between the modified topology and previously introduced MLIs in terms of number of power components, output voltage levels, reactive power supporting capability, total volume, total cost, power density, voltage boosting capability, and so forth.

As listed in Table 2, among 17-level MLIs, the modified structure and the converter of [25] employ the least number of total components, i.e., 16 power components. Compared to other inverters generating output voltage levels less than 17, the modified MLI has also fewer or close number of total components. It should be noted here that compared to these structures, the proposed MLI provides lower total harmonic distortion (THD) at the output since its output voltage levels are higher than other structures. Hence, the output voltage of the modified inverter is closer to a sinusoidal waveform and the output power quality is better. Hence, in terms of total number of components, the modified MLI is one of the best options among the inverters at the same class. Since the number of power switches is an important factor for inverters, at the following, the number of the switches of the modified MLI and others are compared. As seen in Table 2, among 17-level structures, the modified MLI employs 10 power switches granting the second place to it after the inverter of [27] which uses 9 power switches. However, it should

be noted that the modified MLI has fewer total number of components compared to the inverter of [27] which makes the modified one the superior one.

According to Table 2, the modified converter has the capability of supporting reactive power unlike the structures proposed in [27], [39], [40], and [42]. In addition, in terms of power density, the modified MLI shows an acceptable value in comparison to other structures. Based on this table, it is evident that among all compared structures, the modified MLI has the lowest value for ratio of total cost to the total cost, i.e., 12%, making this converter the most suitable topology for industrial applications. It is noteworthy that the modified MLI also possesses the boosting ability which is required in most of the RES applications. It is worth mentioning that the other topologies can also be equipped with the DC-DC converters to gain the boost capability and to enhance the output voltage quality. However, this will increase the number of power components of these inverters which is not desirable. Thus, compared to the converters without boosting ability, the modified inverter is a better option for industrial applications since it inherently has this capability.

Table 3 lists the comparison results where the modified converter is the superior structure or among the best ones. According to this table, the modified MLI is the most suitable structure for industrial applications among the compared ones.

IX. SIMULATION RESULTS

Here, in order to show the performance of the proposed converter in PV connected condition, changes in the input voltage have been made. Also, the output of the inverter is connected to the grid. Fig. 10(a) shows the input voltage waveform. Regarding Fig. 10(a), the input voltage changes from 40V to 65V. In this simulation, the duty cycle value of the flyback converter has been kept constant, so as the input voltage increases from 40 to 65V, the second output voltage changes from 40 to 65V and the first output voltage changes from 120 to 195V. The trend of changes in input voltage and voltage of C_{L2} and C_{U2} is shown in Fig. 10(b), (c), respectively. The maximum discharge time of C_{U2} capacitor is when voltage level ± 8 is produced. When the voltage of the capacitor C_{U2} reaches around 195V, level ± 8 is no longer produced, so it is clear from Fig. 10(c) that the voltage ripple of the capacitor C_{U2} has decreased after increasing the input voltage. In Fig. 11, the voltage and current injected into the grid are shown along with the output voltage of the inverter. It can be seen from this figure that in the process of increasing the input voltage from 40 to 65V, the output voltage of the inverter has changed from 17th levels to 15th levels, then to 13th levels and finally to 11th levels, while the current injected into the grid by the control system is kept constant.

The purpose of this simulation scenario is to show the performance of the proposed improved converter when the input voltage changes, which is expected behavior of the solar panels.

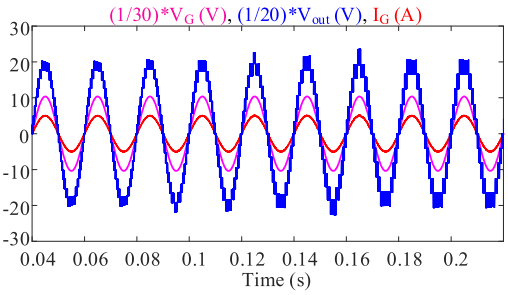


FIGURE 11. Grid voltage and current along with the output voltage of the inverter during the input voltage transition from 40 to 65V.

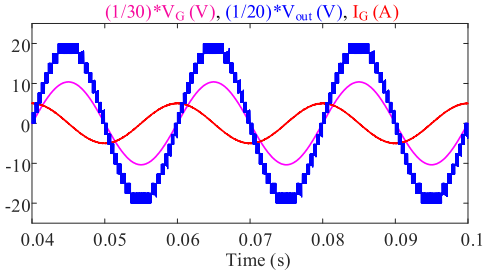


FIGURE 12. Simultion results in output power of 0.77kVAR: grid volatge and current, output volatge of the inverter at leading power factor with PF=0.

In addition, the proposed converter is able to control reactive power, and it can also feed non-unity power factor loads. In order to be able to show the return current path or the reactive power path in operating modes, these modes have been updated and green lines have been added to the path of operating modes. It is well shown by the green lines that the reverse current path is established at all output voltage levels.

Also, in order to show the current passing through L_{LC} and L_{UC} inductors as well as D_{L2} and D_{U2} diodes in non-unity power factor conditions, the proposed inverter has been simulated in leading and lagging power factors and for PF=0. In fact, PF = 0 is the most intense type of inductive or capacitive load, and in this case, the phase difference between the grid voltage and current is equal to 90 degrees. The following figures show the simulation results. In this simulation, the output active power is zero and the reactive power injected into the grid is equal to 0.77kVAR. Fig. 12 shows the grid voltage and current along with the output voltage of the inverter in PF=0 and also the leading power factor. In this simulation mode, the grid current is 90 degrees ahead of the grid voltage and the inverter injects all reactive power into the grid. In Fig. 13, the current passing through the capacitors C_{L2} and C_{U2}, together with the capacitor charging current limiting inductors (L_{LC} & L_{UC}) and the current of the diodes parallel to them (D_{L2} & D_{U2}) are shown. According to the Figs. of 12 and 13, it can be concluded that the proposed inverter is capable of producing reactive power or supplying non-unity power factor loads.

Fig. 14 shows the grid voltage and current along with the output voltage of the inverter. In this figure, PF=0 and

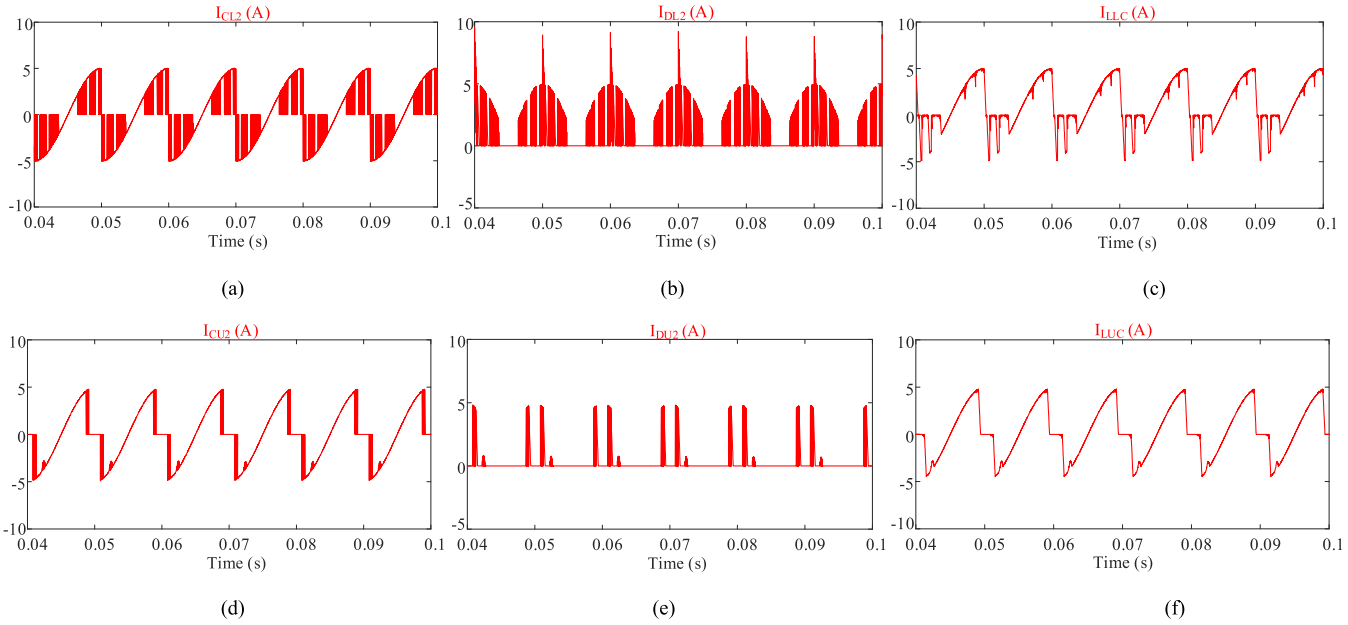


FIGURE 13. Simultion results in output power of 0.77kVAR, lagging power factor with PF=0,: (a) current of capacitor C_{L2}, (b) current of diode D_{L2}, (c) current of inductor L_{LC}, (d) current of capacitor C_{U2}, (e) current of diode D_{U2}, (f) current of inducot L_{UC}.

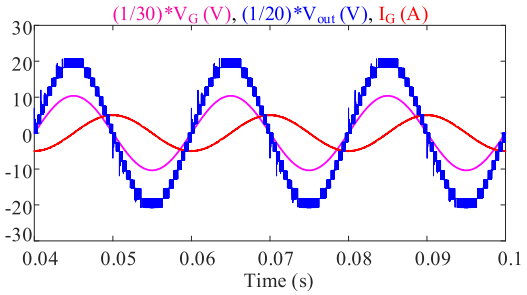


FIGURE 14. Simulation results in output power of 0.77kVAR: grid voltage and current, output voltage of the inverter at lagging power factor with PF=0.

the converter work in lagging power factor mode. Since PF=0, it makes the phase difference between the grid voltage and current equal to 90 degrees. In this case, the active power injected into the grid is zero and the converter injects 0.77kVAR of reactive power into the grid. Fig. 15 shows the current of capacitors C_{L2} and C_{U2} along with the current inductors L_{LC} and L_{UC} as well as the current of parallel diodes with current limiting inductors (D_{L2} & D_{U2}). According to the Figs. of 13(c) and 15(c), it can be seen that both in lagging and leading power factor modes, the current of the L_{LC} and L_{UC} inductors is bidirectional, so it is concluded that the converter is able to handle the return current in the non-unity power factor loads.

Further, the output voltage of the inverter is shown at the output power of 0.77 kW along with the voltage of capacitors C_{L2} and C_{U2}. Fig. 16(a) shows the grid voltage and current along with the output voltage of the inverter. Also, the voltage of capacitors C_{L2} and C_{U2} is shown in Fig. 16(b). In Fig. 16, it has been tried to coincide with each other in terms of time in order to have a better understanding of the capacitors' voltage ripple based on the output voltage of the inverter.

In addition, In Fig. 17, the input current of the converter is shown from the point of view of the input source. In other words, the input of the proposed converter is the same as the input current of the flyback converter. Since there was no access to the laboratory setup at this stage, the simulation results are given. According to Fig. 17, it can be seen that the input current has a negative value, that is actually the energy stored in the leakage inductance of the high frequency transformer, which is returned to the input source. While in the conventional flyback converter, the energy stored in the leakage inductance of the transformer is wasted in the snubber circuit. Although the input current of the converter is discontinuing, the frequency of this current is equal to the switching frequency (30kHz), which can be removed with a low value capacitor. In other words, C_{pv} can easily remove the high frequency ripple of the input current and draw a smooth current from the input source.

X. EXPERIMENTAL RESULTS

Here, the performance of the modified SC-based MLI is validated by presenting thorough experimental results when the modified MLI is connected to the grid. In Fig. 18, the experimental set-up of the modified inverter is shown. In this prototype, SPW47N60C3 (with antiparallel diode and Ron =70mΩ) and MUR1560G are respectively employed as the power switches and diodes. The sizes of the capacitors C_{L1} and C_{U1} are 1000μF. Also, the capacitors C_{L2} and C_{U2} are equal to 2200μF. Besides, a voltage source with an

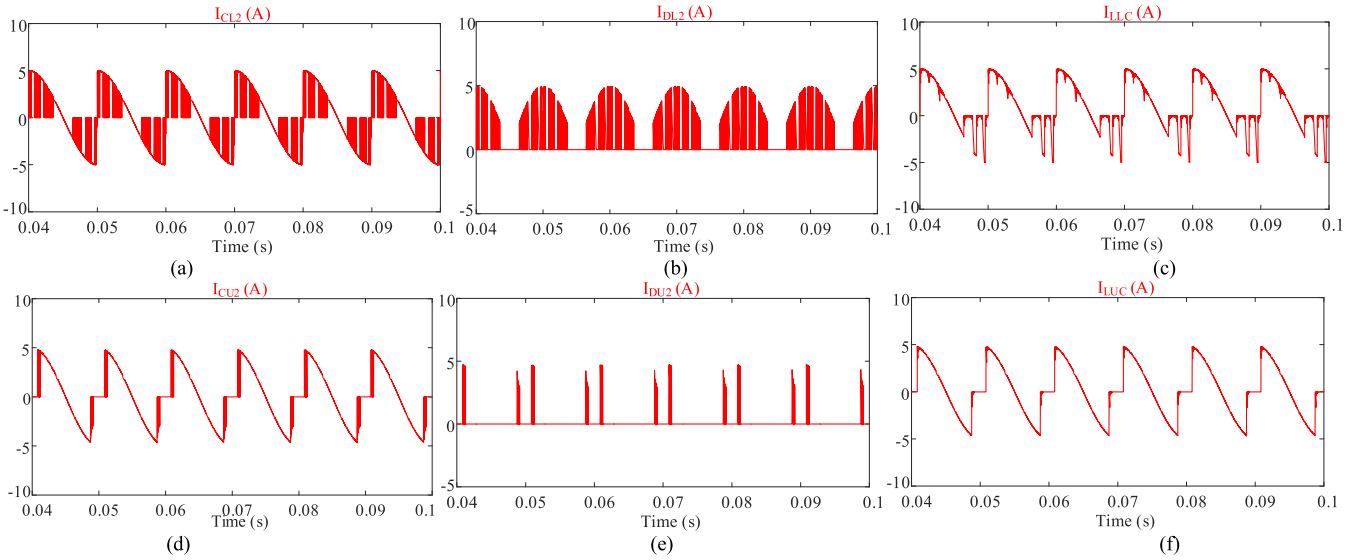


FIGURE 15. Simulation results in output power of 0.77kVAR, lagging power factor with PF=0,: (a) current of capacitor CL2, (b) current of diode DL2, (c) current of inductor L_{LC}, (d) current of capacitor CU2, (e) current of diode DU2, (f) current of inductor L_{UC}.

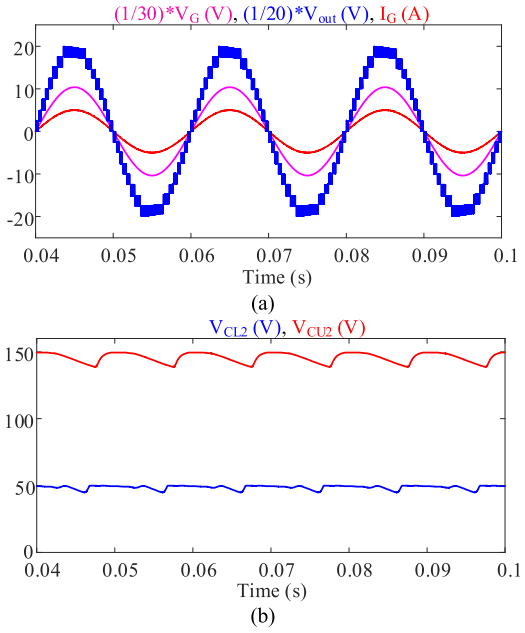


FIGURE 16. Grid voltage and current along with the inverter output voltage at the output power of 0.77kW, (b) the voltage of capacitor C_{L2} and C_{U2}.

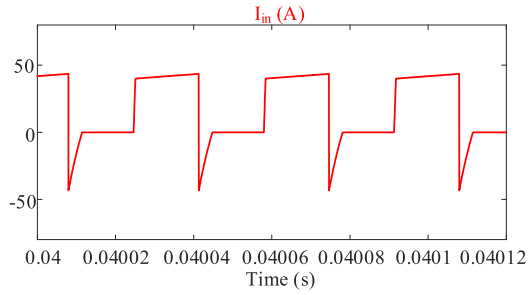


FIGURE 17. Input current of the proposed converter.

amplitude of 50V is used as the DC power supply. To implement the control approach, the ARM microcontroller is utilized. In Table 4, specifications and parameters used in the experiments are listed. Note that the grid frequency is considered as 50Hz. Fig. 19 shows the desirable output voltage of the inverter which is a 17-level waveform with the magnitude of 400V. As seen, in this figure, the injected current to the grid is a sinusoidal waveform with the amplitude of 5A and unity power factor (PF). As seen in Fig. 19, the amplitude of the current injected to the grid is about 5A. Hence, the injected power to the grid is 777W. It should be noted that the THD of the injected current is lower than 1.5% that is totally favorable.

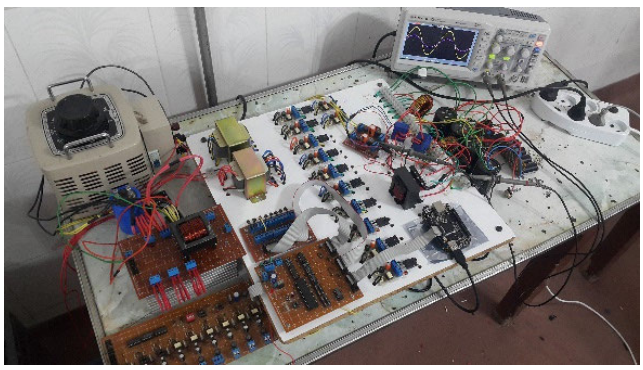


FIGURE 18. Experimental set-up of the proposed inverter.

Based on these results, both of the modified structure and the applied CC technique have desirable performances. Figs. 20(a) and 20(b) respectively show the voltages across the capacitors C_{L1} and C_{U1} which are successfully charged to

50V and 150V. In order to confirm the advantage of limitation capacitor charging current spike of the modified inverter, capacitor charging current waveform of capacitors C_{L2} and C_{U2} without and with suppressant inductor are illustrated in Fig. 21. Fig. 21(a) shows the across voltage and charging current of capacitor C_{U2} without using suppressant inductor. Fig. 19(b) indicates the voltage across and charging current of the capacitor C_{L2} without using suppressant inductor. In Figs. 19(c)-(d), the voltages and charging current of the capacitors C_{L2} and C_{U2} with using suppressant inductor are presented. As seen, the voltages across the capacitors C_{L2} and C_{U2} are the same as the voltages of the capacitors C_{L1} and C_{U1} ($V_{CL1} = V_{CL2}$ and $V_{CU1} = V_{CU2}$) which in turn proves the performance of the control system in balancing the capacitors voltages. Besides, comparing the obtained results without and with using suppressant inductor, it can be seen that the presence of the inductor L_C has drastically reduced the capacitor charging current spike. Considering Fig. 19(a), the peak value of capacitor charging current of capacitor C_{U2} without using inductor is 19 A. However, with respect to Fig. 19(c), the peak value of this current with using inductor is 9.5 A. Also, considering Fig. 19(b), the peak value of capacitor charging current of capacitor C_{L2} is 10 A. However, considering Fig. 19(d), the peak value of this current with using inductor is around 3.5 A.

TABLE 4. Specifications used in the prototype.

Element	Type	Value
S_{U1}, S_{U2}, S_{U3}, S_{U4}, S_{L1}, S_{L2}, S_{L3}, S_{L4}, T_1 & T_2	47N60C	650V/47A
S_{F1} & S_{F2}	IRFP260N	200V/50A
Gate Driver	TLP 250	IC
D_{L1}, D_{L2}, D_{U1} & D_{U2}	MUR1560	600V/15A
D_{F1} & D_{F2}	RURP3060	600V/30A
Current Transducer	LA55P	Hall effect
Microcontroller	-	ARM
Grid frequency	50Hz	-
Sampling frequency	20KHz	-
C_{L1} & C_{U1}	1000µF	220V
C_{L2} & C_{U2}	2200µF	220V
L_f	Ferrite Core	1.3mH
L_{UC} & L_{LC}	Ferrite Core	50μH

As seen, the inductors L_{UC} and L_{LC} successfully limit the maximum peak value of the charging current to about the two times of the peak value of the injected grid current which in turn yields a longer lifetime for the capacitors. In Figs. 22 and 23, the voltages across some of the switches and diodes of the modified inverter are presented. Fig. 22(a) shows the voltages of the diode D_{L1} and the switch T_1 are presented. In Fig. 22(b), Voltages across the diode D_{U1} and the switch T_2 are presented. Besides, the voltage waveforms of the switches S_{L1} and S_{L2} are presented in Fig. 22(c). Moreover, the voltages across the switches S_{L3} and S_{L4} are illustrated in Fig. 22(d). Also, Fig. 23 shows the voltages across the switches S_{U3} and S_{U4}. Based on them, it is obvious

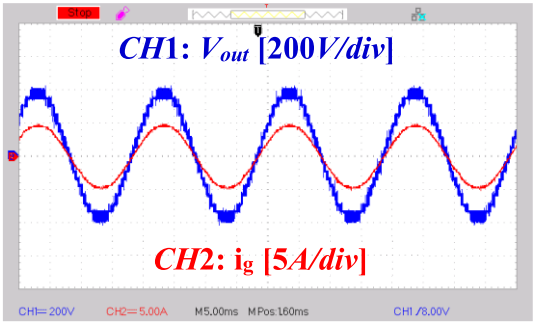
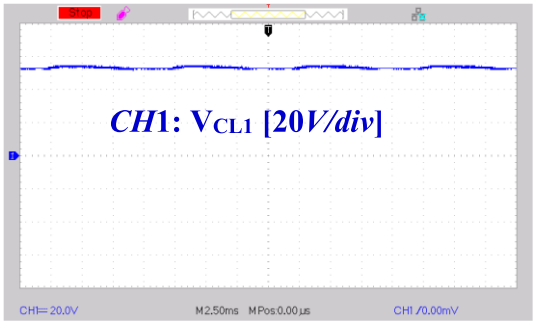
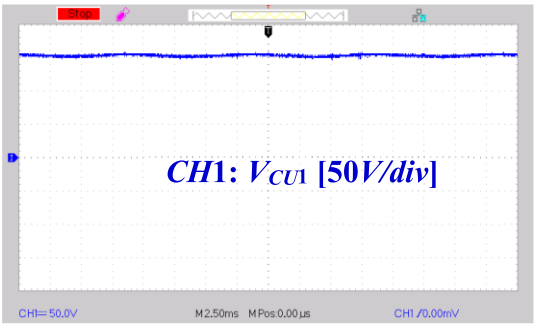


FIGURE 19. The Experimental Results: the output voltage of the inverter (200 V/div) (a) and the injected current (5A/div).



(a)



(b)

FIGURE 20. Voltage across (a) the capacitor C_{L1} (20V/div) (b) the capacitor C_{U1} (50V/div).

that all of the switching devices follow the switching pattern properly. In Figs. 24 and 25, the waveforms of the currents of the switches the modified inverter are shown. In Fig. 24(a), the currents of the switches S_{L1} and S_{U1} are shown which have a maximum value about 5A. In Fig. 24(b), the current waveforms of the switches S_{L3} and S_{L4} are presented. As seen, the switch S_{L3} is On while the switch S_{L4} is Off and vice versa. Fig. 25(a) presents the current waveforms of the switches S_{U3} and S_{U4}. Finally, Fig. 25(b) shows the current waveforms of the switches S_{T1} and S_{T2}. As obviously seen, all of the current waveforms presented in Fig. 24 and Fig. 25 are totally favourable and in agreement with the analysis.

For proving the capability of the modified grid-connected inverter in controlling the active and reactive power flows, the injected current and grid voltage under two different conditions, i.e. lagging and unity PF, are respectively presented in

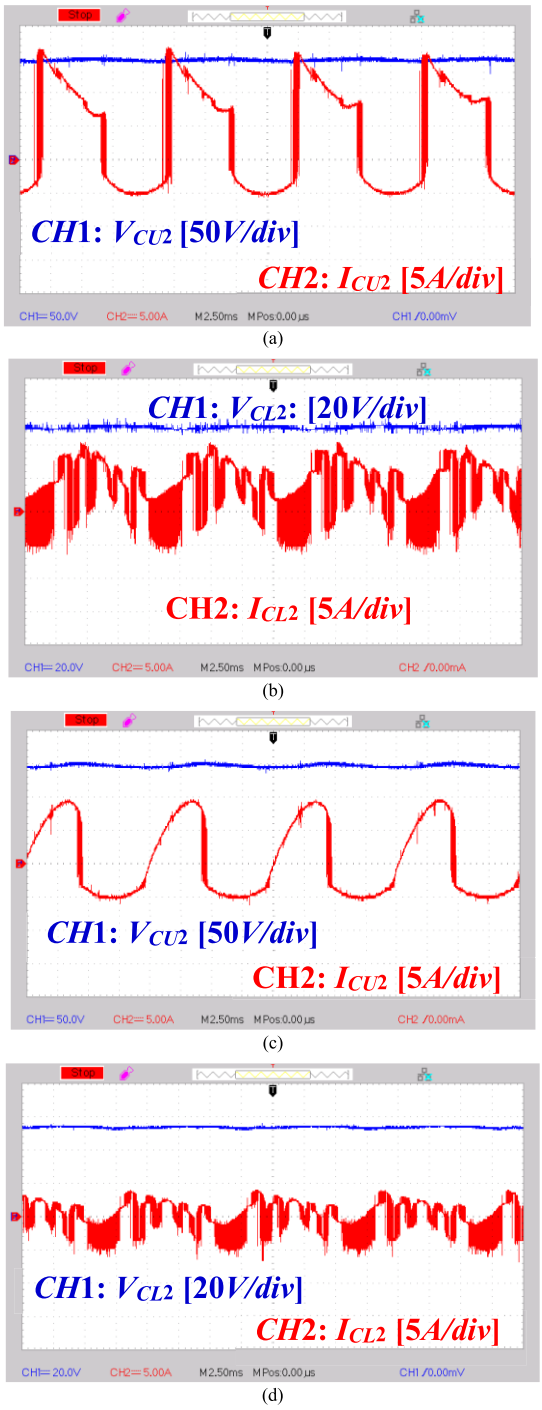


FIGURE 21. Voltage and current of capacitors without using supress inductor (a) the capacitor C_{U2} (50 V/div & 5A/div) (b) the capacitor C_{L2} (20V/div & 5A/div), Voltage and current of capacitors with using supress inductor (c) the capacitor C_{U2} (50 V/div & 5A/div) (d) the capacitor C_{L2} (20V/div & 5A/div).

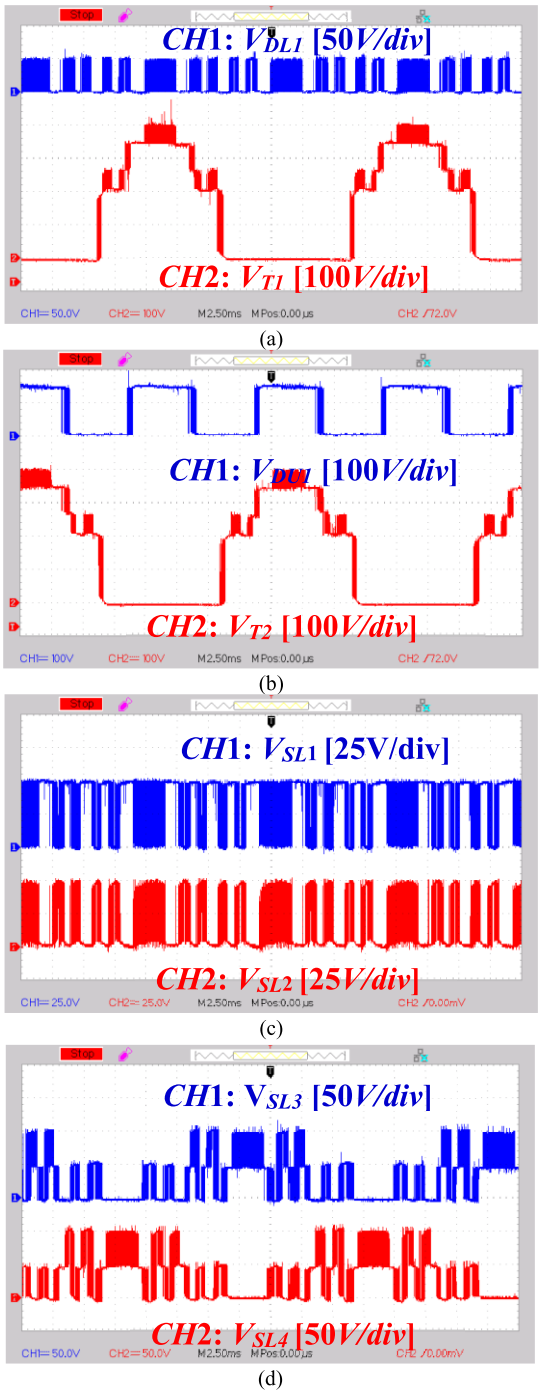


FIGURE 22. Voltages across (a) the diode D_{L1} & the switch T_1 (50 V/div & 100V/div) (b) the diode D_{U1} & the switch T_2 (100V/div & 100V/div) (c) the switches S_{L1} & S_{L2} (25V/div & 25V/div) (d) the switches S_{L3} & S_{L4} (50V/div & 50V/div).

Figs. 26 (a) and (b). In Fig. 26 (a), the inverter current lags its voltage which means that the inverter injects active and reactive power to the grid at the same time. Finally, in Fig. 26(b), the modified inverter works in the unity power factor condition where the inverter only injects active power to the grid. Obviously, the proposed inverter is completely able to show a desirable performance under all above-mentioned conditions. In Fig. 27, the experimental results of the modified grid-tied system by applying a step change in reference current amplitude are shown. In Fig. 27(a), the voltage of the capacitor C_{L2} and the current of the grid are shown. Fig. 27(b) presents the

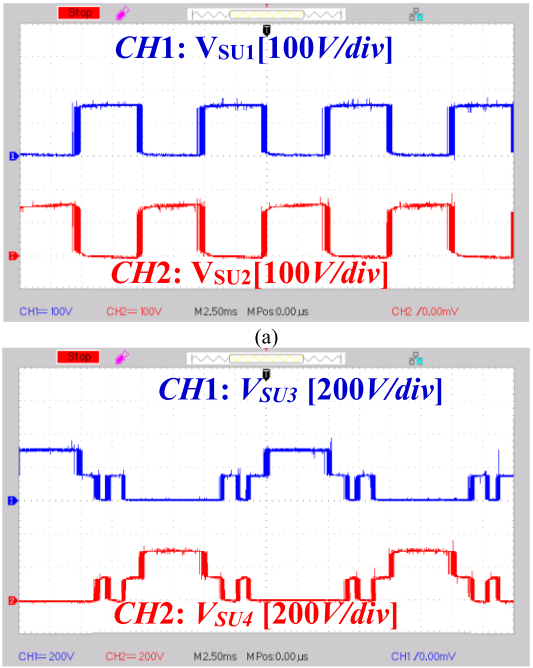


FIGURE 23. Voltages of the diode V_{SU3} & the switch V_{SU4} (200 V/div & 200V/div).

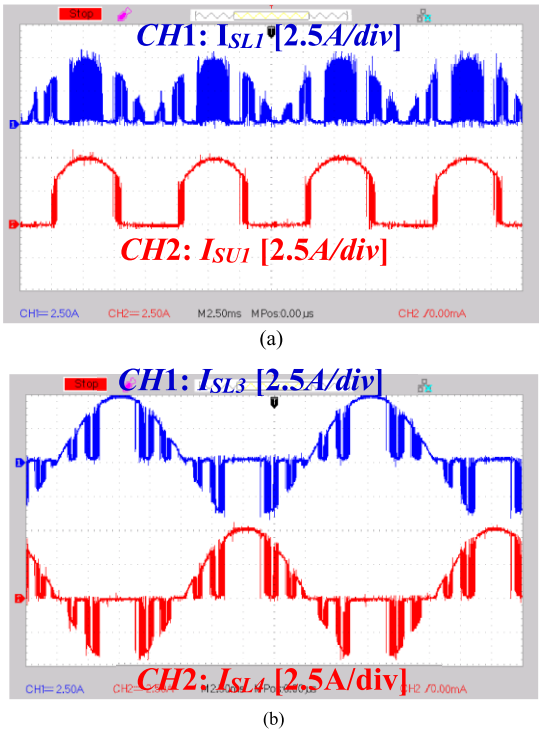


FIGURE 24. Current waveforms of (a) the switches S_{L1} & S_{U1} (2.5A/div & 2.5A /div) (b) the switches S_{L3} & S_{L4} (2.5A/div & 2.5A /div).

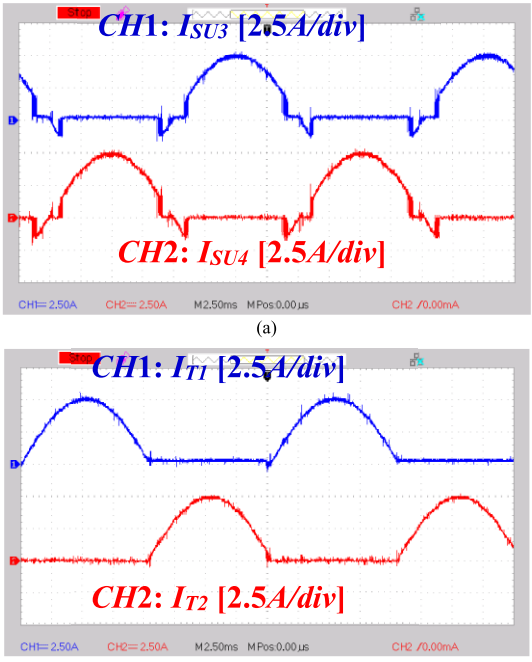


FIGURE 25. Current waveforms of (a) the switches S_{U3} & S_{U4} (2.5A/div & 2.5A /div) (b) the switches S_{T1} & S_{T2} (2.5A/div & 2.5A /div).

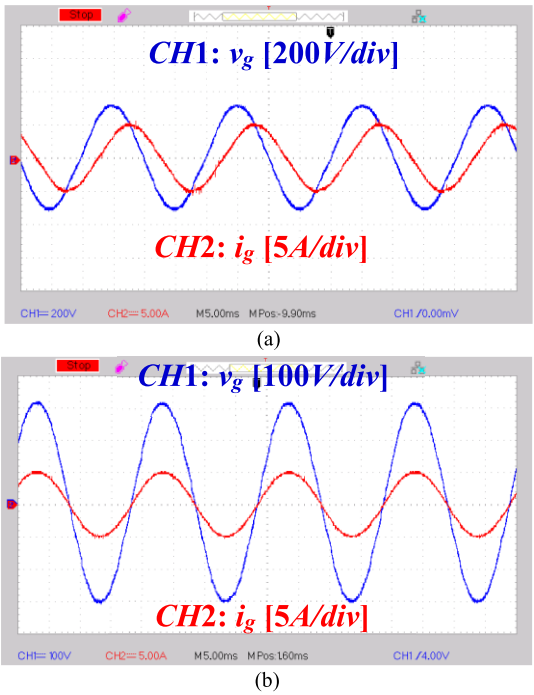
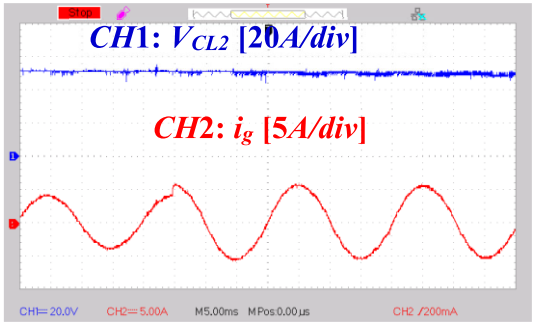
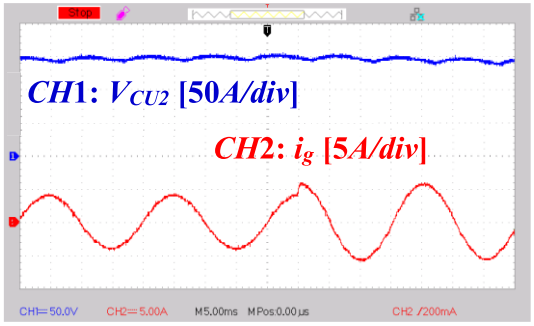


FIGURE 26. The grid voltage and the injected current waveforms under (a) lagging PF (200V/div & 5A/div) and (b) unity PF (100V/div & 5A/div).

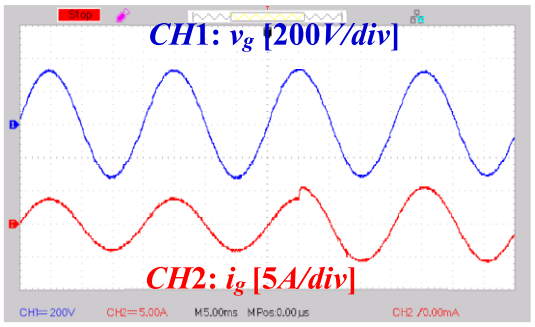
voltage of the capacitor C_{U2} and the current of the grid. In addition, in Figs. 27(c) and 27(d), the voltages and currents of the grid and the inverter are shown respectively. As seen, by changing the amplitude of the injected current into the grid from 4A to 5A, the output power increases from 622W to 777W. As clearly seen, the transient response of the modified system is desirable since in existence of this step change, the modified system is able to maintain its stability and work properly. According to the theoretical analysis presented in



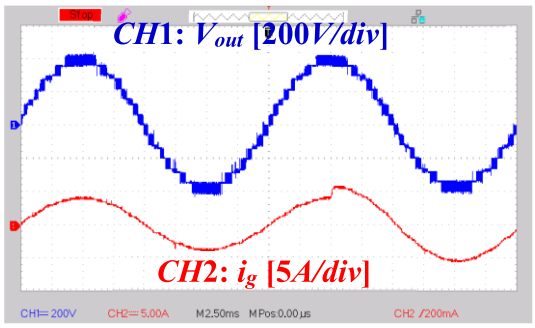
(a)



(b)



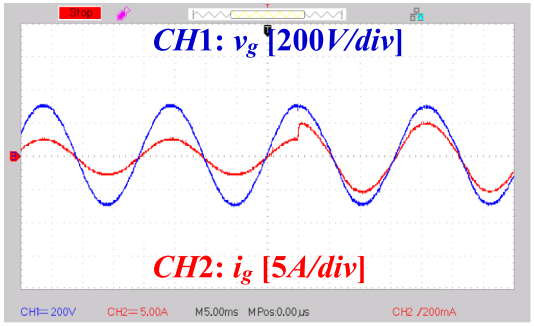
(c)



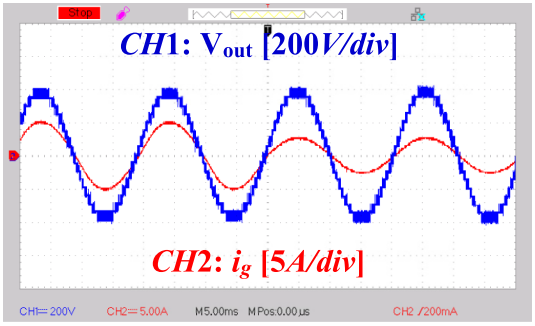
(d)

FIGURE 27. The experimental results under the applied step-change: (a) the voltage of the capacitor C_{L2} and the current of the grid (20V/div & 5A/div) (b) the voltage of the capacitor C_{U2} and the current of the grid (50V/div & 5A/div) (c) the voltage and current of the grid (200V/div & 5A/div) and (d) the voltage of the inverter and current or the grid (200V/div & 5A/div).

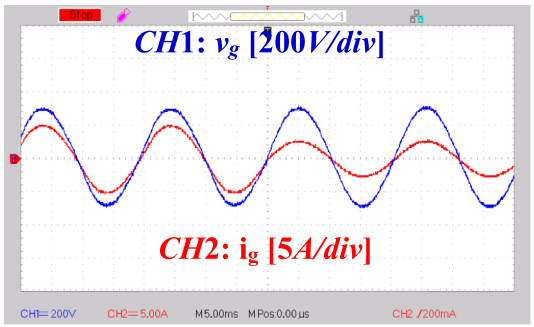
the previous sections, the efficiency of the modified MLI is calculated as 96.5%. In addition, the measured efficiency of the experimental circuit is 95.3%. In order to confirm a good dynamic response of the modified topology, step changes of the value of grid power have been applied.



(a)



(b)

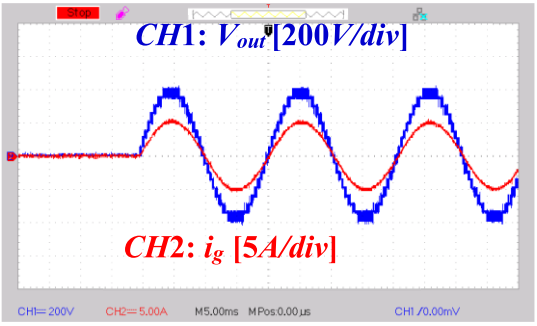


(c)

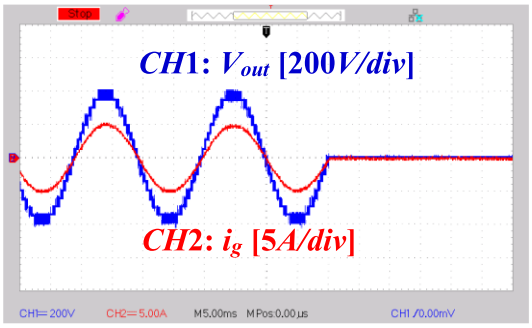
FIGURE 28. Dynamic performance of the proposed inverter under a step change in the amplitude of grid power: (a) Local grid's voltage (200 V/div) and injected current (5 A/div); (b) Output voltage (200 V/div) and injected current (5 A/div); (c) Local grid's voltage (200 V/div) and injected current (5 A/div).

Fig. 28(a) indicates the waveforms of grid voltage and injected current to the grid. Considering Fig. 28(a), the step change of the value of grid power is a change from 388W to 777W. Fig. 28(b) illustrates output voltage of the inverter and injected current to the grid. Fig. 28(c) depicts the waveforms of grid voltage and injected current to the grid. With respect to Fig. 28(b) and Fig. 28(c), the step change of the value of grid power is a change from 777W to 388W.

To verify the accurate performance of the proposed inverter, the experimental results during start to work and stop the working of inverter are presented in Fig. 29. Fig. 29(a) shows the output voltage waveform of the inverter along with injected current to the grid during start to work. Also, Fig. 29(b) illustrates the output voltage waveform of the inverter along with injected current to the grid during stop working.



(a)



(b)

FIGURE 29. Experimental results: (a) start to work, (b) stop the working.

Based on the results, desirable performance of the modified MLI along with the presented control method is validated making it suitable for numerous modern applications where a high-quality power is needed to be injected into the grid.

XI. CONCLUSION

In this paper, a 17-levels SC-based MLI is modified employing the flyback converter which in turn leads to need power components with lower ratings. This inverter possesses the boosting ability and can pass the reverse current for inductive loads through the involved power switches. The DC-DC flyback converter is used to generate two independent DC voltage link from the single input power supply which is an important economic advantage. In this inverter, the capacitors' voltages are balanced using a binary asymmetrical algorithm. In the modified converter an inductor and a parallel diode are used to reduce the capacitor's current spike during the capacitor charging mode. This is one of the most important advantages of the proposed inverter. Besides, by using the current control method, the modified inverter can control the amount of the active and reactive injected power to the grid. Based on the experimental results performed for the modified inverter in grid-connected mode, this SC-based MLI has a promising performance.

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