IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 1 September 2023, accepted 24 September 2023, date of publication 11 October 2023,
date of current version 18 October 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3323880

RESEARCH ARTICLE

3D NAND Flash Memory Cell Current and Interference Characteristics Improvement With Multiple Dielectric Spacer

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This work was supported in part by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (MSIT) under Grant 2021R1F1A1056255; and in part by the IC Design Education Center (IDEC), South Korea, for the EDA tool.

ABSTRACT To achieve high density, the spacer length of three dimensional (3D) NAND device has been scaled down. When the program/erase cycle repeats, problems such as electrons accumulation in the inter-cell region are occurred. To solve this problem, a method of replacing the spacer region material of 3D NAND device with a low-k materials has been proposed. In 3D NAND, carrier's lateral spreading occurs since all cells in the string share a same trap layer. In this work, we observed the change of cell current (I_{cell}) and interference characteristic after retention time on various dielectric constant of spacer region conditions. These two factors exhibit a trade-off characteristic. In this paper, we suggested the appropriate range of dielectric constant value. Based on this observation, we have proposed a suitable range of dielectric constants and suggested the Si_3N_4/ Air / Si_3N_4(N/A/N) multiple dielectric spacer structure to improve both I_{cell} and interference characteristics. In addition, performance improvement can be obtained through high-k / low-k / high-k multiple dielectric spacer structure. Improving the retention characteristics of 3D NAND flash memories through the proposed structure will contribute to improving the reliability of memory devices.

INDEX TERMS 3D NAND flash memory, multiple dielectric spacer, retention, interference, electron trap charge, lateral migration, technology computer aided design (TCAD).

I. INTRODUCTION

The transition from two-dimensional NAND (2D NAND) to three-dimensional NAND flash memory (3D NAND) architecture has brought several advantages in terms of cell lifetime, program speed, power consumption, and high density [1], [2], [3]. In the process of reducing dimension between cells, interference of pass voltage (V_{pass}) within neighbor cells become serious [4]. For reduction of V_{pass} interference which is induced by neighbor cells, low-k materials were applied to spacer region material between gate regions [5]. In the case of 2D NAND, when the dielectric constant of spacer material is reduced, both program and erase characteristics are improved because the capacitance

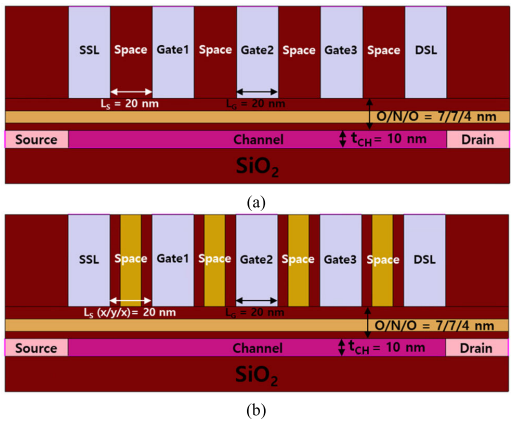

FIGURE 1. Simulation structure of NAND flash memory array (a) Single dielectric spacer and (b) Multiple dielectric spacer consists of x/y/x.

The associate editor coordinating the review of this manuscript and approving it for publication was Cristian Zambelli.

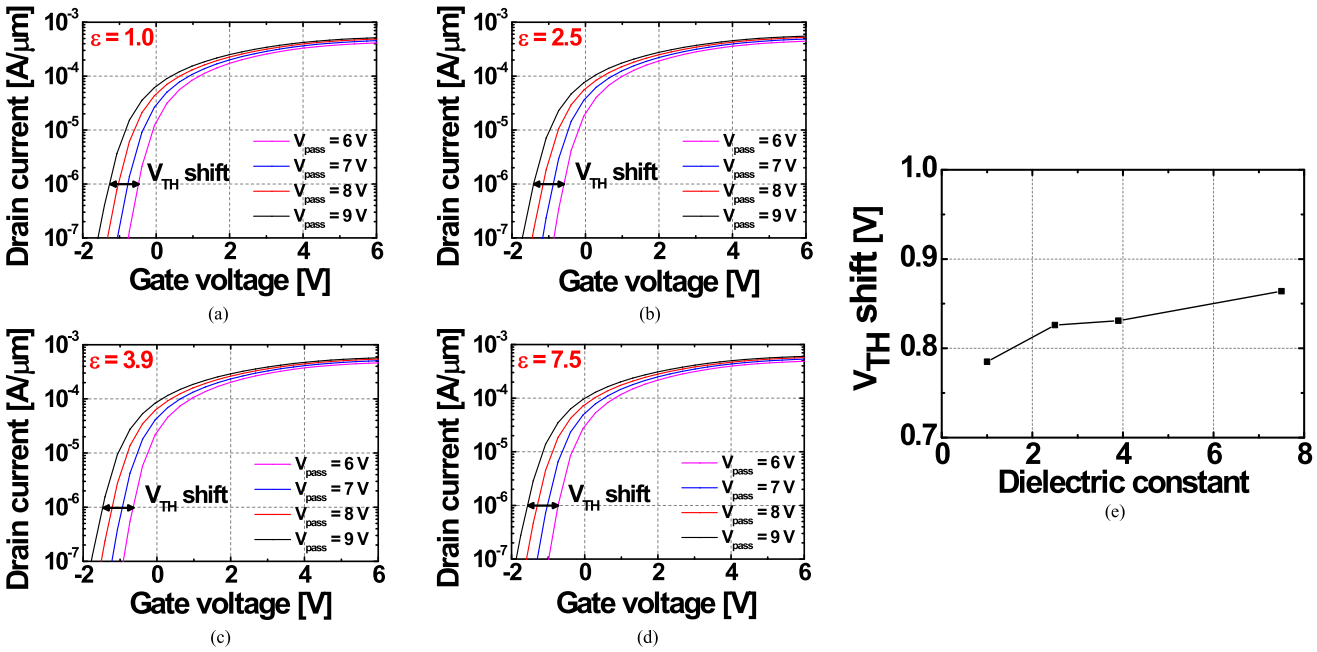

FIGURE 2. Transfer curve when V_{pass} varied from 6 V to 9 V with various spacer materials (a) air, (b) Low-k, (c) SiO_2, (d) Si_3N_4. (e) The variation of V_{TH} with V_{pass} varied from 6 to 9 V according to dielectric constant.

between cells decrease according to dielectric constant value [6], [7], [8]. On the contrary to 2D NAND, the trap layer in recent 3D NAND structure connected to each other [9], which causes many problems such as charge lateral spreading [10] and interference. In particular, when program/ erase cycle is repeated, the number of trapped electrons in the inter-cell region increases which causes a cell current (I_{cell}) reduction. In order to overcome this problem, research on replacing the spacer region material with a low dielectric constant material has been conducted [11]. As the dielectric constant of the spacer region material decreases, the number of trapped electrons in the inter-cell region decreases [12]. Therefore, previous studies have reported that using low-k materials as spacer materials can reduce the impact of the shield electric field. It can help suppress degradation caused by trapped charges in the inter-cell region. However, it has not been reported that the retention characteristic change according to dielectric constant. Since data retention characteristics in memory devices are an important parameter for device reliability, it is necessary to analyze the effect of changing spacer materials on retention characteristics. Therefore, research in 3D NAND flash memory aimed on improving cell current in this direction is essential.

In this study, we observe the variation of I_{cell} and interference characteristics after retention time on various dielectric constant conditions and introduce the optimum range for dielectric constant of spacer material. It would refer to materials that ensure the best reliability when designing device, taking into account the retention state. Furthermore, we proposed multiple dielectric spacer materials of low-k / high-k / low-k and high-k / low-k / high-k to improve properties based on the optimal range. It proposes a new form of dielectric material confirming its characteristics in the future development of 3D NAND technology.

TABLE 1. Device operation conditions.

	Erase	Program	Retention	Read
Selected cell	-18 V	20 V	0 V	-5 ~ 12 V
Unselected cell	0 V	6 ~ 9 V	0 V	6 ~ 9 V
DSL	0 V	7 V	0 V	7 V
SSL	0 V	0 V	0 V	7 V
B/L	0 V	0 V	0 V	1 V
Time	5×10^{-2} s	3×10^{-3} s	1×10^{3} s	-
Temperature	-	-	300 K	-

II. DEVICE STRUCTURE

The structure of single dielectric spacer in 3D NAND is shown in Fig. 1(a). Considering the symmetrical shape of 3D NAND flash memory, this study used a 2D structure, which is a cross-sectional shape. The device consists of two select transistors and three cells, and the length of tungsten used as the gate material is 20 nm. Source/drain doping concentration is n-type 5×10^{18} cm^{-3}, and channel doping concentration is p-type 2×10^{18} cm^{-3}. The thickness of tunneling oxide / nitride / blocking oxide is 4 nm, 7 nm, 7 nm [13], respectively. The channel length is 20 nm [12], and the channel thickness is 10 nm. The spacer length is 20 nm. In order to investigate the differences in the characteristics of 3D NAND based on the dielectric constant, measurements are conducted by changing the material to air ($\varepsilon = 1.0$), low-k ($\varepsilon = 2.5$), SiO_2

($\varepsilon = 3.9$), and Si_3N_4 ($\varepsilon = 7.5$). There is a limitation on the available dielectric materials and their constant when using a single dielectric spacer. The use of multiple dielectric spacers overcomes the limitations of single dielectric spacers and allows high flexibility in tuning the dielectric properties as various dielectric constants can be achieved. Furthermore, we proposed to improve the performance of I_{cell} and interference by conducting simulations and interpreting the results of the multiple dielectric spacer. In Fig. 1(b), a multiple dielectric spacer with a length of 20 nm was configured in an x/y/x structure. Two kinds of cases are applied to the multiple dielectric spacer: one with *1) low-k / high-k / low-k* configuration and the other with *2) high-k / low-k / high-k* configuration. The thickness of the y layer is varied from 2 nm to 16 nm in increments of 2 nm, and the simulation results of that condition are analyzed. In the case of low-k / high-k / low-k configuration using SiO_2/ Si_3N_4/ SiO_2(O/N/O). In case of the high-k / low-k / high-k configuration using Si_3N_4/ Air / Si_3N_4(N/A/N). The simulations are performed for structure of Fig. 1(a) and (b) using Synopsys' Sentaurus technology computer aided design (TCAD). The operation conditions are described in Table 1. Nonlocal tunneling (NLT) model was applied for the interface of the channel and tunneling oxide and Shockley Read-Hall (SRH) [14] is also applied.

III. RESULTS AND DISCUSSION

In this study, I_{cell} and interference were measured to find out the change in retention characteristics of 3D NAND according to dielectric constant. I_{cell} is extracted from the bias condition that gate voltage (V_g) is 10 V and V_{pass} is 8 V. The I_{cell} was 456 μA/μm at $\varepsilon = 1.0$ (air) and 451 μA/μm at $\varepsilon = 7.5$ (Si_3N_4). The I_{cell} remains almost constant regardless of the dielectric conditions, and this can be attributed to the screen effect [12].

Figure 2(a)–(d) depict the threshold voltage (V_{TH}) shift in response to the variation of V_{pass} with different dielectric constant spacers. ΔV_{TH} indicates the range of initial V_{TH} when V_{pass} is varied from 6 V to 9 V, and it can be considered as the amount of V_{pass} interference [4]. V_{TH} was extracted by the constant current method, and the V_{TH} extraction current level is 1 μA/μm [15]. When the V_{pass} increases from 6 V to 9 V, the V_{TH} shift was 0.78 V at ε =1.0. the ΔV_{TH} was 0.83 V at $\varepsilon = 7.5$. It can be analyzed that the interference of the V_{pass} increasing with the higher dielectric constant condition, as shown in Fig. 2(e).

A. SINGLE DIELECTRIC SPACER MATERIAL

Figure 3 shows the I_{cell} at program state before and after 1,000 s retention at 300 K depending on the dielectric constant value of the spacer material, and the interference of the V_{pass} variation. When the dielectric constant of spacer region increases, the interference become worse while the change of I_{cell} is negligible for 0 s, as shown in Fig. 3(a). In Fig. 3(b), when the dielectric constant of spacer region increases, the interference also become worse. On the contrary to results at 0 s, the spacer dielectric material had a dominant effect on the

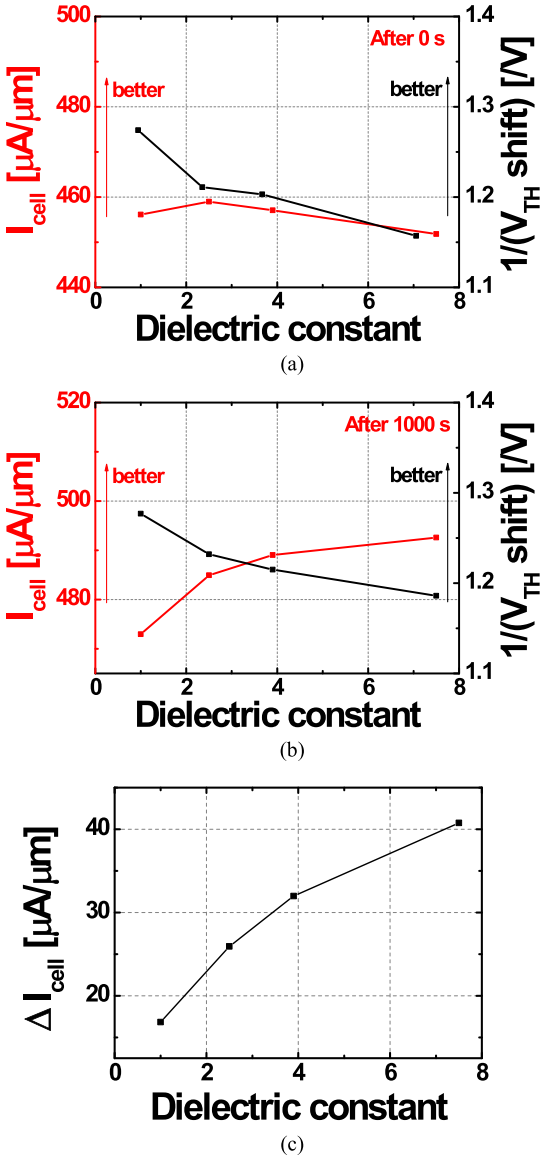

FIGURE 3. The characteristic of I_{cell} and interference according to V_{pass} in single dielectric spacer material (a) when retention time was 0 s, (b) when retention time was 1,000 s. (c) The variation of I_{cell} from retention time 0 s to 1,000 s.

interference characteristic [16], [17]. If the change of I_{cell} is extracted separately, the ΔI_{cell} is 16 μA/μm at $\varepsilon = 1.0$ and 32 μA/μm at $\varepsilon = 3.9$ from retention time after 0 s to 1,000 s, which is increased as the dielectric constant become higher, as shown in Fig. 3(c). It can be explained as trapped electron lateral migration model of Fig. 4 as below.

There are distributions of the etrappedcharge after retention 0 s and the 1,000 s when the dielectric constant of space material is 1.0, 2.5, 3.9 and 7.5, as shown in Fig. 4(a)–(d). Higher dielectric constant is observed to result in an increased etrappedcharge in the selected cell after programming which means retention time is 0 s. Since all cells in the string share the charge trap layer (CTL), the electrons can move to inter-cell region after retention at 300 K. Figure 4(e)

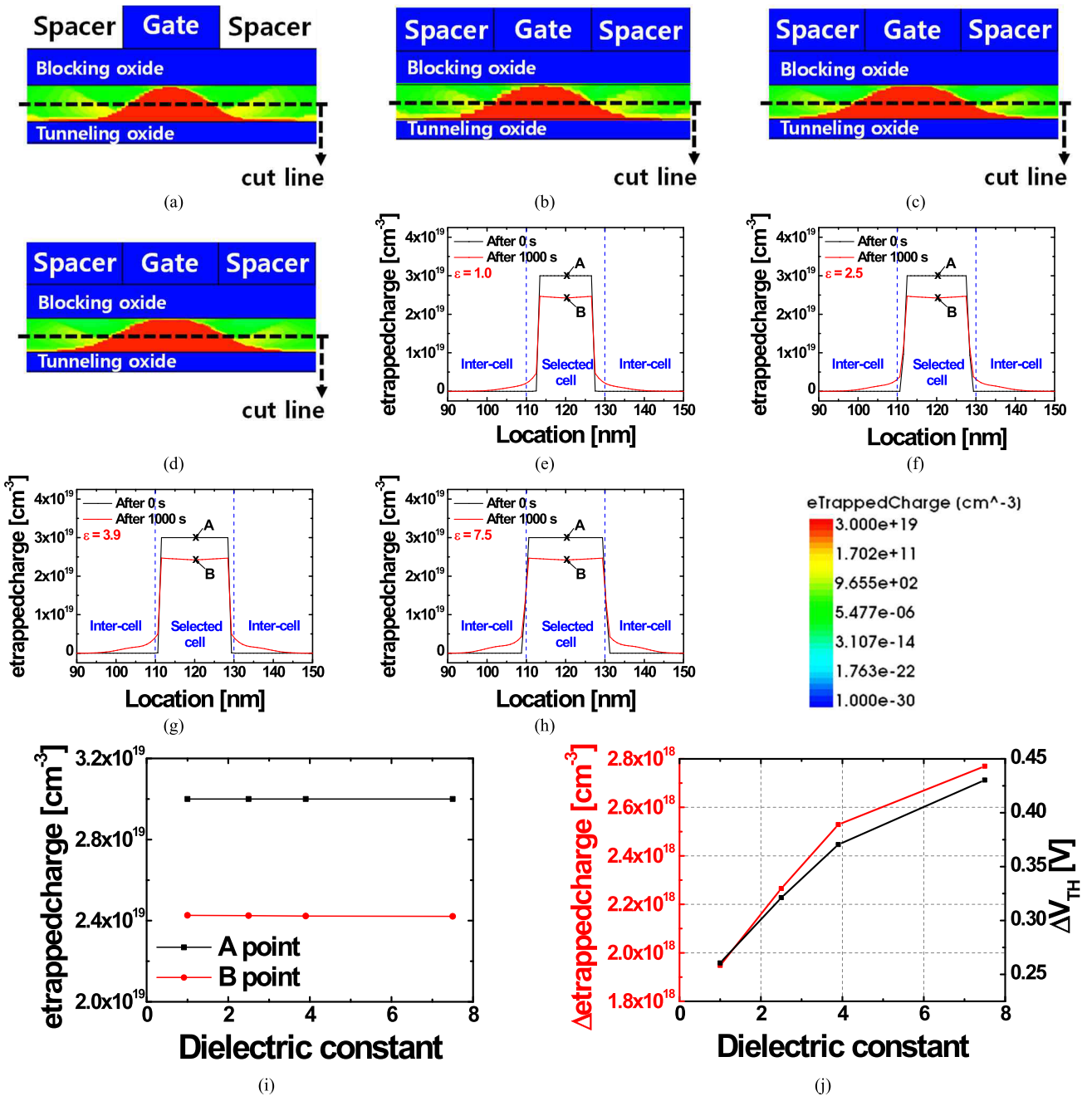

FIGURE 4. The etrappedcharge distribution in nitride layer after program operation with (a) $\varepsilon = 1.0$, (b) $\varepsilon = 2.5$, (c) $\varepsilon = 3.9$, (d) $\varepsilon = 7.5$. The etrappedcharge distribution about cutting the middle of CTL after retention 0 s and 1,000 s with (e) $\varepsilon = 1.0$, (f) $\varepsilon = 2.5$, (g) $\varepsilon = 3.9$, (h) $\varepsilon = 7.5$. (i) The etrappedcharge values at points 'A' and 'B'. (j) Δetrappedcharge in selected cell region and Δ_{VTH} after 1,000 s on various dielectric constant conditions.

shows the amount of etrappedcharge decreased in selected cell region and the amount of V_{TH} change after retention 1,000 s. The distribution of etrappedcharge cut along the cutting line in the middle of the CTL in Fig. 4(a)–(d) is measured in the initial state (retention time = 0 sec), and after 1,000 sec, the distribution changes as shown in Fig. 4. In Fig. 4(e)–(f), the point 'A' refers to the etrappedcharge value at the center of the selected cell for after retention 0 s, the point 'B' refers to the etrappedcharge value at the center of the selected cell for after retention 1,000 s. In Fig. 4(i), the values of points 'A' and 'B' are formed at similar levels after retention 0 s and 1,000 s, regardless of the dielectric constant. However, they are distributed in trap charge distribution range at the border area, as shown in Fig. 4(e)–(h). The changes in the etrappedcharge formed in the selected cell and the remaining etrappedcharge after retention 1,000 s, as shown in Fig. 4(j). As the dielectric constant is increased, the significant lateral migration was observed. As a result, the difference in etrappedcharge amount change for each dielectric constant is shown, in Fig. 4(j) [18], [19],

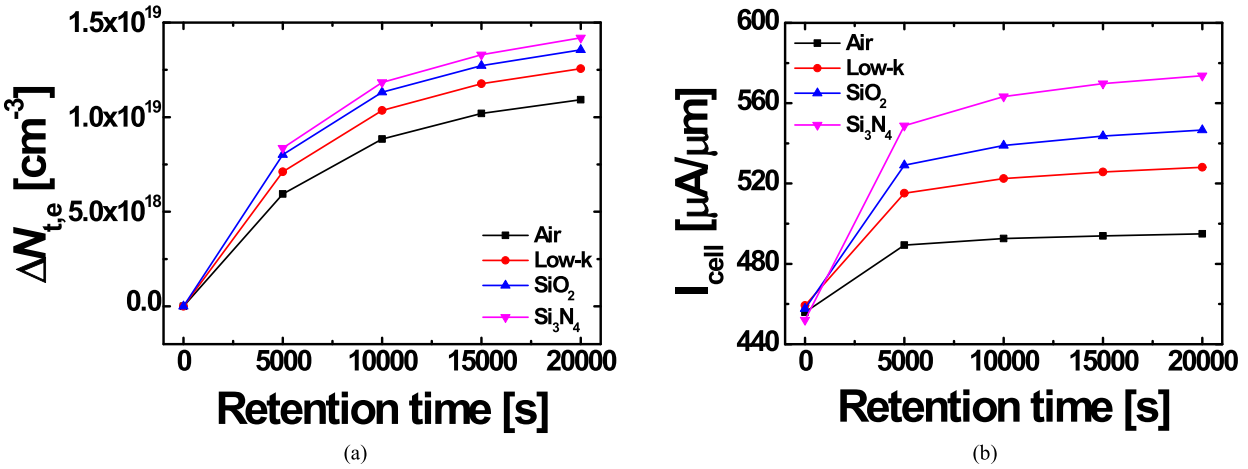

FIGURE 5. Measurement data from retention time 0 s to 20,000 s, increasing 5,000 s (a) the amount of change of etrappedcharge in selected cell region. (b) the variation of I_{cell}.

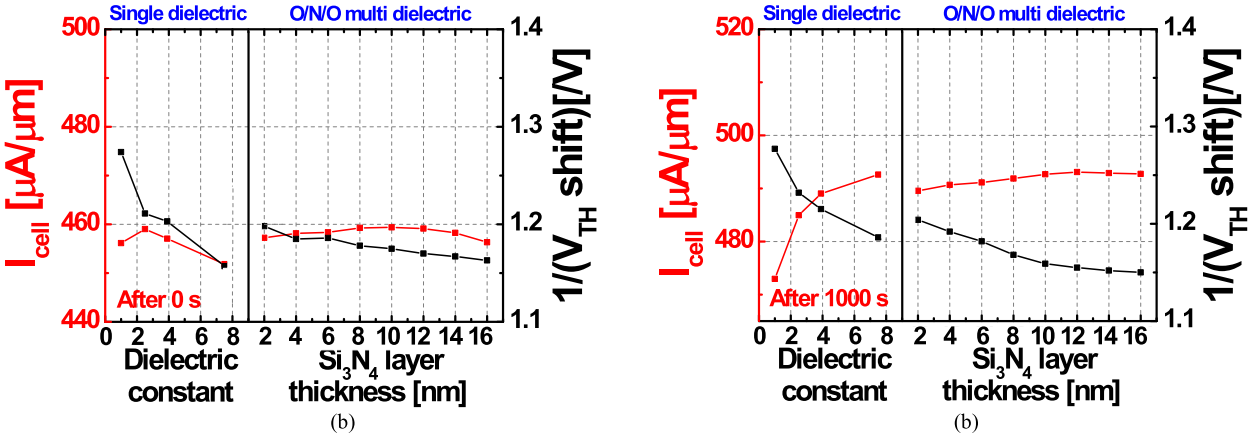

FIGURE 6. The characteristic of I_{cell} and interference according to V_{pass} in single and O/N/O multi dielectric spacer material (a) when retention time was 0 s, (b) when retention time was 1,000 s.

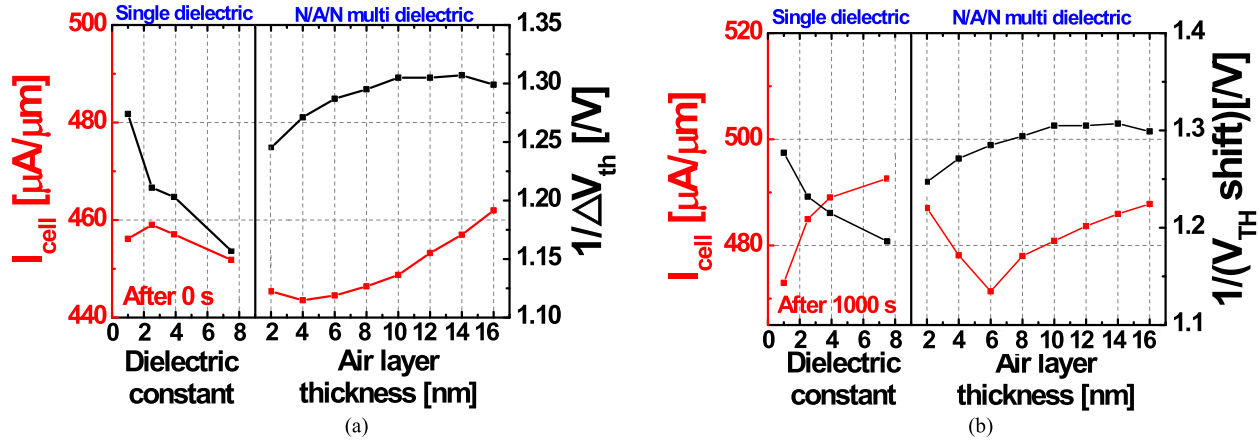

FIGURE 7. The characteristic of I_{cell} and interference according to V_{pass} in single and N/A/N multi dielectric spacer material (a) when retention time was 0 s, (b) when retention time was 1,000 s.

[20], [21]. The etrappedcharge in the cell area, which is caused by being proportional to the change in V_{TH}, has a direct effect on the change in I_{cell}. It means that I_{cell} increases when the spacer material has a high dielectric constant due to a low cell V_{TH} after 1,000 seconds, as shown in Fig. 4(j).

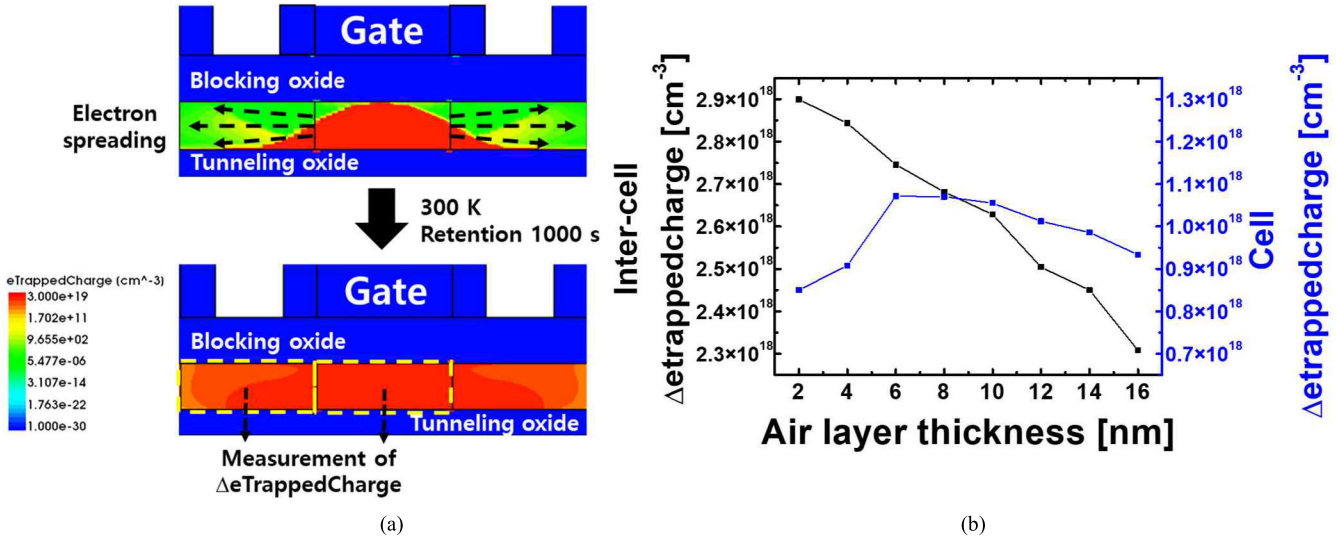

FIGURE 8. (a) The measurement sequence of Δetrappedcharge. (b) The variation of etrappedcharge cell and inter-cell at CTL.

In Fig. 5(a), the total number of electrons stored in the CTL of the selected cell region is measured by increased time from 0 s to 20,000 s. The lateral migration rate gradually decreased with the retention time. Most of the electrons trapped in the program cells do not spread even after a considerable amount of time has passed [18]. Figure 5(b) represents the measurement of I_{cell} as time increases from 0 s to 20,000 s. As the retention time increases, the I_{cell} is saturated. Similar to the result of Fig. 4(j), this cause by ΔV_{TH} due to the difference in etrappedcharge changes in the selected cell region of Fig. 5(a). It can be explained by the effect of the spreading of the etrappedcharge from the selected cell region to the inter-cell region is larger than the screen effect, regardless of the dielectric constant of the spacer material. As a result, it can be concluded that lowering V_{TH} increases I_{cell}.

B. MULTIPLE DIELECTRIC SPACER MATERIAL

In chapter A, considering I_{cell} and interference at the same time, the optimum dielectric constant was in the range of 3.5 to 4.5. However, considering that dielectric materials used in semiconductor processes are limited, it will be difficult to match the optimal dielectric constant value with a single dielectric. If dielectrics with multiple dielectric constants are combined according to their thickness, spacer dielectrics with various equivalent dielectric constants can be obtained. A multiple material spacer can enhance the characteristics of I_{cell} while minimizing the degradation of interference. The simulation is conducted to investigate the changes in I_{cell} and interference characteristics based on the ratio difference between SiO_2 and Si_3N_4, as shown in Fig. 1(b).

Figure 6 shows the I_{cell} and interference characteristics before and after retention. The I_{cell} of O/N/O multiple dielectric spacers is similar with the I_{cell} of a single dielectric spacer regardless of Si_3N_4 thickness due to stronger screen effect at after retention 0 s as shown in Fig. 6(a). After 1,000 s retention, the I_{cell} of the multiple dielectric spacers shows the I_{cell} characteristics combining SiO_2 and Si_3N_4 material as shown in Fig. 6(b). Since the dielectric constant of O/N/O multiple dielectric spacers are determined by the combination of SiO_2 and Si_3N_4 resulting in values between the dielectric constants of SiO_2 and Si_3N_4 materials. Interference characteristic deteriorated as the increase Si_3N_4 layer thickness influenced by the overall dielectric constant. Similar with the before retention state, interference characteristics increased that influenced by the overall dielectric constant.

In Fig. 6 the I_{cell} are not significantly affected by the overall dielectric constant in the O/N/O multiple dielectric spacers. But interference is affected by the overall dielectric constant of the spacer. Based on these results, we propose a modified multiple spacer dielectric layers to achieve high I_{cell} while minimizing interference by using an N/A/N multiple dielectric spacer. Additional analyzes were performed by splitting the air layer thickness from 2 nm to 16 nm in increments of 2 nm. Figure 8 represents the I_{cell} and interference characteristics after retention 0 s and 1,000 s. In Fig. 7(a), the increase of air layer thickness leads to reduction of the screen effect, resulting in an increase of I_{cell} at initial state (0 s) [12]. The interference is improved as the portion of air increases due to the lower capacitance effect by the decrease of effective dielectric constant of the N/A/N structure. Figure 7(b) shows that the I_{cell} gradually decrease by 6 nm and then abruptly increases after 1000 s retention. Also, the interference characteristics are improved with increasement of air layer thickness as expected.

In order to investigate the cause of the variation in I_{cell}, the Δetrappedcharge in both inter-cell and cell region were extracted, as shown in Fig. 8. The etrappedcharge in the cell region spreads to the inter-cell region, as shown in Fig. 8(a) [23], [24], [25]. Figure 8(b) represents the difference between the values at 1,000 s and 0 s in the inter-cell region, and

the difference between the values at 0 s and 1,000 s in the cell region. When the air layer thickness is between 2 nm and 6 nm, Δetrappedcharge in the cell region increases. This increase of Δetrappedcharge leads decrease in I_{cell}. However, when the air layer thickness is over 6 nm, reduction of Δetrappedcharge in the cell region remains relatively constant. On the other hand, Δetrappedcharge significantly decrease in the inter-cell region. This is because when the thickness of the air layer is increased, the electric field effect toward the spacer is weakened and the screen effect is reduced [12], [26]. This phenomenon arises from the reduction of electron charge in the previously shielded inter-cell region due to the screen effect. The mitigation of screen effect in the inter-cell region leads I_{cell} increasing. As a result, the variation of I_{cell} after retention is directly influenced by the migration of etrappedcharge, as well as the screen effect caused by the inter-cell region.

IV. CONCLUSION

In this study, the characteristics of I_{cell} and interference were investigated with the retention state considering the dielectric constant variation. In addition, the structure of O/N/O and N/A/N multiple dielectric spacer are proposed to examine the characteristics of both I_{cell} and interference. In single dielectric spacer, the I_{cell} increased as the V_{TH} shifted due to the change of etrappedcharge between retention states. In this case, a higher dielectric constant resulted in a larger quantity of electrons stored in the cell, causing the tendency of spreading a greater number of electrons during retention. Regardless of retention, interference was directly influenced by the dielectric constant. As a result, it was concluded that there is a trade-off relationship between I_{cell} and interference with a single dielectric spacer. The optimal point is determined to be in the range of $\varepsilon = 3.5$ to 4.5, which is the midpoint between $\varepsilon = 1.0$ and $\varepsilon = 7.5$. In the O/N/O multiple dielectric spacer structure, the increase in I_{cell} was not significant which was attributed to the influence of the vertical electric field formed in the blocking oxide. However, in the N/A/N multiple dielectric spacer structure, the I_{cell} showed a decreasing trend followed by an increasing trend. This is because the decrease of the etrappedcharge in the cell region is followed by an increase trend. While in the inter-cell region, the previously shielded electrons due to the screen effect decreases. Similar to the case of a single dielectric spacer, interference is primarily influenced by the effective dielectric constant. In conclusion, it was confirmed that using the N/A/N multiple dielectric spacer can improve both I_{cell} and interference factors during retention in the 3D NAND flash memory array.

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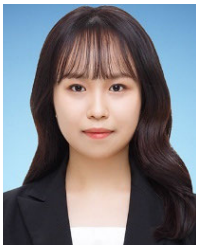

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