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APPLIED RESEARCH

An Improved IPOS LLC Resonant Converter With Sub-Module Output Voltage Sharing in Low Ripple High-Voltage Applications

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ABSTRACT This paper proposed an input-parallel and output-series (IPOS) LLC resonant converter for applications with high voltage gain and low ripple, which considers the sharing of submodule output voltages. The resonant converter proposed has an integrated magnetics, which improves the utilization of the core. The reason is because magnetic fluxes can be superimposed or cancelled each other when the resonant currents are interleaved. Moreover, the influence of parameter mismatch in the resonant tank on voltage and current sharing in IPOS-LLC was analyzed based on the passive impedance theory. The results show that, by selecting smaller quality factors and using N-connections in high-voltage applications, the sharing of output voltage among modules can be well reflected, despite tolerances of the resonance parameters. Meanwhile, the voltage stress distribution of the rectifier diodes in each submodule is optimized, which improves the reliability of the circuit. By using the aforementioned conclusions, a prototype with 90 kHz, 40 V/4.8 kV, and 1.15 kW is established. The measured output voltage mismatch of 3.1% and voltage ripple rate of 0.16% at 3.7 nF output capacitance proves the effectiveness and correctness of the proposed resonant converter design.

INDEX TERMS High-voltage, voltage sharing, magnetic integration, resonant converter.

I. INTRODUCTION

The demand for high-voltage power supplies (HVPS) has grown over the last few decades due to the development of various industrial applications, including microwave generators [1], electrostatic precipitators [2], physical experiment [3], and medical X-ray sources [4]. Resonant converters are widely applied in HVPS designs, due to its capabilities of behaving as soft switches and using parasitic parameters as a resonant component.

Besides the requirements of high voltage output and high efficiency, low ripple and arc energy are also important criteria to evaluate the performance of HVPS. However, the traditional single-phase resonant converter hardly meets these requirements because its AC ripple frequency is only twice the switching frequency [5]. On the one hand, the output capacitor capacity must be increased to achieve low output ripple. On the other hand, the energy of its internal occasional arc discharges must be reduced to safe drive magnetrons, as they typically require operating voltages of tens of kilovolts. The energy stored in the output capacitor of HVPS is proportional to the arc energy. These problems can be solved by the multiphase resonant converter that uses the parallel interleaved approach [6], [7], [8], [9], [10]. Jang et al. [1]uses a multi-module resonant converter with input parallel and output series (IPOS) to increase the output voltage. The outputs of each module are stacked in series to obtain a higher output voltage, so the DC gain of each module is limited to a lower level [11], [12], [13], [14]. Moreover, each primary module is controlled using a parallel interleaved method.

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As a result, the output ripple presents a higher frequency and a lower amplitude, thus reducing the output capacitance and the arc energy concurrently. In addition, Marzang et al. [25] proposes a novel non isolated step-up circuit. By properly configuring the active LC network, high voltage gain is achieved without the use of coupled inductors, and the high voltage stress of power devices is reduced, which provides a reference for reducing device voltage stress in high-voltage applications.

However, there are other technical difficulties for IPOS resonant converters. Since the tolerance exists in resonant devices, it is hard to achieve output voltage sharing among the submodules of the IPOS converter, which will seriously affect the reliability of HVPS. At present, this problem is unresolved. Li [15] reported a coupling transformer such that equal flux flows through the secondary side of each module transformer, to achieve a balanced output voltage for both modules. Nevertheless, this approach cannot be extended to applications with more than two phases.

Before applying the parallel interleaving technique, the input current mismatch must be solved [16]. Because of the current mismatch [17], [18], [19], [20], [21], [22], the conduction losses and temperature rise of each module be significantly different. The approach of determining current phase of each module is used in literature [23] to assess the degree of current mismatch before using a phase shift operation to reduce the mismatch. In literature [16], a low-power DC-DC auxiliary converter is added to the output of each phase. The current sharing effect is optimized by varying the duty cycle of the auxiliary converter, which can be extended to multi-phase converters. However, all the methods mentioned above require the introduction of additional sampling circuits, which complicates the design. A passive impedance technique was presented in literature [22] to accomplish automatic current sharing with better performance. It enables all converters to operate in the same phase, which significantly increased the output ripple.

In this paper, an IPOS-LLC resonant converter for high-voltage applications is proposed, to obtain low output voltage ripple and low arc energy. In particular, the design of output voltage sharing among sub-modules is accomplished in the presence of tolerances in the resonant devices. There are three main contributions in this paper. Firstly, by analyzing the resonant tank characteristics, a design method with reducing the output voltage mismatch between sub-modules is presented. Secondly, it is found that the neutral point grounded configuration outperforms the neutral point floating configuration in terms of output voltage sharing. Thirdly, a three-phase magnetically integrated transformer topology based on flux cancellation is presented to decrease the volume of the core. It has smaller parasitic parameters and core losses compared to the single high-voltage transformer. Finally, in order to verify the high-voltage operating performance of the proposed converter, a maximum output power of 1.15 kW, 40 V/4.8 kV, voltage ripple of 0.16%, and output voltage

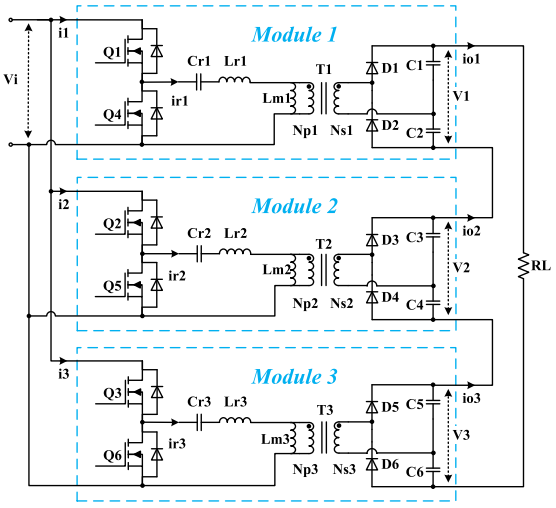

FIGURE 1. Scheme of proposed IPOS-LLC.

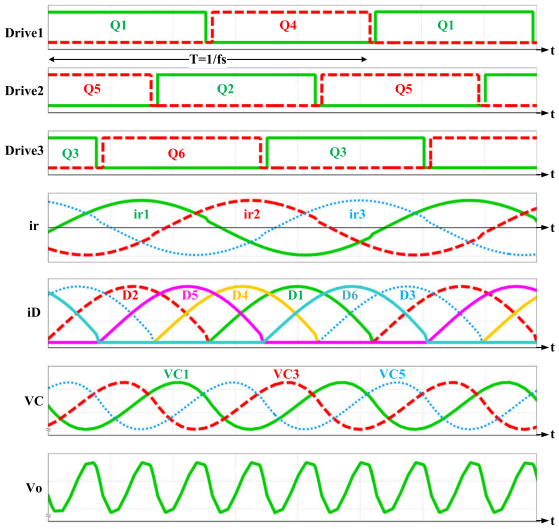

FIGURE 2. Key operating waveforms of IPOS-LLC.

mismatch of 3.1% are established. The experimental results show that the converter has excellent output voltage-sharing capability with a peak efficiency of 95.1%.

II. CONFIGURATION OF PROPOSED CIRCUIT

The principle of the LLC resonant converter is well known [5], [6], [7] and no longer described in detail. It has excellent high-frequency operation characteristics and provides zero voltage switching (ZVS) in the primary and zero current switching (ZCS) on the secondary. Since only half the components of a full-bridge circuit and half the number of turns of the primary coil are used in a half-bridge circuit, which usually is applied in step-up circuit [1], [2], [3]. Fig. 1 shows the schematic diagram of the proposed IPOS-LLC, which consists of three half-bridge LLC converter modules.

To increase the output voltage, the output rectification structure of the LLC converter uses three voltage-doubler rectifiers stacked in series to supply the load. On the one

hand it reduces the number of diodes by half compared to the full-bridge rectifier circuit, and no taps are required, which greatly simplifies the system's structure. On the other hand, the output voltage of a single rectifier module is only one third of the total output. As a result, the transformer can use less insulation material. Inspired by the multi-phase parallel interleaved current sharing method [16], the rectifier is connected in series with the output to make the voltage stress on the diodes evenly distributed. Meanwhile, the number of turns in the secondary winding of a single transformer is greatly reduced. Moreover, the parasitic capacitance of the transformer can be ignored.

On the primary side, $Q_1 - Q_3$ represents MOSFET switches, $L_{r1} - L_{r3}$ represents the resonant inductors, $C_{r1} - C_{r3}$ represents the resonant capacitor, and $L_{m1} - L_{m3}$ represents the magnetizing inductors of transformer. Transformers $T_1 - T_3$ realizes the energy transfer as well as the step-up function, and the turns ratio of the secondary winding to the primary winding is $n = N_s/N_p$.

On the secondary side, each voltage-doubler rectifier module consists of two diodes with two capacitors, corresponding to $D_1 - D_6$ and $C_1 - C_6$. Fig. 2 shows the key operating waveforms of the IPOS-LLC, where the half-bridge inverter on the primary side of each module is controlled by a set of complementary drive signals, and a sufficient dead time is inserted to ensure that ZVS is achieved. During a completed switching cycle, the rectifier diodes of the voltage-doubler rectifier module complete two charging behaviors, as shown in Fig. 2. For example, module 1 charges C_1 through D_1 and C_2 through D_2. The phase difference of the three driving signals is 120°, and the resonant currents $i_{r1} - i_{r3}$ on the primary side always operate in continuous mode, keeping the interleaving of phase and equal of amplitude, therefore lowering output ripple. The ripple V_c of the output voltage of each module is interleaved and cancelled each other, as a consequence the converter can achieve low ripple output by configuring a small output capacitor.

III. PARAMETER CHARACTERISTICS ANALYSIS

A. PREREQUISITES FOR IPOS-LLC OUTPUT VOLTAGE SHARING

To avoid avalanche breakdown of the semiconductor devices and ensure stable operation, the output voltage needs to be evenly distributed among the different modules. Moreover, the current of each module also need to be evenly distributed to balance the conduction losses of each circuit [14]. Ideally, the mathematical relationship of all modules are represented as follows:

$$\begin{cases} i_o = i_{oj} \\ i_1 = i_2 = i_3 \\ V_o = \sum_{j=1}^{3} V_j \\ P_j = V_j \cdot i_{oj} \end{cases} \tag{1}$$

where V_o is the total output voltage, i_o is the total output current, V_j is the output voltage of each module, i_{oj} is the output current of each module, i_j is the average value of the input current of each module, P_j is the input power of each module, $j = 1, 2, 3$. It can be derived from the above equations that the equivalent input impedance of each module is equal, and the output voltages will be balanced, when the input power of each module is balanced.

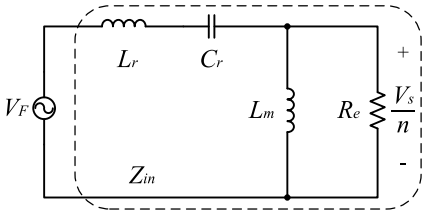

FIGURE 3. Equivalent circuit of resonant tank.

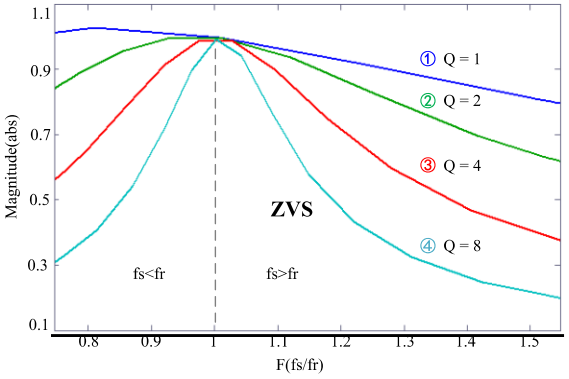

FIGURE 4. Relationship between voltage gain and switching frequency (k=6).

B. CHARACTERISTICS OF LLC RESONANT TANK

Based on the fundamental wave analysis method, the equivalent circuit of a single LLC module is shown in Fig. 3. where V_F is the Fourier fundamental component of the voltage at the midpoint of the half-bridge arm, which supplies the resonant cavity. V_S is the fundamental component of the voltage at the secondary winding. The resonant tank is shown as follows:

$$\begin{cases} f_r = \dfrac{1}{2\pi\sqrt{L_r C_r}}, F = \dfrac{f_s}{f_r}, k = \dfrac{L_m}{L_r} \\ Z_r = \sqrt{\dfrac{L_r}{C_r}}, Q = \dfrac{1}{R_e}\sqrt{\dfrac{L_r}{C_r}}, R_e = \dfrac{2R_L}{n^2\pi^2} \end{cases} \tag{2}$$

$$V_F = \frac{2V_i}{\pi}\sin(\omega_s t + \varphi) \tag{3}$$

$$Z_{out} = j\omega L_m // R_e = \frac{j\omega L_m R_e}{R_e + j\omega L_m} \tag{4}$$

$$Z_{in} = j\omega L_r + 1/j\omega C_r + (j\omega L_m // R_e) \tag{5}$$

where f_r is the series resonant frequency, F is the normalized frequency, Z_r is the characteristic impedance of the resonant tank, k is the ratio of excitation inductance to resonant inductance, and Q is the quality factor. R_L is the output load, R_e is the equivalent load. Phase-lead or phase-delay between

V_F and the resonant current is $\varphi.f_s$ is the switching frequency, the input impedance of the resonant tank is Z_{in}, and the output impedance is Z_{out}. Considering (2)-(5), the voltage gain can be defined as (6), and further obtained as (7):

$$G(j\omega) = \frac{Z_{out}}{Z_{in} + Z_{out}} = \frac{\dfrac{j\omega L_m R_e}{R_e + j\omega L_m}}{j\omega L_r + \dfrac{1}{j\omega C_r} + \dfrac{j\omega L_m R_e}{R_e + j\omega L_m}} \tag{6}$$

$$G(k, F, Q) = \frac{kF^2}{\sqrt{\left[(1+k)^2\left(F^2-1\right)\right]^2 + \left[QkF\left(F^2-1\right)\right]^2}} \tag{7}$$

Fig. 4 illustrates the relationship between voltage gain and normalized frequency for different Q values by plotting several voltage gains from Eq. (7). It can be found that, the converter can be ensured to operate in the ZVS state when $F > 1$. In addition, a larger Q value will accomplish a wide range of gain control within a narrow frequency conversion interval, which is beneficial to reducing the high-frequency eddy current loss of the transformer. However, too large a Q value will lead to a very small frequency conversion range, resulting in a poorly robust system.

C. TOLERANCE ANALYSIS OF THE RESONANT TANK

Since device tolerances are unavoidable in manufacturing process, resonant tank parameters are different from each other. Consequently, Z_{in}, G, and Z_r are different from module to module. The following analyses consist of two parts, which consider the effect of device tolerance on the input impedance and voltage gain of the resonant tank, respectively. The tolerances are expressed as follows:

$$\begin{cases} \Delta i = \left|\dfrac{i_{r\Delta} - i_r}{i_r}\right| \\ \Delta_L = \left|\dfrac{L_{r\Delta} - L_r}{L_r}\right| \\ \Delta_C = \left|\dfrac{C_{r\Delta} - C_r}{C_r}\right| \end{cases} \tag{8}$$

where Δi, Δ_L, and Δ_C are the resonant current, inductance and capacitance tolerances, respectively. $i_{r\Delta}$, $L_{r\Delta}$, and $C_{r\Delta}$ are the module parameters affected by the tolerances. Further, tolerances of the input impedance are as follows:

$$|Z_{in+\Delta L} - Z_{in}| = FZ_{in}\Delta_L \tag{9}$$

$$|Z_{in+\Delta C} - Z_{in}| = \frac{Z_{in}\Delta_C}{F(\Delta_C + 1)} \tag{10}$$

The resonant current mismatch caused by the difference in input impedance is as follows (11) and (12). Where $Z_{in+\Delta L}$ is the input impedance affected by the inductance tolerances, and $Z_{in+\Delta C}$ is the input impedance affected by the capacitance tolerances. Based on R_e and Q, different combinations of L_r and C_r can be determined, and the combination is bound by the same resonant frequency f_r. Therefore, the resonant current mismatch for a fixed device tolerance will be different when Q is chosen at different values, which are described by (11) and (12).

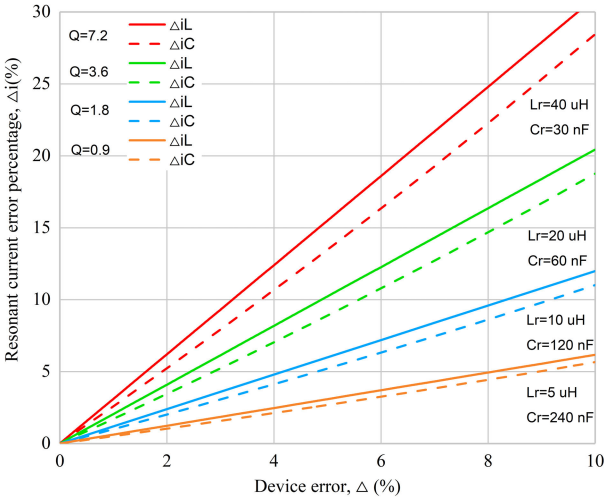

FIGURE 5. Relationship between device tolerance and resonant current mismatch ($F = 1.1$, $R_e = 5\ \Omega$, and $k = 6$).

$$\Delta i_L = \left|\frac{Z_{in+\Delta L} - Z_{in}}{Z_{in+\Delta L}}\right| = \frac{FZ_r\Delta_L}{\left(1 - \dfrac{1}{F^2}\right)Z_r + Z_{out} + FZ_r\Delta_L} \tag{11}$$

$$\begin{aligned} \Delta i_C &= \left|\frac{Z_{in+\Delta C} - Z_{in}}{Z_{in+\Delta C}}\right| \\ &= \frac{Z_r\Delta_C/(F + F\Delta_C)}{\left(1 - \dfrac{1}{F^2}\right)Z_r + Z_{out} + Z_r\Delta_C/(F + F\Delta_C)} \end{aligned} \tag{12}$$

Fig. 5 depicts the relationship between device tolerances and resonant current mismatch with different Q, where the solid and dashed lines, represent the current mismatch brought on by inductance tolerance and capacitance tolerance ($F = 1.1$,$R_e = 5\Omega$, and $k = 6$). The imbalance of resonant current among each module is caused by both inductance and capacitance tolerance, and the current mismatch caused by inductance tolerances is more serious. In addition, the design errors are more likely to occur in resonant tanks with higher Q values. For instance, when $Q = 7.2$, an inductor inaccuracy of 10% results in a resonant current mismatch of more than 30%. The severity of the situation will worsen as the Q number rises. In fact, the length of the core air gap is difficult to precisely control during processing, and the permeability is easily affected by the operating temperature [10]. Therefore, the manufacturing accuracy of inductors can usually only be controlled within ±5%, while the manufacturing accuracy of capacitors can be controlled within ±1%.

In order to investigate the effect of inductance tolerance on the resonant tank characteristics, only the inductance error is set here, three sets of parameters are given: $L_{r1} = 1.05\ L_{r2}$, $L_{r3} = 0.95\ L_{r2}$, and $\Delta_L = 5\%$. This tolerance is typical

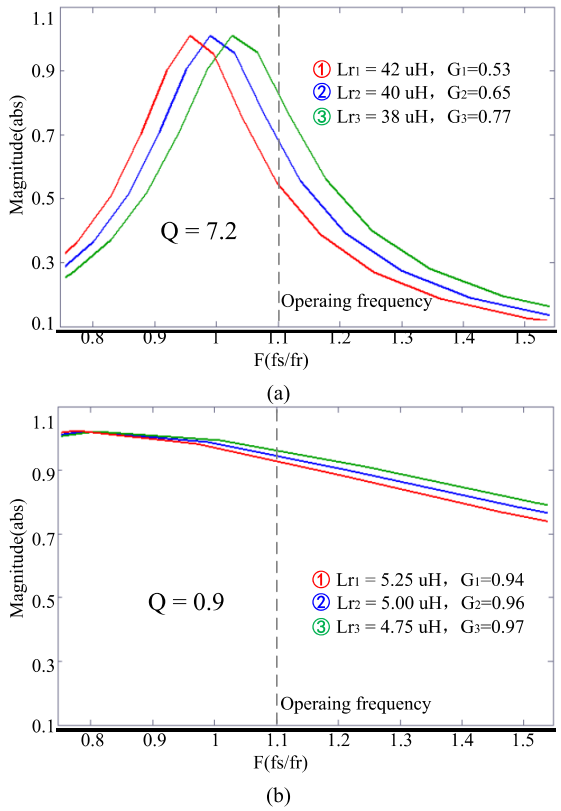

FIGURE 6. Relationship between Δ_L and G ($R_e = 5\ \Omega$, and $k = 6$).

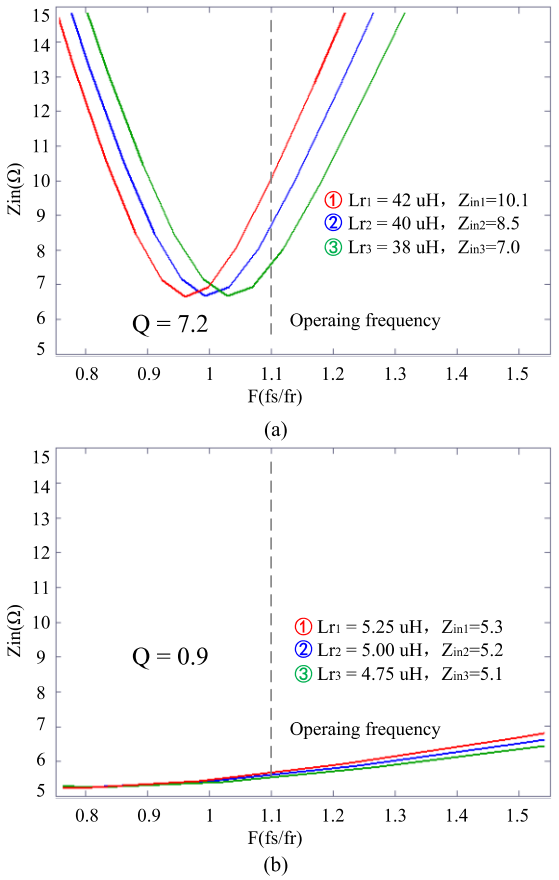

FIGURE 7. Relationship between Δ_L and Z_{in} ($R_e = 5\ \Omega$, and $k = 6$).

TABLE 1. Impact of characteristic impedance on gain.

Q	G_1	G_2	G_3	$\Delta G=(G_3-G_1)/G_2$
7.2	0.53	0.65	0.77	36.9%
0.9	0.94	0.96	0.97	3.1%

TABLE 2. Impact of characteristic impedance on input impedance.

Q	Z_{in1}	Z_{in2}	Z_{in3}	$\Delta Z_{in}=(Z_{in3}-Z_{in1})/Z_{in2}$
7.2	10.1	8.5	7.0	36.5%
0.9	5.3	5.2	5.1	3.8%

in reality. Fig. 6 and Fig. 7 respectively show the effect of inductance error on the gain and input impedance of the resonant tank. According to Eq. (2), since the inductance error is only 5%, it can be approximated that the Q values of each resonant tank are kept equal.

Fig. 6(a) shows that the voltage gain of each module is significantly different when the converter operates near the resonant frequency, with a maximum mismatch of 36.9% ($Q = 7.2$). On the contrary, the voltage gain mismatch is only 3.1% ($Q = 0.9$) in Fig. 6(b), illustrating that the voltage gain is more susceptible to inductance tolerance with larger the Q value of the resonant tank. Similarly, the input impedance mismatch among modules reaches 36.5% for $Q = 7.2$ and only 3.8% for $Q = 0.9$, comparing Fig. 7(a) and Fig. 7(b).

Corresponding data are listed in Table 1 and Table 2. As mentioned above, the error among resonant inductors will cause the voltage gain of resonant tanks and input impedance to be inconsistent, which is the reason for the current mismatch and voltage mismatch in each module. When the converter operates near the resonant frequency, the larger the Q of the resonant tank, the more sensitive it is to the inductors error. Smaller resonant inductor errors will cause greater differences in the voltage gain of resonant tanks. When Q is small, the amplitude and phase of the resonant tank are less affected by the inductance error. Therefore, in order to obtain the input impedance and output voltage sharing results required for the safe operation of the proposed converter, the Q value of the resonant tank needs to be reduced in the design.

D. Y-CONNECTION OR N-CONNECTION

As shown in Fig. 1, the neutral point of the three transformers is connected to the negative terminal of the input in the proposed IPOS converter, called the N-connection in this paper. Another alternative option in parallel interleaved converters is to floating the neutral point of the transformer, called the

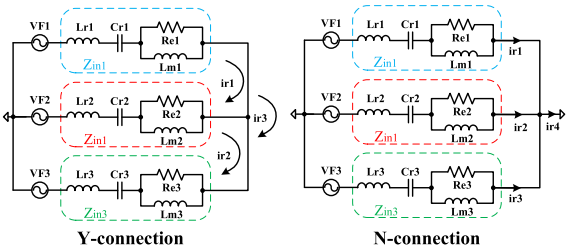

FIGURE 8. Resonant tank with different connection methods.

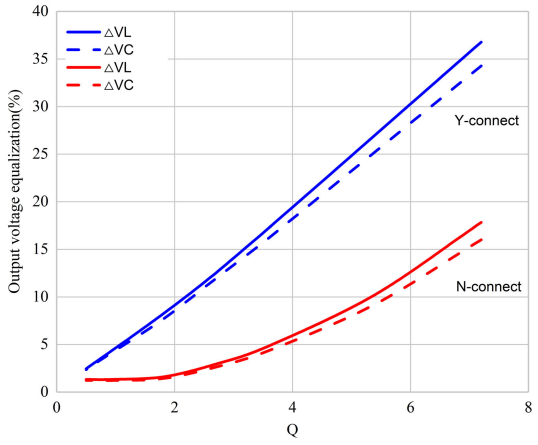

FIGURE 9. Relationship between voltage mismatch and Q.

Y-connection [7]. The reasons for abandoning Y-connection show as follows:

$$\begin{cases} L_r = L_{r1} + L_{r2} \approx 2L_{r1} \\ C_r = \dfrac{C_{r1}C_{r2}}{C_{r1}+C_{r2}} \approx \dfrac{1}{2}C_{r1} \end{cases} \tag{13}$$

$$i_{r1} + i_{r2} + i_{r3} = i_{r4} \tag{14}$$

Fig. 8 shows an equivalent model of the circuit for these two connections. When using a Y-connection, if output equivalent loads are balanced, resonant currents will also be balanced with each other. However, when the output equivalent loads are unbalanced, the sum of the three-phase current vector of the Y-connection is forced to zero according to Kirchhoff's current theorem. Therefore, the current amplitude of the phase cannot be balanced which causes the current of each phase must travel through the two resonant tanks. As the result, the equivalent resonant inductance is doubled, the resonant capacitance is reduced by half, and Q is doubled, as described in (13) and (14). In contrast, the N-connection will provide an additional current path, the unbalanced current of each phase will only return into the ground, such as $i4$, because it is a zero-impedance path [6], which keeps the Q value fixed.

Fig. 9 shows the relationship between output voltage mismatch and different Q values, when the devices exist tolerance ($F = 1.1, R_e = 5\ \Omega$, and $k = 6$). ΔV_L and ΔV_C, represent the voltage mismatch caused by the inductor' and capacitor' tolerances ($\Delta_L = 5\%$, $\Delta_C = 5\%$), respectively. The output

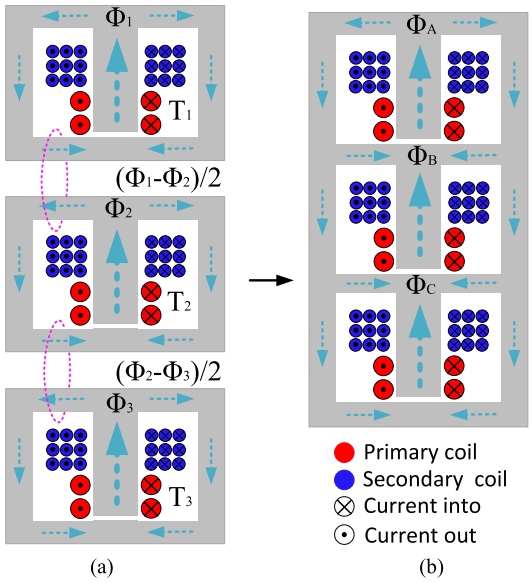

FIGURE 10. Arrangement of transformers. (a) Independent transformers. (b) Magnetic integrated transformer.

voltage mismatch is shown as follows (15):

$$\Delta V = \frac{|V_{j\max} - V_{j\min}|}{(V_1 + V_2 + V_3)/3} \tag{15}$$

Regardless of whether the device tolerance exist in the inductor or the capacitor, the output voltage mismatch is much lower with the N-connection than that of a Y-connection. Consequently, N-connection is utilized in the proposed design.

IV. INTEGRATION OF MAGNETICS WITH FLUX CANCELLATION

A. MAGNETIC INTEGRATION METHOD

IPOS converters usually consist of several DC-DC modules, each of them requiring a separate transformer. It is possible to achieve higher power densities in LLC resonant converters through magnetic integration. Their applications in high-voltage and high-power scenarios have attracted researchers' interest [15], [24]. The model of transformer is set up according to Fig. 10(a). The fluxes flowing at the top and bottom of T_2 will interact with those of T_1 and T_3. Due to the interleaved operation of the three modules, the resonant currents on the primary side exist 120° phase difference, and the flux fluctuation in the core likewise follows this pattern. The flux circled by the pink dashed line, is the opposite, as shown in Fig. 10(a). In other words, the bottom of T_1 and the top of T_3 can be removed. The fact that T_1, T_2, and T_3 combine to produce a common component and a closed magnetic circuit, rendering possible the magnetically integrated method presented in Fig. 10(b).

B. MAGNETIC CIRCUIT MODEL

Two assumptions were performed to maintain acceptable accuracy and to simplified the reluctance model. ① Compared

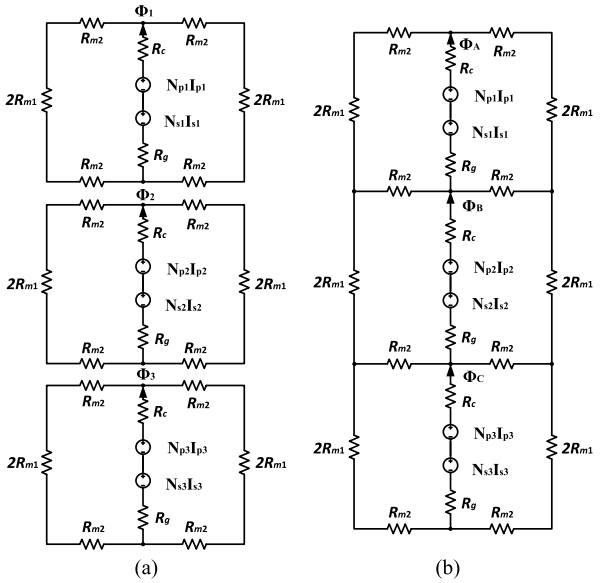

FIGURE 11. Reluctance model of transformer arrays. (a) Independent transformers. (b) Magnetic integrated transformer.

to the air, the core has a substantially higher magnetic permeability. ② Since the leakage flux in the air is negligible, the effect of edge at the air gap also can be ignored. The fluxes of the three independent transformers are derived from Kirchhoff's voltage law and the magnetic circuit law, following (16).

$$\begin{cases} \Phi_i = F_i/\Re \\ \Re = R_{m1} + R_{m2} + R_c + R_g \\ F_i = N_{pi} i_{pi} + N_{si} i_{si} \end{cases} \tag{16}$$

The flux of the magnetic integration is shown as follows (17).

$$\begin{cases} \Phi_B = \dfrac{F_2\Re + (F_1 + F_3)R_{m2}/2}{\Re^2 - R_{m2}^2/2} \\ \Phi_A = \dfrac{F_1}{\Re} + \dfrac{\Phi_B R_{m2}}{2\Re} \\ \Phi_C = \dfrac{F_3}{\Re} + \dfrac{\Phi_B R_{m2}}{2\Re} \end{cases} \tag{17}$$

where R_c is the reluctance of the middle leg of the core, R_g is the reluctance of the air gap, R_{m1} is the reluctance of the outer legs, and R_{m2} is the reluctance of the top and bottom materials, as shown in Fig. 11.

Since the permeability of the air gap is much smaller than the permeability of the core, as result $R_g \gg R_{m2}$. Φ_B is approximated as (18).

$$\Phi_B \approx \frac{F_2}{\Re} + \frac{(F_1 + F_3)R_{m2}}{2\Re^2} \tag{18}$$

Ideally, the resonant currents are balanced and interleaved in phase by 120°, so $F_1 + F_2 + F_3 = 0$, $|\Phi_B| \gg |\Phi_2|$. The top and bottom of the cores will be used less than that of the independent core in the proposed magnetic integration structure. By utilizing the flux cancellation of the adjacent core and setting the magnetic circuit, it is possible to reduce the size and weight of the magnetic device.

TABLE 3. Prototype details.

Parameter	Value
Input voltage V_i	40 V-50 V
Output voltage V_o	4.8 kV
Load R_L	20 kΩ/1.15 kW
Resonant inductor L_{r1}-L_{r3}	8 μH
Resonant capacitor C_{r1}-C_{r3}	400 nF
Characteristic impedance Z_r	4.5 Ω
MOSFET Q_1-Q_6	IRF250P225
Rectifier diode D_1-D_6	ESJW03
Output capacitor C_1-C_6	22 nF
Digital controller	STM32F334
Switching frequency	85 kHz-200 kHz

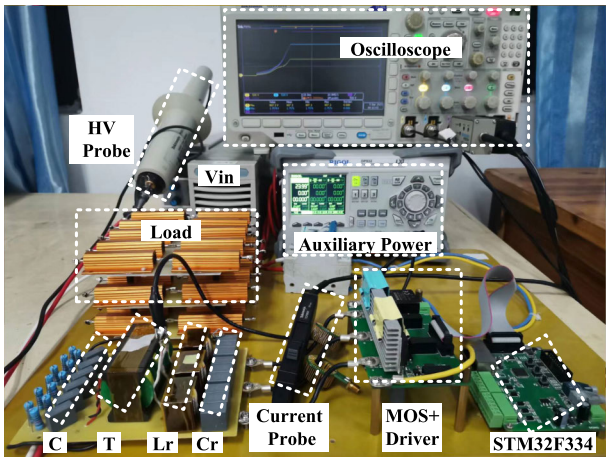

FIGURE 12. Experimental prototype of proposed converter.

V. EXPERIMENTAL RESULTS

A. PROTOTYPE

An experimental prototype is built following the specifications in Table 3 to test the proposed topology's ability to share the output voltage. The prototype, operates as a boost converter, that can take variable inputs and control the system's voltage at a maximum output of 4.8 kV/1.15 kW using the PFM method. Where, the MOSFET is IRF250P225, values of the turn-on resistance and the gate charge are 22 mΩ and 64 nC, respectively. In order to avoid the effect of diode junction capacitance on the circuit under high-voltage and high-frequency operation [24], a fast recovery diode ESJW03, with low junction capacitance (7 pF) and high reverse breakdown voltage (3 kV) is used in the voltage-doubler rectifier to reduce the reactive power in the resonant circuit and to avoid avalanche breakdown of the rectifier under high-voltage conditions.

The output capacitors are all MKP film capacitors with a withstand voltage of 1.6 kV. The test equipment mainly contains a high-voltage probe (P6015A), 3 current probes

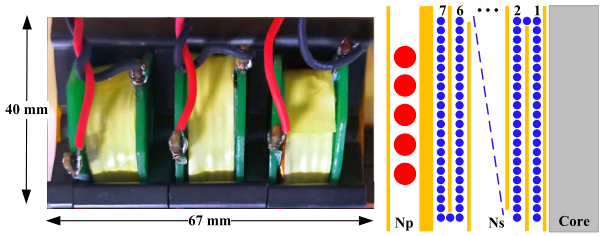

FIGURE 13. Schematic of magnetic integrated transformer.

TABLE 4. Integrated transformer details.

Parameter	Value
Primary number of turns N_{p1}-N_{p3}	5
Transformers ratio n	42
Magnetic inductance L_m	45 μH
Primary leakage inductance L_{kp}	0.5 μH
Primary coil resistance R_{cp}	8 mΩ
Secondary coil resistance R_{cs}	4.2 Ω
Cross section area A_e	201 mm^2
Core Volume V_e	35250 mm^3

(TCP2020), an input DC power supply (ZXD2400), an auxiliary power supply (DP832), an oscilloscope (MDO3014) and resistive load.

In high-voltage applications, the electrical safety of the prototype should be considered and the PCB cannot be compact (length: 200 mm, width: 100 mm, height: 45 mm). Furthermore, as illustrated in Fig. 12, the primary side inverter is split into two sections, the primary side and the high-frequency transformer, which renders the measurements easier.

B. SIMULATION AND IMPLEMENTATION OF TRANSFORMERS

The integrated transformer is constructed following the specification in Table 4. The commercial PQI4026 core is selected as the transformer and power ferrites PC95 (TDK) as the core material. The wide temperature characteristics and low eddy current losses make them suitable for high switching frequencies. Reduce the magnetic flux density of the core and the total number of windings turns to lower transformer losses. The minimum number of turns on the primary side is as follows (19).

$$N_p = \frac{V_i}{4A_e \Delta B f_s} \tag{19}$$

where N_p is calculated based on the maximum input voltage to avoid saturation of the core, $N_p = 4.5$ is calculated and finally $N_p = 5$ is obtained ($V_i = 50$ V, $\Delta B = 0.15$ T, and $f_s = 90$ kHz). According to the maximum voltage gain of the prototype, $n = 42$ is suitable. Because LLC resonant converters achieve an excellent soft switching performance when operating near the resonant frequency [7].

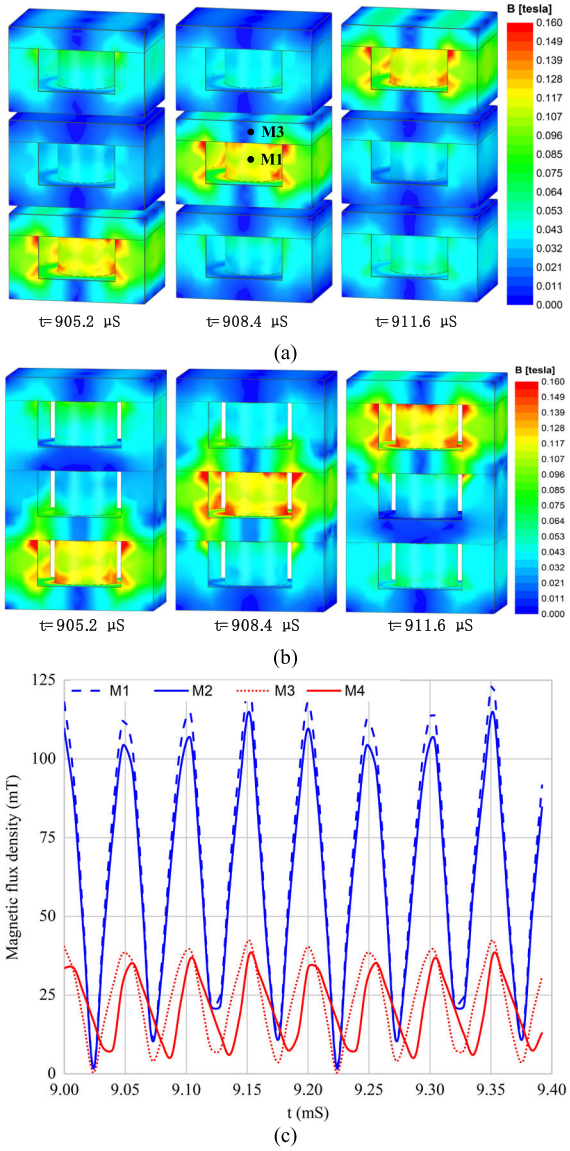

FIGURE 14. Magnetic flux density distribution of transformers. (a) Independent transformers. (b) Magnetic integrated transformer. (c) Simulation results of magnetic flux density at different positions.

The integrated transformer as shown in Fig. 13, which needs only three PQ cores and one I-bottom. Two I-bottom sections are saved, compared to using three group cores. The volume of the designed integrated transformer is 35250 mm^3, which only contains 79.7% of the volume of independent transformers, where the volume of a single PQ core is 10250 mm^3, and the volume of a single I-core is 4500 mm^3.

Using insulated wire with a diameter of 0.2 mm to make the secondary and litz wire with a diameter of 0.1 mm×400 to wind the primary. The secondary windings are close to the bobbin and follow the Z-winding method, with 30 turns per layer for a total of 7 layers. For a more uniform wire arrangement, the primary is wound in 1 layer with litz wire and positioned in the outermost layer. Therefore, the leakage inductance and the parasitic capacitance are more lower.

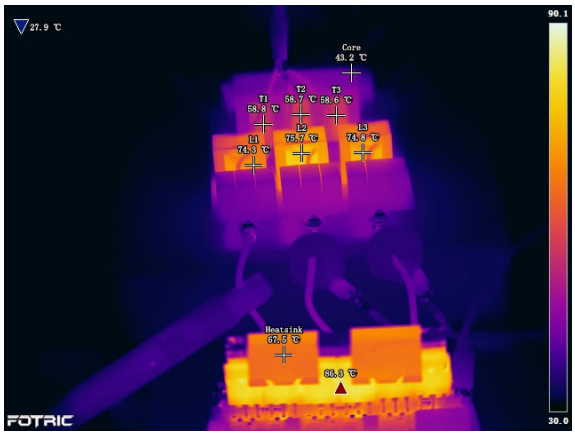

FIGURE 15. Thermal distribution of the prototype at full load.

At last, an LCR meter operates at 100 kHz. The magnetic inductance is measured to be $L_m = 45\ \mu$H, the leakage inductance to be $L_{kp} = 0.5\ \mu$H, and the primary and secondary resistances to be $R_{cp} = 8$ mΩ and $R_{cs} = 4.2\ \Omega$, respectively.

In order to prevent high-voltage arcing between the windings, in this work, polyimide tape with a breakdown field strength of 80 kV/mm is employed as the insulating material between the primary and secondary.

Achieving sufficient electrical insulation distance for PCB windings is a challenge, which is the reason why it does not allow the design of a transformer with a high step-up turn ratio. More crucially, since the area between adjacent PCB windings is much larger than the area between windings made of wires, there is a high secondary parasitic capacitance.

Figs. 14(a) and (b) show the 3D finite element simulation of the independent transformer and the integrated magnetic at different moments, respectively. As the interleaved and balanced operation of the resonant currents is maintained, the flux in each center leg increases sequentially. The proposed magnetic integration's flux distribution is more uniform, leading to a higher core utilization. Furthermore, the leakage flux is confined within the core instead of air.

Therefore, the magnetic flux density at the junction of PQ and I is very low. The result in Fig. 14(c) demonstrates that the magnetic integration possess a lower core loss. Because it has a lower flux density at the corresponding marked locations, which is consistent with the analysis in Part IV.

Fig. 15 shows the thermal distribution of the proposed converter under full load. As most HVPS operate in pulse mode, and the time for outputting high voltage is usually a few seconds rather than the long-term operation [1], [2], [3], [4]. The prototype operates continuously for 30 minutes in a non-closed environment at 27.9 °C and achieved thermal equilibrium, which is enough to show the heat distribution of the prototype. The case temperature of the MOSFET is 86.3 °C, which is acceptable because it is well below the maximum allowable junction temperature of 175 °C. The flux and winding are distributed in the center leg of the transformer, so the core loss and copper loss cause higher thermal

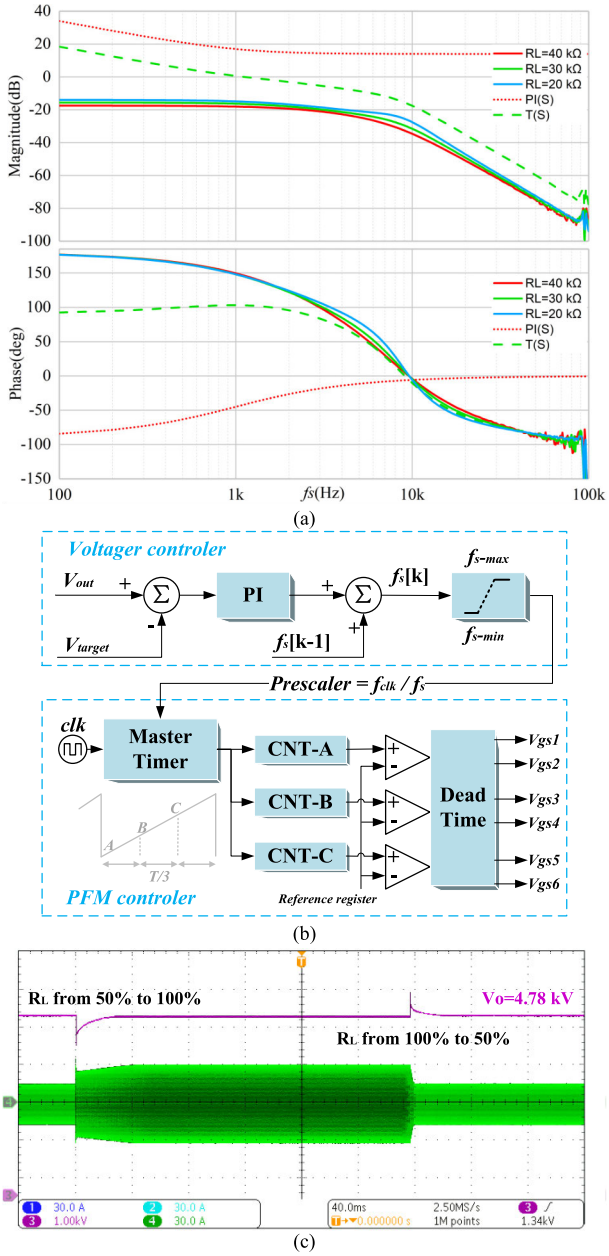

FIGURE 16. Control strategy and dynamic response. (a) Bode diagram. (b) PFM controller and three phase interleaved PWM generator. (c) Dynamic response test during load step.

generated here than in the surrounding area. The temperature at the window of $T_1 - T_3$ is almost equally bright in the thermal figure, illustrating that the magnetic integrated transformer converter is in balanced operation. The temperature on the side of the transformer is lower than the I core in the middle, and there are no hot spots at the junction of the PQ core and I core. These results are consistent with the magnetic flux distribution in Fig. 14 (b).

C. CONTROL STRATEGY OF THE PROPOSED TOPOLOGY

The three-phase interleaved LLC converter has so many variables that it is complicated to solve the generalized space

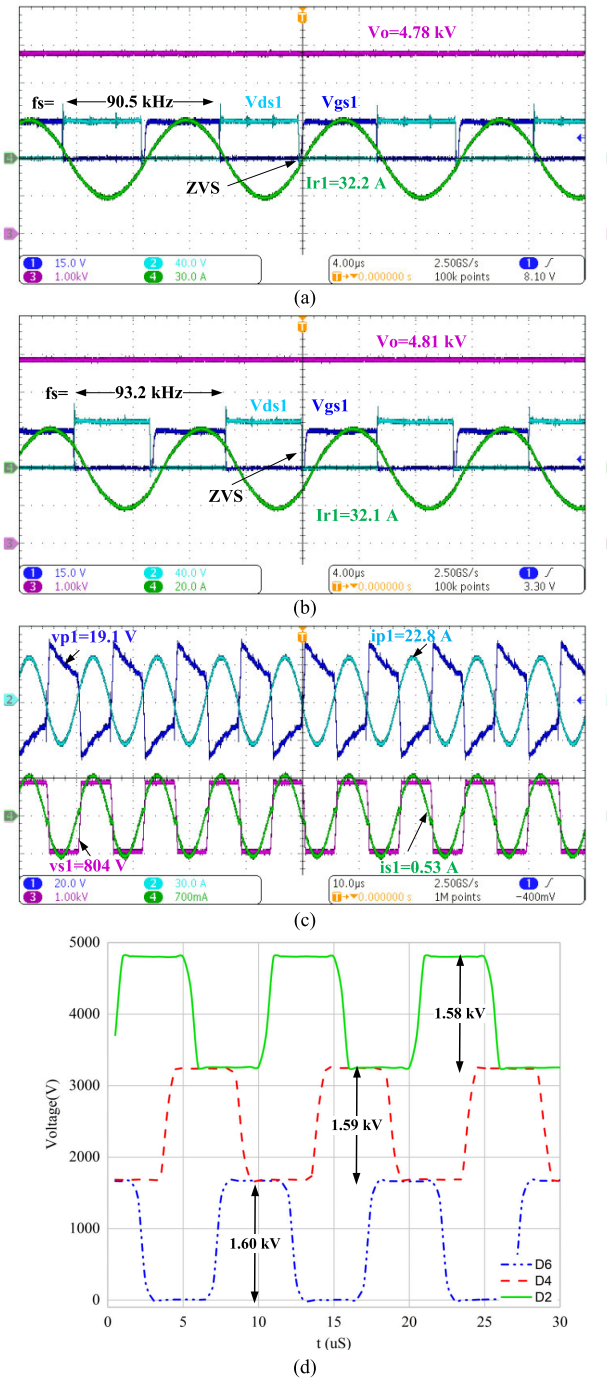

FIGURE 17. Full load operation. (a) $V_i = 40$ V. (b) $V_i = 50$ V. (c) Transformer test. (d) The voltage waveform between the cathode terminal and the output negative of the rectifier diode.

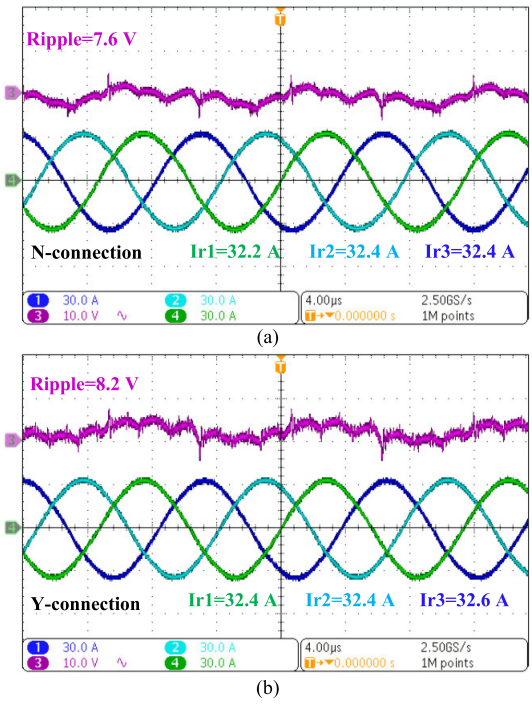

FIGURE 18. Waveforms of resonant current and voltage ripple in differences connection. ($V_i = 40$ V, $Q = 1.9$, and $R_L = 20$ kΩ). (a) N-connection. (b) Y-connection.

state equation directly [26]. Therefore, the bode diagram of switching frequency to output voltage is obtained using simulation, as shown in Fig. 16(a), in an open loop state. The proposed converter' magnitude of bode plot shows LC filter-like characteristics from full load to half load, and the difference is very small among them. It is worth noting that the phase decreases from 180° instead of 0° at low frequencies, so the voltage loop needs to be designed as positive feedback. Combining these features, the PI controller is used for loop compensation in the proposed converter, and the control diagram is shown in Fig. 16(b).

Using the PFM method to regulate the output voltage, which is performed as for other resonant converters by changing the switching frequency. The compensated switching frequency is used to update the counting period of the master timer and cause the three slave timers to generate three pairs of drive signals interleaved at 120° in phase for controlling the converter. The ADC sampling frequency is 1MHz, as a result the discrete period of the controller is 1 μs. The discrete expression of the PI controller using bilinear transformation is as follows ($k_p = 5$, $k_i = 31400$, $T_d = 1$ μs):

$$\frac{\Delta f(z)}{\Delta V(z)} = \frac{(2k_p + k_i T_d) - (2k_p - k_i T_d) z^{-1}}{2(1 - z^{-1})} \tag{20}$$

After using the PI compensation, the system has a crossing frequency of 1 kHz and a phase margin of 90°. The dynamic response of the converter is tested in Fig. 16(c), and the experiment shows that the system can adapt to a wide range of load fluctuations. However, due to the small output capacitance of the converter, the output voltage will have a transient voltage dip with overshooting spikes during load switching.

D. EXPERIMENTAL WAVEFORM

Fig. 17 shows the operation of the proposed converter at full output. ($V_o = 4.8$ kV and $R_L = 20$ kΩ). Fig. 17(a) shows the test results at $V_i = 40$ V, where V_{gs1} is the driving signal of Q_1, $V_{gs1} = 15$ V, and I_{r1} is the peak resonant current

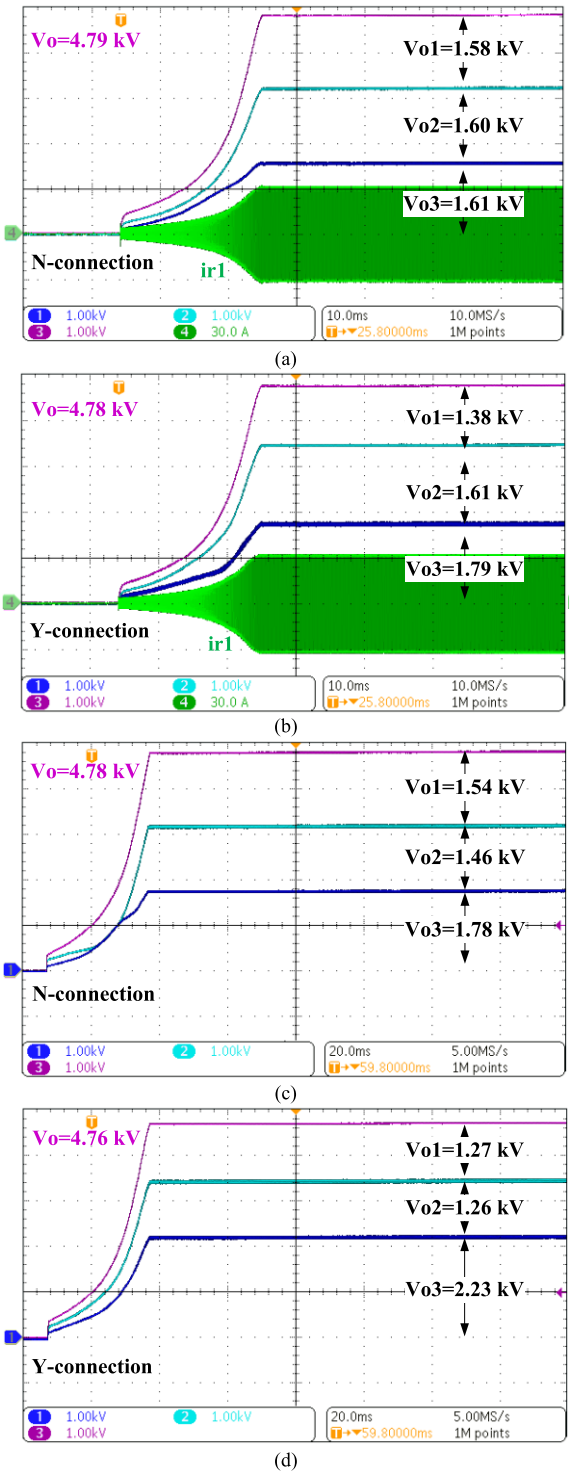

FIGURE 19. Waveform of output voltage. (V_i = 40 V, R_L = 20 kΩ). (a) N-connection, Q= 1.9, Δ_C = 5%. (b) Y-connection, Q = 1.9, Δ_C = 5%. (c) N-connection, Q = 3.7, Δ_C = 5%. (b) Y-connection, Q = 3.7, Δ_C = 5%.

of module 1, with $V_o = 4.78$ kV, $I_{r1} = 32.2$ A, and $f_s = 90.5$ kHz. $V_{ds1} = 0$ V is turned on before Q_1, and ZVS is achieved. Fig. 17(b) shows the test results at $V_i = 50$ V and $f_s = 93.2$ kHz, the output voltage is regulated by increasing the switching frequency. The entire procedure accomplishes ZVS and complies with the design specifications.

To verify the efficiency of the transformer, the input and output waveforms of T_1 were tested, as shown in Fig. 17(c). The RMS values of the primary voltage and current are $v_{p1} = 19.1$ V as well as $i_{p1} = 22.8$ A, respectively, and the input power of the transformer is 435.5 W. The RMS values of the secondary voltage and current are $v_{s1} = 804$ V as well as $i_{s1} = 0.53$ A, respectively, and the input power of the transformer is 426.1 W. Due to the winding conduction losses and the core losses at high frequencies, resulting in the efficiency of the transformer is 97.8%.

Fig. 17(d) shows the peak voltages between the cathode and the negative output terminal of diodes D_2, D_4, and D_6 are 1.58 kV, 1.59 kV, and 1.6 kV, respectively. Only a little difference in the voltage among them and a maximum voltage mismatch of 1.5% when the resonant device tolerance is less than 1%. Contributing to the soft-switching characteristic of the LLC, the voltage of the diode does not have any significant spike, and the output voltage sharing performance of the whole IPOS-LLC converters is excellent.

Fig. 18 shows the output voltage ripple and resonant current waveforms for the proposed converter with different connections. Fig. 18(a) uses the N-connection with resonant currents $I_{r1} = 32.2$ A, $I_{r2} = 32.4$ A, and $I_{r3} = 32.4$ A respectively, the current balance of each phase is excellent. The voltage ripple is 7.6 V with ripple rate of $\Delta_{rpp} = 0.16\%$.

Fig. 18(b) uses the Y-connection with voltage ripple is 8.2 V, and $\Delta_{rpp} = 0.17\%$. Both connection methods reflect a very low output ripple rate at full load, even if the output capacitor is only 3.7 nF. According to the experimental results, the proposed converter shows ultra-low output ripple in high-voltage applications using parallel interleaving technology.

Fig. 19 compares the effects of different Q values and connection methods on the output voltage-sharing performance of converter, when there is a 5% tolerance exists in the resonant device. Comparing Fig. 19(a) and Fig. 19(b), the voltage mismatch with N-connection and Y-connections at $Q = 1.9$ is $\Delta V = 3.1\%$ and $\Delta V = 12.9\%$, respectively ($L_{r1} = 8$ μH, $C_{r2} = 400$ nF, $C_{r1} = 1.05C_{r2}$, and $C_{r3} = 0.95$ C_{r2}). However, when Q increases from 1.9 to 3.7 ($L_{r1} = 16$ μH, $C_{r2} = 200$ nF, $C_{r1} = 1.05$ C_{r2}, and $C_{r3} = 0.95$ C_{r2}), the voltage-sharing performance of the converter becomes more worse, as shown in Fig. 19(c) and Fig. 19 (d). When using N-connection, the voltage mismatch achieves 20%, and the outputs of each submodule are 1.54 kV, 1.46 kV, and 1.78 kV, respectively, as shown in Fig. 19(c). The worst case is shown in Fig. 18(d), where $V_1 = 1.27$ kV, $V_2 = 1.26$ kV, and $V_3 = 2.23$ kV, using Y-connection. The output voltage of module 3 is approximately twice that of module 2, the maximum voltage imbalance among modules exceeds 60%, which affects the safety of the IPOS-LLC in high-voltage applications seriously.

The results show that voltage mismatch among submodules with a lower Q value is significantly reduced at the

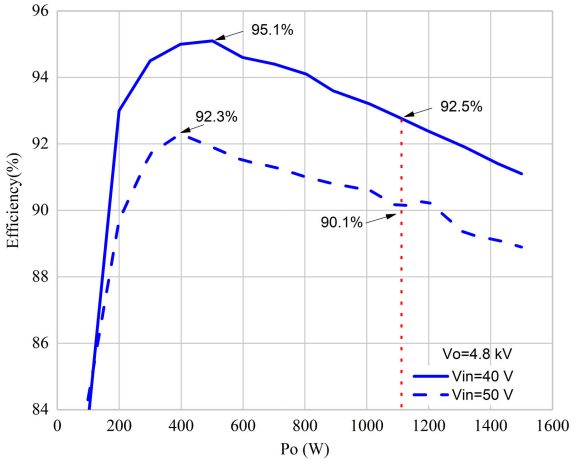

FIGURE 20. Efficiency test at different input voltages.

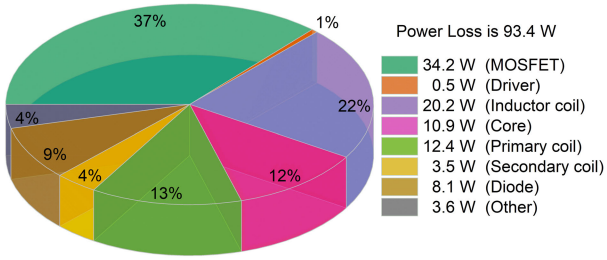

FIGURE 21. Power loss of the prototype under full load.

same percentage of device tolerance. In addition, the use of N-connections contributes to the reduction of voltage mismatch because the voltage mismatch is reduced by a factor of 3 compared to Y-connections.

E. EFFICIENCY AND LOSS ANALYSIS

The efficiency of the proposed converter was tested at $V_i = 40$ V and $V_i = 50$ V, respectively, as shown in Fig. 20, the efficiency is 92.5% at $V_i = 40$ V and $P_o = 1.15$ kW. In addition, the peak efficiency of the converter reaches 95.1% at $V_i = 40$ V and $P_o = 500$ W.

At this point, the input voltage is lowest, and the switching frequency is closest to the resonant frequency. Not only is ZVS achieved in the primary, but the switch also has a lower turn-off current. When $V_i = 50$ V, the efficiency is decreases, to reach the set output voltage, the f_s should be increased, resulting in increased switching losses. Moreover, the switching losses and the AC conduction losses of coil are further increased as the output power increase.

Fig. 21 shows the full load losses of the various sections in the prototype ($V_i = 40$ V), a total of 93.4 W, which are divided into three sections. Firstly, the losses include MOSFET losses and driver. The small area of I_{r1} overlaps V_{ds1} in Fig. 17(a), which clarifies that the crossover losses in the device are small. Therefore, the conduction losses of the MOSFET are mainly considered, as follow (21) and (22).

$$P_{mos} = 22\ \text{m}\Omega \times \left(\frac{32.2\ \text{A}}{2}\right)^2 \times 6 = 34.2\ \text{W} \tag{21}$$

TABLE 5. A comparison between the proposed converter and other IPOS resonant converters is reported in the literature.

Reference	Methods	V_i/V_i	ΔV	C_o	Δ_{rpp}
[24]	2 modules paralleled	100	6%	1.5nF	2%
[1]	3 modules interleaved	100	4.2%	6.7nF	1%
This work	3 modules interleaved	120	3.1%	3.7nF	0.16%

$$P_{driver} = 15\ \text{V} \times 64\ \text{nC} \times 90\ \text{kHz} \times 6 = 0.5\ \text{W} \tag{22}$$

Secondly, losses in magnetic devices, mainly refers to inductors and transformers, can be attributed to core losses and coil losses. According to the Steinmetz formula, the losses in the core are proportional to the volume of the core, the flux density, and the frequency of operation. However, commercial cores loss curves usually be obtained. The designer only needs to find the loss factor for the corresponding operating condition to calculate the losses. Where, the PC95 material has a loss factor of 250 kW/m^3 for operation at 100 kHz and 150 mT. The inductor coil has a resistance of 13 mΩ at 100 kHz, using a PQ2020 core, volume 2790 mm^3. The core loss is as follows (23).

$$\begin{cases} P_{L\_core} = 2790\ \text{mm}^3 \times 250\ \text{kW/m}^3 \times 3 = 2.1\ \text{W} \\ P_{T\_core} = 35250\ \text{mm}^3 \times 250\ \text{kW/m}^3 = 8.8\ \text{W} \end{cases} \tag{23}$$

$$\begin{cases} P_{L\_coil} = 13\ \text{m}\Omega \times \left(\frac{32.2\ \text{A}}{\sqrt{2}}\right)^2 \times 3 = 20.2\ \text{W} \\ P_{sec\_coil} = 4.2\ \Omega \times (0.53\ \text{A})^2 \times 3 = 3.5\ \text{W} \\ P_{pri\_coil} = 8\ \text{m}\Omega \times \left(\frac{32.2\ \text{A}}{\sqrt{2}}\right)^2 \times 3 = 12.4\ \text{W} \end{cases} \tag{24}$$

$$P_{diode} = 3.6\ \text{V} \times \left(\frac{0.75\ \text{A}}{2}\right) \times 6 = 8.1\ \text{W} \tag{25}$$

The coil loss is shown in Eq. (24). The sum of losses in the resonant inductor is 22.3 W, the loss of the transformer is 24.7 W.

Finally, the losses of the rectifier are mainly the conduction losses of the diode, where the high voltage diode ESJW03 has a forward turn-on voltage of 3.6 V and losses of 8.1 W for all diodes. In addition, due to the losses of parasitic parameters is difficult to calculate, such as losses in PCB lines and connection terminals, which are referred to as other losses.

Compared to previously reported experimental results of IPOS converters described in [1] and [24], the proposed converter has the lowest voltage ripple rate, which is attributed to its effective voltage-sharing performance among modules. The output ripple is large because Mao S is simply connected in parallel in literature [24] and does not investigate the two resonant converter modules by the interleaved situation method. Furthermore, it is noteworthy that only this research has examined and offered a workable design strategy to address the output voltage mismatch problem of interleaved parallel IPOS resonant converters caused by device tolerances. This helps to further improve the IPOS-LLC for

high-voltage applications. The Table 5 summarizes the above comparison.

VI. CONCLUSION

For the application of high voltage gain with low ripple, an IPOS-LLC resonant converter considering output voltage sharing is proposed. Through theoretical analysis, the design suggests that a smaller Q value with an N-connection should be selected for the IPOS-LLC design. Excellent output voltage sharing is achieved even with tolerance on the device. The voltage stress distribution of each rectifier diode in high-voltage applications is optimized to improve the reliability of the circuit. An integrated transformer structure with mutually canceling fluxes is proposed, which is only 79.7% the size of the conventional solution. The structure has been verified on a prototype with 90 kHz, 40 V/4.8 kV, and 1.15 kW. The results show that the converter designed has excellent output voltage sharing capability with 3.1% and output voltage mismatch, 0.16% voltage ripple rate, and only 3.7 nF output capacitance. Future work will be focused on further increasing the number of interleaved modules and efficiency to drive high-power magnetrons.

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