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RESEARCH ARTICLE

A Family of High Step-Up Soft-Switching Integrated Sepic Converter With Y-Source Coupled Inductor

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ABSTRACT This paper proposes a single-switch integrated Sepic converter with a Y-source coupled inductor that can be applied to the output of photovoltaic (PV) arrays. The three-winding coupled inductor has higher voltage regulation efficiency, and the three-port tap of the y-source is easier to integrate with other structures to form a composite power cell. The proposed topology gives a new type of Y-source voltage multiplication cell. While ensuring the continuous input current, it can flexibly adjust the voltage gain, increase the power capacity, and reduce the voltage stress of the switch. The diode-capacitor branch in the integrated topology is used as a clamp to suppress the voltage shock while using the absorbed leakage energy to achieve soft-switching characteristics, mitigate diode reverse recovery, and improve the efficiency of the converter. A detailed theoretical analysis of the converter is carried out, and the general extension of the topology and the extension of the converter family are given. Finally, a 150 W prototype was built to verify that the converter can achieve high gain under high efficiency of 94.3%.

INDEX TERMS Coupled inductor, high step-up, sepic, soft-switching, Y-source.

I. INTRODUCTION

The yearly increase in global electricity consumption necessitates the further development and utilization of renewable energy sources [1], especially in the area of PV power generation. A high-quality PV system must be equipped with efficient DC-DC converters [2] to complete the voltage boost from the input of the PV array to the inverter before grid connection to meet the needs of high-voltage transmission and distribution. The conventional converter structure [3] has a limited boost effect and low efficiency, much less than the grids need.

From the perspective of high gain and high power density of the converter, on the one hand, the superposition and combination of topological structures can be used, on the other, the introduction of voltage doubling technology and structural expansion are required. The converter can consist of multiple switches, capacitors, and inductors, or a combination of switched-capacitor and switched-inductor units [4], [5], which helps to improve the boost capability. It is often designed as a symmetrical structure to reduce the difficulty of control, while the existence of multiple switching tubes and semiconductor structures, the voltage stress of the device is hard to drop, and the power consumption is relatively high. In [6], the quadric Sepic converter is proposed, the input side current is continuous while the coupling inductor is introduced to improve the voltage gain, and a passive clamping branch is added to solve the parasitic problem. However, there is hard switching, so current ripple and voltage spikes in the diode are unavoidable, which add to the losses in the component and lead to overall performance degradation. Converters [7], [8], [9], [10] adopt an integrated structure, but those all lack soft-switching design. The sepic-integrated boost converter [8] shares the front-end switching tube and input inductor. Still, the boost effect is limited, and using an isolated sepic converter complicates the topology. Integrated

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Buck and Modified Push-Pull DC-DC Converter [9] also combines non-isolated topology with isolated topology, but the converter is large in size and low in efficiency. Connect the Buck-Boost part at the back end of the Sepic topology for integration, increase the gain to achieve functional complementarity, and realize continuous input current but large ripple [10]. For high step-up integrated DC-DC converters, the pairwise combinations of various standard converters are analyzed in detail, and an alternative method is given [11].

Considering the high efficiency and stability of the converter, it is necessary to reduce the control difficulty and improve the efficiency of each device. The integrated Buck-Boost quadric type in [12] solves the hard switching problem of the diode, it needs to add a synchronous control switch. The use of interleaved parallel connection can effectively reduce the number of devices when increasing the power capacity, control the volume of the equipment, and realize zero-voltage-switching (ZVS) through the interleaved structure, which must use dual-switch control while increasing the difficulty of designing [13]. The Sepic converter [14] magnetically integrates the inductance in the original structure to reduce the current ripple. Yet simple magnetic integration cannot improve the voltage gain and requires the addition of voltage multiplier units [15], [16]. Although the integrated Boost-SEPIC Converter [17] utilizes the improved topology and dual coupling inductors to achieve zero-ripple input current, the maximum efficiency is only about 94%. Using the back-end inductor as a coupled inductor, a high-gain non-isolated DC-DC converter is proposed. For the existence of parasitic capacitance and parasitic inductance, only an independent capacitor is added to alleviate it, and soft-switching cannot be realized [18], an integrated Buck-boost-Cuk converter [19] realizes zero-current-switching (ZCS). Continue to improve the topology to achieve ZVS, but the proposed high-frequency converter needs to work in discontinuous conduction mode (DCM), and the stability of the device is poor [20]. Modified ZVT integrated SEPIC-Boost converter [21] realizes both ZCS and ZVS but requires the cooperation of dual switches and three-winding coupled inductors. The number of components reaches 20, and the equipment is large, making it hard to control losses.

Structural improvement through the cooperation of each component can improve the voltage gain, as that can also realize the soft-switching function and gradually form the impedance network research. The classical DC-DC converters based on an impedance network are summarized, where the coupled inductor impedance network is more widely used and more reliable [22]. The introduction of coupled inductors can effectively and flexibly increase the gain without increasing the number of components. Selecting the three-winding coupled inductor has higher voltage regulation efficiency than a single ordinary winding coupled inductor and a smaller structural volume than the dual coupled inductor. Three-winding types such as Z source [23], Δ source [24], [25], [26], and Y-source [27], [28], [29]. Among them, the three-port tap of the y-source network is easier to integrate with other voltage multiplier structures to form a composite power cell, and the winding method is simpler. For the Y-shaped network, the working principle of its traditional structure is analyzed in detail and applied to the conventional converter [28]. The specific coupled inductor transformer model and winding method are given in [29], yet, the structure of directly adding coupled inductors does not consider leakage inductance and the like. Subsequently, the concept of the quasi-Y source was developed, and additional diodes and capacitive elements [30], [31], [32], [33] were added to the impedance network to absorb leakage inductance and eliminate voltage spikes. Apply the quasi-Y source network to conventional converters, such as Sepic converter [34] and Buck-Boost converter [35], change the Y-shaped three-port position to match the diode-capacitor branch [36], or add a snubber diode [37]. At the same time, an active clamp can be introduced to reduce the voltage stress of the switch [38]. However, additional components in the network only serve to suppress spikes and improve device characteristics, not to increase the output voltage. To further increase the gain, a four-winding impedance network is used, which makes the design of the coupled inductor more difficult, the restrictive conditions of the turn ratio relationship are strict, and the adjustment flexibility is poor [39].

This paper is based on the Sepic transformer. Firstly, the continuity of its topological input current is preserved, and a Y source impedance network of a three-winding coupled inductor is introduced at the capacitor-inductor-diode (C-L-D) of the structure. Then other traditional topologies are connected in parallel at the input end for merging and transformation to achieve gain superposition and increase power density. The Buck-Boost-Sepic integrated structure can not only ensure that the input current continuously reduces the current ripple, but also realize the gain superposition of different topologies, improve the power density of the converter, and cooperate with the y-source to be flexibly applicable to different step-up and step-down occasions. Finally, the original diode-capacitor branch is cleverly used to further multiply the voltage using leakage inductance, while acting as a clamp to achieve a soft-switching design and alleviate the reverse recovery problem of the diode. This converter can select the appropriate clamping node according to diverse application requirements, the voltage stress of the device is low, and it has the characteristics of high gain and high efficiency.

The structure of this paper is as follows: Section II introduces the proposed converter topology; Section III analyzes the working principle and performance of the specific topology; Section IV gives the general extension of the proposed converter and the extension of the converter family. The horizontal comparison of converter performance is made; Section V completes the design guidelines; Section VI conducts experiments and verification analysis on the converter; Section VII gives the conclusion.

II. CONVERTER TOPOLOGY PROPOSED

The proposed integrated Buck-Boost-Sepic converter with Y-source coupled inductor (YSCI-BBS) is constructed as shown in Fig. 1(a). The diode-capacitor (D_1-C_1) branch in the Buck-Boost structure can be shared as a passive clamping branch of the switch S to absorb leakage inductance energy. Fig. 1. (b) shows the equivalent circuit of the proposed converter, where the Y-source coupled inductance structure can be composed of leakage inductance L_k, magnetizing inductance L_m, and three windings with turn ratios $n_1 = N_{s1}/N_p$, $n_2 = N_{s2}/N_p$ ideal transformer. The floating ground is used between the input and output terminals so that the circuit is not affected by the performance of the earth and prevents electromagnetic interference caused by the coupling of the common ground impedance circuit. But the disadvantage is that it is susceptible to the influence of parasitic capacitance, which changes the ground potential and increases the induction interference to the analog circuit.

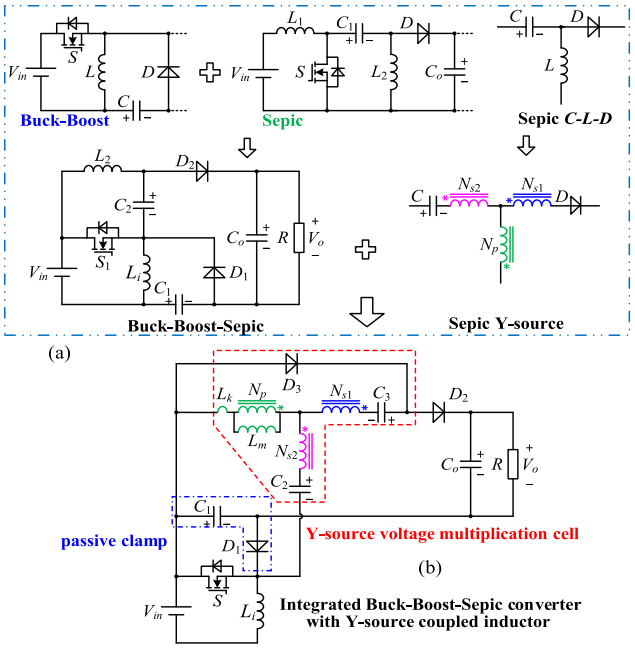

FIGURE 1. Proposal of YSCI-BBS converter. (a) Construction idea, and (b) Equivalent circuit.

III. ANALYSIS OF YSCI-BBS CONVERTER

The YSCI-BBS converter proposed in Fig. 1. is theoretically analyzed and the following assumptions are made: 1) All diodes are ideal devices, i.e., the on-time is zero, the off-resistance is infinite, and the on-state voltage drop is neglected; 2) All capacitors are ideal devices, and capacitors C_1 and C_2 are large enough that their ripple voltage and parasitic effects are negligible. 3) All inductor currents are continuous, i.e., the YSCI-BBS converter operates in continuous conduction mode (CCM).

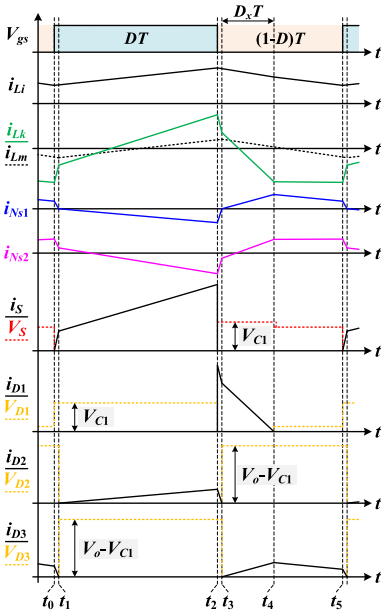

FIGURE 2. Basic waveforms of the proposed converter.

A. OPERATING PRINCIPLE

There are 5 operating modes within one switching period T. The basic waveforms of the converter are shown in Fig. 2. The equivalent circuit of each operating mode is shown in Fig. 3.

Mode I[t_0-t_1]: In this time interval, diode D_3 is turned on, and D_1 and D_2 are turned off. At $t = t_0$, the switch S starts to conduct, the current i_S rises from zero, and the ZCS turn-on can be achieved. The input power V_{in} gives energy to the inductor L_i, and the current i_{Li} rises linearly. At the same time, the primary side N_p of the coupled inductor starts to store energy, the current i_{Lk} starts to rise rapidly, the secondary side currents i_{Ns1} (i_{D3}) and i_{Ns2} both start to drop to zero quickly, and the diode D_3 is turned off at t_1, and the mode ends. In this mode, the current i_{D3} can be expressed as:

$$i_{D3}(t) = i_{D3}(t_0) + \frac{-\frac{1+n_1}{1-n_2}V_{C2} - V_{C3}}{n_1^2 L_k}(t - t_0) \quad (1)$$

Mode II[t_1-t_2]: In this mode, the diodes D_1 and D_3 are turned off, D_2 starts to conduct, and switch S is still in the ON state. On the secondary side N_{s1}, the capacitors C_3, and C_1 are connected in series to release energy to the load through the diode D_2, the current i_{D2} rises linearly from zero, and the diode D_2 realizes the ZCS turn-on. The capacitor C_2 charges the primary side N_p through the switch S, and the current i_{Lm} and i_{Lk} rise linearly. The inductor L_i keeps storing energy, and the current i_{Li} continues to increase linearly. In this mode, the following voltage and circuit equations can be expressed as:

$$\begin{cases} V_{Li} = V_{in} \\ V_{Lm} = \dfrac{V_{C2}}{1 - n_2} \end{cases} \quad (2)$$

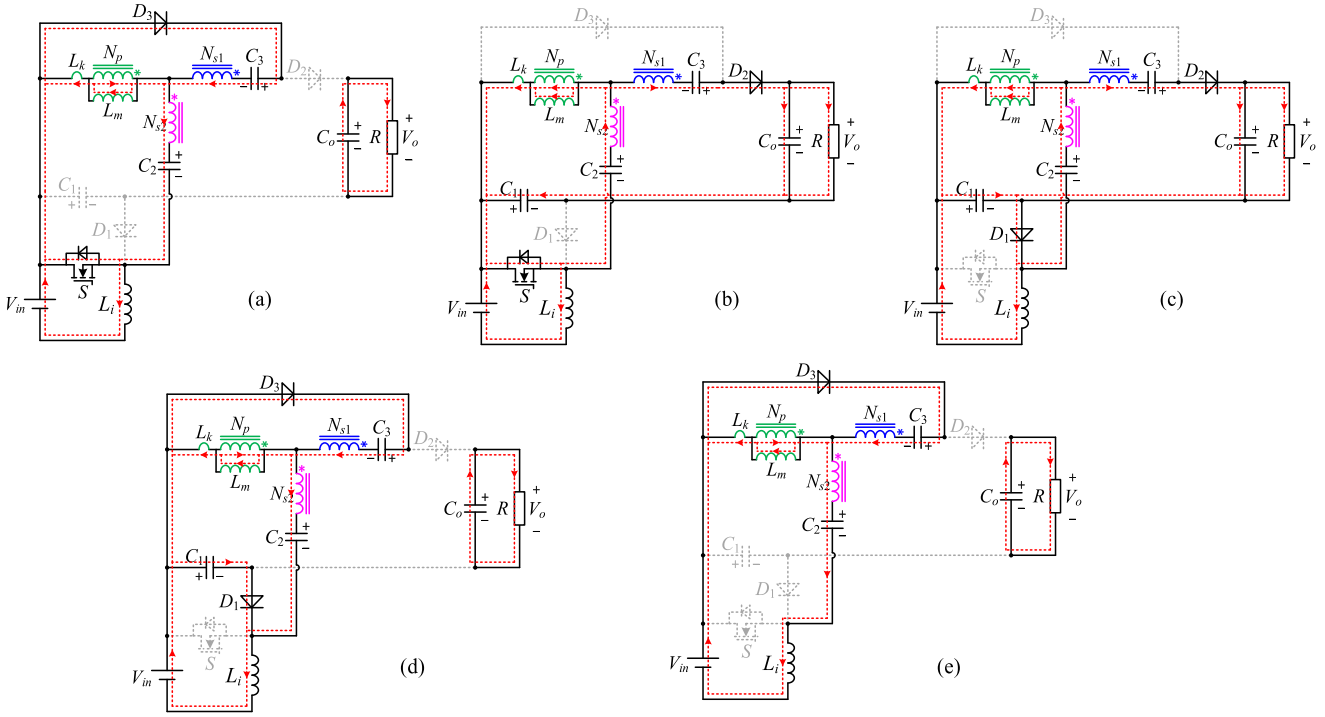

FIGURE 3. The equivalent circuit of YSCI-BBS converter in (a) mode I. (b) mode II. (c) mode III. (d) mode IV. (e) mode V.

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_1) + \dfrac{V_{C1}+V_{C2}+V_{C3}-V_o}{(n_1+n_2)L_m}(t-t_1) \\ i_{Lk}(t) = i_{Lk}(t_1) \\ \quad + \dfrac{(n_1+n_2)V_{C2}-(1-n_2)(V_{C1}+V_{C2}+V_{C3}-V_o)}{(n_1+n_2)L_k} \\ \quad (t-t_1) \\ i_{D2}(t) = \dfrac{V_{C1}+\frac{1+n_1}{1-n_2}V_{C2}+V_{C3}-V_o}{n_1^2 L_k}(t-t_1) \end{cases} \tag{3}$$

Mode III[t_2-t_3]: At $t = t_2$, the switch S is turned off, the diodes D_1 and D_2 are turned on, and D_3 is turned off. The voltage of switch S is clamped to $V_{in} + V_{C1}$. The inductor L_i charges the capacitor C_1 through the diode D_1, and the current i_{Li} decreases linearly. The primary side N_p starts to release energy, the current i_{Lk} starts to drop rapidly, and the secondary side current i_{Ns1} (i_{D2}) also starts to drop rapidly. Current i_{Ns1} (i_{D2}) drops to zero, diode D_2 turns off at t_3, and the mode ends. In this mode, the current i_{D2} can be expressed as:

$$i_{D2}(t) = i_{D2}(t_2) + \frac{V_{C2}+V_{C3}-\frac{n_1+n_2}{1-n_2}(V_{C1}-V_{C2})-V_o}{n_1^2 L_k} \times (t-t_2) \tag{4}$$

Mode IV[t_3-t_4]: In this mode, the switch tube S remains off, the diode D_2 is turned off, and D_1 & D_3 are turned on. The secondary side N_{s1} charges the capacitor C_3 through the diode D_3, the current i_{D3} rises linearly from zero, and the diode D_3 realizes the ZCS turn-on. The energy of the leakage inductance L_k is transferred to the capacitor C_1 through the diode D_1, and the current i_{D1} decreases linearly. The primary side N_p of the coupled inductor continues to discharge, and the current i_{Lk} and i_{Lm} decrease linearly. The current i_{D1} drops to zero, the diode D_1 realizes ZCS turns off at t_4, and the mode ends. In this mode, the following voltage and circuit equations can be expressed as:

$$\begin{cases} V_{Li} = V_{in} - V_{C1} \\ V_{Lm} = \dfrac{V_{C2}-V_{C1}}{1-n_2} \end{cases} \tag{5}$$

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_3) + \dfrac{V_{C1}-V_{C2}-V_{C3}}{(n_1+n_2)L_m}(t-t_3) \\ i_{Lk}(t) = i_{Lk}(t_3) \\ \quad + \dfrac{(n_1+n_2)(V_{C2}-V_{C1})-(1-n_2)(V_{C1}-V_{C2}-V_{C3})}{(n_1+n_2)L_k} \\ \quad (t-t_3) \\ i_{D3}(t) = \dfrac{\frac{1+n_1}{1-n_2}(V_{C1}-V_{C2})-V_{C3}}{n_1^2 L_k}(t-t_3) \end{cases} \tag{6}$$

Mode V[t_4-t_5]: In this mode, the switch S remains off, the diodes D_1 and D_2 are turned off, and D_3 is turned on. The secondary side N_{s1} continues to charge the capacitor C_3 through the diode D_3. The primary side N_p of the coupled inductor continues to discharge, and the current i_{Lk} and i_{Lm} decrease linearly. The inductor L_i continues to discharge, and the current i_{Li} decreases linearly. In this mode, the current i_{D3}

can be expressed as:

$$i_{D3}(t) = i_{D3}(t_4) + \frac{-V_{C3} - (1+n_1) V_{Lm}}{n_1^2 L_k} (t - t_4) \quad (7)$$

B. VOLTAGE GAIN

First analyze the ideal voltage gain of the YSCI-BBS converter, i.e., the influence of the leakage inductance L_k is not considered. For the convenience of steady-state analysis, transition mode I and mode III are ignored.

According to modes II and IV, there are the following voltage expressions:

$$V_{C1} + V_{C2} + (n_2 + n_1) \frac{V_{C2}}{1 - n_2} + V_{C3} = V_o \quad (8)$$

$$V_{C3} = (1 + n_1) \frac{V_{C1} - V_{C2}}{1 - n_2} \quad (9)$$

According to the volt-second balance law of inductors L_i and L_m, there are equations:

$$V_{in} DT + (V_{in} - V_{C1})(1 - D)T = 0 \quad (10)$$

$$\frac{V_{C2}}{1 - n_2} DT + \left(\frac{V_{C2} - V_{C1}}{1 - n_2}\right)(1 - D)\, T = 0 \quad (11)$$

Given the above relationships, the ideal voltage gain of the YSCI-BBS converter can be obtained as:

$$G_{\text{ideal}} = \frac{V_o}{V_{in}} = \frac{2 + n_1 - n_2}{(1 - n_2)(1 - D)} \quad (12)$$

Derive the voltage gain considering the leakage inductance. According to the ampere-second balance law of capacitance, the average current of each diode is equal to the output current I_o. Combined with the steady-state analysis, the average currents expressions of L_i and L_m, are obtained as:

$$\begin{cases} I_{Li} = \dfrac{2 + n_1 - n_2}{(1 - n_2)(1 - D)} I_o \\ I_{Lm} = 0 \end{cases} \quad (13)$$

From Fig. 2, the mathematical expression of the time $D_x T$ for the diode D_1 current to drop to zero is:

$$D_x = \frac{2(1 - n_2)(1 - D)}{2 + n_1 - n_2} \quad (14)$$

During the rising period DT of diode D_2:

$$\frac{V_{C1} + \frac{1+n_1}{1-n_2} V_{C2} + V_{C3} - V_o}{n_1^2 L_k} = \frac{2 I_o}{D^2 T} \quad (15)$$

During the rising period $D_x T$ of D_3:

$$\frac{\frac{1+n_1}{1-n_2}(V_{C1} - V_{C2}) - V_{C3}}{n_1^2 L_k} = \frac{(2 + n_1 - n_2)^2 I_o}{2(1 + n_1)(1 - n_2)(1 - D)^2 T} \quad (16)$$

According to (13)-(16) and the volt-second balance law of L_i and L_m, the voltage gain expression considering the leakage inductance is obtained as:

$$G = \frac{V_o}{V_{in}} = \frac{2 + n_1 - n_2}{(1 - n_2)[1 - D + \mathrm{A}Q]} \quad (17)$$

where, $\mathrm{A} = n_1^2 \left(\frac{(2+n_1-n_2)^2}{2(1-D)(1+n_1)^2} + \frac{2(1-D)}{D^2}\right)$, $Q = \frac{L_k}{RT}$ is the influence factor of leakage inductance.

Based on (17), the influence of leakage inductance on gain can be drawn under different turn ratios, as shown in Fig. 4. The voltage gain is positively correlated with the duty cycle. The larger the duty cycle is, the more leakage inductance of the Y-source will increase. Excessive leakage inductance will reduce the gain and loss of the duty cycle. In practical applications, the turn ratios n_1 and n_2 should be adjusted reasonably to ensure that the converter does not work at the limited duty cycle in the steady state to reduce the influence of leakage inductance, where $n_1 > 1$, $n_2 < 1$.

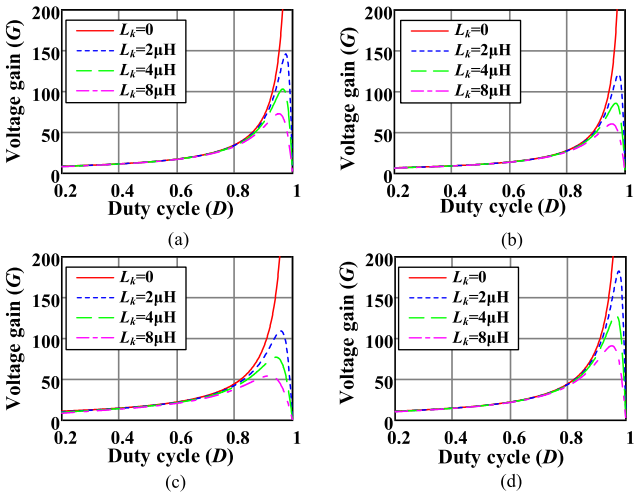

FIGURE 4. The curve of voltage gain G in (a) $n_1 = 1$, $n_2 = 0.5$. (b) $n_2 = 2$ $n_2 = 0.5$. (c) $n_1 = 1$, $n_2 = 0.4$. (d) $n_1 = 1$, $n_2 = 0.6$.

C. STRESS ANALYSIS

According to the steady-state analysis, the voltage stress of each capacitor is obtained:

$$V_{C1} = \frac{1}{1 - D} V_{in} = \frac{1 - n_2}{2 + n_1 - n_2} V_o \quad (18)$$

$$V_{C2} = V_{in} = \frac{(1 - n_2)(1 - D)}{2 + n_1 - n_2} V_o \quad (19)$$

$$V_{C3} = \frac{(1 + n_1) D}{(1 - n_2)(1 - D)} V_{in} = \frac{(1 + n_1) D}{2 + n_1 - n_2} V_o \quad (20)$$

The voltage stress of the switch S and each diode can be expressed as:

$$V_S = \frac{1}{1 - D} V_{in} = \frac{1 - n_2}{2 + n_1 - n_2} V_o \quad (21)$$

$$V_{D1} = \frac{1}{1 - D} V_{in} = \frac{1 - n_2}{2 + n_1 - n_2} V_o \quad (22)$$

$$V_{D2} = V_{D3} = \frac{1+n_1}{(1-n_2)(1-D)} V_{in} = \frac{(1+n_1)(1-n_2)}{2+n_1-n_2} V_o \tag{23}$$

According to the current balance of C_1 and C_2, there are equations:

$$\int_{t_0}^{t_1} 0dt + \int_{t_1}^{t_3} -i_{D2}(t)dt + \int_{t_3}^{t_4} i_{D1}(t)dt + \int_{t_4}^{t_5} 0dt = 0 \tag{24}$$

$$\int_{t_0}^{t_1} \frac{1+n_1}{1-n_2} i_{D3}(t)dt + \int_{t_1}^{t_3} -\frac{1+n_1}{1-n_2} i_{D2}(t)dt + \int_{t_3}^{t_5} \frac{1+n_1}{1-n_2} i_{D3}(t)dt = 0 \tag{25}$$

According to the ampere-second balance law of capacitance, the average current of those diodes D_1, D_2, and D_3 is equal to the output current I_o.

Considering the current ripple of L_i and L_m, their respective increments are:

$$\begin{cases} \Delta i_{Li} = \dfrac{V_{in}DT}{L_i} \\ \Delta i_{Lm} = \dfrac{V_{in}DT}{(1-n_2)L_m} \end{cases} \tag{26}$$

Get the current stress of the switch S and each diode:

$$i_{S\max} = i_{D1\max} = \frac{2+n_1-n_2}{(1-n_2)(1-D)} I_o + \frac{2(1+n_1)}{D} I_o + \frac{1}{2}(\Delta i_{Li} + \Delta i_{Lm}) \tag{27}$$

$$i_{D2\max} = \frac{2I_o}{D} \tag{28}$$

$$i_{D3\max} = \frac{2+n_1-n_2}{(1-n_2)(1-D)} I_o + \frac{n_1-2+3n_2}{2(2+n_1-n_2)}(\Delta i_{Li} + \Delta i_{Lm}) \tag{29}$$

The root-mean-square currents expression of each device:

$$i_{Li\text{rms}} = \sqrt{\frac{(2+n_1-n_2)^2 I_o^2}{(1-D)^2(1-n_2)^2} + \frac{\Delta i_{Li}^2}{12}} \tag{30}$$

$$i_{Lk\text{rms}} = \frac{n_1+n_2}{1-n_2} I_o \sqrt{\text{B+C}} \tag{31}$$

$$i_{Ns1\text{rms}} = i_{C3\text{rms}} = I_o \sqrt{\text{B+C}} \tag{32}$$

$$i_{Ns2\text{rms}} = i_{C2\text{rms}} = \frac{1+n_1}{1-n_2} I_o \sqrt{\text{B+C}} \tag{33}$$

$$i_{C1\text{rms}} = I_o \sqrt{\frac{2[2+Dn_1-(2-D)n_2]}{3D(1-D)(1-n_2)}} \tag{34}$$

$$i_{Co\text{rms}} = I_o \sqrt{\frac{4(1-D)^2}{3D} + \frac{1}{3}} \tag{35}$$

$$i_{S\text{rms}} = I_o \sqrt{(1+n_1)\text{E} + \text{F}} \tag{36}$$

$$i_{D1\text{rms}} = I_o \sqrt{\frac{2(2+n_1-n_2)}{3(1-n_2)(1-D)}} \tag{37}$$

$$i_{D2\text{rms}} = 2I_o \sqrt{\frac{1}{3D}} \tag{38}$$

$$i_{D3\text{rms}} = \frac{I_o}{(1+n_1)(1-n_2)} \sqrt{\frac{(2+n_1-n_2)(2+3n_1+n_2)}{3(1-D)}} \tag{39}$$

where

$$\begin{cases} \text{B} = \dfrac{3(2+n_1-n_2)-(1-n_2)}{3(1-D)(1+n_1)(1-n_2)^2} \\ \text{C} = -\dfrac{1}{3(1-D)(1+n_1)^2} + \dfrac{4}{3D} \\ \text{E} = \dfrac{2+D+(2-D)n_1-2[(1-D)n_1+1]n_2}{(1-n_2)^2(1-D)^2} \\ \text{F} = \dfrac{[(1-D)n_1+(4-D)]^2-6(2-D)}{3D(1-D)^2} + \dfrac{n_1^2}{D}. \end{cases}$$

D. RESISTANCE ANALYSIS

In actual work, there are impedances in the converter. Fig. 5(a) below is an equivalent circuit with impedances that ignores the leakage inductance. In the figure, r_{Np}, r_{Ns1}, and r_{Ns2} are the impedances of the three windings, r_S is the on-resistance of the switch, and r_{Li} is the resistance of the input inductor. V_{FD1}, V_{FD2}, and V_{FD3} are the forward bias voltage drop of each diode, r_{D1}, r_{D2}, r_{D3} are the on-resistance of each diode, r_{C1}, r_{C2}, r_{C3}, and r_{Co} are the resistance of each capacitor.

The voltage gain considering impedance can be derived as:

$$G_r = \frac{\frac{2+n_1-n_2}{(1-n_2)(1-D)} - \frac{1}{V_i}(V_{FD1}+V_{FD2}+V_{FD3})}{1+\frac{a}{DR}+\frac{Dr_S+b}{(1-D)^2R}+\frac{c+d}{D(1-D)R}+\frac{(2-D)r_{Li}}{D(1-D)^2R}} \tag{40}$$

where

$$\begin{cases} a = r_{D2} + r_{Co} \\ b = \dfrac{(1+n_1)(n_1-2Dn_2+2D+1)r_S + (n_1-2n_2+3)r_{Li}}{(1-n_2)^2} \\ c = r_{Ns1} + r_{Np} + r_{C1} + r_{C3} \\ d = \dfrac{(1+n_1)(r_{Ns2}+r_{C2}) + (n_1+2n_2-1)r_{Np}}{(1-n_2)^2}. \end{cases}$$

Fig. 5(b) shows the relationship between voltage gain and duty cycle considering the impedances. From Fig. 5(b), the voltage gain of the converter varies with the duty cycle and the internal resistance, when duty cycle $D > 0.943$, the efficiency drops sharply. To ensure the stable working of the converter and maintain high efficiency, a duty cycle D less than 0.94 is more suitable.

E. BOUNDARY CONDITION ANALYSIS

The YSCI-BBS converter has two operating patterns: CCM and DCM. When the switching tube remains off and all diodes are turned off, the YSCI-BBS converter enters the inductor current discontinuous mode. The simplified current waveform of DCM is shown in Fig. 6.

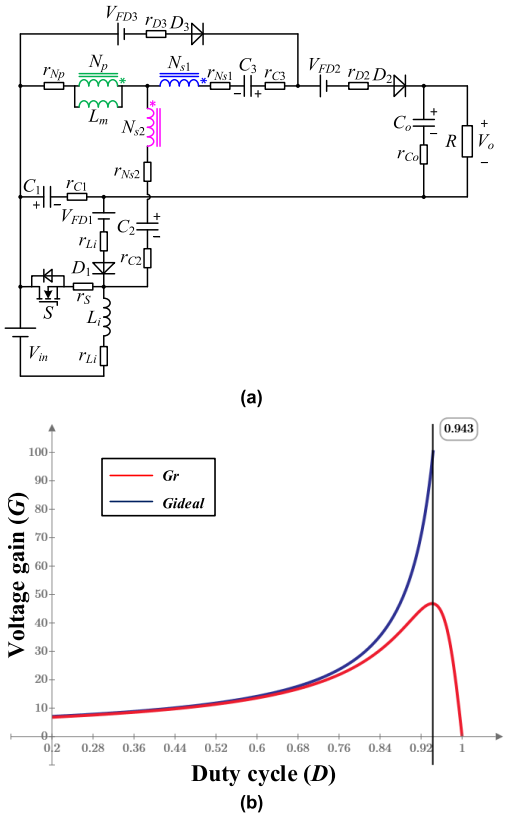

FIGURE 5. Effect of resistance (a) Equivalent circuit (b) Voltage gain vs. duty ratio curve(n_1 = 16:12, n_2 = 0.5, V_i = 20V, r_{Li} = 20mΩ, r_S = 8.5mΩ, V_{FD1} = V_{FD2} = V_{FD3} = 0.7V, r_{Np} = 20mΩ, r_{Ns1} = 25mΩ, r_{Ns2} = r_{D1} = r_{D2} = r_{D3} = r_{C1} = r_{C2} = r_{C3} = r_{Co} = 10mΩ, R = 266.6667Ω).

According to Fig. 6, the current relationship is as follows:

$$(1-n_2)\, i_{Li} + i_{Lm} = 0 \tag{41}$$

Therefore, the current of the equivalent inductance can be expressed as:

$$i_{Leq} = (1-n_2)\, i_{Li} + i_{Lm} \tag{42}$$

Suppose the maximum current expression of the equivalent inductance is:

$$\begin{aligned} i_{Leq\_peak} &= (1-n_2)\,\Delta i_{Li} + \Delta i_{Lm} \\ &= \frac{(1-n_2)\, V_{in} DT}{L_i} + \frac{V_{in} DT}{(1-n_2)\, L_m} = \frac{V_{in} DT}{L_{eq}} \end{aligned} \tag{43}$$

$$L_{eq} = \frac{L_i L_m}{\frac{L_i}{1-n_2} + (1-n_2)\, L_m}.$$

where

The average currents of diodes D_1 and D_3 can be expressed as:

$$I_{D1} = \frac{i_{Leq\_peak} D_x T}{2T} = I_o \tag{44}$$

$$I_{D3} = \frac{\frac{1}{1+n_1}\frac{D_y - D_x}{D_y} i_{Leq\_peak} D_y T}{2T} = I_o \tag{45}$$

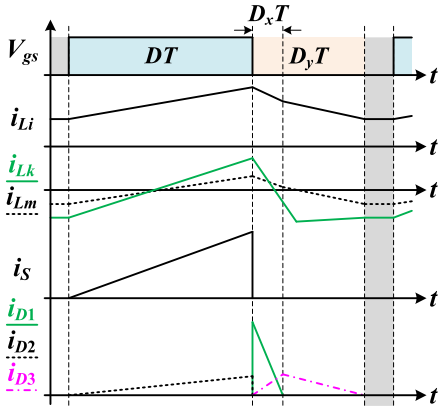

FIGURE 6. DCM simplifies waveforms.

where D_xT is the turn-on time of diode D_1; D_yT is the turn-on time of diode D_3.

Assume the time constant of the equivalent inductance is:

$$\tau_{Leq} = \frac{L_{eq}}{RT} \tag{46}$$

When $Dy = 1\text{-}D$, YSCI-BBS works in the boundary conduction mode (BCM). From (43) ~ (46), the time constant of the critical equivalent inductance can be obtained as:

$$\tau_{Leq\_B} = \frac{D\,(1-D)^2\,(1-n_2)}{2\,(2+n_1)\,(2+n_1-n_2)} \tag{47}$$

Based on (47), the boundary condition of the converter is shown in Fig. 7. When $\tau_{Leq} > \tau_{Leq\_B}$, the converter operates in CCM, otherwise, it is operated in DCM mode.

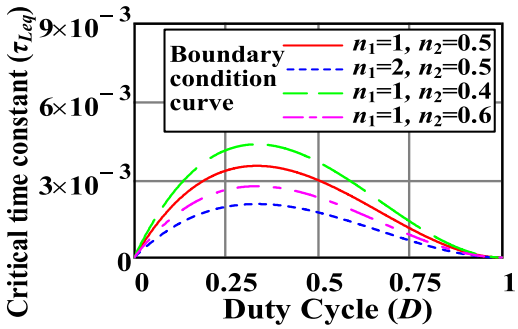

FIGURE 7. Boundary condition curve.

F. SOFT-SWITCHING ANALYSIS

The presence of leakage inductance affects the rate of change of the current in the diode and switch. According to Fig. 2 and Fig. 3, mode I and mode III have the following relationships:

$$i_{D3}(t) = i_{D3}(t_0) + \frac{-\frac{1+n_1}{1-n_2} V_{C2} - V_{C3}}{n_1^2 L_k}(t - t_0) \tag{48}$$

$$\begin{aligned} i_{D2}(t) = i_{D2}(t_2) + \frac{V_{C2} + V_{C3} - \frac{n_1+n_2}{1-n_2}(V_{C1} - V_{C2}) - V_o}{n_1^2 L_k} \\ \times\ (t - t_2) \end{aligned} \tag{49}$$

And get:

$$L_k = \frac{(1+n_1)\,V_o}{n_1^2\,(2+n_1-n_2)\,\frac{di_{D2(3)}}{dt}} \tag{50}$$

The leakage inductance can be used to realize the ZCS turn-on of the switch S (the current change rate $< 30\text{A}/\mu\text{s}$) and alleviate the reverse recovery problem of the diode D_2 and D_3.

IV. CONVERTER EXPANSION AND PERFORMANCE COMPARISON

A. GENERAL TOPOLOGY OF YSCI-BBS CONVERTER

The proposed YSCI-BBS converter can add more diode-capacitor voltage multiplier cells (CD-VMC) to increase the voltage gain. Its general extended topology is shown in Fig. 8.

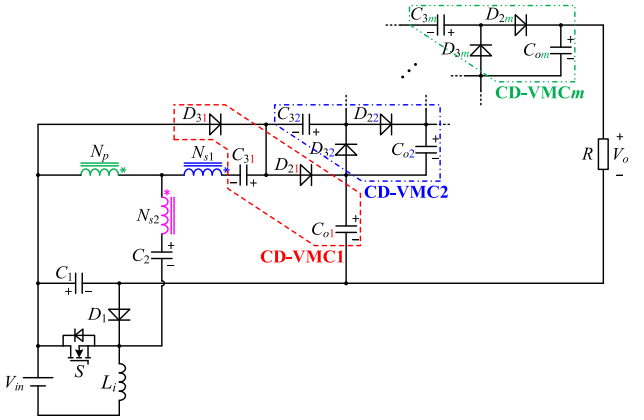

FIGURE 8. The general topology of the YSCI-BBS converter.

The general voltage gain and switch voltage stress expressions of adding CD-VMC cells are:

$$G = \frac{V_o}{V_{in}} = \frac{1-n_2+m\,(1+n_1)}{(1-n_2)\,(1-D)} \tag{51}$$

$$V_{vs-S} = \frac{1-n_2}{1-n_2+m\,(1+n_1)}V_o \tag{52}$$

More voltage multiplier cells can further increase the voltage gain of the YSCI-BBS converter while reducing the voltage stress of the switch. According to the cost in diverse application occasions, the turns ratio of the Y-source coupled inductor and the number of voltage multiplier cells can be flexibly selected to achieve better performance.

B. PERFORMANCE COMPARISON

The key parameters and performance of the YSCI-BBS converter proposed in this paper are compared horizontally with other converters that also introduce coupled inductors. The parameters are in Table 1.

Among them, the sepic-integrated boost converter [8], integrated Buck-Boost converter [12], integrated Boost-SEPIC converter [17], Sepic converter [20], and Quasi Z-Source converter [23] adopt a dual-winding structure. The coupled inductor is small, but the corresponding boosting capability is limited. These converters are designed with soft-switching but suffer from disadvantages such as limited boost effect [8], multi-switch control [12], and only one coupled inductor in the double-coupled structure that plays a role in boosting voltage meanwhile with great voltage stress on the device [17], ZVS can only work in discontinuous mode [20], and significant duty cycle loss [23]. Some converters have lower component counts to reduce cost among the three-winding impedance networks. But in this way, the voltage stress of the switching tube is difficult to control, the duty cycle adjustment is limited [28], or the soft-switching design is lacking [34]. The Y-source converter input measurement current is discontinuous, and the ripple is large [28]. The input measurement current of the Y-source converter is discontinuous and has a strong ripple [28].

Taking the fixed turn ratio of the coupled inductor $n^{2W} = 1{:}1$, $n^{3W} = 1{:}1{:}2$ as a reference, the comparison curve of the corresponding voltage gain is shown in Fig. 9. Through comparison and synthesis, it is found that the new converter proposed in this paper has the advantages of continuous input current and low ripple, soft-switching, improved converter efficiency, and wide ratio range while maintaining high voltage gain and low voltage stress performance.

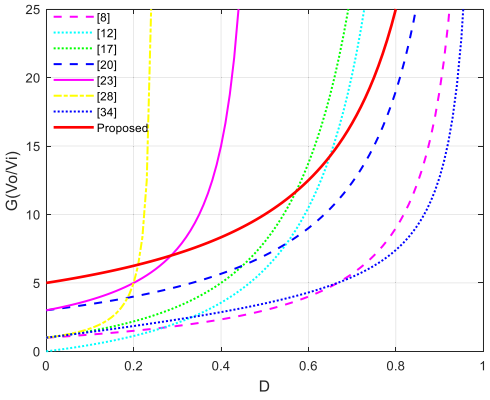

FIGURE 9. Boundary condition curve.

C. CONVERTER FAMILY EXPANSION

According to the construction ideas in Section II, based on the traditional Sepic converter, the integrated topology construction scheme is introduced by introducing Y-source coupled inductance voltage multiplying technology. This type of converter combines a three-winding coupled inductor, a voltage multiple unit, and two power switches with synchronous operation. The constructed topology can realize very high voltage gain and very low switch tube voltage stress while using fewer components. The integrated topology technology can share the diode-capacitor branch in the topology and absorb leakage inductance energy as a passive clamping branch, suppressing the large voltage impact at both ends of the switch tube. The Boost type and Buck-Boost type, i.e., YSCI-BS converters and other YSCI-BBS converters are given, and respective corresponding topological structures

TABLE 1. Performance parameter comparison.

Converter	Voltage gain	Number of * S/D/C/CI+L	Maximum voltage stress on switch (V/V_o)	Total voltage stress on diodes (V/V_o)	Duty cycle Range	Soft*
[8]	$\frac{1+nD}{1-D}$	1/2/3/1^{2W}+1	$\frac{1+D}{1+nD}$	$\frac{1+nD}{1-D}$	1	Yes
[12]	$\frac{(n+1)D(2-D)}{(1-D)^2}$	2/3/4/1^{2W}+2	$\frac{(1-D)}{(n+1)D}$, $D<0.5$ $\frac{1}{n+1}$, $D>0.5$	$\frac{2+n-D}{(n+1)D}$	1	Yes
[17]	$\frac{Dn_2+1+D}{(1-D)^2}$	1/4/4/2^{2W}+1	$\frac{\frac{(n_2+1)(1-D)}{Dn_2+1+D}+1}{n_2+2}$	$2+\frac{(n_2+1)(1-D)+n_2+2}{Dn_2+1+D}+\frac{2n_2+2}{(n_2+1)(n_2+2)}$	1	Yes
[20]	$\frac{2n+1+D}{1-D}$	2/5/5/1^{2W}+1	$\frac{1}{2n+1+D}$	$\frac{4n+2}{2n+1+D}$	1	Yes
[23]	$\frac{n+2}{1-2D}$	1/4/5/1^{2W}+1	$\frac{1}{n+2}$	$\frac{2n+3}{n+2}$	0.5	Yes
[28]	$\frac{1-n_{23}}{(1-n_{23})-(1+n_{13})D}$	1/2/2/1^{3W}	1	$\frac{1-n_{23}}{(1+n_{13})D}$	$\frac{1-n_{23}}{1+n_{13}}$	Yes
[34]	$G=\frac{KD+1}{1-D}$ $K=\frac{N_3+N_1}{N_3-N_2}$	1/2/3/1^{3W}+1	$\frac{1}{(1-D)G}$	$\frac{KG+2K+K^2}{1+KD}+\frac{G+K}{(1+K)G}$	1	No
Proposed	$\frac{2+n_1-n_2}{(1-n_2)(1-D)}$	1/3/4/1^{3W}+1	$\frac{1-n_2}{2+n_1-n_2}$	$\frac{(3+2n_1)(1-n_2)}{2+n_1-n_2}$	1	Yes

*S: Switch, D: Diode, C: Capacitor, CI: Coupled Inductor, 2W=2 windings; 3W=3 windings, L: Inductor, Soft: Soft-Switching.

are shown in Fig. 10 and Fig. 11. Among them, Boost type Fig. 10(a), (b), (d), Buck-Boost type Fig. 11(d), and the Buck-Boost-Sepic topology analyzed in this paper can also realize continuous input current.

V. DESIGN GUIDELINES

This section gives the design guideline of the converter, where the input voltage $V_i = 20$ V; the duty cycle $D = 0.5$; the switching frequency $f_s = 50$ kHz; the rated power $P_o = 150$ W.

A. Y-SOURCE COUPLED INDUCTOR

Set the inductor current ripple coefficient ε, the increment of the inductor current Δi_{Lm}, and calculate L_m:

$$L_m \geq \frac{V_i D T_s}{\Delta i_{Lm}} = \frac{V_i D T_s}{\varepsilon I_{Lm}} \tag{53}$$

The coefficient ε is taken as 35%, determine $L_{\mathrm{m}} = 100\ \mu$H is determined.

B. INPUT-INDUCTOR

$$L_i \geq \frac{V_i D T_s}{\Delta i_{L_i}} = \frac{V_i D T_s}{\varepsilon I_{Li}} \tag{54}$$

The coefficient ε is 35%, determining the input inductance $L_i = 90\ \mu$H.

C. CAPACITOR

Assuming the capacitor voltage ripple coefficient δ, the pulsating voltage Δv_c of the capacitor, calculate the lower limit of the value:

$$C \geq \frac{P_{\mathrm{o}}}{V_o \Delta v_C f_s} = \frac{P_{\mathrm{o}}}{V_o \delta V_{cp} f_s} \tag{55}$$

C_{o} ripple coefficient δ is 0.5%, C_1-C_3 ripple coefficient δ is 2%, take $C_1 = 5 \times 10\ \mu$F, $C_2 = C_3 = 2 \times 5.6\ \mu$F, output capacitance $C_{\mathrm{o}} = 100\ \mu$F.

D. CONTROL CIRCUIT

Fig. 12 is a block diagram of the converter control circuit. The error value is obtained with the reference voltage V_{ref} and the feedback value V_{fd} of the sampled output voltage. The PWM signal of the power switch is given after the error signal goes through the PI controller and the PWM generation. Then complete the control of MOSFET through the driving circuit. When the system is disturbed, the converter can adjust the

TABLE 2. The key parameter of the prototype.

Item	Value
Y-source coupled inductor	L_k=1.63 μH,L_m=100.61 μH; N_p: N_{s1}: N_{s2}=12:16:6;
input inductance L_i	91.25 μH
Capacitor C_1	5×10 μF/50 V film capacitor
Capacitors C_2,C_3	2×5.6 μF100 V film capacitor
Output Capacitor C_o	100 μF/250 V electrolytic capacitor
Switch S	NCEP0178A
Diode D_1	MBR20100CT
Diodes D_2,D_3	MBR20200CT
Switching frequency f	50 kHz

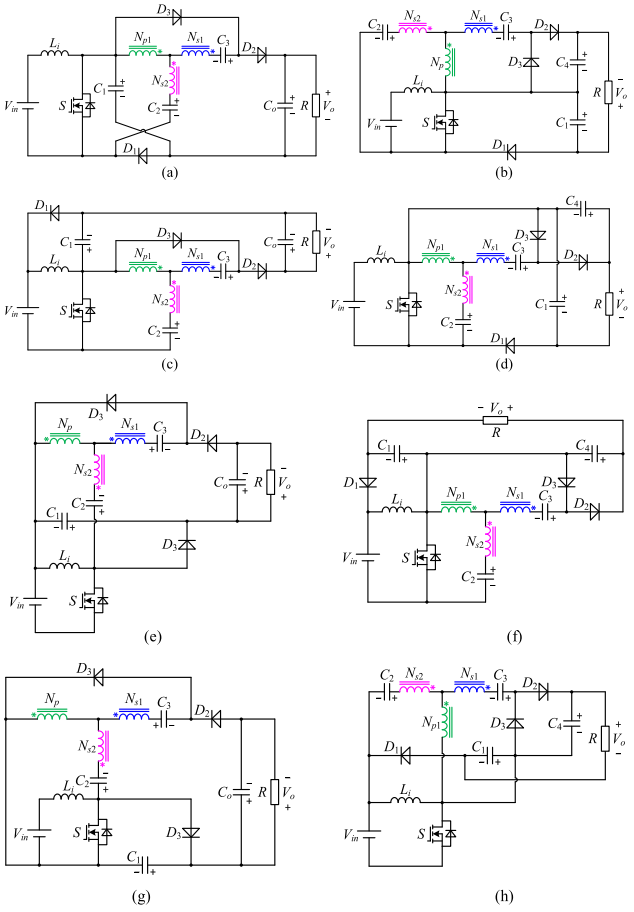

FIGURE 10. A family of YSCI-BS converter.

duty cycle D under the closed-loop PWM control to achieve stable output.

VI. EXPERIMENT AND ANALYSIS

A. EXPERIMENTAL VERIFICATION

To verify the correctness of the principle of the proposed converter, a 150 W laboratory platform was built. The critical parameters of the prototype are shown in Table 2, and the experimental platform is shown in Fig. 13.

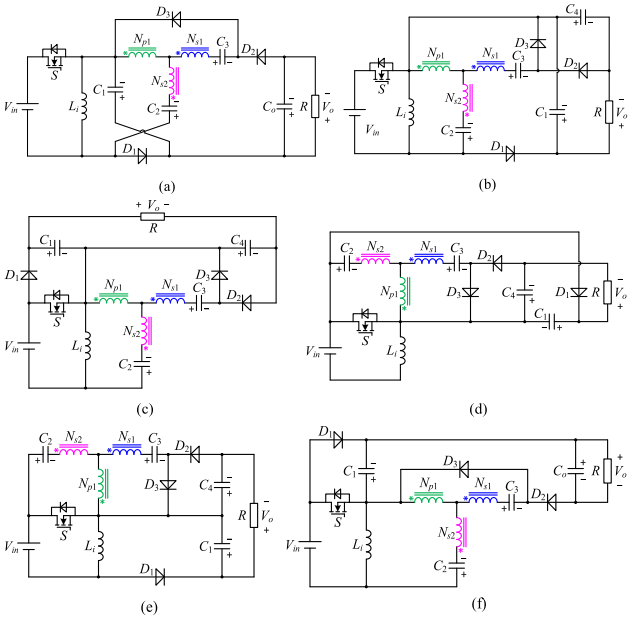

FIGURE 11. A family of YSCI-BB converter.

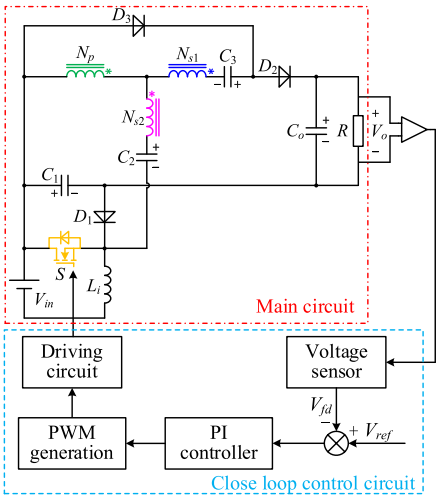

FIGURE 12. Control block diagram.

Fig. 14(b) shows the primary and secondary winding currents of the Y-source coupled inductor. It can be seen that the winding current waveform is the same as the theoretical analysis. Fig. 14(c) is the voltage and current waveform of the switch. It can be seen that the voltage stress of the switch tube is about 46 V, which is about 22.5% of the output voltage, and the converter has very low voltage stress. In Fig. 14(c), the phenomenon of spike switching voltage of about 68V is due to: the dv/dt being very large at the moment of S switching, the resonance is affected by the parasitic capacitance, wiring inductance, etc., and there is a certain peak. The passive clamp. The circuit of the proposed converter can reduce the voltage spike of the switch. It can be seen in Fig. 14(d) that the current rises linearly from zero when the switch tube is turned on, i.e., ZCS turn-on. The

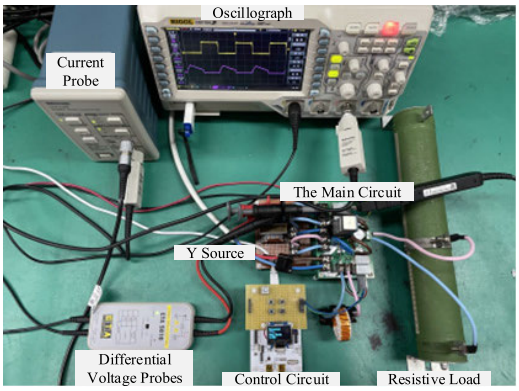

FIGURE 13. Prototype test platform of YSCI-BBS.

FIGURE 15. The thermal picture.

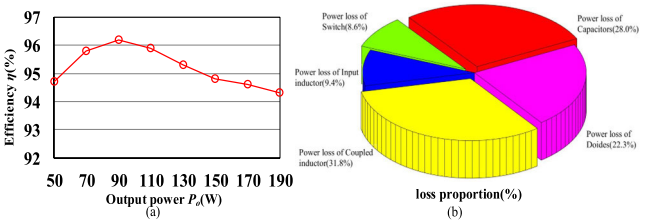

FIGURE 16. Efficiency Analysis. (a) Test efficiency. (b)Power loss proportion.

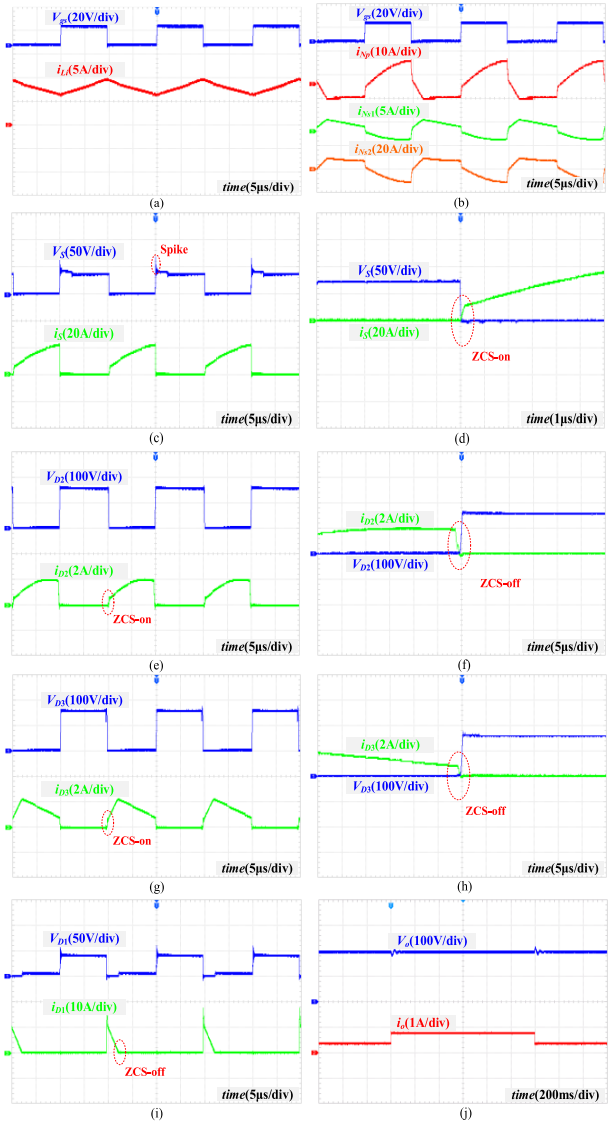

FIGURE 14. Experimental waveforms. (a) V_{gs} & i_{Li}. (b) V_{gs} & i_{Np} & i_{Ns1} & i_{Ns2}. (c) V_S & i_S. (d) S_{ZCS-on}. (e) V_{D2} & i_{D2}. (f) D_{2-off}. (g) V_{D3} & i_{D3}. (h) D_{3-off}. (i) V_{D1} & i_{D1}. (j) Closed-loop control effect.

voltage and current waveforms of each diode are shown in Fig. 14(e), (g), and (i) respectively. Where the voltage stress of diode D_1 is the same as that of switch S. Diodes D_2 and D_3 have the same voltage stress of about 157 V, both of which are lower than the output voltage. Diode D_1 realizes ZCS turn-off and diodes D_2 and D_3 realize ZCS both on and off. In addition, according to Fig. 14(f) and (h), it can be seen that the presence of the leakage inductance limits the current drop rate of the diodes D_2 and D_3, effectively alleviating the reverse recovery problem of the diodes. The above experimental results are the same as the theoretical analysis, verifying the correctness and feasibility of the converter design. Fig. 14(j) is the control effect waveform obtained according to the closed-loop design in section V, which achieves the design purpose, the fluctuation is slight, and the converter works stably and efficiently.

Fig. 15 shows the thermal picture of the prototype at a rated power of 150W using an actual infrared thermal imager. The measured maximum and minimum temperatures are 49.3°C and 28.5°C, respectively, the switching tube has the highest temperature.

B. EFFICIENCY AND LOSS ANALYSIS

Fig. 16 shows the tested efficiency of the converter and the device losses. According to the measured efficiency curve in Fig. 16 (a), the prototype reaches its maximum at around 90W, around 96.2%. As the output power increases, the temperature of the device increases, and the loss becomes larger, which affects the efficiency. Then the efficiency showed a downward trend. At the preset normal operating power of 150 W at full load, the efficiency of the prototype is about 94.8%. According to theoretical calculations, the

full-load efficiency of the prototype is 95.35%, which is close to the measured value. According to the device parameters selected in Table 2, combined with the steady-state analysis, the loss ratio of each component of the YSCI-BBS prototype is obtained, as shown in Fig. 16(b). Among them, since the switching tube realizes ZCS conduction, the loss ratio of the switch is not large. On the other hand, the current stress in the Y-source coupled inductor is higher, so the proportion of inductance and capacitance losses is large.

VII. CONCLUSION

This paper proposes a new type of Buck-Boost integrated Sepic converter, which introduces a Y-source coupled inductor. The single-switch converter retains the characteristics of continuous input current and low ripple of the Sepic topology, improves the integrated structure to achieve gain superposition, reduces voltage stress, and realizes the fusion of topological advantages. Furthermore, the diode-capacitor branch in the original structure is used as a passive clamping branch to absorb leakage inductance and suppress the voltage impact of the switching tube. On the other hand, the leakage inductance energy is used to limit the current rise/fall rate of the switch tube and the diode, so that the ZCS of the switch tube is turned on, and the reverse recovery problem of the diode is alleviated. The efficiency is improved by reducing the voltage stress of the device, reducing the internal current surge, and realizing soft switching to drop losses. In this way, the converter can work stably, extend the lifespan of components prevent equipment from overheating effectively, and convert input power into output electric energy as much as possible. Through the horizontal comparison with other converters, it is proved that the proposed converter has high gain and high efficiency. The feasibility of the theoretical design has been verified by the 150 W YSCI-BBS prototype experiment. The measured efficiency of 50W-190W is around 94.3%-96.2%, higher than the usual 90% of traditional converters. And the voltage stress of the switching tube is only 22.5% of the output voltage. At the same time, the general extension of the YSCI-BBS converter and the extension of the converter family with two topologies under the same construction idea is given. Expanding in general can fulfill the demands for high power and high gain applications. Family expansion can be flexibly configured according to different project site needs while retaining key performance. Briefly, it can flexibly adjust the voltage to achieve high gain and expand to deal with high power and different actual sites, whether it is the step-up link before large-scale PV arrays are connected to the grid or the power consumption needs of household low-power solar panels. This type of converter has good adaptability in high-gain applications and can be flexibly applied in the field of photovoltaic renewable energy.

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