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RESEARCH ARTICLE

Improving Performance of Three-Phase MAF-PLL Under Asymmetrical DC-Offset Condition

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ABSTRACT Synchronization is a critical aspect of integrating renewable energy sources and inverter-based power plants into the electrical grid. Phase-Locked Loops (PLLs) are widely used for this purpose, providing rapid and accurate phase and frequency estimation. In PLLs, the Moving Average Filter (MAF) is commonly employed to extract the fundamental grid voltage component, particularly in the presence of harmonic distortions. Traditional PLLs with a full-cycle time-window MAF perform well in grids with sinusoidal voltage waveforms and DC offsets. However, this approach sacrifices the speed of dynamic response due to the extended time window. In this paper, we introduce a novel approach to address this trade-off. Our method involves reducing the MAF's time window to one cycle by incorporating a delay operator, effectively reducing model complexity and runtime by 50%. Through comprehensive simulations and experimental scenarios, we demonstrate the practical advantages of the proposed method. Comparison of the proposed approach is provided with existing algorithms in the literature, which illustrate its effectiveness in terms of mitigating PLL oscillations in the presence of DC offsets and other non-ideal grid conditions while achieving a 50% improvement in the execution speed. Therefore, the contribution of this paper is in the field of grid synchronization by providing a balanced solution that enhances dynamic response without compromising DC-offset rejection. The proposed method can improve the stability and efficiency of grid-connected systems involving renewable energy sources and inverter-based power plants.

INDEX TERMS DC offset, delay signal cancellation, moving average filter, phase locked loop, real-time simulation, synchronization.

I. INTRODUCTION

Proliferation of renewable energy plants, microgrids, distributed generation, and power-electronics-based equipment into the electric grid mandates more comprehensive and efficient control techniques for power generation, transmission, and distribution [1]. Synchronization is a vital step for integration of the renewable energy sources and converter-based plants into the grid. A main component used in the synchronization procedure is a phase-locked loop (PLL) which can extract the frequency and phase angle based on voltage magnitude measurements.

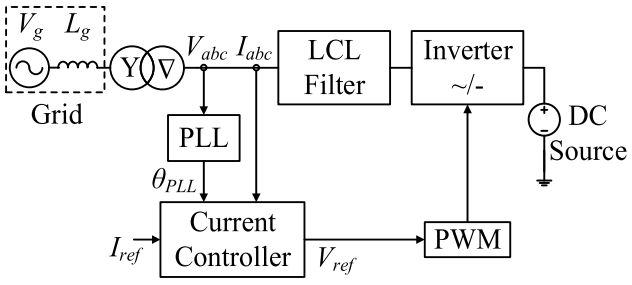

FIGURE 1. A typical grid-tied inverter utilizing a PLL.

A PLL is a control system that generates an output signal whose frequency and phase are related to the frequency and phase of the input signal. Keeping the input and output phase

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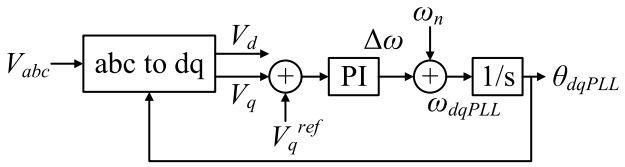

FIGURE 2. SRF-PLL [7], [8].

in lock implies keeping the input and output frequencies the same. PLLs are widely employed in telecommunications, power electronics, and power system applications where fast and accurate estimation of phase and frequency is needed. Figure 1 shows the block diagram of a typical grid-tied converter utilizing a PLL for synchronization.

A typical PLL consists of a closed-loop feedback control system consisting of a coordinate-transformation block (from abc to dq or $\alpha\beta$), a component extractor to calculate voltage-sequence components, a phase detector to estimate the phase difference between input signal and the signal generated by the internal oscillator, a loop filter, and a voltage-controlled oscillator to calculate the correct phase angle [2].

Fast and accurate estimation of grid voltage's frequency and phase angle during balanced and unbalanced conditions is a major challenge for grid-connected converters. Unbalanced grid conditions may arise due to the presence of DC offset, noise and harmonic distortion, voltage sag and swell, frequency and phase jumps, and grid faults [3]. Many PLL algorithms have been designed and implemented in the last three decades to improve the accuracy and speed of three-phase grid synchronization in normal and abnormal conditions [4]. PLLs in the abc coordinate system are not immune to grid voltage distortions [5]. Under ideal grid conditions, the conventional synchronous reference frame (SRF) PLL, shown in Figure 2, provides fast and accurate dynamic response. Despite its simple structure and satisfactory performance under symmetrical grid conditions, SRF-PLL shows very poor performance in adverse grid conditions and limited disturbance-rejection and harmonic-filtering capabilities [6].

In practice, the grid voltage waveform can be far from an ideal sine wave. One of the major nonidealities of grid voltage is the DC offset on phase voltages. DC offset can be present due to grid faults, transformer saturation, thermal drift of the analog elements, geomagnetic phenomena, DC injection from distributed generation systems, power-electronic components, and sensors. PLLs must have a high DC-offset rejection capability; otherwise, they might have a wrong phase lock, poor dynamic response, and periodic ripples [9].

To improve the performance of SRF-PLL under adverse grid conditions, different in-loop and pre-loop filters have been incorporated, including notch filters [10], moving average filters (MAF) [11], complex coefficient filters [12], [13], Kalman filters [14], delayed signal cancellation (DSC) operator [15], [16], [17], [18], space vector filters [19], digital filters [20], dual second-order generalized integrators (DSOGI) [21], [22], band-pass filters (BPF) [23], adaptive low-pass filters (LPF) [24], and sliding Fourier transform (SFT) [25].

The integration of a first-order MAF within the control loop of the SRF-PLL has garnered significant interest in academic literature [26]. MAF is a linear finite-impulse-response filter that can act as an LPF to extract the fundamental component of the grid voltage. Using MAF, the average value of the input signal sampled in the sliding time window, T_w, is calculated continuously as the filter output. The MAF passes the DC component while showing a low-pass filtering characteristic with periodic notch-type attenuation at frequency components of integer multiples of $1/T_w$ [1].

Having a signal free of harmonic oscillations and containing only the mean value of the input signal makes MAF-PLL a good solution for adverse grid conditions. The MAF technique has significant advantages including easy implementation, disturbance rejection capability, better accuracy, and low computational burden [27]. However, applying MAF introduces a considerable phase delay in the PLL control loop leading to slower dynamic response and reduced bandwidth. To deal with this challenge, several approaches such as pre-loop MAFs [7], [8], Quasi-Type-1 (QT1) PLL structure [28], hybrid PLL structure [29], PID controller [30], and lead compensator [31] have been proposed in the literature.

The MAF-PLL with a window width equal to the input fundamental period can remove the DC offset and all the harmonics up to the aliasing frequency in addition to the fundamental-frequency disturbance components. Other choices for the window width of the MAF are $T_w = T/2$ and $T_w = T/6$, which, respectively, are suitable for odd-order and non-triplen harmonic rejection [26]. The MAF needs a time equal to its window width to reach a steady-state condition. A wider window width will result in a slower transient response and a smaller PLL bandwidth [27].

Shortening the MAF's time window can result in poor rejection capability of the PLL and can affect the stability of the system. Some of the proposed techniques also increase the computational burden significantly. If the grid frequency deviates from the nominal value (f_n), the frequencies of characteristic harmonics will also deviate from integer multiples of f_n; as a result, the MAF can only partially attenuate them [32]. Making T_w adaptive with the grid frequency is possible by adjusting the sampling period to the grid frequency deviation. The real-time implementation of the frequency-adaptive MAF needs a higher computational effort and a larger memory [33]. Since PLL is a small part of the control strategy, implementation of a variable sampling rate PLL may not always be practical [30].

MAF with a fundamental-cycle time window provides unity gain at zero frequency, and zero gain for harmonics. Reducing the time window significantly reduces the DC-offset-rejection capability of MAF [30]. The presence of DC offset in the signals feeding the PLL's input is a major problem as it results in an oscillatory frequency output signal.

In this paper, we propose a method to enhance the performance of a three-phase MAF-PLL structure by adding a single delay operator and reducing the MAF's time window to half cycle which halves the filter's runtime. In the proposed method, MAF and the delay operator are merged to increase the time efficiency of the algorithm which reduces the PLL's response delay by approximately 50%. This method can be applied to any MAF-based PLL to improve its efficiency.

The rest of this paper is structured as follows. In Section II, we review MAF-PLL and analyze the impact of MAF's time-window width on PLL's DC-offset rejection capability. In Section III, the proposed method to improve the performance of MAF-PLL is explained in detail. Also, using simulation and experimental tests, we verify how the proposed method improves the dynamic response of the PLL and its DC-offset and harmonic rejection capability with low additional computational burden. In Section IV, the performance of the proposed PLL is tested using several contingency scenarios for adverse grid conditions and the results are compared with those of other popular algorithms in terms of accuracy and complexity. In Section V, we present the concluding remarks.

A. NOMENCLATURE

- CDSC: Cascaded Delayed Signal Cancellation
- CF: Comb Filter
- DC: Direct Current
- DSC: Delay Signal Cancellation
- DSOGI: Dual Second-Order Generalized Integrators
- FIFO: First In, First Out
- LPF: Low-Pass Filter
- MAF: Moving Average Filer
- MDSC: Multiple Delay Signal Cancellation
- PC: Personal Computer
- PID: Proportional, Integral, Derivative
- PLL: Phase Locked Loop
- PWM: Pulse-Width Modulation
- SPWM: Sinusoidal Pulse-Width Modulation
- QSG: Quadrature Signal Generators
- QT1: Quasi-Type 1
- RTC: Real-Time Controller
- SFT: Sliding Fourier Transform
- SRF: Synchronous Reference Frame
- VSC: Voltage Source Converter

II. MAF-PLL

MAF, shown in Figure 3 (a), is a common method for smoothing noisy data that can extract the fundamental component of the grid voltage. A variation of this structure is used in MATLAB/SIMULINK's three-phase PLL block. The adoption of a first-order MAF within the control loop of the SRF-PLL has attracted notable attention in the literature [26]. In a typical MAF-PLL, the three-phase input signal undergoes transformation into the dq0 rotating frame (Park transformation) utilizing the angular speed of an internal oscillator (as illustrated in Figure 3 (b)). The quadrature axis of the

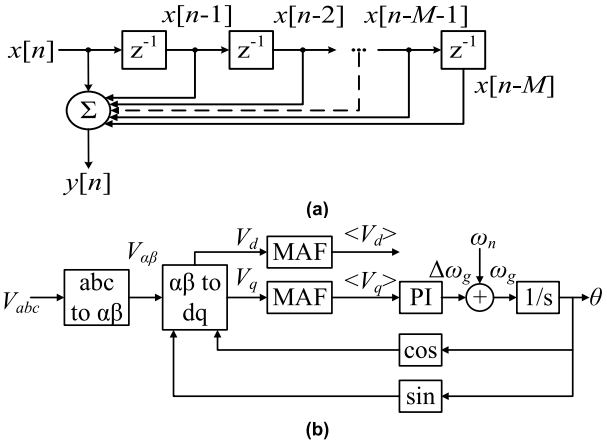

FIGURE 3. (a) MAF; (b) MAF-PLL.

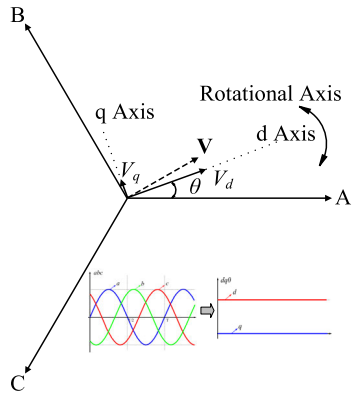

FIGURE 4. Park transformation.

transformed signal, calculated based on the phase difference between the abc signal and the rotating reference frame, is filtered using an MAF.

In an MAF, the average value of the input signal sampled in the sliding time window T_w is calculated continuously as the filter output. Addition of MAF in an SRF-PLL control loop provides the PLL with disturbance rejection capability and better accuracy. This benefit comes at the cost of an additional computational complexity and time delay. If the window width of MAF is set to the input fundamental period, it can remove the oscillations caused by a DC offset and higher-order harmonics. However, applying MAF with a wide time window introduces a considerable phase delay in the PLL control loop, leading to slower dynamic response and reduced bandwidth. Shortening the MAF's time window can reduce the delay but may result in poor DC-offset rejection capability of the PLL.

A. IMPACTS OF DC OFFSET

The first component of an MAF-PLL closed-loop feedback control system is Park's transformation from abc to dq0 coordinate system. Park's transformation, given in (1), transforms three-phase sinusoidal voltage signals into constant values in

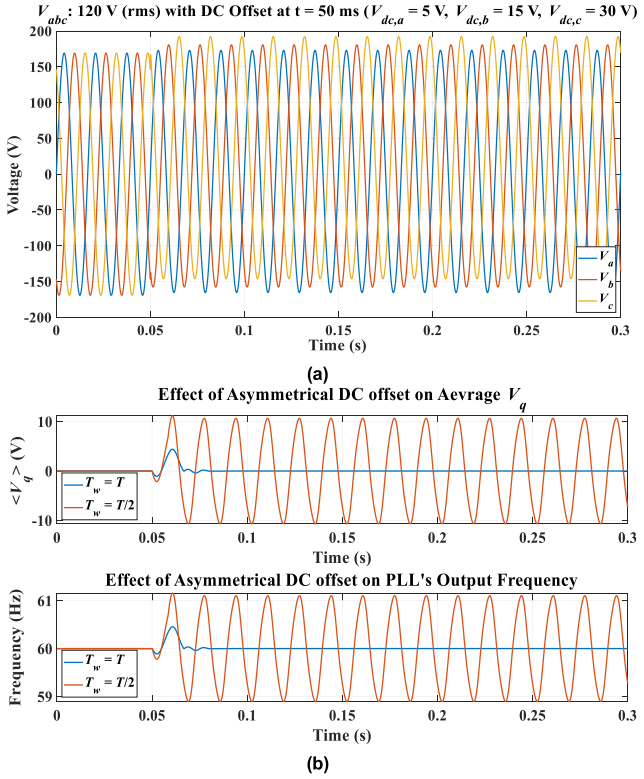

FIGURE 5. (a) Three-phase input voltage subjected to asymmetrical DC offset at $t = 0.05$ s; (b) Effect of asymmetrical DC offset on MAF output with the window width of $T_W = T$ and $T/2$.

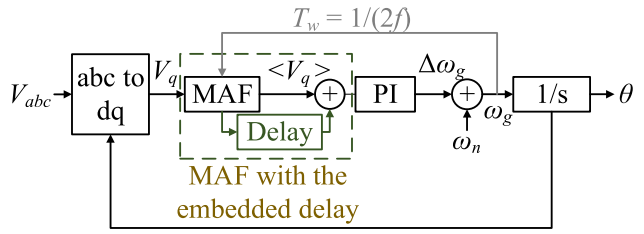

FIGURE 6. Modified MAF with DC-cancellation capability.

the dq rotating coordinate system (see Figure 4).

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1}$$

However, if *abc* voltage signals have DC offsets, dq components will have an oscillatory behaviour. For instance, if $v_a(t) = V_{pk}\sin(\theta(t)) + V_{a,dc}$, $v_b(t) = V_{pk}\sin(\theta(t) - 120^o) + V_{b,dc}$, and $V_c(t) = V_{pk}\sin(\theta(t) + 120^o) + V_{c,dc}$, dq0 voltage components can be derived as (2), shown at the bottom of the next page, where $V_{a,dc}$, $V_{b,dc}$, and $V_{c,dc}$ represent the DC offsets on each phase. In this case, both v_q and v_d voltage components show oscillatory behavior which can be cancelled if an MAF filter with $T_w = T = 1/f$ is used. Shorter window width cannot

```
1  function y = meanDelayFunction(u, f)
2    %u is the input signal and f is the measured frequency
3    freq = 2 * f; % MAF's fundamental frequency, Tw = 1 / freq
4    persistent buffMean buffDelay yf
5    fs = 10000; % Sampling rate
6    winSize = ceil(fs / freq); % MAF window size
7    % Initialize buffMean and buffDelay with zeros
8    if isempty(buffMean)
9      buffMean = nan(1, winSize + 1);
10     buffDelay = zeros(1, winSize);
11     yf = 0; %filtered output
12   end
13   % Use buffMean as FIFO (First In, First Out)
14   buffMean = [buffMean(2 : end), u];
15   if ~isnan(buffMean(1))
16     yf = sum(buffMean(2 : end)) / winSize;
17   end
18   % Use buffDelay as FIFO
19   buffDelay = [buffDelay(2:end) yf];
20   y = yf + buffDelay(1);
   end
```

FIGURE 7. Pseudocode implementation of "MAF + delay" function.

cancel these oscillations, while MAF's wider time window results in a slower MAF transient response.

To demonstrate this, a three-phase voltage system of 120 V (rms) value is subjected to asymmetrical DC offsets as shown in Figure 5 (a). Figure 5 (b) shows that asymmetrical DC offset on three phase input of an MAF-PLL results in an oscillatory V_q that can only be cancelled by the window width of $T_w = T$. When $T_w = T/2$, average quadrature-axis voltage, denoted as $<V_q>$, shows a periodic oscillatory behaviour which consequently results in non-damped ripples in PLL's output frequency.

III. METHODOLOGY

Adding a parallel transport delay of $T/2$ to the MAF with window width of $T/2$ can significantly improve the DC-offset rejection capability of MAF without affecting its computational burden. This concept of delay signal cancellation has been used in other PLL methods such as cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC) for harmonic cancellation. In our work, we propose a single MAF and delay operator, merged into one block, to lower the PLL's execution time. Figure 6 shows the proposed MAF-PLL with the addition of one parallel delay block. The window width of MAF is reduced to $T/2$, where $T = 1/f$. This window width can be adjusted adaptively based on PLL's output frequency. Addition of the parallel delay block can be implemented along with MAF with very low computational speed and memory implications.

Pseudocode implementation for MAF and transport delay are shown in Figure 7. MAF is a linear function, and its time complexity is O(n) where n is the number of samples in the time window. Therefore, reduction of the MAF's window width to half, halves the filter's runtime.

Time and memory efficiency of the code shown in Figure 7 can be further improved using Welford's formulation if one

TABLE 1. Harmonic orders in the abc and dq frames, and maf's harmonic-cancellation capability.

Harmonic order in the abc frame	…	-11	-5	-1	0	+1	+7	+13	…
Harmonic order in the dq frame	…	-12	-6	-2	-1	0	+6	+12	…
Harmonics canceled when $T_w = T/2$	…	✓	✓	✓	x	x	✓	✓	…
Harmonics canceled when $T_w = T$	…	✓	✓	✓	✓	x	✓	✓	…

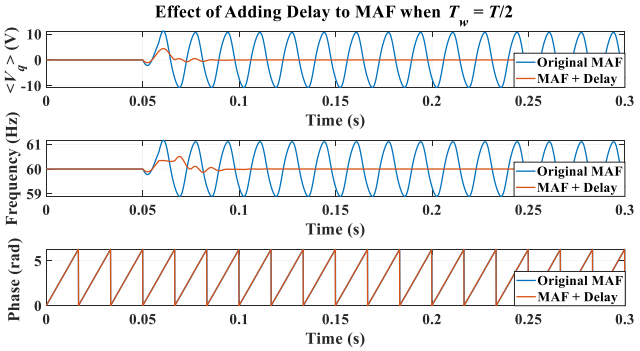

FIGURE 8. Effect of adding delay to an MAF with $T_W = T/2$.

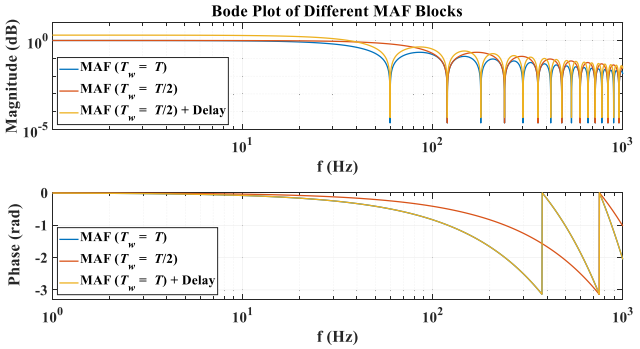

FIGURE 9. Frequency response of the "MAF + delay" block compared with that of MAFs with time window of T and $T/2$.

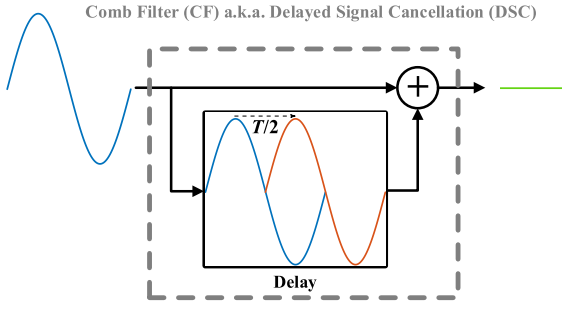

FIGURE 10. Comb filter with a delay value of $T/2$.

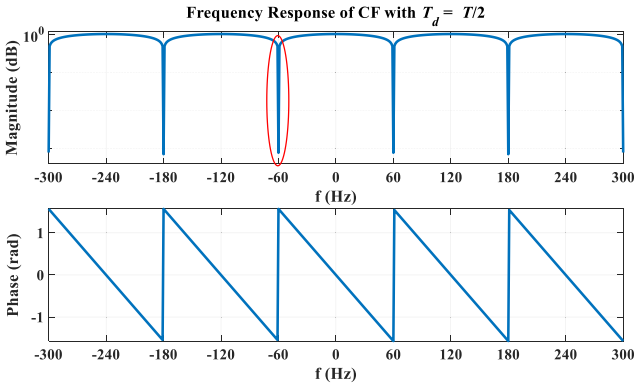

FIGURE 11. Frequency response of CF with a delay of and $T/2$.

chooses to use approximate moving average value instead of calculating the exact one [34].

The voltage average $<V_q>$, frequency, and phase angle of a PLL with the window width of $T_W = T/2$, with and without the delay block are shown in Figure 8. An asymmetrical DC offset is introduced at $t = 50$ ms. The frequency oscillations are significantly damped with the addition of the delay block within approximately 35 ms. This settling time can be further reduced by real-time fine tuning of the PI controller parameters.

Based on MAF's transfer function given in (3), the low-pass frequency response of MAF with $T_w = T/2$ is calculated and compared with the case of the same filter with a delay block, and with the case of $T_w = T$ in Figure 9. The low-pass frequency response of the implemented modified MAF is the same as that of an MAF with $T_w = T$ except for a factor of 2 which is compensated by the proportional gain of the PI controller.

$$G_{MAF}(\mathrm{s}) = \frac{1 - e^{-\mathrm{s}T_w}}{\mathrm{s}T_w} \tag{3}$$

To further study the impact of T_w on the harmonic rejection capability of MAF, we assumed that the three-phase grid volt-

$$\begin{cases} v_q = -V_{pk} - \left(\dfrac{\sin(\theta)\left(2V_{a,dc} - V_{b,dc} - V_{c,dc}\right) + \sqrt{3}\cos(\theta)\left(V_{c,dc} - V_{b,dc}\right)}{3} \right) \\ v_d = \dfrac{\cos(\theta)\left(2V_{a,dc} - V_{b,dc} - V_{c,dc}\right) + \sqrt{3}\sin(\theta)\left(V_{b,dc} - V_{c,dc}\right)}{3} \\ v_0 = \dfrac{V_{a,dc} + V_{b,dc} + V_{c,dc}}{3} \end{cases} \tag{2}$$

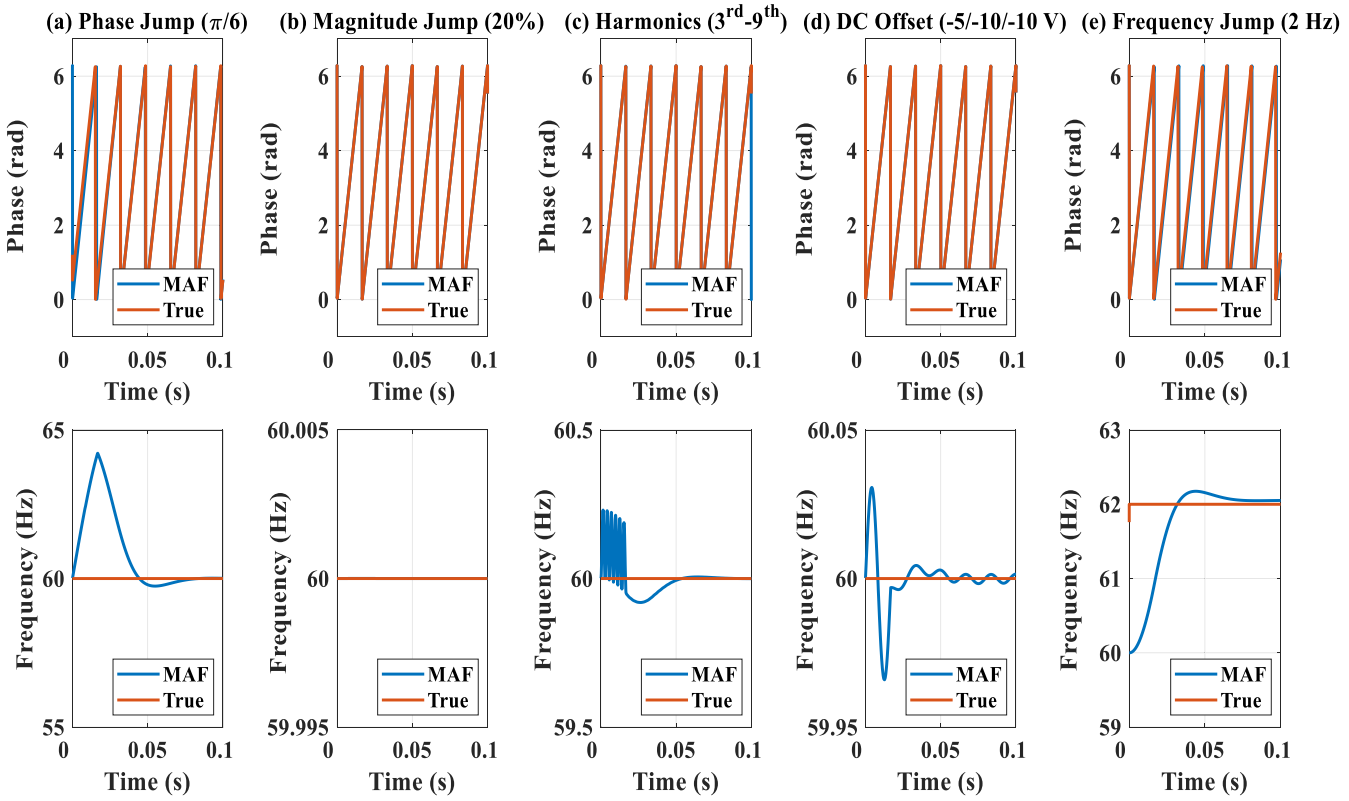

FIGURE 12. Phase (top) and frequency (bottom) output of implemented MAF-PLL for five abnormal grid conditions: (a) phase jump; (b) magnitude jump; (c) odd harmonics injection; (d) asymmetrical DC offset; (e) frequency jump.

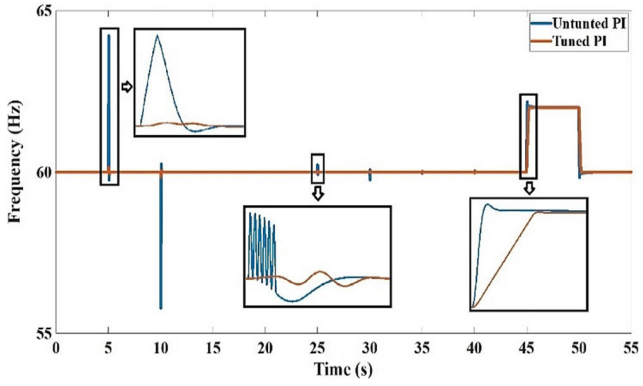

FIGURE 13. Transient response improvement with automatic tuning of PI controller parameters.

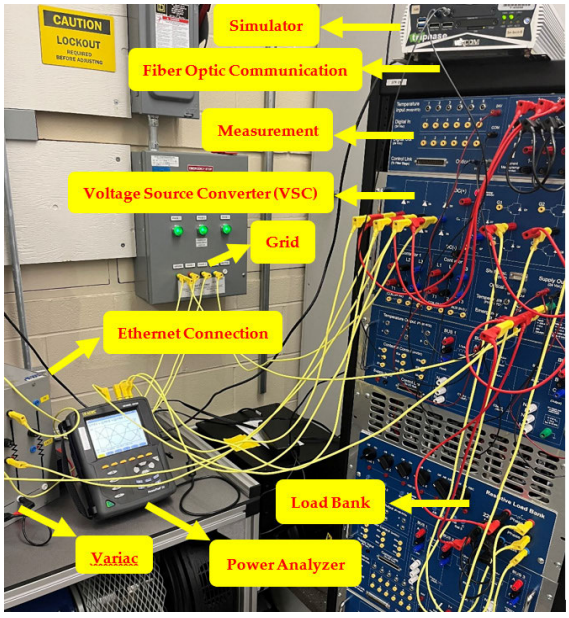

FIGURE 14. Experimental setup.

age contains fundamental positive- and negative-sequence components, dc offset, and dominant non-triplen odd harmonics (-5^{th}, $+7^{th}$, -11^{th}, $+13^{th}$, ...) [32]. After Park transformation, the fundamental positive-sequence, DC offset, fundamental negative-sequence, and n^{th}-order harmonics in the abc frame are respectively transformed into the DC offset, negative-sequence, negative 2^{nd}-order, and $(n-1)^{th}$-order harmonics in the dq frame [35]. The transformation of harmonic orders from the abc to the dq frame is summarized in Table 1 [6], [8].

In signal processing, adding the delayed version of the signal to itself (shown in Figure 10) is known as comb filter (CF) [36]. This is also known as delay signal cancellation (DSC) in PLL applications [37]. The transfer function of a

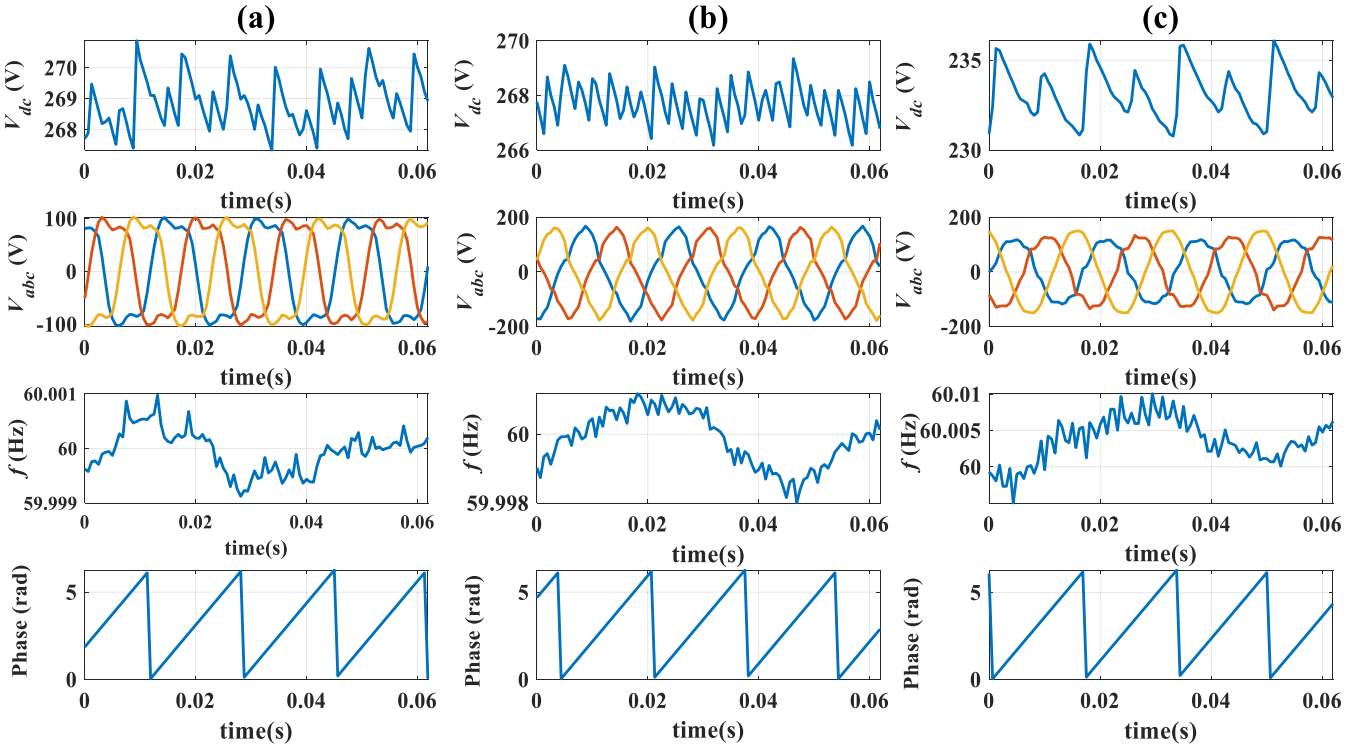

FIGURE 15. The DC-side voltage, the inverter's three-phase output voltages, and PLL's output frequency and phase signals: (a) under-modulation SPWM $m_a = 0.9$; (b) over-modulation SPWM $m_a = 1.4$; (c) asymmetrical three phase scenario created using a variac.

comb filter with a delay value of T_d is given in (4):

$$G_{CF}(s) = 1 + e^{-T_d s} \tag{4}$$

As shown in Table 1, MAF with $T_w = T/2$ cannot cancel the DC component. The frequency response of a CF with the delay value of $T_d = T/2$ is shown in Figure 11. This CF has periodic notch-type attenuation at odd frequencies which removes the fundamental negative-sequence component in the dq frame corresponding to the DC value in the abc frame. In our work, CF and MAF are merged in one block to optimize the time efficiency of the code and reduce its complexity. This filter can reject any integer harmonic and can be utilized in other versions of MAF-based PLLs. Using this filter, the same filtering capability of an MAF with full-cycle time window is achieved at 50% reduced runtime.

A. SIMULATION OF ABNORMAL GRID CONDITIONS

To show the effectiveness of the implemented MAF-PLL, five contingencies are simulated as shown in Figure 12. These contingency scenarios are listed below:

- Phase jump of $\pi/6$ rad
- Magnitude jump or voltage swell of 20%
- Odd harmonic injection (3^{rd}: 30%, 5^{th}: 30%, 7^{th}: 15%, 9^{th}: 20%)
- Asymmetrical DC offset ($V_{a,dc} = -5$ V, $V_{b,dc} = -10$ V, and $V_{c,dc} = -10$ V)
- Frequency jump of 2 Hz

Phase and frequency response of the implemented PLL is displayed in Figure 12.

Figure 12 shows the PLL's output frequency and phase versus the "true" values. For all five contingencies, transient response settles to the true value in about 0.1 s. For this study, simulation time step was 0.1 ms; nominal voltage and frequency were 120 V (rms) and 60 Hz, respectively; and the PI controller parameters were set to $k_p = 0.18$ and $k_i = 0.32$.

PI tuning for MAF-PLL is done using the symmetrical optimum method that maximizes the phase margin at the grid frequency [38]. The proportional and integral gains can be calculated using (5) [30]:

$$k_p = \frac{2}{V_1^+ b T_w} \text{ and } k_i = \frac{2}{V_1^+ b^3 T_w^2} \tag{5}$$

where $V_1^+ = 1$ pu, and b is calculated using (6) to provide a phase margin of about 45° for the PLL to guarantee its stability [3].

$$\text{Phase Margin} = \tan^{-1}\left(\frac{b^2 - 1}{2b}\right) \tag{6}$$

As shown in Figure 13, automatic tuning of the PI controller can significantly reduce the overshoot and settling time values at the cost of higher computational time. The waveforms are enlarged at the onset of phase jump, harmonic injection, and frequency jump for more clarity.

B. REAL-TIME SIMULATION RESULTS

Further analysis was done using a prototyping system that allows the algorithm to be tested rapidly. This system, shown in Figure 14, is comprised of a real-time controller (RTC) which is a standard x86/AMD64 PC running a Linux operating system. The operating system allows compiled C code, generated by MATLAB Simulink's automatic code generation, to be executed in real-time. The main hardware block is a voltage-source converter (VSC) which is an industrial-grade variable-frequency-drive controlled by the RTC. The system comes with a data acquisition panel containing six isolated voltage and three current measurements ports that can send data back to the workstation for control or measurement visualization. The data acquisition panel contains isolated inputs capable of measuring up to 1000 V and current measurements up to 15 A.

The experimental setup makes use of a fiber-optic communication system that facilitates communication among VSC, RTC, and the data acquisition block at the speed of 250 Mbps. Information and commands exchanged with the RTC are time-synchronized and assembled for scheduled data exchange with the workstation PC through a standard Ethernet connection. Data logging is done at the sampling rate of 16 kHz.

As shown in Figure 14, a load bank was connected to the inverter side of the VSC, and a variac was utilized to generate asymmetrical three-phase voltages. We used a power analyzer for further measurement verifications. The inverter in this setup was controlled using the sinusoidal pulse-width modulation (SPWM) scheme in which gate firing signals are generated by comparing a sawtooth carrier signal with a sinusoidal reference signal.

Three abnormal conditions were created and tested using this experimental setup. The ratio of the reference signal's amplitude to that of carrier, known as amplitude modulation index (m_a), was varied to generate different harmonic-polluted non-ideal voltage signals. Cases (a) and (b) are under-modulation ($m_a = 0.9$) and over-modulation ($m_a = 1.4$) scenarios for the inverter which cause high harmonic content. Case (c) is an asymmetrical scenario implemented using a variac in addition to harmonics added due to under-modulation. The PI controller parameters were set to $k_p = 0.18$ and $k_i = 0.32$. The PLL estimates the voltage frequency and phase based on the three-phase voltage measurements. No additional information about the system is needed. The DC-side voltage, the inverter's three-phase output voltages, as well as PLL's output frequency and phase signals are provided in Figure 15.

As clearly seen in Figure 15, the modified MAF-PLL algorithm successfully identifies the frequency of the fundamental component as well as the phase angles in all three scenarios. The absolute error value in case (c), where there is asymmetry, is ±0.01 Hz. In comparison, in cases (a) and (b) where harmonic content is symmetrical among the three phases, the absolute error value is ±0.001 Hz.

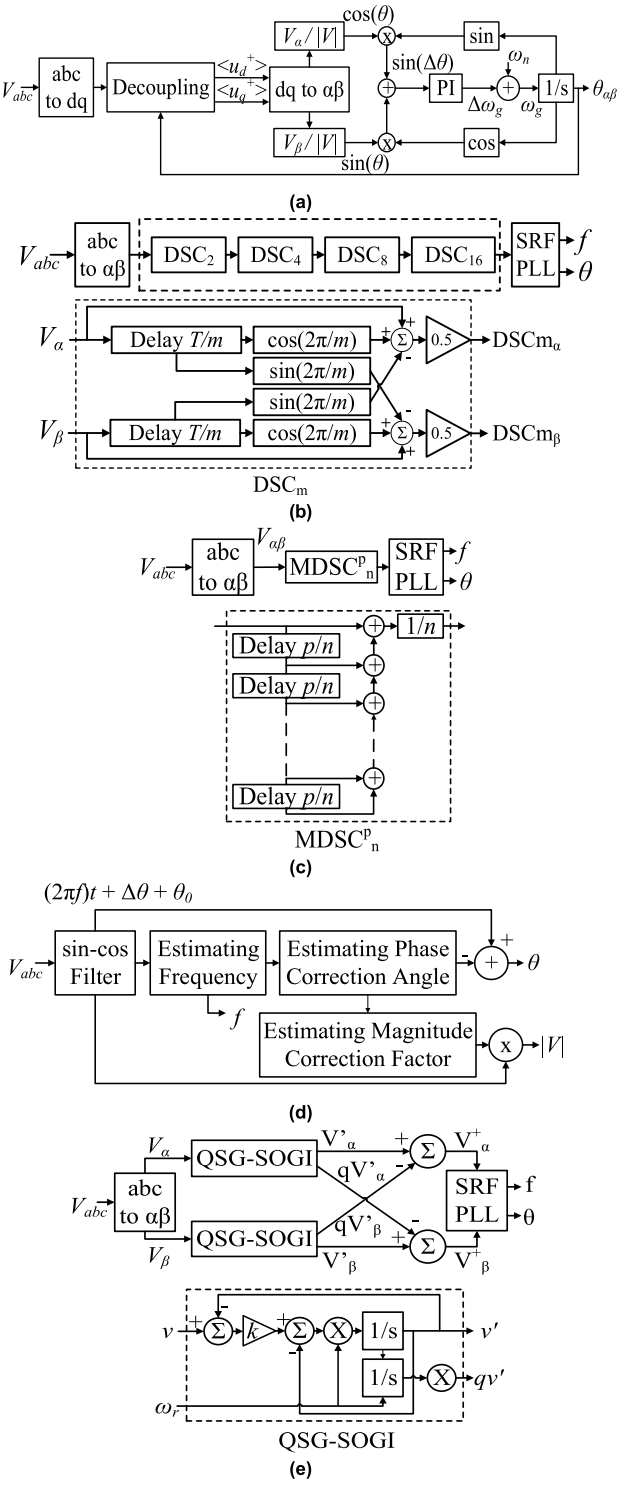

FIGURE 16. PLL algorithms implemented for comparison: (a) dαβPLL; (b) CDSC-PLL; (c) MDSC-PLL; (d) SFT-PLL; (e) DSOGI-PLL.

IV. COMPARATIVE ANALYSIS

To verify the accuracy and time efficiency of the modified MAF-PLL proposed in this paper, we implemented six other popular PLL algorithms and compared their accuracy and

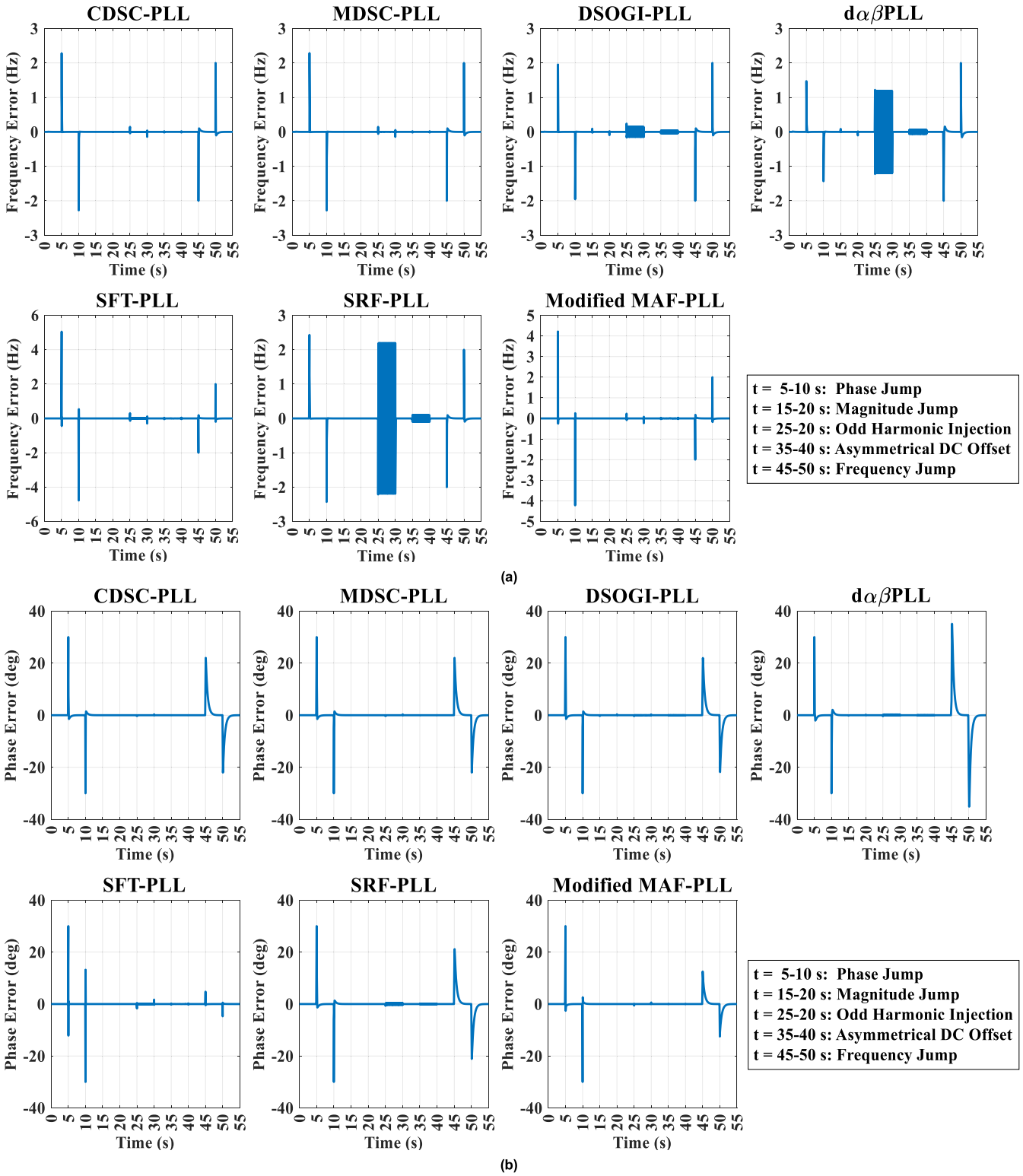

FIGURE 17. (a) Frequency and (b) phase angle errors for seven PLL algorithms. Five contingency events are applied according to the following sequence: phase jump at t = 5-10 s, voltage swell at t = 15-20 s, harmonic injection at t = 25-30 s, asymmetrical DC offset at t = 35-40 s, and frequency jump at t = 45-50 s.

runtime for the simulated abnormal grid conditions presented in Section III. The algorithms implemented for comparative analysis are listed here:

- SRF-PLL
- dαβPLL
- CDSC-PLL

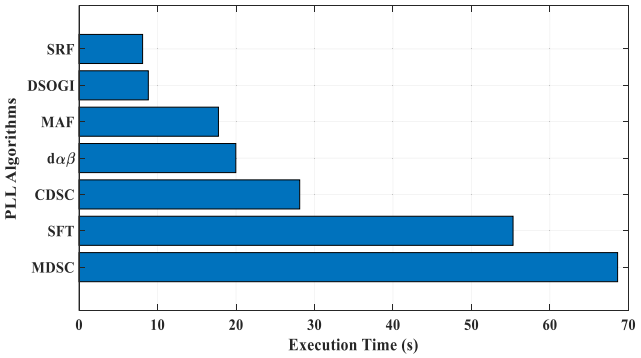

FIGURE 18. The execution time of seven PLL algorithms for the 55-second scenarios simulated in Figure 17.

- MDSC-PLL
- SFT-PLL
- DSOGI-PLL

Block diagram of SRF-PLL was shown previously in Figure 1. The block diagrams for the five other algorithms are shown in Figure 16.

The d$\alpha\beta$-PLL method, shown in Figure 16 (a), is based on decoupling the positive and negative voltage sequences and estimating the phase angle. This PLL has the advantage of a lower frequency overshoot and accurate estimation under unbalanced operation [39]. The CDSC-PLL, shown in Figure 16 (b), uses DSC operators as a preprocessing filter to eliminate the lower-order harmonics [40]. The MDSC-PLL, shown in Figure 16 (c), is an enhancement to CDSC-PLL that can provide more flexibility to configure the lowest undesired harmonics [18], [41]. The Sliding Fourier Transform (SFT) method, shown in Figure 16 (d), is a recursive algorithm based on discrete Fourier transform that can be used for phase angle estimation, providing a high degree of immunity against harmonics [25], [42]. The DSOGI-PLL, shown in Figure 16 (e), uses two quadrature signal generators (QSG) to extract the filtered direct and quadrature voltages as inputs for the SRF-PLL [43].

Five contingencies introduced in Section III were modelled in MATLAB/SIMULINK and applied to a three-phase system to analyze the effectiveness of different PLL algorithms for each event. Figure 17 (a) and (b) show the frequency and phase angle errors for each PLL when five events are applied according to the following sequence: phase jump at t = 5-10 s, voltage swell at t = 15-20 s, harmonic injection at t = 25-30 s, asymmetrical DC offset at t = 35-40 s and frequency jump at t = 45-50 s. A recovery time of 5 s was applied after each event. PI controller values for each method were kept the same since the purpose of this comparison was to analyze the stability of the algorithms as opposed to the overshoot and settling time values. The simulation started when the three-phase system was at steady state.

As seen in Figure 17 (a), for the harmonic injection event, SRF, d$\alpha\beta$, and DSOGI PLLs showed an oscillatory erroneous performance. For the SRF and d$\alpha\beta$ PLLs, these ripples affected the phase angle output as well. In the DC offset event, SRF, d$\alpha\beta$, and DSOGI showed an erroneous and unacceptable performance with high ripples at the fundamental nominal frequency. For the phase, magnitude, and frequency jump events all the methods showed an acceptable response. In this comparison, we did not focus on the overshoot and settling time values as they can be improved by fine tuning the PI controller parameters as previously demonstrated in Figure 13. Based on these simulations, CDSC, MDSC, SFT, and MAF methods showed stable response to all five contingencies.

To analyze the computational complexity of each PLL algorithm, the execution time of each PLL block was calculated using the Simulink profiler. This model advisor option can provide an insight into the time efficiency of each method. The execution time of each block for a 55-second simulation is compared in Figure 18.

The horizontal bar plot in Figure 18 shows that among the four methods with stable and accurate contingency response (i.e., CDSC, MDSC, SFT, and MAF), MAF has the fastest response. This verifies the low computational burden of this method as well as its immunity toward abnormal grid conditions.

This work can be further expanded to reduce the window width of the MAF and adjust the delay time adaptively in real-time for different abnormal grid conditions based on the calculated average voltage values. Non-linear control algorithms such as extremum seeking [44] can be utilized to find the smallest MAF's time window that can provide dampened transient response in both ideal and non-ideal grid conditions.

V. CONCLUSION

This paper first provides a review of using MAF in PLL applications and compares the DC-offset rejection capability for different MAF window widths. MAF with full-cycle window width provides DC-offset rejection at the cost of slower response time. Applying original MAF-PLL with the half-cycle window width results in oscillatory behaviour if subjected to three-phase voltages with asymmetrical DC offset values. In this work, we enhanced the performance of the three-phase MAF-PLL structure platform by concurrent reduction of the MAF's time window to half cycle and addition of a delay operator. Reduction of the MAF's window width to half cycle cuts down its execution time by approximately 50%. This improvement adds minimal computational burden to the PLL block while significantly damping the oscillations caused by DC offset and odd harmonics. Performance of this algorithm under distorted voltage signals was tested successfully using a real-time simulator. The accuracy and speed of the implemented modified MAF-PLL were also compared with six popular PLL algorithms for adverse grid conditions. The implemented PLL showed stable and accurate performance at lower execution time. It was demonstrated that the transient response of the PLL can be further improved by fine tuning the PI controller parameters.

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