IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 9 September 2023, accepted 30 September 2023, date of publication 4 October 2023, date of current version 10 October 2023.

*Digital Object Identifier 10.1109/ACCESS.2023.3321858*

RESEARCH ARTICLE

# Gate Grounded Trench I-MOS as an ESD Clamp for Sub-2V Applications

**AVINASH LAHGERE, (Member, IEEE), AND DHRUV SHIKHAR GUPTA**
Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India

Corresponding author: Avinash Lahgere (alahgere@iitk.ac.in)

This work was supported in part by the Indian Institute of Technology Kanpur under Grant IITK/EE/2022047, and in part by the Department of Science and Technology-Science and Engineering Research Board (DST-SERB) under Grant EEQ/2022/000023.

**ABSTRACT** In this paper, using calibrated 2-D simulations we have reported a new gate grounded trench impact ionization MOS (GGTIMOS) electrostatic discharge (ESD) protection device for sub-2V operating voltage applications. The proposed GGTIMOS ESD device exhibits ∼3x, and ∼1.75x reduction in the trigger voltage in comparison to the traditional GGIMOS, and GGNMOS, respectively. The proposed GGTIMOS ESD device also exhibits a hold voltage of ∼2.2 V, which is ∼2x higher than the recently published $\pi$-SCR ESD device, hence, the proposed GGTIMOS is a suitable ESD device for the sub-2V operating voltage applications. Moreover, for the 2 kV human body model (HBM) the proposed GGTIMOS ESD device requires ∼28% less device width than its counterpart GGIMOS ESD device, which makes it more area efficient. In addition, through 2 kV HBM simulation, we have shown that the GGTIMOS ESD device eliminates ESD stress ∼1 $\mu$s and the maximum temperature reached during the event is approximately 750 K which is well within the failure limits. Therefore, the results demonstrated in this paper can pave the way for future ESD design for the technology nodes where the maximum voltage handling capacity of the input/output (I/O) driver is in the range of 1.2 V to 1.8 V.

**INDEX TERMS** Electrostatic discharge (ESD), impact ionization MOS (I-MOS), GGNMOS, trigger voltage, human body model, impact ionization.

## I. INTRODUCTION

The continuous miniaturization of technology nodes has fueled innovation in the integrated circuits (ICs) industry. While the technology node scaling has enhanced the ICs performance, several reliability challenges have also emerged [1]. Among them, electrostatic discharge (ESD) is a serious threat to the IC industry as it is responsible for majorities of the total failures of ICs [2]. Thus, to insulate the ICs from ESD stress, various devices, and circuits have been reported by different researchers in the literature [3], [4], [5], [6], [7], [8]. For example, the gate grounded NMOS (GGNMOS) device [3] is highly used in the semiconductor industry as an ESD protection device because of its immunity to false triggering. Similarly, for the high voltage applications drain extended NMOS (DeNMOS) [5], and silicon-controlled rectifier (SCR) based ESD devices [7] have been investigated. In addition, researchers have also investigated steep slope devices such as tunnel FET, impact ionization MOS, etc. for the ESD design [9], [10]. For example, Sithanandam and Kumar [9] have reported a novel impact ionization MOS (IMOS) based gate grounded IMOS (GGIMOS) device for 5 V applications, whereas Kranthi and Shrivastava [10] have demonstrated the application of tunnel field effect transistor as an ESD protection device. Furthermore, it has been reported in the literature that designing ESD at lower technology nodes is very difficult due to a significant reduction in the ESD design window [11], [12]. Therefore, devices and circuits that require an operating voltage of <2 V, will need the ESD protection device with a triggering voltage of <3 V [13].

Therefore, to overcome the low trigger voltage requirement different ESD devices have been published [14], [15], [16], [17]. Among them, Chatterjee and Polgreen [14] have

The associate editor coordinating the review of this manuscript and approving it for publication was Marcelo Antonio Pavanello.

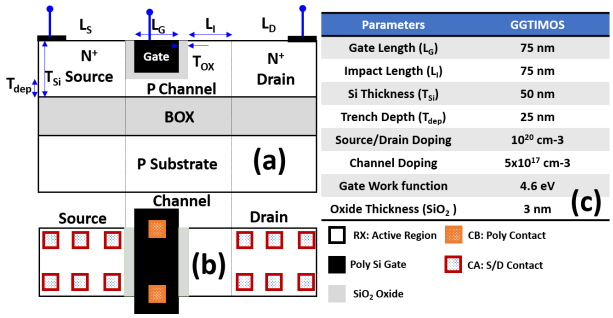


**FIGURE 1.** (a) 2-D schematic of the proposed gate grounded trench I-MOS (GGTIMOS) ESD device, (b) The layout of the proposed GGTIMOS without metallization layers and cross-section view, and (c) the proposed GGTIMOS device dimensions, and doping in the source/channel/drain regions.

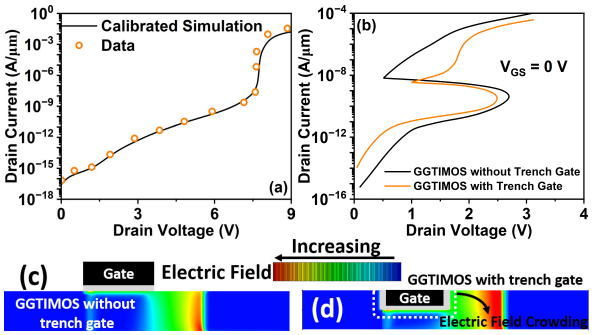


**FIGURE 2.** (a) The impact ionization model parameters calibration by reproducing the conventional IMOS output characteristics at $V_{GS} = 0$ V. (b) The output characteristics comparison of the proposed IMOS with and without trench gate at $V_{GS} = 0$ V. (c), and (d) The contour plots of the electric field at $V_{GS} = 0$ V for the proposed IMOS without and with trench gate, respectively.

reported a low voltage trigger SCR (LVTSCR) device using the integration of an NMOS device with SCR. Although the LVTSCR device exhibits good CMOS compatibility, the low holding voltage restricts its uses for lower operating voltage. To enhance the holding voltage of the LVTSCR ESD device, recently, Song et al. [15] have reported a novel LVTSCR (NLVTSCR) by embedding a gate to VDD PMOS and GGNMOS transistor in the LVTSCR ESD device. The NLVTSCR ESD device shows a holding voltage in the range of 3.44 V to 4.93 V, however, the use of an extra transistor makes it area inefficient ESD device. Similarly, Liu et al. [16] have proposed a novel voltage divider trigger SCR (VDTSCR) ESD device with a low trigger voltage of ∼2.88 V. The VDTSCR consists of two series capacitors and an NMOS transistor which are used to form a voltage divider and trigger the SCR device, respectively. Circuit techniques are also demonstrated in the literature to decrease the trigger voltage [18], [19], [20]. For example, in [18] an extra trigger circuit is incorporated to reduce trigger voltage, which would introduce complexity in the circuit and cause more area consumption. In each of the previously published ESD devices and circuits have two major challenges: (a) they need an additional device or trigger circuit for reducing the trigger voltage, and (b) they are very area inefficient.

Therefore, in this context, to mitigate the shortcomings of the previously published ESD protection devices, in this paper, we have proposed a gate grounded trench I-MOS (GGTIMOS) ESD device. Unlike the conventional IMOS ESD device, in the proposed ESD device we have doped the source, and the drain regions with a similar dopant [9]. The gate is placed near the source side, as a result, the accelerated electrons will travel to the drain without passing the channel region underneath the gate region, consequently, one can expect a lower hot carrier injection in the case of the proposed device [21]. To obtain the trigger voltage < 3 V, there are two major differences between the GGTIMOS and GGIMOS: (1) open base BJT configuration breakdown mechanism is included to trigger the avalanche mechanism at lower voltages [22], [23], [24], and (2) we have adopted a trench gate that results in crowding of the electric field near the gate edges, consequently, further cut downs the trigger voltage [25]. In addition, it is worth mentioning that GGTIMOS has been investigated for neuromorphic applications [25], however, there are no researchers that have investigated GGTIMOS for ESD clamp design. Using calibrated electro-thermal simulations, we have shown that the GGTIMOS ESD protection device shows a trigger voltage of ∼ 2.85 V, which is significantly lower than the other counterpart ESD protection devices. The proposed ESD device is targeted for operating voltage < 2 V. In addition, the proposed ESD protection device is very area efficient in comparison to the GGIMOS, as it exhibits a ∼ 29% reduction in width. Furthermore, we have also tested the proposed ESD device's suitability as a protection device using 2 kV human body model (HBM) simulations.

## II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The 2-D cross-section view of the proposed GGTIMOS ESD device is shown in the Fig. 1(a). The proposed GGTIMOS ESD device layout with the poly gate, and source/drain contacts is shown in Fig. 1(b). The channel region that has not been covered by the gate is referred to as the impact ionization region ($L_I$), which is used to modify the trigger voltage of the ESD device, hence the proposed ESD device can be adopted for the different operating voltages. The proposed GGTIMOS ESD device dimensions along with the doping in the source, the channel, and the drain regions are displayed in Fig. 1(c).

The 2-D electro-thermal TCAD simulations are adopted to demonstrate the GGTIMOS ESD device performance [26]. The bandgap narrowing (BGN), Fermi-Dirac, concentration, and field dependent models are included in the simulation setup [22], [23], [24], [25]. The band-to-band tunneling model (me.tunnel = 0.3, and mh.tunnel = 0.2), and Shockely-Read-Hall ($\tau_n = \tau_p = 100$ ns) models are also considered. The Selberherr's impact ionization model is also activated. The electron and hole impact ionization rates $\alpha_n$, and $\alpha_p$, respectively are [9]:

$$\alpha_n = \text{ANexp}\left(-\frac{\text{BN}}{\text{E}_{\text{eff,n}}}\right)$$

$$\alpha_p = \text{APexp}\left(-\frac{\text{BP}}{\text{E}_{\text{eff,p}}}\right)$$

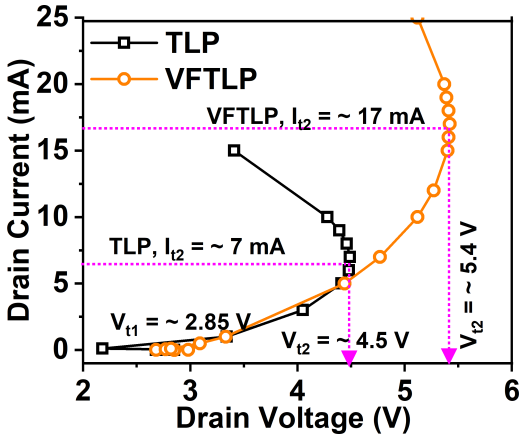


**FIGURE 3.** The transmission line pulsing (TLP) and very fast transmission line pulsing (VFTLP) characteristics of the proposed GGTIMOS ESD device. For the TLP and VFTLP extraction, the gate, and the source terminal of the GGTIMOS are connected to the ground whereas the drain terminal is connected to the input/output (I/O) pad.

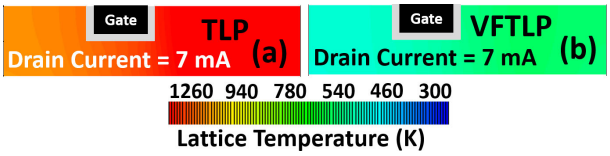


**FIGURE 4.** The contour plots of the lattice temperature or the maximum temperature of the proposed GGTIMOS ESD device: (a) TLP, and (b) VFTLP at drain current of 7 mA. It is clearly evident that for the slower transient operation the self-heating is more pronounced than the faster transient operation.

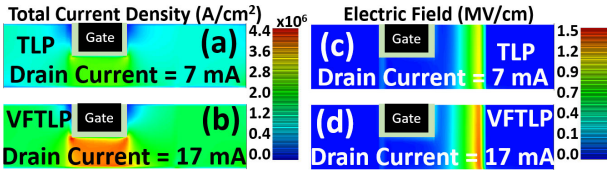


**FIGURE 5.** The proposed GGTIMOS ESD device contour plots of the total current density, and electric field: (a) & (c) TLP, and (b) & (d) VFTLP at failure current of 7 mA, and 17 mA, respectively.

where AN = 3.8 × $10^6$/cm, AP = 2.25 × $10^7$/cm, and BN = 1.23 × $10^6$ V/cm, BP = 1.69 × $10^6$ V/cm. The impact ionization parameters are calibrated by recreating the previously published results [24], as shown in Fig. 2(a). The thermal model i.e. Lat.Temp, and energy balance transport models i.e. HCTE are also incorporated into the simulation setup [9]. For the thermal simulation, the heat sink has been placed 5 $\mu$m below the BOX in the substrate, which is similar to [9]. This is because the thermal diffusion length for a 100 ns TLP is 3.3 $\mu$m. To cover the worst-case self-heating, the heat sink contact at the source, the drain, and the gate have not considered in the simulation test bench. The transient simulations based on ESDA specifications are used to extract the proposed ESD device transmission line pulsing (TLP), and very fast transmission line pulsing (VFTLP) characteristics [27], [28].

## III. RESULTS AND DISCUSSION

### A. OUTPUT CHARACTERISTICS

The output characteristics of the proposed IMOS are shown in Fig. 2(b). It can be seen that in comparison to the conventional IMOS (Fig. 2(a)), the proposed IMOS (Fig. 2(b)) exhibits a lower breakdown voltage. This happens due to the presence of the internal current gain mechanism [21]. In other words, with $V_{GS}$ = 0 V, the proposed IMOS device can be considered to be an open-base BJT with an internal positive feedback mechanism that triggers the avalanche process at a lower voltage than conventional IMOS [25]. Furthermore, to understand the need for the trench gate, we have compared the output characteristics of the proposed IMOS with and without the trench gate at $V_{GS}$ = 0 V (Fig. 2(b)). For a fair comparison, we have kept the other device dimensions the same. Although both the device configurations use the open base BJT configuration breakdown mechanism, due to the trench gate, the proposed IMOS with the trench gate demonstrates a ~1.2x reduction in the breakdown voltage as compared to the IMOS without the trench gate. This happens due to crowding of the electric field near the gate edges (Fig. 2(c), and (d)), which is similar to the past reported paper [25]. The higher electric field causes a higher impact ionization (II) rate, hence, a lower DC breakdown voltage. Furthermore, the electric field for the GGTIMOS with the trench gate is ~1.67x higher than the GGTIMOS without the trench gate.

### B. TLP AND VFTLP CHARACTERISTICS OF GGTIMOS

The GGTIMOS ESD behavior is simulated through the transmission line pulsing (TLP) and very fast transmission line pulsing (VFTLP) simulations. The transient TLP and VFTLP simulations are performed based on the ESDA specifications [27], [28]. For the TLP simulations, the current pulse of rise time ($t_{rise}$) of 10 ns and pulse width ($t_{width}$) of 100 ns has been used, whereas for the VFTLP simulation, the $t_{rise}$ of 200 ps and $t_{width}$ of 10 ns has been used. To calculate the average voltage, we have considered the drain voltage in the 30%-90% of the pulse width interval and averaged out those values [9].

The averaged values of the voltages are used to extract the proposed GGTIMOS ESD device TLP and VFTLP characteristics, as shown in Fig 3. We can observe that for the TLP and VFTLP characteristics the trigger voltage ($V_{t1}$) is <3 V, which is ~3x lower than the past reported GGIMOS ESD device [9]. This happens due to two major reasons: (1) the proposed ESD device uses the open base BJT configuration breakdown mechanism, which triggers the avalanche mechanism at lower drain voltage due to the presence of the positive feedback [21], and (2) the use trench gate allows crowding of the electric near the gate edges, which further lower the trigger voltage [25]. In addition, the hold voltage during the TLP and VFTLP operation is also > 2 V, therefore, the proposed GGTIMOS will be a suitable ESD device for the sub-2 V voltage applications.

Furthermore, after the hold voltage, the current starts rising up to the failure current ($I_{t2}$). The $I_{t2}$ is the point of thermal

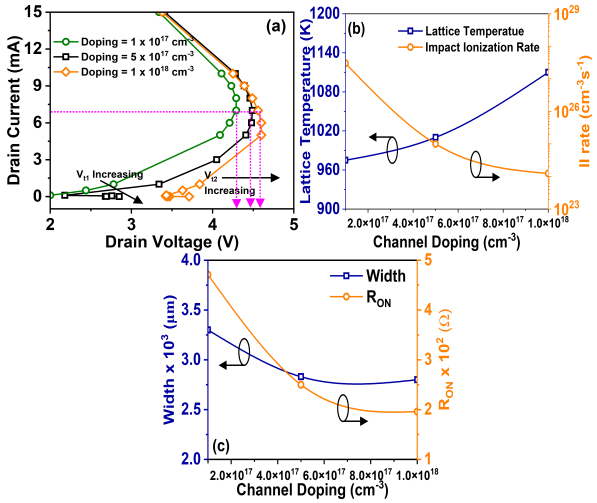


**FIGURE 6.** (a) The TLP characteristics of the proposed GGTIMOS at different channel dopings, (b) the variation in the lattice temperature, and the impact ionization rate vs channel doping, and (c) extracted device width using 2 kV HBM $I_{peak}$, and On-state resistance vs channel doping.

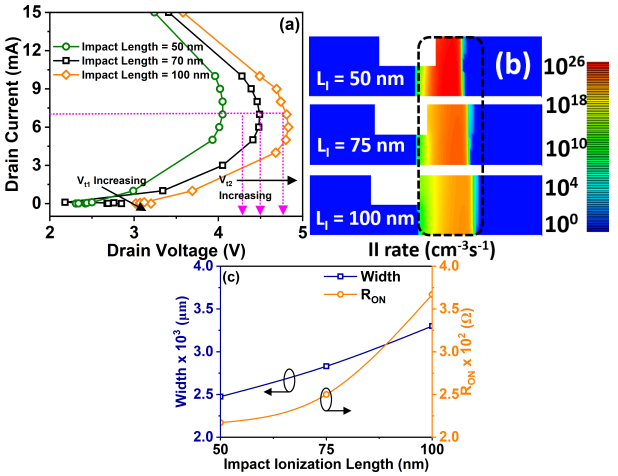


**FIGURE 7.** (a) The TLP characteristics of the proposed GGTIMOS at different impact ionization lengths, (b) the II rate contour plots at different impact ionization lengths, and (c) extracted device width using 2 kV HBM $I_{peak}$, and On-state resistance vs impact ionization length.

breakdown of the device, which is the point at which we observed the second snapback [9]. Owing to the slower transient, the $I_{t2}$ for the TLP characteristics is ∼59% less than that of the VFTLP characteristics. The slower transient results in a higher impact ionization rate, hence, the ESD device during TLP operation shows an early thermal breakdown in comparison to the VFTLP operation (Fig. 3). Also, due to the higher II rate, the maximum device temperature during the TLP operation is significantly higher than the VFTLP operation, as shown in Fig. 4(a), and (b). It can be seen that during TLP operation at $I_{t2} = 7$ mA, the GGTIMOS ESD device maximum temperature is ∼1010 K, which is ∼1.8x higher than the VFTLP operation. The reduced self-heating in the case of the VFTLP also results in a steeper characteristic, which implies an improved ON-state resistance ($R_{ON}$) (Fig. 3). The ON-state resistance during the VFTLP operation is ∼37% less than the TLP. Furthermore, the failure current per unit width for the TLP and VFTLP characteristics is ∼0.46 mA/$\mu$m, and ∼1.13 mA/$\mu$m, respectively. The contours plots for the total current density and the electric field at the failure points for both TLP and VFTLP characteristics can be seen in Fig. 5. One can see that for the VFTLP operation, the total current density (∼2x) and the electric field (∼1.3x) are much higher than the TLP operation.

Further, for a 2 kV human body model (HBM) having an $I_{peak}$ of 1.32 A [28], we can calculate the width of the GGTIMOS to be around ∼2870 $\mu$m. The width of the proposed GGTIMOS ESD device is ∼ 28% less than the past published GGIMOS ESD device [9] and hence, the proposed ESD device is more area efficient.

### C. IMPACT OF CHANNEL DOPING VARIATION ON GGTIMOS TLP CHARACTERISTICS

With technology node advancement, the number of dopants in the channel region is significantly reduced. As a result, fluctuation in channel doping can significantly affect the device's performance. Therefore, it will be worthy to evaluate the impact of channel doping on the proposed GGTIMOS ESD device performance. Therefore, in Fig. 6(a) we have simulated the impact of the channel doping on the proposed ESD device TLP characteristics. We can observe that increasing the channel doping causes an increment in the trigger voltage. The increment in trigger voltage is due to the reduction in the impact ionization (II) rate, as displayed in Fig. 6(b). When the channel doping is varied from $10^{17}$ cm$^{-3}$ to $10^{18}$ cm$^{-3}$, the II rate is reduced by ∼$10^3$x. While a lower channel doping can reduce the trigger/hold voltage of the GGTIMOS further, but completely depleted channel could lead to a very small trigger/hold voltage, which can restrict the use of the device for sub-2V voltage applications. Furthermore, due to a higher II rate at lower channel doping, the GGTIMOS ESD device exhibits an early thermal failure, as a result, at lower channel doping the device width increases (Fig. 6(c)). In addition, increasing the channel doping also causes ∼59% improvement in the $R_{ON}$. This happens due to a rise in the failure current with an increase in channel doping. Moreover, for the channel doping of $10^{18}$ cm$^{-3}$, the proposed ESD device $V_{t1}$ is >3 V, therefore, it may restrict the use of the GGTIMOS ESD device for operating voltage <2 V. Therefore, there is a tradeoff between the $V_{t1}$ and $R_{ON}$.

### D. IMPACT OF IMPACT IONIZATION LENGTH SCALING ON GGTIMOS TLP CHARACTERISTICS

In [21], [22], [23], and [24] the authors have demonstrated that varying the impact ionization length can significantly impact the device breakdown characteristics. Therefore, in this sub-section, we have also evaluated the impact of the impact ionization length on the proposed GGTIMOS ESD characteristics. In Fig. 7(a), we have simulated the impact of impact ionization length on the proposed ESD device TLP characteristics. One can deduce that scaling the $L_I$ results in

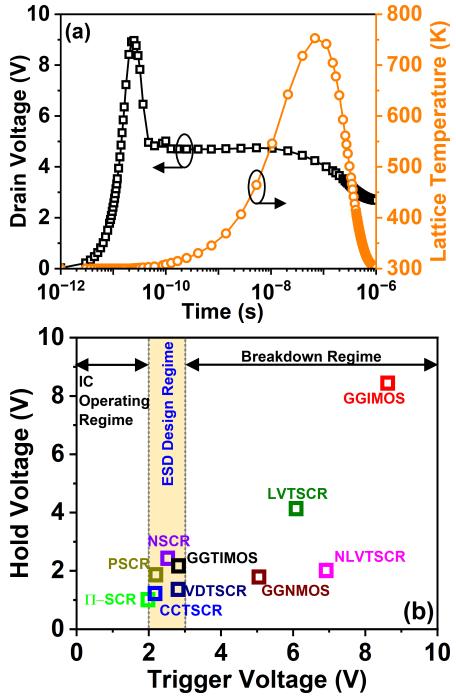


**FIGURE 8.** (a) 2 kV human body model response of the proposed GGTIMOS. It is clearly evident that the proposed GGTIMOS ESD device releases the ESD stress in few microseconds. (b) The benchmarking of the proposed GGTIMOS ESD device trigger voltage, and the hold voltage against the past published GGIMOS [9], GGNMSO [9], LVTSCR [14], NVLVTSCR [15], VDTSCR [16], $\pi$-SCR [17], PSCR [18], NSCR [18], and CCTSCR [20].

an enhanced electric field in the impact ionization region, consequently, the impact ionization rate increases (Fig. 7(b)), hence, the trigger voltage reduces. As the impact ionization length scales from 100 nm to 50 nm, the trigger voltage reduces ∼1.32x. Also, scaling the impact ionization length from 100 nm to 50 nm, improves the ON-state resistance (∼28%), and device width (∼0.8x), as shown in Fig. 7(c). Therefore, a small impact ionization length is suitable for the area improvement, but, a very small impact ionization length could lead to a trigger/hold voltage <2 V, which may hinder the use of the proposed ESD device for application voltage <2 V.

### E. 2 KV HUMAN BODY MODEL RESPONSE OF GGTIMOS

The human body model (HBM) is most dominantly used in the semiconductor industry for qualifying the ESD clamping device. In this paper, therefore, to qualify the proposed GGTIMOS ESD device we have used a 2 kV HBM response to simulate the ESD event where the discharge occurs by the human body. For a 2 kV HBM having an $I_{peak}$ of 1.32 A [29], we can calculate the width of the GGTIMOS to be around ∼2870 $\mu$m. The proposed device width is higher, which indicates the proposed ESD device robustness needs to be improved in the future. The proposed device's robustness can be further enhanced by increasing the failure current of the proposed device. This can be obtained either by using a high thermal conductivity material [30] or using silicide blocking [31]. The 2 kV HBM response for a 1.32A $I_{peak}$ of the GGTIMOS can be seen in Fig. 8(a). One can see that the clamp voltage is the same as the $V_{T1}$. The proposed device eliminates the ESD stress in ∼1 $\mu$s and the maximum temperature reached during the event is ∼750 K which is well within the limits of the actual melting point of Silicon (∼1687 K). In addition, the turn-on time of the device can predict whether the proposed device has CDM capability or not [9]. The turn-on time of the device is defined as the time taken for the oscillation to settle down. The turn-on time of the proposed device is ∼180 ps, which is well within the CDM standards, therefore, the proposed device is suitable for the CDM standards.

### F. BENCHMARKING OF GGTIMOS

In Fig. 8(b), we benchmarked the trigger voltage and the hold voltage of the proposed GGTIMOS ESD device with the previously published papers. One can see that the proposed GGTIMOS ESD device offers a better solution for ESD applications for operating voltage <2 V than the other traditional ESD devices. It can be seen that the trigger voltage of the GGTIMOS is ∼3x, and ∼1.75x less than the GGIMOS [9], and GGNMOS [9], respectively. This is highly beneficial as a reduced breakdown voltage would ensure that in an ESD event, the device is triggered early and thus, minimizing damage. Although the $\pi$-SCR [17] device shows ∼1.4x reduction in the trigger voltage in comparison to the GGTIMOS, the hold voltage of the $\pi$-SCR ESD device is <1.2 V, which restricts its application for the 1.2 V to 1.8 V applications. Moreover, it will be worth mentioning that while the other past reported PSCR [18], and NSCR [18] ESD devices based on the 28 nm High-k metal gate CMOS process demonstrate a hold voltage >2 V, and the trigger voltage <3 V, they require extra gates to cut down the trigger voltage, hence, make them area inefficient. Also, the trigger voltage of the proposed GGTIMOS can be modified according to the requirements by varying the impact ionization length determined by designers and hence the proposed GGTIMOS ESD device is technology independent.

## IV. CONCLUSION

In this paper, we have reported a new gate grounded trench I-MOS (GGTIMOS) ESD protection device for sub-2 V applications. Through calibrated 2-D simulations we have demonstrated that the GGTIMOS trigger voltage is ∼3x, and 1.75x less than the GGIMOS, and GGNMOS, respectively. Also, the proposed GGTIMOS ESD device suitability for I/O applications is demonstrated using the human body model (HBM). The proposed GGTIMOS ESD device shows significant a reduction in trigger voltage in comparison to the previously published ESD protection devices. In addition, the proposed ESD device exhibits significant area improvement as it requires ∼28% less width than the past reported GGIMOS ESD device. Although the proposed ESD shows improvement in the trigger voltage and the area, this will need experimental demonstration in the future.

## REFERENCES


[1] C. Hu, "Future CMOS scaling and reliability," *Proc. IEEE*, vol. 81, no. 5, pp. 682–689, May 1993, doi: 10.1109/5.220900.

[2] Z. Pan, C. Li, W. Hao, X. Li, and A. Wang, "ESD protection designs: Topical overview and perspective," *IEEE Trans. Device Mater. Rel.*, vol. 22, no. 3, pp. 356–370, Sep. 2022, doi: 10.1109/TDMR.2022.3178420.

[3] W.-C. Chen, S.-H. Chen, T. Chiarella, G. Hellings, D. Linten, and G. Groeseneken, "ESD nMOSFETs in advanced bulk FinFET technology with dual S/D epitaxy," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5357–5362, Sep. 2022, doi: 10.1109/TED.2022.3190822.

[4] Y. Wang, G. Lu, and Y. Wang, "A new behavioral model of gate-grounded NMOS for simulating snapback characteristics," *IEEE Access*, vol. 8, pp. 64730–64738, 2020, doi: 10.1109/ACCESS.2020.2972042.

[5] N. K. Kranthi, J. D. Sarro, R. Sankaralingam, G. Boselli, and M. Shrivastava, "System-level IEC ESD failures in high-voltage DeNMOS-SCR: Physical insights and design guidelines," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4242–4250, Sep. 2021, doi: 10.1109/TED.2021.3100810.

[6] M. Elghazali, M. Sachdev, and A. Opal, "An nMOS static ESD power supply clamp with thyristor delay element and 180 pA leakage in 65 nm CMOS technology," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 1, pp. 97–104, Mar. 2018, doi: 10.1109/TDMR.2018.2802378.

[7] H. Liang, Q. Xu, L. Zhu, X. Gu, G. Sun, F. Lin, S. Zhang, K. Xiao, and Z. Yu, "Design of a gate diode triggered SCR for dual-direction high-voltage ESD protection," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 163–166, Feb. 2019, doi: 10.1109/LED.2018.2890105.

[8] Z. Shen, Y. Wang, X. Zhang, and Y. Wang, "Area-efficient power-rail ESD clamp circuit with false-trigger immunity in 28 nm CMOS process," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 876–884, 2022, doi: 10.1109/JEDS.2022.3199421.

[9] R. Sithanandam and M. J. Kumar, "A novel cascade-free 5-V ESD clamp using I-MOS: Proposal and analysis," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 2, pp. 200–207, Jun. 2016, doi: 10.1109/TDMR.2016.2557360.

[10] N. K. Kranthi and M. Shrivastava, "ESD behavior of tunnel FET devices," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 28–36, Jan. 2017, doi: 10.1109/TED.2016.2630079.

[11] C. Duvvury, "Paradigm shift in ESD qualification," in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2008, pp. 1–2, doi: 10.1109/RELPHY.2008.4558855.

[12] Y. Solaro, P. Fonteneau, C.-A. Legrand, D. Marin-Cudraz, J. Passieux, P. Guyader, L.-R. Clement, C. Fenouillet-Beranger, P. Ferrari, and S. Cristoloveanu, "Innovative ESD protections for UTBB FD-SOI technology," in *IEDM Tech. Dig.*, Dec. 2013, pp. 7.3.1–7.3.4, doi: 10.1109/IEDM.2013.6724580.

[13] *Deep Sub-Micron Processes 130 nm, 65 nm, 40 nm CMOS*, CMP Annual Users Meeting, ST Microelectronics, Geneva, Switzerland, Jan. 2011.

[14] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," in *Dig. Tech. Papers. Symp. VLSI Technol.*, Jun. 1990, pp. 75–76, doi: 10.1109/VLSIT.1990.111015.

[15] W. Song, F. Du, F. Hou, J. Liu, X. Huang, Z. Liu, and J. J. Liou, "Design of a novel low voltage triggered silicon controlled rectifier (SCR) for ESD applications," in *Proc. Int. EOS/ESD Symp. Design Syst. (IEDS)*, Jun. 2021, pp. 1–4, doi: 10.23919/IEDS48938.2021.9468851.

[16] J. Liu, Y. Liu, A. Han, Y. Nie, Q. Huang, and Z. Liu, "A novel voltage divider trigger SCR with low leakage current for low-voltage ESD application," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2534–2542, May 2022, doi: 10.1109/TED.2022.3162557.

[17] C. -Y. Lin and Y. -H. Lai, "$\pi$-SCR device for broadband ESD protection in low-voltage CMOS technology," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 4107–4110, Sep. 2019, doi: 10.1109/TED.2019.2926813.

[18] C. -Y. Lin, Y. -H. Wu, and M. -D. Ker, "Low-leakage and low-trigger-voltage SCR device for ESD protection in 28-nm high-$k$ metal gate CMOS process," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1387–1390, Nov. 2016, doi: 10.1109/LED.2016.2608721.

[19] C.-H. Lai, M.-H. Liu, S. Su, T.-C. Lu, and S. Pan, "A novel gate-coupled SCR ESD protection structure with high latchup immunity for high-speed I/O pad," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 328–330, May 2004, doi: 10.1109/LED.2004.826529.

[20] M. Li, S. Dong, J. J. Liou, B. Song, and Y. Han, "A novel capacitance-coupling-triggered SCR for low-voltage ESD protection applications," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1089–1091, Oct. 2010, doi: 10.1109/LED.2010.2058844.

[21] M. J. Kumar, M. Maheedhar, and P. P. Varma, "Bipolar I-MOS—An impact-ionization MOS with reduced operating voltage using the open-base BJT configuration," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4345–4348, Dec. 2015, doi: 10.1109/TED.2015.2492358.

[22] A. Lahgere and M. J. Kumar, "The charge plasma n-p-n impact ionization MOS on FDSOI technology: Proposal and analysis," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 3–7, Jan. 2017, doi: 10.1109/TED.2016.2622741.

[23] A. Lahgere and M. J. Kumar, "1-T capacitorless DRAM using bandgap-engineered silicon-germanium bipolar I-MOS," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1583–1590, Apr. 2017, doi: 10.1109/TED.2017.2669096.

[24] A. Lahgere and M. J. Kumar, "1-T capacitorless DRAM using laterally bandgap engineered Si-Si:C heterostructure bipolar I-MOS for improved sensing margin and retention time," *IEEE Trans. Nanotechnol.*, vol. 17, no. 3, pp. 543–551, May 2018, doi: 10.1109/TNANO.2018.2825394.

[25] A. Lahgere, "Design of leaky integrate and fire neuron for spiking neural networks using trench bipolar I-MOS," *IEEE Trans. Nanotechnol.*, vol. 22, pp. 260–265, 2023, doi: 10.1109/TNANO.2023.3278537.

[26] *ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, USA, 2020.

[27] *Electrostatic Discharge Sensitivity Testing—Transmission Line Pulse (TLP)—Component Level*, document ANSI/ESD STM5.5.1-2008, May 2008.

[28] *Electrostatic Discharge Sensitivity Testing—Very Fast Transmission Line Pulse (VF-TLP)—Component Level*, document ANSI/ESD SP5.5.2-2007, Nov. 2007.

[29] *Electrostatic Discharge Sensitivity Testing—Human Body Model (HBM)—Component Level*, document ANSI/ESDA/JEDEC JS-001-2012, Apr. 2012.

[30] F. Cao, C. Shan, Y. Wang, X. Luo, and C. Yu, "Reliability improvements in SOI-like MOSFET with ESD and self-heating effect," *IET Micro and Nano Lett.*, vol. 13, no. 12, pp. 1649–1652, Dec. 2018, doi: 10.1049/mnl.2018.5124.

[31] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Trans. Device Mater. Rel.*, vol. 1, no. 4, pp. 190–203, Dec. 2001, doi: 10.1109/7298.995833.


**AVINASH LAHGERE** (Member, IEEE) received the master's degree in electronics and communication from the PDPM Indian Institute of Information Technology, Jabalpur, in 2015, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology Delhi, in 2018. He is currently an Assistant Professor of electrical engineering with the Indian Institute of Technology Kanpur. He has ∼5 years of industry experience as a Device Compact Model Engineer. He has published several articles in reputed journals, such as IEEE TRANSACTIONS ON ELECTRON DEVICES and IEEE TRANSACTIONS ON NANOTECHNOLOGY. His research interests include science and technology of semiconductor devices and circuits, with a focus on advances in the von Neumann computing field, such as low-power, low-voltage, beyond-CMOS logic and memory devices, and associated materials. During his tenure at GF, he received many spotlight and appreciation awards for his outstanding work.

**DHRUV SHIKHAR GUPTA** received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Kanpur, Kanpur, in 2023. He has gained experience in domains, such as electrostatic discharge (ESD) devices and circuit designing using CMOS technology, during his time at IIT Kanpur. He is currently with Texas Instruments, India. During this time, he developed a keen interest in microelectronics and semiconductor device physics.