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RESEARCH ARTICLE

Design of Advanced Fault-Tolerant Control System for Three-Phase Matrix Converter Using Artificial Neural Networks

FAIZAN AHMAD[1], TURKI M. ALSUWIAN[2], ARSLAN AHMED AMIN[1], (Senior Member, IEEE), MUHAMMAD ADNAN[1], (Member, IEEE), AND MUHAMMAD BILAL QADIR[3]

[1]Department of Electrical Engineering, FAST National University of Computer and Emerging Sciences, Chiniot Faisalabad Campus, Chiniot, Punjab 35400, Pakistan
[2]Department of Electrical Engineering, College of Engineering, Najran University, Najran 11001, Saudi Arabia
[3]School of Engineering and Technology, National Textile University, Faisalabad 37610, Pakistan

Corresponding author: Arslan Ahmed Amin (dr.arslanamin@gmail.com)

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ABSTRACT The Matrix converters (MCs) are widely used in a large number of applications such as Aircraft, Submarines, and AC drives. In these applications, because of the many chances of occurrence of a critical fault that leads to a halt of the system, and due to the failure of power electric switches, the MC operations can be compromised and there is a fear of burning of the components caused by the whole system shutdown. Therefore, a Fault-Tolerant Control System (FTCS) is extremely necessary for the continued operations of the Three-Phase Matrix Converter (TPMC) to improve the reliability and productivity of the system under faulty conditions. In this paper, an advanced FTCS is proposed based on detection, and dual hardware redundancy for TPMC. Two types of faults are injected into the system to observe the performance of the proposed system: internal open circuit faults on switches and external short circuit faults at the load side. A Fault Detection and Isolation (FDI) unit is used to detect and isolate the faulty switches using Artificial Neural Networks (ANN), and dual hardware redundancy in the switches has been proposed for fault tolerance. In case of external fault, a load-side fault detector is implemented using ANN. The simulation results in MATLAB/Simulink environment show the accurate and stable working of TPMC under faulty conditions, and hardware-in-the-loop is implemented with STM32-Nucleo-F103RB board to verify open circuit fault results. The proposed dual redundant FTC with FDI unit offers an excellent solution for the continued performance of TPMC which ultimately enhances the reliability of the system.

INDEX TERMS Redundant switches, fault-tolerant control, fault detection, artificial neural networks, insulated gate bipolar transistor.

I. INTRODUCTION

The fault is mostly expressed as the abnormal changing of the parameters of output in a system from their actual value. Fault tolerance is known as continuing system operations when a fault occurs in a system. Due to a fault occurring in a system, the operation of the system is compromised which causes the whole system to shutdown. Fault-tolerant control (FTC) approaches are used to overcome the fault and enhance the durability and reliability of the system by preventing it from shutdowns. Articles [1] and [2] describe the details of FTC and its applications. Many critical faults occur in a system where production loss cannot be compromised such as aircraft, oil and gas, submarine, and fertilizer facilities. Redundancy is one of the most used techniques to overcome the fault which has two main types: hardware and analytical

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redundancy. In hardware redundancy, healthy components are added in parallel to the faulty components. The analytical redundancy is further categorized into three types active, passive, and hybrid. The active FTC used fault detection and isolation unit and reconfiguration module but due to high computation, it's very slow. The passive FTC does not have any detection and isolation unit, no doubt it's a very easy and fast method but fails to detect multiple faults.

The Active Fault-Tolerant Control System (AFTCS) consists of a Fault Detection and Isolation (FDI) unit and reconfiguration module. The observer-based mechanism is implemented parallel to the controller in the FDI unit which gives an estimated value of output in [3] and [4]. If the difference between the estimated values is high as compared to actual values, the AFTCS declares fault and vice versa. After detecting the fault, the next steps are to isolate the fault to give the estimated value to the controller and replace the faulty value with the estimated value. The architecture of AFTCS is very complex and large computations are required to process it but it detects multiple faults discussed extensively in the articles [5], [6], [7], [8], [9], [10]. The architecture of a Passive Fault-Tolerant Control System (PFTCS) does not require any FDI unit. Its architecture is quite simple and gives quick response because PFTCS is a robust control and easily works under uncertain conditions in paper [11]. The computation of PFTCS is much less as compared to AFTCS due to the elimination of the FDI unit. The advantages of PFTCS are easily detecting faults under non-linearity conditions but failing to detect multiple faults. In the structure of hardware redundancy, add a copy of the healthy component parallel along with the main component. If any fault occurs in the main component, the healthy component takes action and the overall system is prevented from shutdowns. It is a conventional technique where redundancy is used in hardware which enhances the reliability of the system. In Figure 1, Dual Hardware Redundancy (DHR) has been shown. The DHR system will fail if and only if both main components and redundant components are faulty otherwise the system will continue operation in normal condition.

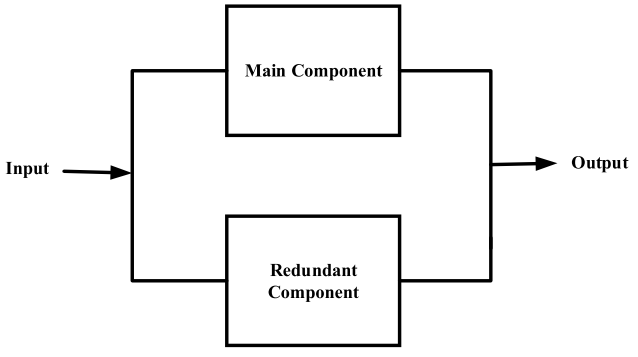

FIGURE 1. Dual hardware redundant system [1].

The FTC is needed for carry-on operations of Three-Phase Matrix Converters (TPMC) because Matrix Converters (MCs) are widely used in a large number of applications such as Aircraft, Submarines, AC drives, etc. [12]. There are a lot of advantages of MCs such as bi-directional power flow capability due to the usage of bi-directional switches, sinusoidal input and output current waveforms, removal of the reactive energy storage elements, controllable unity power factor, compact power design, and no need to use dc link capacitor. The beauty of a Matrix converter is that it can do all conversions such as Alternating Current (AC) to Direct Current (DC), DC to AC, DC to DC, and AC to AC. In this paper, the TPMC is used for three-phase AC-to-AC conversion applications. There are two ways to convert AC to AC, First, indirect conversion of AC to DC using a rectifier and dc-link capacitors then DC to AC using an inverter which has high hardware cost. The second method is the direct conversion of AC to AC using a cyclo-converter. The property of cyclo-converters is that they give variable frequency and fixed output voltage but the advantage of TPMC, it gives variable frequency in [13] and variable voltage. In the structure of TPMC, the V_{AN}, $V_{BN,}$ and V_{CN} are the input voltages, and nine bi-directional Insulated Gate Bipolar Transistors (IGBTs) switches are used to convert AC to AC as shown in Figure 2. Some conditions should be followed while controlling the switching operations. The input phase should not be short, and the output phase should not be opened. Therefore, only 27 states could be able to control switching operations, and to control the switching of switches Space Vector Modulation (SVM) is used which is extensively discussed in these articles [14], [15].

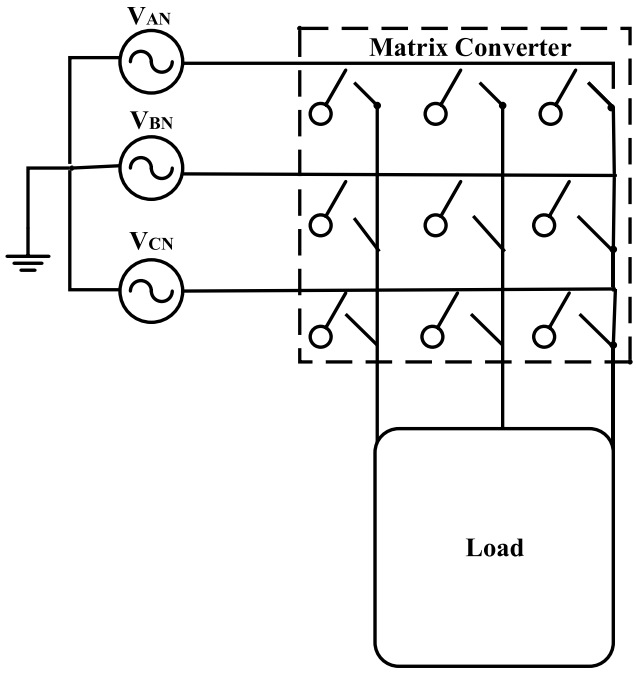

FIGURE 2. Three-Phase matrix converter structure [16].

Controlling the continuous operation of a three-phase matrix converter is always a challenge as the power electronic

switches can fail for several reasons. If a reverse current flows through the switch, it will make it faulty. Due to these faults, the Matrix Converter operation can be degraded and there is a fear of burning of the components which causes the whole system to shut down, especially on large applications like aircraft and submarines to control the speed of AC drives. Therefore, advanced FTCS is proposed in this paper based on injection, detection, and DHR systems to overcome this problem. According to existing literature, the proposed method has not been done for TPMC. The proposed method enhances the durability and productivity of the system.

A. LITERATURE REVIEW

In Paper [16], the author investigates a novel FTC motor drive system for TPMC. There are two types of FTC MCs are discussed, direct MCs and Indirect MCs, and also proposed an open circuit FD method for the continued operation of a three-phase motor drive. The main contribution of this paper is to detect faults very fast but fails to detect short-circuit faults and non-linear faults. In the paper [17], Sangshin Kwak proposed a modulation technique to overcome single-phase open and short-circuit faults. The fault is fixed by reconfiguring the parameters of MCs. The advantages of this method are to overcome hardware redundant modules and reduce the hardware cost of the system but there is a need to improve the accuracy of the system.

In the paper [18], the authors investigate the sensors and actuators faults in the non-linear system and propose a Neural Network (NN) based FTC that generates alarms under faulty conditions. The advantages of this method are not only reduced time delay in fault detection but also eliminated the requirement of FDI unit. This technique failed to detect multiple faults in sensors as well as actuators. Shen Yin proposed an adaptive NN-based FTC technique for non-linear systems in [19] and worked on a time delay system with unmodeled dynamics. The main advantage of this technique is that the controller easily deals with sensor faults, dynamic disturbance, and time delay. If the time delay in fault is very high, the system will be shut down. The author overcomes all time delay problems which was the main contribution of this paper. The drawback of this method is that due to uncertain conditions, the accuracy of the proposed method is reduced. In this paper [20], a backstepping NN-based method has been proposed for Multi-Input and Multi-Output (MIMO) systems. The main advantage of this technique is accurately worked under external disturbance and non-linearity but this approach also fails to detect multiple faults. The authors proposed an ANN controller-based method for a five-level diode-clamped converter [21] to reduce the complexity and cost of the overall system. The authors not only reduce cost but also decrease the total harmonic distortion due to uncertainties.

For fault detection, Kalman filters are mostly used for linear systems. In this method, the estimated value of faulty components is easily predicted by using time update and measurement update of residuals which are thoroughly discussed in these articles [22], [23]. This method easily detects faults and gives a more stable response for linear systems. The drawback of this technique is only used in linear systems but fails in non-linear systems. The linear parameter varying method is also used for fault detection. In [24] a discrete parameter varying method is used for both the sensor's and actuator's fault. This method gives accurate fault estimation as compared to other methods but this method is also applicable only to linear systems. The Kalman and linear parameters both are the AFTCS methods. The multiple faults are easily detected by using AFTCS but due to the high computations required to detect multiple faults, the speed is slow and in case of external noise the performance is also degraded. Therefore, robust control is required to overcome these issues which are discussed below.

The AFTCS is not used in critical situations where a single fault causes the whole system to shut down. The intelligent PFTCS is used to overcome single-point failure. In [25], a robust FTC is used to overcome critical faults. The main advantage of this method is to detect faults very fast and easily works in nonlinear conditions.

In article [26], Sliding Mode Control (SMC) is implemented for the detection of a fault in non-linear systems. This technique is more reliable and accurate due to easily dealing with non-linearity but in SMC chattering problems or high frequency of control, the signal is caused by the nonlinear switching control. Some additional components are also used which increase the cost of the system. To overcome this problem, a higher-order SMC was proposed [27]. This method gives an accurate estimated value of the faulty component and reduces the requirement for additional components but fails to detect multiple faults. Article [28], [29], and [30] authors implemented a hybrid FTC technique for air-fuel ratio control of internal combustion engines. Hybrid FTC is the combination of both AFTCS and PFTCS. The advantages of this technique are to detect and isolate fast very fast and diagnose a wide range of faults but the structure of hybrid FTC is complex and large computations are required due to multiple fault analysis [31].

In the paper [32], the authors analyzed symmetric and un-symmetric faults in power systems and artificially injected the short circuit fault into the system to check the behavior of the system under faulty conditions. They analyze many types of un-symmetric faults such as a single line-to-ground fault, double line-to-ground fault, and line-to-line fault. Due to the injection of fault, the frequency of a signal is disturbed, and the system takes some time to overcome this fault.

The advanced FTC proposed by the author in [4] improves the reliability of process plants under faulty conditions. They proposed DHR in [4] and Triple Modular Redundancy (TMR) in [33] concept to tolerate the faults in process industries. In DHR add a copy parallel to the faulty component which enhances the reliability of the system. In [33], the authors implemented TMR in the switches of H-bridge to tolerate the fault in separately excited DC motors with an FDI unit that detects and isolates fault, and to overcome the fault TMR is

used. The main advantage of this technique is to improve the durability and reliability of the system but due to hardware redundancies, the cost of the system is increased.

The paper [34] presents a state space modeling technique for matrix converter drives, which allows for a thorough understanding of the MC's system dynamics. This approach provides precise drive system modeling and analysis, improving control design and performance assessment. The limitation of this strategy was due to temperature variation the model parameters are changed. Therefore, a control system is required to handle the temperature variation. This [35] paper addresses the modeling and control aspects of a modular multilevel MC specifically designed for low-frequency AC transmission. The voltage balance method was proposed to reduce the sub-module switching frequency. The proposed system is only applicable to low-frequency transmission.

B. ARTIFICIAL NEURAL NETWORKS

Artificial Neural Networks (ANN) is a technique of artificial intelligence that is the most powerful solution for data mining. The concept of ANN is introduced by inspiring the neurons of the human brain as mentioned in [36]. The ANN models learn from experience and give accurate information as our brain neurons. Due to parallel computation in ANN, it gives a very quick response as compared to other algorithms. The architecture of ANN consists of input, hidden networks, and output networks as shown in Figure 3.

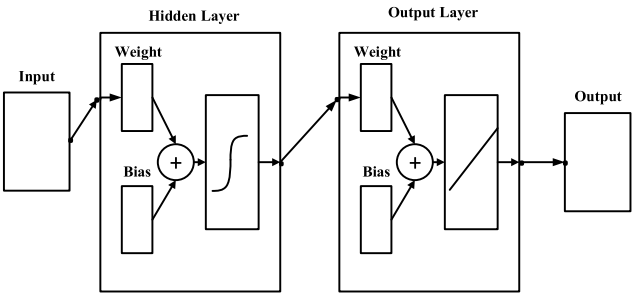

FIGURE 3. Architecture of ANN.

By increasing the hidden layers, the accuracy of the model is improved. For a large dataset, the hidden layer is also increased according to requirement. In the backup of ANN, an equation is implemented which is as follows:

$$\sum_{i=1}^{n} w_i \cdot x_i + b \tag{1}$$

Here x_i is the input feature of the neural network and w_i is the weightage and b is the bias vector component of ANN. The activation function is applied to the specific value of the input to get the accurate output.

In this paper, our contribution is the design of an advanced FTCS for TPMC based on detection, and dual hardware redundancy. Two types of faults are injected into the system to observe the performance of the proposed system: internal open circuit faults on switches and external short circuit faults at the load side. An FDI unit is used to detect and isolate the faulty switches using ANN, and DHR in the switches has been proposed for fault tolerance. In case of external fault, a load-side fault detector is implemented using ANN. The simulation results in MATLAB/Simulink environment show the accurate and stable working of TPMC under faulty conditions. The proposed work dual redundant FTC with FDI unit offers an excellent solution for the continued performance of TPMC which enhances the reliability of the system.

The remaining paper is organized in a way that section II gives the methodology of the overall system. Section III presents the results with a discussion of this paper's findings. Lastly, section IV presents the concluding remarks and future research directions.

II. RESEARCH METHODOLOGY

The above Section I-A discussed the approaches that are mostly just detecting the fault; an advanced FTC method is proposed based on Fault Injection (FI), Fault Detection (FD), and DHR. First, two types of internal open circuit faults on switches and external short circuit faults are injected artificially at the load side. In case of internal fault, a Fault Detection and Isolation (FDI) unit is used for fault detection and isolation in switches using ANN, and then overcome this fault a DHR-FTC system has been proposed to prevent the system from shutdowns which have not done in the literature of TPMC. In case of external fault, a load-side fault detector is used by using ANN. The fault-tolerant TPMC to control the switching operation is proposed in the MATLAB/Simulink environment. For external fault detection, the ANN-based load side fault detector unit is proposed which is integrated with MATLAB/Simulink TPMC.

In the model of TPMC which is used as a reference [37], bi-directional IGBT switches are used for the operations; each phase includes three IGBT switches. The benefit of bi-directional switches is the power flow in both directions source to load and load to source and the polarity of AC changes from positive to negative, therefore bi-directional switches are required for this purpose. For controlling the switching operations of IGBTs, space vector modulation is used [8]. Fixed voltage and fixed frequency are provided at the input and the TPMC gives us variable voltage and variable frequency at the output which is the main advantage of TPMC. At least one switch is turned on in one phase; otherwise, the input and output phases are open-circuited. At most one switch is turned on in one phase because if two or more switches are turned on, it will cause the short-circuited two or more phases.

The output voltage of TPMC is evaluated by using the following matrix:

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \begin{bmatrix} S_1 & S_2 & S_3 \\ S_4 & S_5 & S_6 \\ S_7 & S_8 & S_9 \end{bmatrix} \begin{bmatrix} V_{Ao} \\ V_{Bo} \\ V_{Co} \end{bmatrix} \tag{2}$$

$$V_{aN} = S_1 V_{Ao} + S_2 V_{Bo} + S_3 V_{Co} \tag{3}$$

$$V_{bN} = S_4 V_{Ao} + S_5 V_{Bo} + S_6 V_{Co} \quad (4)$$
$$V_{cN} = S_7 V_{Ao} + S_8 V_{Bo} + S_9 V_{Co} \quad (5)$$

Here V_{aN}, V_{bN}, and V_{cN} are the output voltage, V_{Ao}, V_{Bo}, and V_{Co} are the input voltages and S_1 to S_9 are the nine bi-directional switching variables of the matrix converter. Multiply the rows of S_1 to S_3 by the column of input voltages to compute $theV_{AN}$ output voltage. The same method is followed to compute V_{BN} and V_{CN}.

The output current of TPMC is evaluated by using the following matrix:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} S_1 & S_2 & S_3 \\ S_4 & S_5 & S_6 \\ S_7 & S_8 & S_9 \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad (6)$$
$$I_a = S_1 I_A + S_2 I_B + S_3 I_C \quad (7)$$
$$I_b = S_4 I_A + S_5 I_B + S_6 I_C \quad (8)$$
$$I_c = S_7 I_A + S_8 I_B + S_9 I_C \quad (9)$$

Here I_a, I_b, and I_c are the output current, I_A, I_B, and I_C are the input current and S_1 to S_9 are the nine bi-directional switches of the matrix converter. Multiply the rows of S_1 to S_3 to the column of input current to compute I_a output voltage. The same method is followed to compute I_b and I_c.

To overcome this problem, first, the short circuit fault is artificially injected in each phase and detected this fault using the ANN Algorithm. The DHR system is implemented to overcome this fault. The overall block diagram of the proposed system is shown in Figure 4. The structure of TPMC consists of nine bi-directional IGBT switches from Switch S1 to S9. In case of internal fault, the FI dashboard is used to artificially inject internal open circuit faults in switches, and the FDI unit is implemented to detect faults in switches using the ANN Algorithm. For example, if an artificially injected fault in any switch from switch S1 to S9 the FDI unit detects the fault and isolates the faulty switch, and a copy of the main switch is taken charge to avoid shutdowns, this method is known as AFTCS. In the case of an external fault, a phase short circuit fault is artificially injected through load-side fault injection. Then, detect short circuit faults at the load side using the ANN Algorithm. The proposed system not only enhances the durability but also increases efficiency and the reliability of the system.

The AFTCS modeling in state space to implement observer-based architecture is explained in [1]:

$$\dot{x} = Ax + Bu \quad (10)$$
$$y = Cx + Du \quad (11)$$
$$\dot{\bar{x}} = A\bar{x} + Bu \quad (12)$$
$$\bar{y} = C\bar{x} + Du \quad (13)$$
$$\left(\dot{\bar{x}} - \dot{x}\right) = A(\bar{x} - x) \quad (14)$$
$$(\bar{y} - y) = C\,(\bar{x} - x) \quad (15)$$
$$\dot{\bar{x}} = A\bar{x} + Bu + L\,(\bar{y} - y) \quad (16)$$

L is a feedback gain

$$\dot{\bar{x}} - \dot{x} = A\,(\bar{x} - x) + L\,(\bar{y} - y) \quad (17)$$
$$(\bar{y} - y) = C\,(\bar{x} - x) \quad (18)$$
$$\dot{\bar{x}} - \dot{x} = (A + LC)\,(\bar{x} - x) \quad (19)$$
$$\dot{e}_x = (A + LC)\,e_x \quad (20)$$
$$(\bar{y} - y) = Ce_x \quad (21)$$

No fault is detected by the FDI unit if the residual "e_x" goes to zero. If the residual becomes out of the normal threshold, an error will be detected.

The proposed FD detected external faults very fast by using the ANN algorithm due to parallel computation. The proposed method for internal fault an FDI unit is used to detect and isolate fault using ANN and to overcome this fault DHR is implemented. The DHR FTC approach increases the reliability of the overall system, DHR consists of the main actual component and the backup component. If the main actual component fails, the backup of the component takes action to continue the operation of TPMC under faulty conditions. It will eliminate critical faults that cause the whole system shutdowns. The eighteen IGBTs used in the proposed DHR with nine IGBTs acting as the main component and other nine acting as backup components. In normal operations, the main component works properly for continued operation. If any fault occurs in the main components, the backup components take action to prevent the system from shutting down. If the reliability of the DHR system is L_{dr} the reliability of Component 1 is L_1 and Component 2 is L_2 and the fail reliability is $1 - L$, then the reliability of DHR is calculated by the following equations.

$$L_{dr} = 1 - (\textit{both components are failed}) \quad (22)$$
$$\textit{If } L_1 = L_2 = L \quad (23)$$
$$L_{dr} = 1 - (1 - L)^2 \quad (24)$$
$$L_{dr} = 2L - L^2 \quad (25)$$
$$\textit{If } L = 0.9, \textit{ then } L_{dr} = 0.99 \quad (26)$$

The flowchart of the DHR FTC system has been shown in Figure 5. The system is initialized with the simulation of input parameters. The TPMC structure consists of nine bi-directional switches, if any of the nine primary switches is faulty, the fault is detected using the FDI unit then redundant switches are utilized to provide backup of faulty switches to operate the TMPC in a faulty condition. For external faults, the fault is detected by using the ANN algorithm. If no fault is detected, the TPMC is operated in normal condition.

The limitation of this method is that the system fails if and only if both the primary component and redundant component are failed. The proposed DHR FTC increases the size and cost of the hardware system. Ideally, the switches have zero resistance, when they are operated, and infinite resistance, when switches are opened, but practically the switches have some resistance in operation and little time delay with high resistance offers when they will not operate Also an FTC is required at the load side.

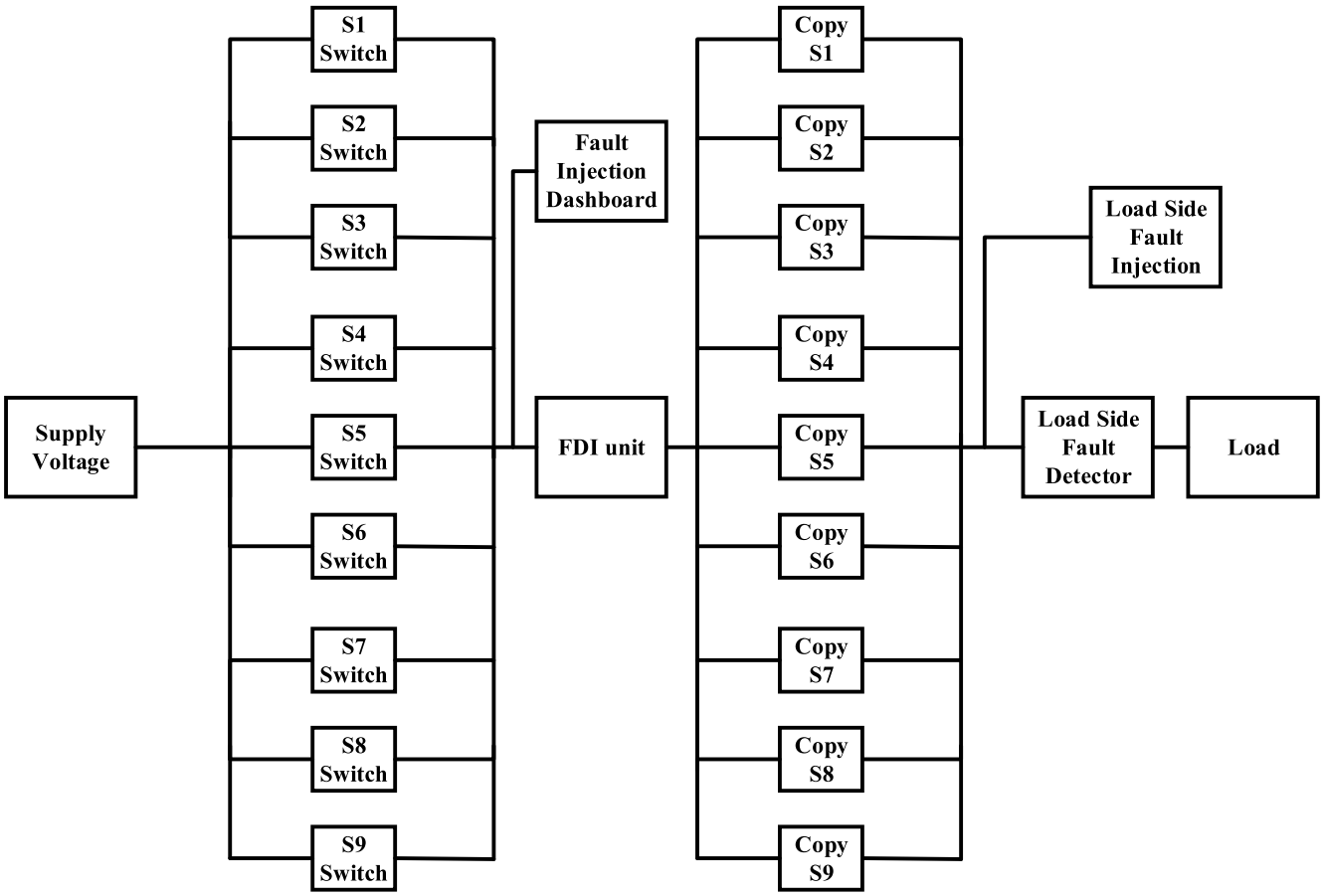

FIGURE 4. Overall proposed system block diagram.

III. RESULTS AND DISCUSSION

To control the switching operations of TPMC, a MATLAB/Simulink-based provided model is implemented in [35].

A. PARAMETERS INITIALIZATION

The fixed voltage and frequency are applied at the input and TPMC provides variable voltage and variable frequency at the output which can be controlled by space vector modulation. The supply voltage 314V peak and 50Hz frequency are supplied to each phase of TPMC and it will give us 540V peak voltage and 80Hz frequency at the output as shown in Table 1.

The switching frequency of voltage and current modulation is 6000Hz. Due to the selection of a 6000Hz switching frequency, the output is 540 Vp at 80Hz frequency. If the switching frequency of voltage and current modulation or the input voltage and frequency are changed, the output voltage and current are changed but the V/F ratio is the same. It is not necessary that the voltage and frequency should be 540Vp at 80 Hz, and the output voltage and frequency could be controlled by selecting input and switching frequency according to requirement.

TABLE 1. System inputs and outputs.

Parameters	Value
Input Phase Voltage	314 V
Input Frequency	50 Hz
Switching Frequency	6000 Hz
Output Phase Voltage	540 V
Output Frequency	80 Hz

There are nine bi-directional IGBT switches from S1 to S9 with a freewheeling diode used in the TPMC model. Each switch includes two IGBTs and two diodes to control the bi-directional power flow of switches from source to load and load to source. The IGBTs are used due to their good power-handling capabilities. The supply voltage 314V and 50Hz frequency are provided to each phase of TPMC as input for normal operation. Switch S1, S4, and S7 are connected with phase A of input, switches S2, S5 to S8 are connected with phase B of input, and switches S3, S6 to S9 are connected

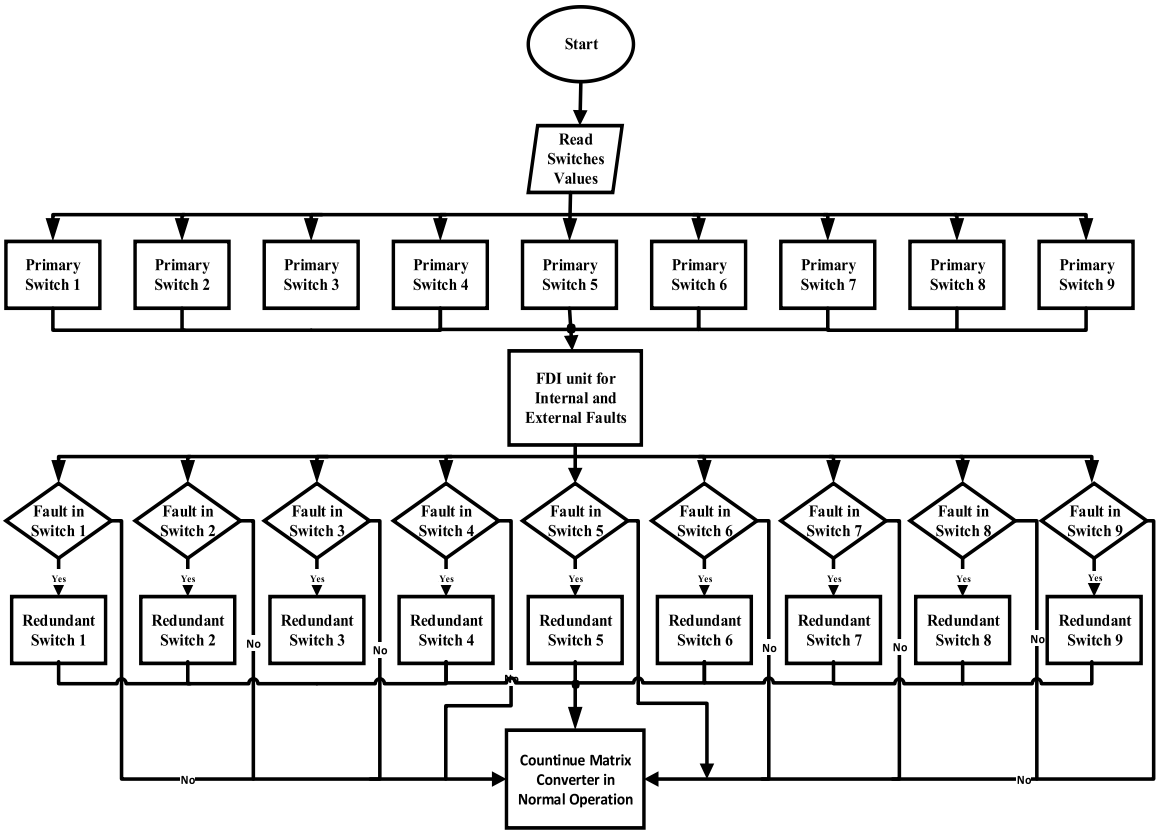

FIGURE 5. Flowchart of dual redundant fault-tolerant TPMC.

with phase C of input voltage. Switch S1 to S3 are connected with phase a of output, switch S4 to S6 are connected with phase b of output, and switch S7 to S9 are connected with phase c of output. If S1 and S2 are turned on at the same time, then phases A and B will be short-circuited, and if S2 and S3 are turned on at the same time, then phases B and C will be short-circuited same as for other switches. If switch S1 to S3 are turned off, then the output phase a will be opened. Therefore, at least one switch should be turned on for output phases to avoid an open circuit, and at most one switch should, be turned on for input phases to prevent short circuits. The gate pulse is required to turn-on for any switch which is given by the MATLAB/Simulink model. Some conditions should be fulfilled to control the switching operations such as the output phase should not be opened and the input phase should not be shorted which is controlled by space vector modulation discussed in [8].

The proposed TPMC topology with fault injection, detection, and an FTC is shown in Figure 6. In the Simulink model of the proposed TPMC, four main scopes are used for measurement. Scope 1 is used for the measurement of three-phase input voltage, scope 2 provides the single-phase input voltage, scope 3 is used to measure the three-phase output voltage, and scope 4 provides the information on the single-phase output voltage, and other scopes all used to measure voltage and current of each switch.

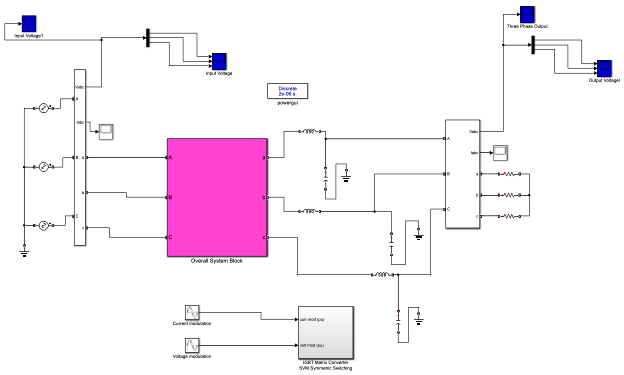

FIGURE 6. Simulink model of proposed TPMC with fault injection, detection, and FTC.

The internal structure of overall system block is shown in Figure 7.

First, three-phase input is applied, and then two three-phase VI measurement blocks are used to measure three-phase voltages and current of both the input side and output side, and a pink color block consists of the overall proposed system of TPMC. For controlling the switching operation, space vector modulation is used for both current modulation and voltage modulation. Here a three-phase resistive load is used to check

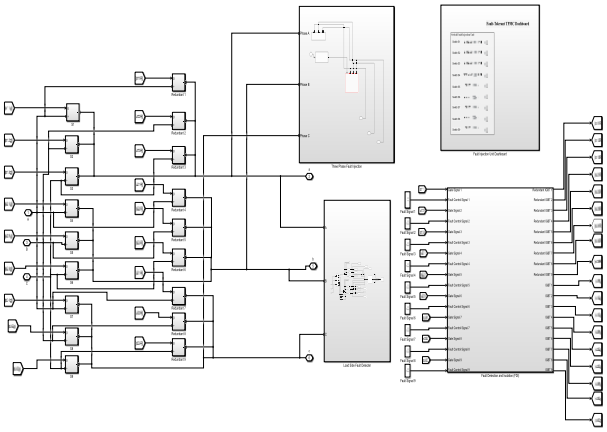

FIGURE 7. Internal structure of overall system block.

the performance of TPMC in normal and faulty conditions as shown in Figure 8.

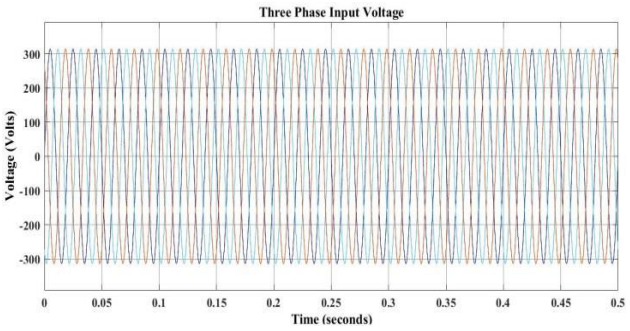

FIGURE 8. Three-phase input voltage.

The proposed fault injection, detection, and FTC have been divided into three parts. The three-phase input is applied to the system with 314V voltage and 50 Hz frequency in each.

In scope 2, every phase is displayed individually for a better understanding of the waveform as shown in Figure 9.

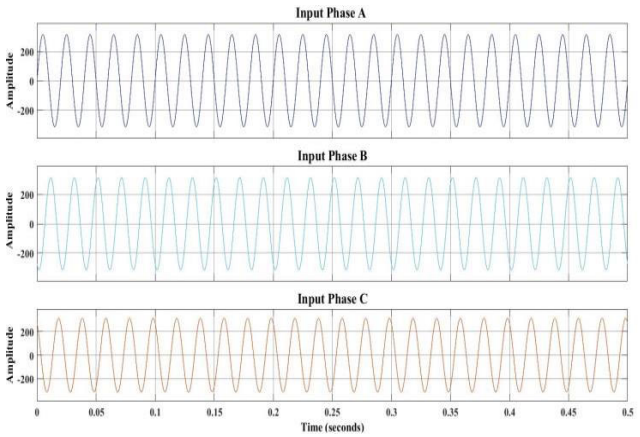

FIGURE 9. Input voltages of each phase.

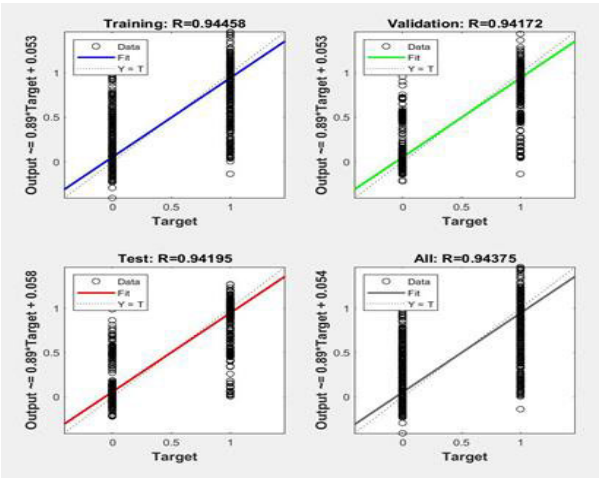

FIGURE 10. Regression plot of model.

In the structure of ANN, the Route Mean Square (RMS) value of three-phase voltage and current is used as an input. Ten hidden layers and four output layers are used for accurate results. If any disturbance occurs in phase voltages and current, the ANN works on it and declares the fault. In the dataset of a neural network, 70% of the data for the training set, 15% validation set, and 15% of the data for testing are used for this algorithm. To train the model, the Levenberg-Marquardt algorithm is used. This algorithm requires more memory but it will detect the fault in less time. The regression plot is shown in Figure 10 which indicates the network outcomes for corresponding targets. If the network is overlapped with the regression linear line then the network is trained correctly as discussed in [36], if not then more training is required. In our case, the target line is approximately overlapped with the output line, and the regression value is R=0.94, therefore, our model is trained correctly.

Figure 11 shows the gradient descent whose value is 0.0006076. The value of gradient descent indicates that the local minima after 218 iterations are 0.0006076.

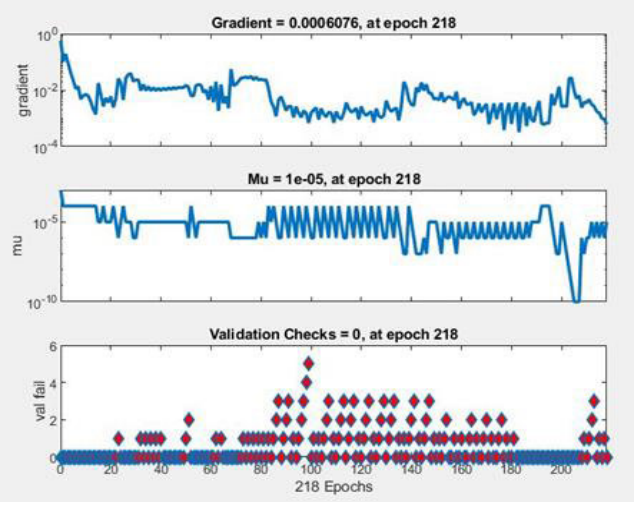

FIGURE 11. Traning performance of ANN model.

Two types of faults are injected such as external faults on the load side and internal faults on the switch side to check the behavior of TPMC under faulty conditions. For external faults, an ANN-based FD unit is implemented. In case of internal fault, the FDI unit is detected and isolates the fault, and to overcome this fault DHR is proposed which is extensively discussed below.

B. EXTERNAL FAULT

First of all, a three-phase symmetric short circuit fault is artificially injected in all phases of output at the load side by using a fault injection block as shown in Figure 12. The on-resistance is set of fault 0.001Ω and 1Ω for ground resistance and adds external switching time from 0 to 0.5 sec for fault injection to check the response of TPMC under faulty conditions.

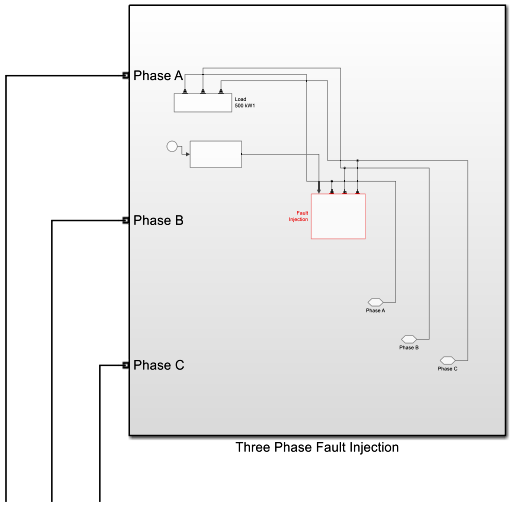

FIGURE 12. Three-Phase fault injection unit.

The short circuit fault is injected with a 500kW load in every phase of TPMC by using a fault injection block; the timing of the fault has been set from the timing block as shown in Figure 13.

In case of external fault ANN ANN-based FD unit is implemented and ANN model results are explained below. If any fault occurs in phase PA, phase PB, and phase PC, the FD unit detects the fault as shown in Figures 14 and 15. The faults are detected by using the ANN algorithm which detects faults very fast because of the parallel computation of neural networks. The route to mean square values of voltage and current of all phases are taken as an input of ANN and trained and tested the model by using 6000 sample values of the dataset and a dual switch attached to the output of ANN. The data of all phase voltages and currents are collected using the To Workspace block which generates a column vector of each value in MATLAB workspace. The fault display block is used to display the fault.

Then train the ANN model using the Levenberg-Marquardt Algorithm. Then the output is compared with a dual switch

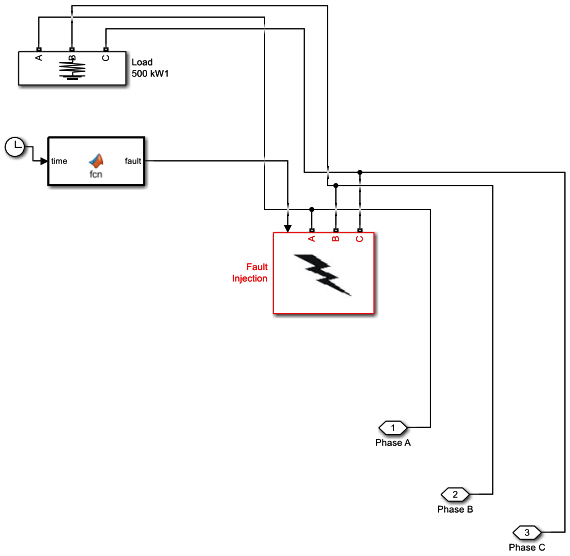

FIGURE 13. Internal structure fault injection unit.

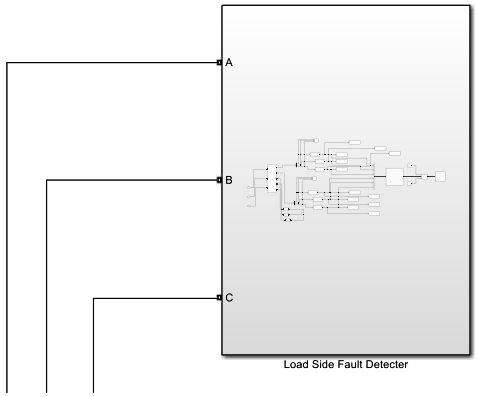

FIGURE 14. Fault detection unit.

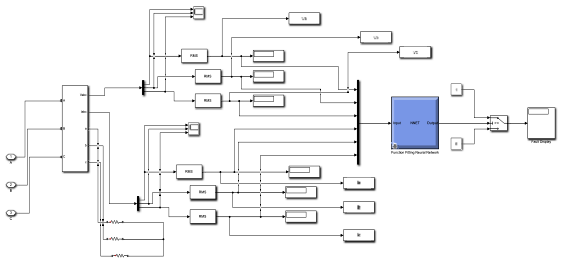

FIGURE 15. Internal structure of fault detection unit.

for pure binary conversion. The internal structure of the FD unit is shown in Figure 15.

The ANN output prediction is shown in Table 2.

The ANN algorithm receives its inputs from the RMS values of voltage and current across all phases at the load side. The model is subsequently trained and tested using a dataset made up of 6000 sample values. The To-Workspace block, which creates a column vector for each value in the MATLAB workspace is used to collect the data of voltage and current

TABLE 2. Fault type and ANN output prediction.

Fault Type	Line	ANN Output
No-Fault		0000
LLL Fault	ABC	1110
LL Fault	AB	1100
	AC	1010
	BC	0110
LG Fault	A to G	1001
	B to G	0101
	C to G	0011
LLG Fault	AB to G	1101
	AC to G	1011
	BC to G	0111
LLLG Fault	ABC to G	1111
No-Fault		0000
LLL Fault	ABC	1110

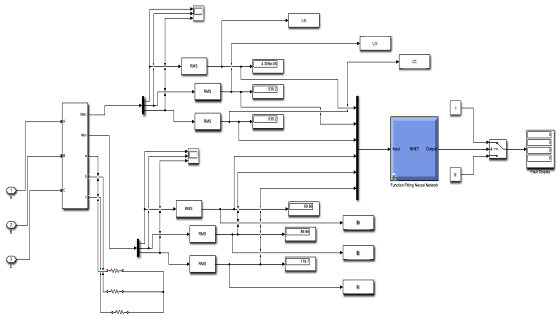

FIGURE 16. Load side fault detector output under no-fault.

for all phases. The output of the ANN is further connected to a dual switch as shown in Figure 16. The fault display block is used to show any detected fault in binary form as shown above in Table 2.

If no fault occurs in any phases, then TPMC operates in normal conditions, and 0000 is displayed at the output of the FD unit.

In the case of triple line LLL fault, it means the fault occurred in each line ABC and 1110 are displayed at the output of the FD unit as shown in Figure 17.

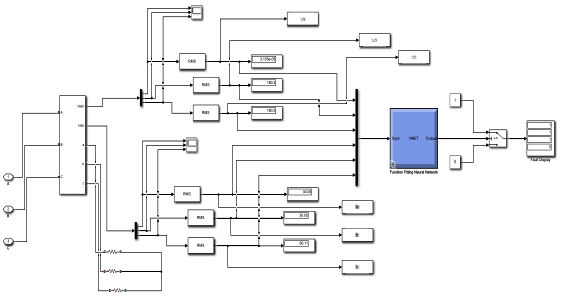

FIGURE 17. Load side fault detector output under LLL fault.

The TPMC gives variable voltage and frequency which are the main advantage of it. The output of TPMC under no-fault and LLL faults is shown in Figure 18.

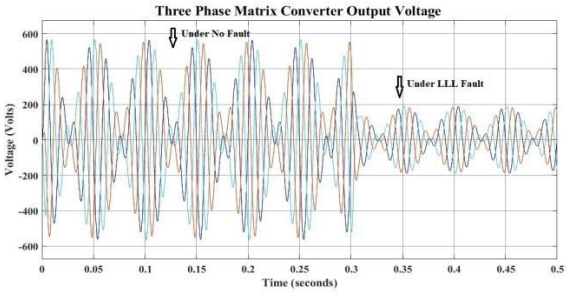

FIGURE 18. Three-phase output voltage under normal and faulty condition.

As you see after some time all three phases are disturbed. When a short circuit has occurred, the voltage of phases is reduced to its main value and the FD unit displays 0000 to 1110. In this case, the fault occurred in each phase; therefore each phase voltage is reduced to its main value.

For better visualization, the output voltages of each phase are displayed under the no-fault condition as shown in Figure 19.

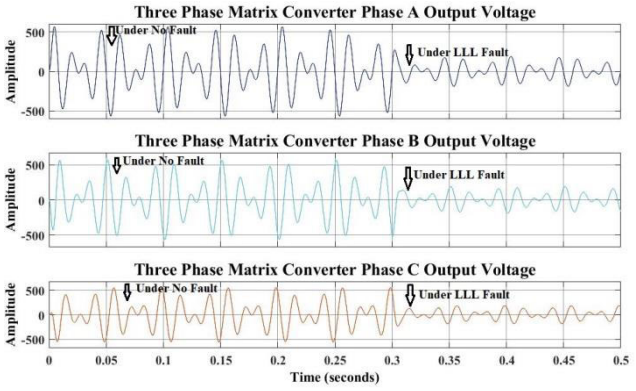

FIGURE 19. Output voltages under normal and faulty conditions.

In the case of LG fault, it means fault occurred in one line to ground, first, the fault is injected in line A w.r.t ground, and 1001 is displayed at the output of the FD unit as shown in Figure 20. Line A is short-circuited w.r.t ground, when any short circuit is detected then ANN predicts 1 at the output. If a fault is injected in line B w.r.t ground, and 0101 is displayed at the output of the FD unit, the same behavior shows if the fault is injected in Line C w.r.t ground and 0011 is displayed at the output of the FD unit. The same behavior is shown in the case of LLG and LLLG faults.

The three-phase output voltage for A to G of TPMC is shown in Figure 21. It can be seen that the phase A voltage is disturbed w.r.t ground under A to G faulty condition.

For better visualization, the output voltages are displayed for each phase under the AG-fault condition as shown in Figure 22.

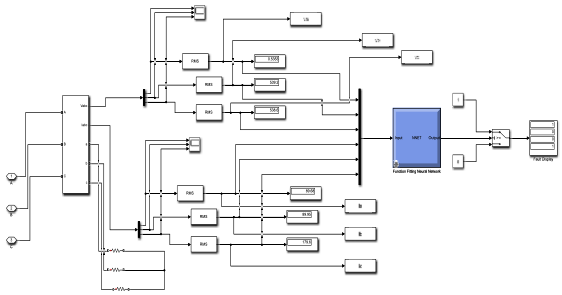

FIGURE 20. Load side fault detector output under A to G fault.

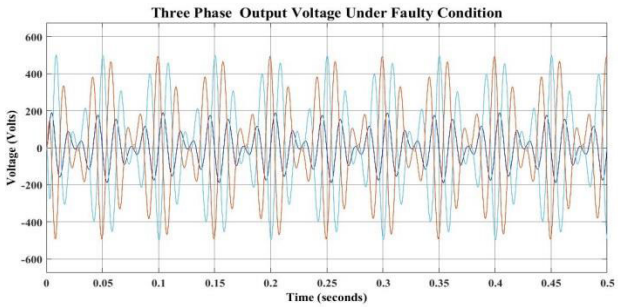

FIGURE 21. Three-phase output voltage under A to G fault.

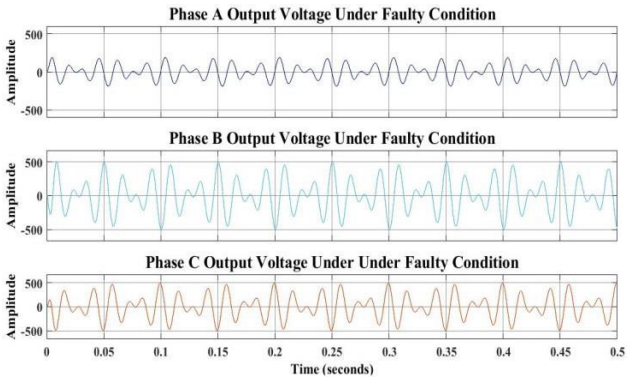

FIGURE 22. Output voltages under A to G fault.

In case of internal fault, the FDI unit is detected and isolates the fault, and to overcome this fault DHR is proposed which is extensively discussed below.

C. INTERNAL FAULT

First of all, the algorithm monitors the RMS values of current in each switch and gives the RMS values of each switch to the input of the ANN module as shown in Figure 23.

If the fault occurs in switch S1 ANN predicts 0. The outputs of the ANN module are given to the nine fault detector blocks in the FDI unit. The fault detector block isolates the faulty switch S1 and enables the redundant switch S1 after the transverse delay of 0.2 sec. The switch is interchanged in microseconds that's why some delay is introduced for better visualization, and MC continues its operation normally. If the fault does not occur in switch S1 then ANN predicts 1.

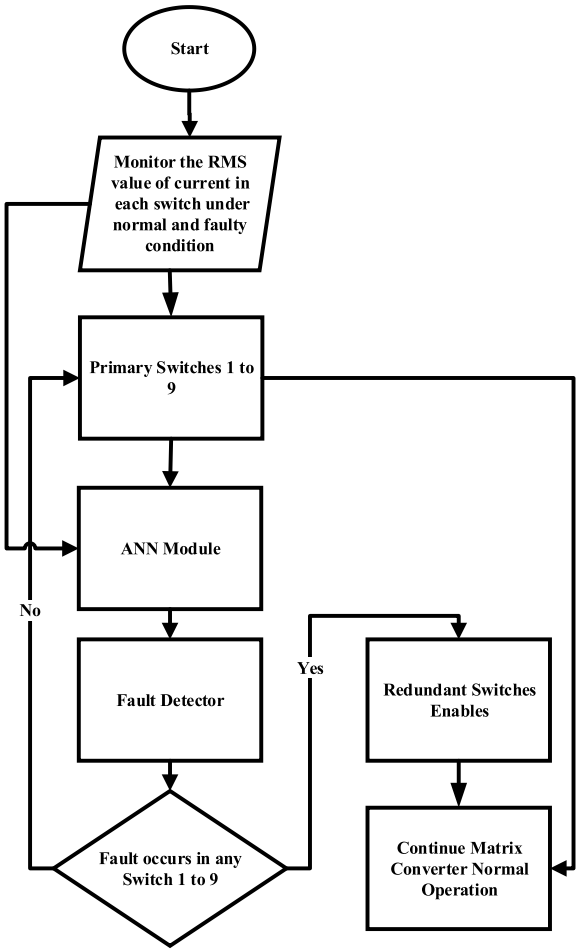

FIGURE 23. Flowchart of proposed switch fault tolerance in TPMC.

Similarly, the ANN output gives to the respective fault detector block where the fault does not occur, and the primary switch S1 operates normally. The System shows the same behavior for all other switches. Under switch fault, the current through the faulty switch is approximately zero and voltage is maximum near to supply voltage, and the redundant switches take charge. Due to the proposed algorithm, the switch fault does not affect the performance of the system. The system fails only if both primary and redundant components are failed.

The internal faults are injected into switches to check the behavior of switches under faulty conditions. The FI dashboard consists of nine slider-type switches S1 to S9 and nine bulbs are shown in Figure 24.

The switches are operated in two modes normal and failure mode and connect these switches with the fault control signal of the FDI unit. In normal mode, the switch gives a normal current value and the bulb indicates the green color, and in failure mode, it will give 0 and the bulb indicates red to the fault control signal. Their inputs go to ANN and it predicts 1 under normal conditions and 0 under faulty conditions.

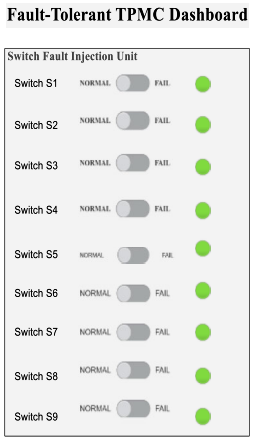

FIGURE 24. Fault injection dashboard.

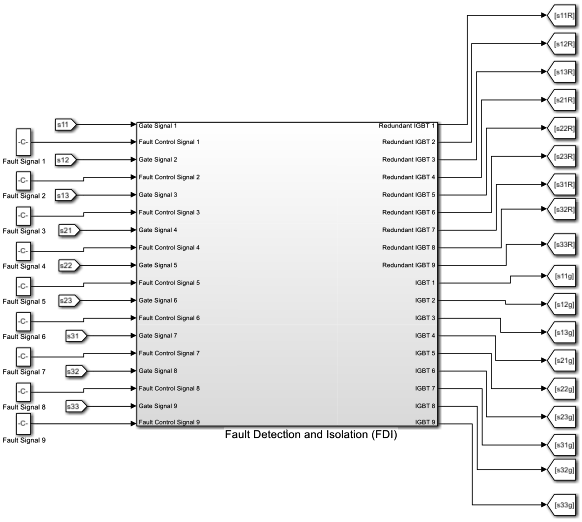

FIGURE 25. Fault detection and isolation (FDI).

In Figure 25, an FDI unit is used which detect and isolate the fault. Inside the FDI unit, the fault detector is used which checks the behavior of the switch and isolates the faulty switch by turning off the gate pulse, and immediately applying the gate pulse to the redundant switch which continues the operation of TMPC under faulty conditions.

The internal structure of the FDI unit consists of nine fault detectors, an ANN model, and nine dual switches. First ANN predicts fault control signal provided to ANN trained model and ANN predicts 1 under normal conditions and 0 under faulty conditions, and then nine dual switches are used to convert the predicted value to binary value and give to the fault detector block. If any fault has occurred in nine switches, every fault detector will diagnose the fault and isolate faulty components and healthy components take charge to avoid shutdowns. The isolation is taking place in the faulty switch by turning off the gate pulse and immediately applying the gate pulse to the redundant switch which continues the operation of TMPC. In the case of a short circuit fault, the voltage

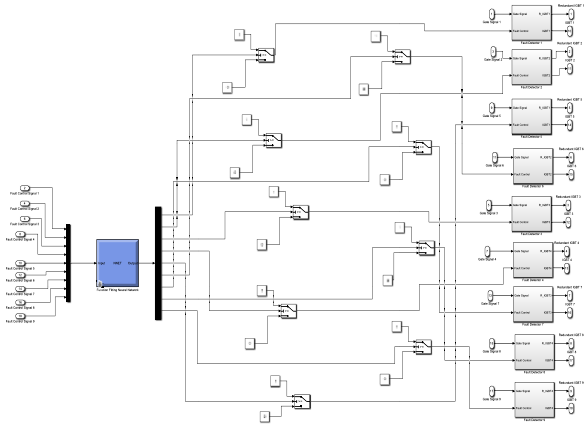

FIGURE 26. Internal structure of FDI unit.

is zero across the switch and the current will be increased from its main value but the work is being on an open circuit fault. In an open circuit fault, the current through a switch is zero and the voltage will increase approximately equal to the supply voltage. When a fault is not injected in any switch, the primary switches work properly as shown in Figure 26. When the fault is detected properly, then overcoming the fault DHR FTC is proposed which is discussed in this section.

The fault detector consists of the fault control signal, gate signal, and zero gate-off signals as shown in Figure 27.

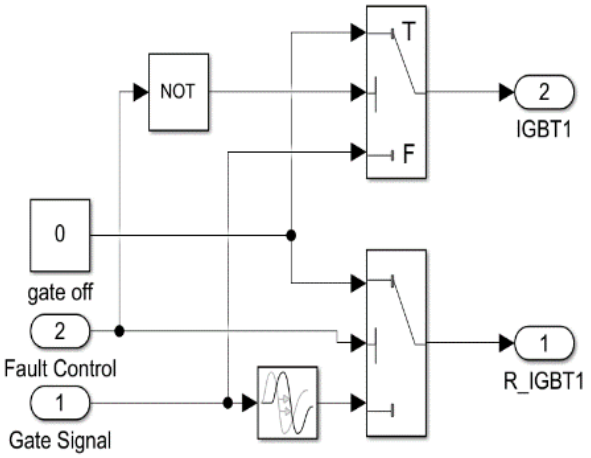

FIGURE 27. Fault detector.

Initially, when no fault is detected the zero gate-off signals are connected to a redundant switch which turns off the redundant switch, and the gate pulse is connected to a primary switch for normal operation. In faulty condition, the gate off signal is connected to a primary switch which turns off the primary switch and after 0.2 delays the redundant switch takes charge to continue the operation of the system and prevent the system from shutting down.

In the structure of ANN, the route mean square value current is used for each switch as an input, ten hidden layers, and nine output layers to predict switch value. ANN

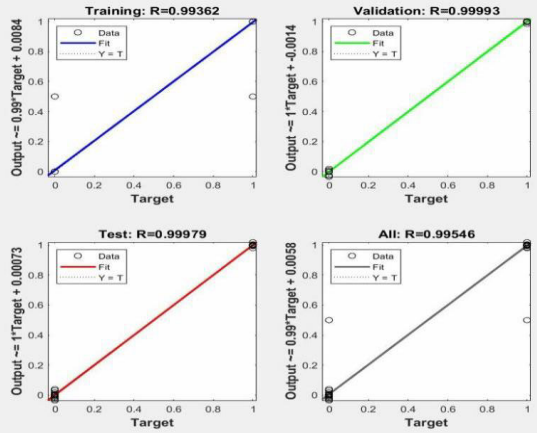

FIGURE 28. Regression plot of model.

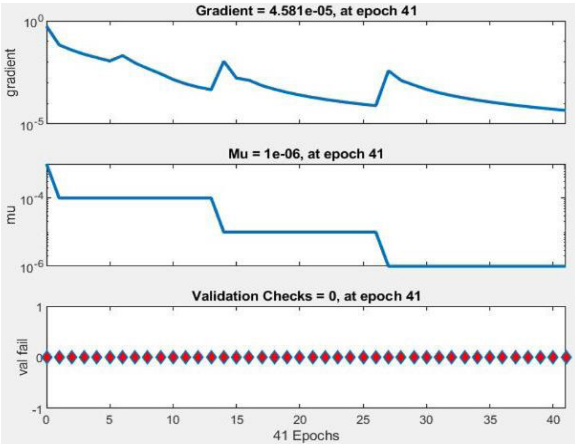

FIGURE 29. Traning performance of ANN model.

predicts 1 under normal operations and 0 under faulty conditions. In the dataset of a neural network, 70% data for the training set, 15% validation set, and 15% of the data for testing the algorithm are used. To train the model, the Levenberg-Marquardt algorithm is used. This algorithm requires more memory but it will detect the fault in less time. The regression plot is shown in Figure 28 which indicates the network outcomes for corresponding targets. If the network is overlapped with the regression linear line then the network is trained correctly as discussed in [38].

Figure 29 shows the gradient descent whose value is $4.581e^{-05}$. The value of gradient descent indicates that the local minima after 41 iterations are $4.581e^{-05}$.

In the case of an open circuit fault, the current through a switch is zero and the voltage will be maximum around about supply voltage. When no fault is injected in switch S1, the primary IGBTs of the S1 switch work properly and the current and voltage across S1 are shown in Figures 30 and 31. At the same time, the redundant switch is opened due to the zero gate pulse being applied to the redundant switch.

Due to current modulation, the peak value of current at switch S1 is high and for all other switches, the peak value

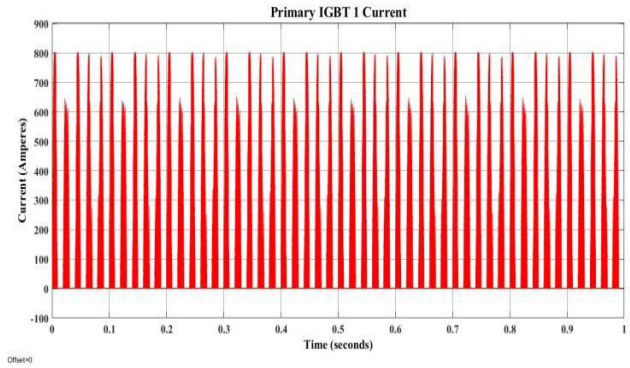

FIGURE 30. Current through IGBTs switch S1 under no fault.

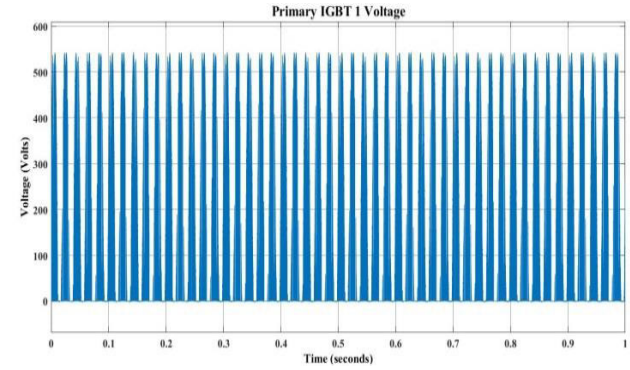

FIGURE 31. Voltage across IGBTs switch S1 under no fault.

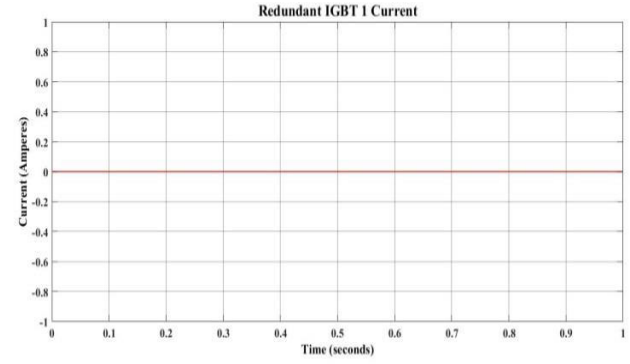

FIGURE 32. Current through redundant switch S1 under no fault.

of current is the same under normal conditions. The primary switch S1 works properly, there is not any short circuit. This suggests that the observed increase in current at switch S1 is within the expected range for its normal functioning. Due to the open circuit, the current through redundant S1 is zero but the voltage will be maximum.

There will not be any disturbance at output under no-fault as shown in Figure 34.

When an open circuit fault occurs in the switch, the output voltage and current of TPMC are disturbed which causes the whole system to shut down. If a fault is injected in switch S1 using the fault injection dashboard. The primary IGBTs of

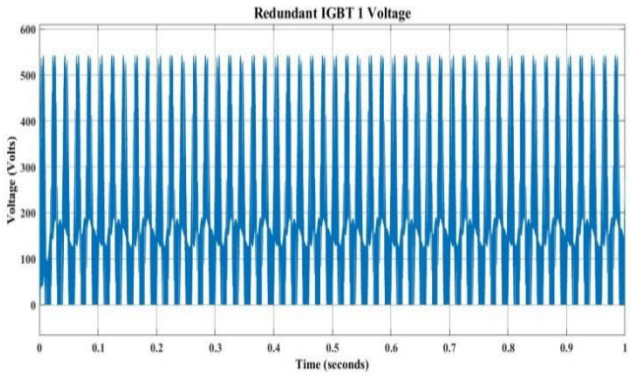

FIGURE 33. Voltage across redundant switch S1 under no fault.

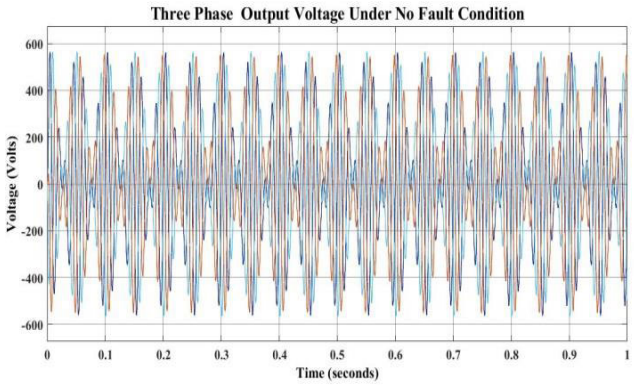

FIGURE 34. Three-phase output voltage under no fault.

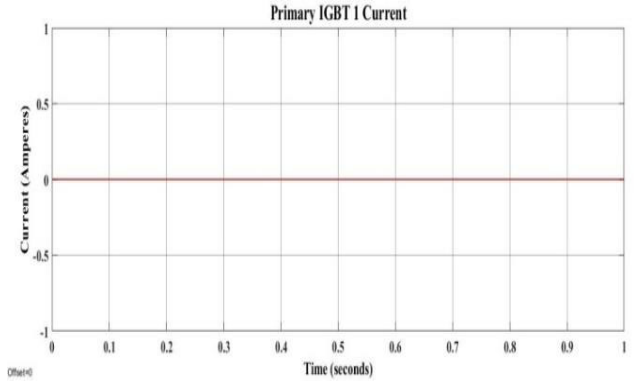

FIGURE 35. Current through IGBTs switch S1 under faulty condition.

the S1 switch are opened due to an open circuit fault. Due to an open circuit, the current through primary switch S1 is zero but the voltage is maximum as shown in Figures 35 and 36.

The redundant switch S1 takes charge after some time to prevent the TPMC from shutdowns. The same behavior is shown for all other switches. If all swiches are faulty that means all drop are accrossed faulty switches, and output of TPMC is zero.

There is not any researcher who takes corrective action using redundant switches on TPMC but in 2020, Soban

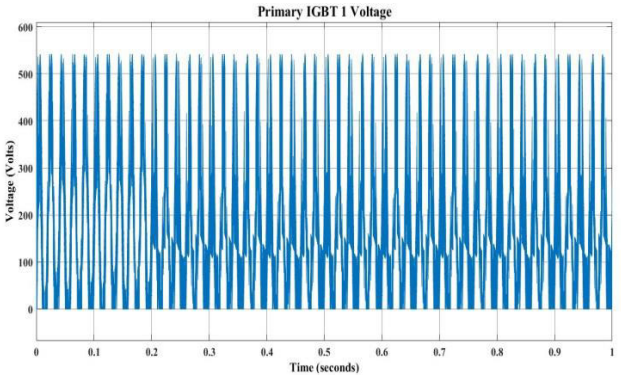

FIGURE 36. Voltage across IGBTs switch S1 under faulty condition.

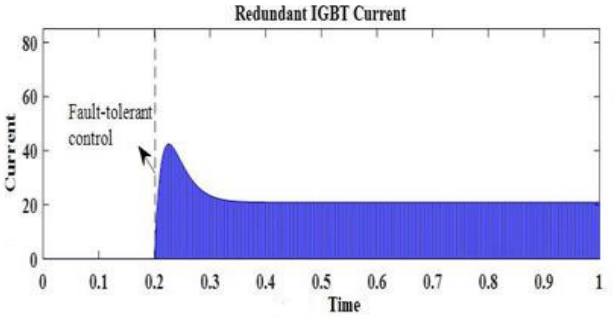

FIGURE 37. Redundant IGBT current during Fault [4].

Ahmed proposed a hardware redundant system based on fault-tolerant H-bridge. The author worked on speed control of DC motors using FTC H-bridge [4]. According to his proposed method, when a fault occurs in any IGBT switch of the H-bridge replace the faulty switches with redundant switches to prevent the system from shutdowns. As you see in Figure 37 when an open circuit fault occurs in the IGBT switch, the current is zero, and after 0.2 sec the redundant takes charge to continue the operation of the DC motor.

Utilizing the fault injection dashboard, a fault is artificially introduced into switch S1. This leads to the primary IGBTs of switch S1 opening due to the presence of an open circuit fault. Consequently, the current flowing through primary switch S1 becomes zero, while the voltage reaches its maximum value as shown in Figures 38 and 39 respectively.

By comparing the result with existing literature, due to a fault occurring in the primary switch, the redundant takes charge and continues its operation under the faulty condition which shows the feasibility of the proposed method. After 0.2 sec the redundant enabled to avoid shutdowns.

As you see in Figure 40, from 0 to 0.2 sec the voltage of one of the phases is disturbed due to fault but after 0.2 the fault is overcome by redundant components.

For better visualization, the output voltages are displayed for each phase under the Switch S1 fault as shown in Figure 41.

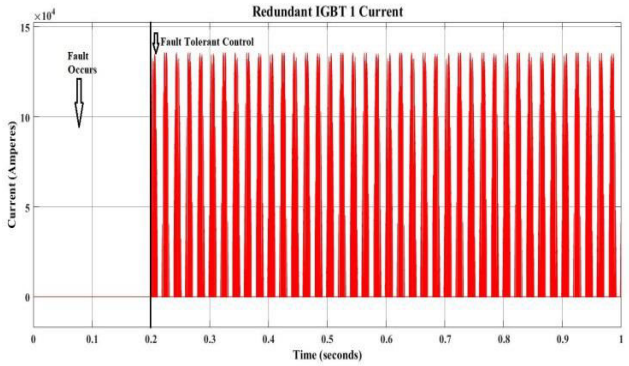

FIGURE 38. Current through redundant switch S1 under faulty condition.

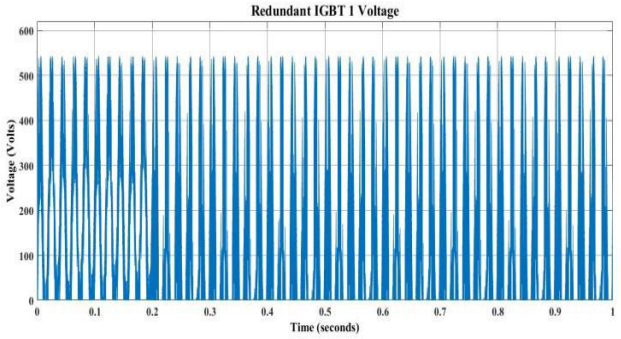

FIGURE 39. Voltage across redundant switch S1 under faulty condition.

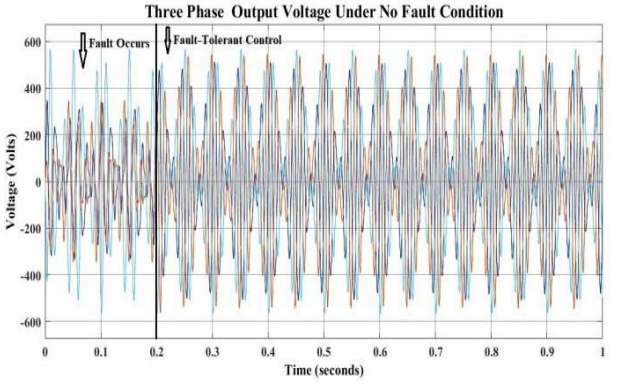

FIGURE 40. Three-Phase output voltage of TPMC under S1 switch faulty condition.

D. HARDWARE-IN-THE-LOOP

There are three modes to work with hardware from the MATLAB/Simulink; Connected Input Output (CIO), External Mode (EM) monitor and tune, and EM build deploy and start. To verify the above simulation results, hardware-in-the-loop is implemented for the switch fault. The code of the TPMC model is burned into the STM32-Nucleo-F103RB board. The EM monitor and tune mode of configuration is used to implement the model in hardware and set the

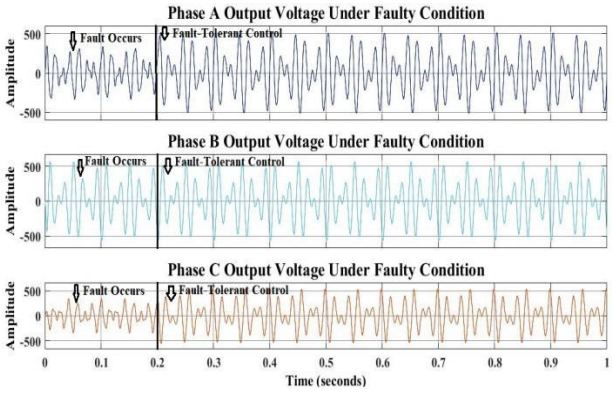

FIGURE 41. Output voltage of each phase of TPMC under S1 switch faulty condition.

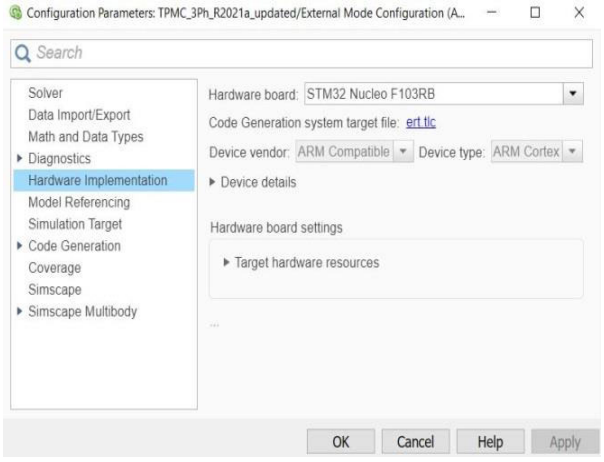

FIGURE 42. Hardware implementation settings.

hardware setting. Select the hardware board and com-port where STM32 is connected as shown in Figure 42.

When the model is monitored and tuned, the C code is automatically generated and burned the code into the hardware board.

Under open circuit fault conditions, the hardware results are shown below which are approximately matched with simulation results. Figures 43 and 44 show the current and voltage of TPMC switch S1 under an open circuit fault. As you see in these Figures, when a fault occurs the current is zero and the voltage is maximum near to supply voltage which is similar to simulation results.

All results matched with simulation results but the peak value of redundant switch current is reduced as shown in Figure 45 because in hardware many component resistances are affected by the current value and the behavior of results are same as well. Figure 46 shows the redundant voltage of Switch S1, but the little voltage drops from 0 to 0.2 sec due to hardware components. The same behavior will be shown in all other switches.

The DHR is proposed to increase the durability and reliability of the system. In DHR, a copy is added of the main

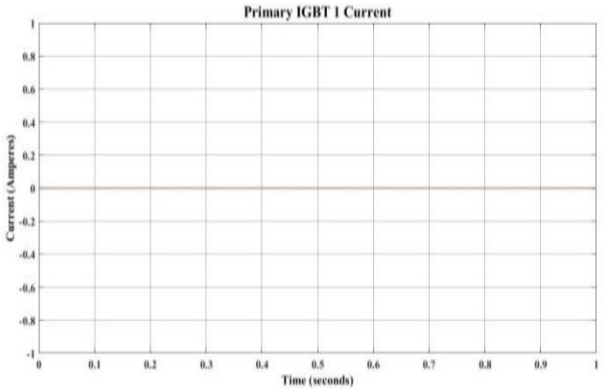

FIGURE 43. Current through IGBTs switch S1 under faulty condition with hardware implementation.

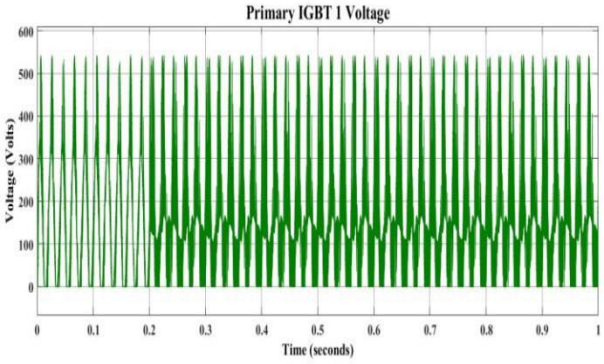

FIGURE 44. Voltage across IGBTs Switch S1 under faulty condition with hardware implementation.

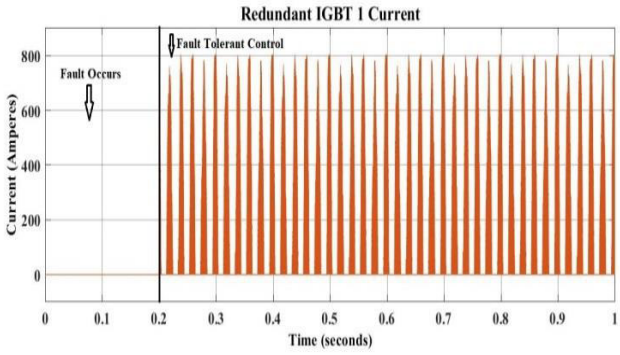

FIGURE 45. Current through redundant switch S1 under faulty condition with hardware implementation.

component parallel along with the redundant component. If any fault occurs in the main component, the redundant component takes charge to prevent the system from shutting down. The system fails if both the main and redundant fail. In the structure of TPMC, nine di-directional switches S1 to S9 are used to control the switching operation. The nine more redundant switches redundant S1 to redundant S9 are used parallel to the other switches, each switch consists of two IGBTs and two freewheeling diodes as shown in Figure 47.

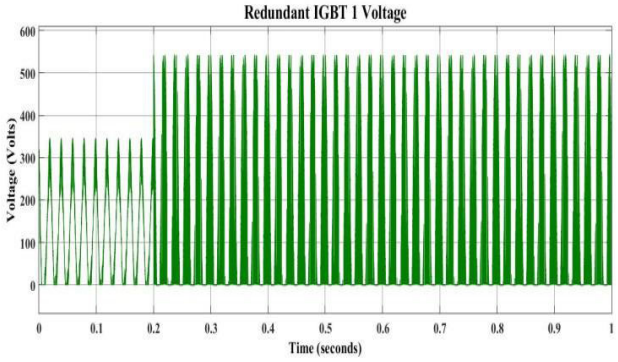

FIGURE 46. Voltage across redundant switch s1 under faulty condition with hardware implementation.

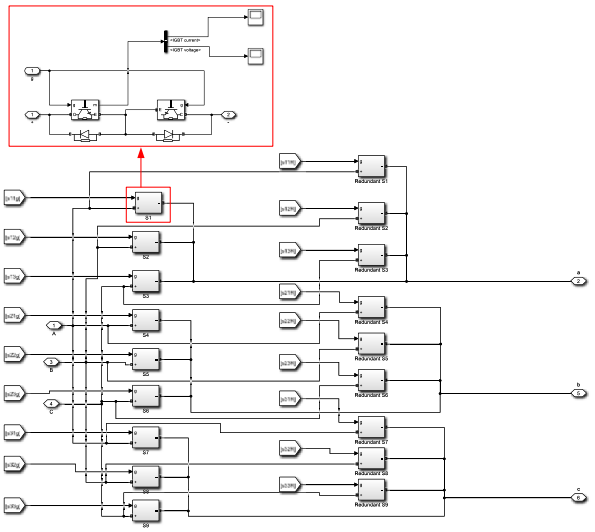

FIGURE 47. Proposed dual hardware redundancy.

When a fault is injected in any switch, the FDI unit detects and isolates the fault, and then to prevent the whole system from shutdown the DHR system has been implemented above. If a primary component is faulty, then the redundant component is enabled to prevent shutdowns. The proposed method is the best solution under faulty conditions.

The existing approaches may include Kalman Filters, clamp circuits, and linear regression which were only applicable to linear systems. Due to parallel computations of ANN detect fault very fast as compared to existing literature approaches.

The proposed system can be utilized mostly in AC Drives and AC-AC power converters for the integration of a wind energy conversion system into a grid that functions as a distributed load system. The overall cost of the proposed system will be approximately $900 with the three-phase motor as a load if each switch condition is monitored. No doubt the cost is high, due to redundant switches but reliability is more important than the cost and high hardware cost of ANN [39]

TABLE 3. Abbreviations explanation.

Abbreviations	Explanation
FTCS	Fault-Tolerant Control System
TPMC	Three-Phase Matrix Converter
MCs	Matrix Converters
FTC	Fault-Tolerant Control
ANN	Artificial Neural Networks
FD	Fault Detection
AFTCS	Active Fault-Tolerant Control System
FDI	Fault Detection and Isolation
PFTCS	Passive Fault-Tolerant Control System
IGBTs	Insulated Gate Bipolar Transistors
MIMO	Multi-Input and Multi-Output
SMC	Sliding Mode Control
DHR	Dual Hardware Redundancy
TMR	Triple Modular Redundancy
FI	Fault Injection

but it is a very powerful controller which gives accurate and fast fault detection under non-linearity conditions as compared to existing literature.

IV. CONCLUSION

In this paper, an advanced FTCS was proposed based on detection, and DHR system. Two types of faults were injected into the structure of TPMC; internal open circuit faults on switches and external short circuit faults at the load side. A dual redundant FTC system had been implemented based on an FDI unit with a trained ANN Algorithm in the case of internal faults. For external faults, a fault detector using a neural network was proposed in the MATLAB/Simulink environment. First, an open circuit fault was injected on switches using the FI unit then the FDI unit detected and isolated it. To overcome this fault a dual redundant fault-tolerant system was proposed. Hardware-in-the-loop has been implemented to verify the simulation result at the switch side. Secondly, a three-phase short circuit fault was injected artificially at the load side to check the behavior of TPMC under faulty conditions and then detect this fault using the ANN algorithm. The present approaches which are only applicable for linear systems, include Kalman Filters, clamp circuits, and linear regression but the proposed ANN-based algorithm is the best solution for both linear and non-linear systems. The ANN is a very powerful tool that outperforms existing methods described in the literature in terms of its capability to quickly identify problems. The proposed method was a very effective and reliable solution for TPMC under faulty conditions by comparing existing methods. There are lots of applications of TPMC such as aircraft, submarines, and compact motor drives where variable speed is required.

Future works may include the hardware verification of the proposed FTC at the load side. Another future direction is FTC implementation with a deep learning algorithm for fault diagnosis and TMR for hardware redundancy in TPMC.

ABBREVIATIONS AND SYMBOLS

All the abbreviations and explanations of this paper are provided in Table 3.

The entire symbol and its description are provided in Table 4.

TABLE 4. Symbols and description.

Symbols	Description
x_i	Input Feature of Neural Network
w_i	Weightage of Feature
b	Bias
L_{dr}	Reliability of DHR
L_1	Reliability of Component 1
L_2	Reliability of Component 2
$1-L$	Failure Reliability

CONFLICT OF INTEREST

The author(s) declare no conflict of interest in preparing this paper.

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FAIZAN AHMAD received the B.Sc. and M.Sc. degrees in electrical engineering with specialization in electronics and fault tolerant control systems from the National University of Computer and Emerging Sciences, Faisalabad, Pakistan. He possesses more than three years of relevant industrial and academic experience with three years served as a Laboratory Engineer with the FAST National University of Computer and Emerging Sciences (FAST NUCES) and an Electrical Intern for three months with SHAH Dying Textile Mills, where automated dying using programmable logic controllers. He has achieved various academic distinctions, such as a winner of IEEE Student Tech Talks, being three times on the Dean's List, and getting three bronze medals, which show his excellent performance in academics. His research interests include control systems and automation.

TURKI M. ALSUWIAN received the B.Sc. degree in electrical engineering from King Saud University, Riyadh, Saudi Arabia, the M.Sc. degree in electrical engineering from Gannon University, PA, USA, in 2011, and the Ph.D. degree in electrical engineering from the University of Dayton, OH, USA, in 2018. He was an Electrical Power Engineer with Saudi Electricity Company, from April 2004 to January 2009. Currently, he is an Assistant Professor with the Electrical Engineering Department, Najran University, Saudi Arabia. His research interests include applied control in different fields, such as flight control, power control, power electronics control, communication control, adaptive control, and modeling control.

ARSLAN AHMED AMIN (Senior Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering with specialization in control systems from the University of Engineering and Technology, Lahore, and the M.B.A. degree with specialization in management from the Virtual University of Pakistan. He possesses more than 13 years of relevant industrial and academic experience in Pakistan's reputed organizations, such as Pakistan Petroleum Ltd. (PPL), National Textile University (NTU), and FAST National University of Computer and Emerging Sciences, where he is currently an Associate Professor. He has achieved various academic distinctions, such as overall top in BISE Faisalabad, standing among the top ten students with UET Lahore in the B.Sc. program, and selection for the prestigious Fulbright Ph.D. USA Scholarship. He has numerous publications in the international prestigious impact factor peer-reviewed journals. His research interests include fault-tolerant control systems, control system's reliability, safety control systems, nonlinear control, and control system stability and design.

MUHAMMAD ADNAN (Member, IEEE) received the B.Sc. degree in electrical engineering from the National University of Computer and Emerging Sciences, Peshawar, Pakistan, in 2013, the M.S. degree in electrical engineering from the COMSATS Institute of Information and Technology, Islamabad, Pakistan, in 2015, and the Ph.D. degree in electrical engineering from the National University of Computer and Emerging Sciences. He was a Research Fellow with the Department of Electrical Power Engineering, National University of Computer and Emerging Sciences, from January 2017 to December 2019. Currently, he is an Assistant Professor with the Department of Electrical Engineering, FAST National University of Computer and Emerging Sciences (FAST NUCES), CFD Campus. His research interests include energy management systems, load flow balancing, load forecasting, power systems dynamic analysis, protection, stability, and intelligent control in renewable energy resources using a fuzzy controller and unified power flow controller.

MUHAMMAD BILAL QADIR received the B.Sc. and M.Sc. degrees in textile engineering from National Textile University (NTU), Pakistan, in January 2007 and October 2012, respectively, and the Ph.D. degree in organic and nano engineering from Hanyang University, South Korea, in 2016. After the Ph.D. degree, he continued his research as a Postdoctoral Researcher, in 2016, for six months with Hanyang University. He is currently an Assistant Professor with the Yarn Manufacturing Department, NTU. His research interests include the modification of electrospinning machines for better productivity, and the development of multifunctional nano webs for filtration, functional textiles, and medical applications. He is leading his team in the yarn manufacturing nowadays and striving for the betterment of education and research with NTU. He is also motivated to collaborate with the industry to solve their issues and to give solutions for the current and upcoming challenges. He is also a Coordinator of Graduate Research with the School of Engineering and Technology.