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RESEARCH ARTICLE

Super Twisting Sliding Mode Control Strategy for Input Series Output Parallel Converters

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ABSTRACT In this paper, a super twisting sliding mode control method (ST-SMC) is proposed for an isolated input series output parallel current source converter (ISOP-CSC). The main idea behind the input series output parallel connection is to share the input voltage and output current among the converter cells. Since the input current of each cell has to be identical, the control strategy should be able to provide an accurate phase angle to each cell at the same time. The decentralized control method requires a current sensor for each cell. Therefore, the controller performance can be affected by faults, measurement errors and noises in the slave cell's current sensor. To overcome this issue, the proposed ST-SMC method generates the phase shift between the primary side switching signals of the master cell. After that, the generated phase shift value is transferred to the slave modules. Thus, the same phase angle value is used for each cell and the current sensor is only needed for the master cell. Furthermore, the proposed method doesn't need any voltage sensor. The effectiveness of the proposed control method is investigated by experimental studies that are performed on an ISOP-CSC prototype. The results reveal that the proposed method successfully regulates the input current to reference value under both steady-state and dynamic transition conditions.

INDEX TERMS Isolated input series output parallel current source converter, sliding mode control, current control.

ABBREVIATION

ST-SMC	Super twisting sliding mode control.
ISOP	Input-series output-parallel.
IPOS	Input-parallel output-series.
ISOS	Input-series output-series.
CSC	Current source converter.
DAB	Dual active bridge.
IVS	Input voltage sharing.
OCS	Output current sharing.
PWM	Pulse width modulation.
ADC	Analog digital conversion.
PI	Proportional-integral.
VSC	Voltage source converter.

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I. INTRODUCTION

High-voltage DC is extensively used in electric vehicle charging stations, rail transport and DC grids [1], [2], [3]. The power conversion in these systems is provided by various configurations of DC/DC converters such as input-series output-parallel (ISOP), input-series output-series (ISOS), input-parallel output-series (IPOS), and input-parallel output-parallel (IPOP) [4], [5], [6], [7]. Due to flexibility and modularity features, these configurations can easily be adapted to high-voltage and high-power systems. ISOP converters become increasingly attractive for high-voltage applications. The input voltage and total system power are shared by each cell with the ISOP configuration. Since the input series connection, the cell's topology should have galvanic isolation. Recently, isolated converter topologies have become popular due to their distinct advantages such as high efficiency,

operability under wide input voltage range, high power density, bidirectional power flow and low electromagnetic interference. LLC resonant and dual active bridge (DAB) converters are very popular among these topologies. Similar to these topologies, an isolated topology based on the current source converter is presented in [8]. Compared to LLC and DAB, the key advantage of this topology is the small-size capacitor requirement [8], [9], [10].

The choice of topology in an ISOP configuration has significant implications for size, efficiency, cost, and reliability. However, it is equally important to consider the control method employed to guarantee the converters' optimal operation. Numerous studies emphasize the fundamental principles of input voltage sharing (IVS) and output current sharing (OCS) that underpin the ISOP configuration. Consequently, the control objectives are carefully chosen to facilitate these characteristics [11], [12], [13], [14], [15].

The control methods used in ISOP converters can be categorized as decentralized and centralized methods. The decentralized control method aims to eliminate the performance degradation caused by parameter mismatches between cells. The IVS and OCS are achieved by implementing the control strategy into each cell's controller. Since each cell contains a controller, the number of Pulse Width Modulation (PWM) and Analog Digital Conversion (ADC) channels of the microcontroller doesn't limit the modularity. A decentralized control strategy is proposed for the ISOP converter in [15]. The absence of a central controller is a key characteristic of the method, making each cell self-contained. The control strategy revolves around maintaining the desired output voltage of the ISOP. To enable this control method, the reference voltage value and input voltage of each cell need to be specified or communicated in the control algorithm of each cell, which operates independently. The reference voltage is then compared with the measured output voltage, and the sum of each cell's input voltage is utilized in the control strategy. Therefore, it is crucial for each cell's microcontroller to accurately measure all the system voltages simultaneously. Failure to do so would impede the achievement of both input voltage sharing (IVS) and output current sharing (OCS). Consequently, this requirement introduces new challenges regarding the sensing mismatches among the system variables.

On the other hand, the centralized control strategy aims to achieve IVS and OCS using a master controller. The centralized control strategy presented in [11] contains input voltage feedback and output current feedback controllers for sharing the input voltage or output current between cells. The method includes one output voltage regulator for ISOP. In addition, an input voltage regulator is required for each cell. Therefore, the control strategy is quite complicated. The controller generates a separate duty ratio for each cell. Thus, the performance deviations caused by the parameter mismatch between the cells are eliminated. The duty ratios generated at the controllers' output are sent to the slave modules. The input voltages of each cell and the output voltage of the ISOP converter should be measured for implementing such a control method. Since many signals should be received/sent between master and slave cells, the control strategy limits the modularity and reliability. Similarly, a centralized control strategy is implemented using a single microcontroller in [16]. IVS and OCS are achieved with the control strategy that needs to measure the voltages of each cell and ISOP converter. Thanks to using a single microcontroller, the data/signal transfer issues are eliminated. However, the modularity of the system is restricted due to the limited number of PWM and ADC channels of the microcontroller.

Although the separate controller usage in both decentralized and centralized methods provides a stable operation under parameter mismatch, the common duty ratio techniques that lead to extremely simple implementation are also existing in the literature [17], [18], [19]. The common duty ratio technique was first presented in [17]. In [18], a detailed analysis of the common duty ratio technique is presented to show the effectiveness of the method. The key advantage of this method is that it does not require the sense of slave converter parameters. Therefore, the method offers improved modularity, less data or signal transfer between the cells and reduced total system cost. The method provides IVS and OCS by only sensing the output current and load voltage of the master cell. The control algorithm is implemented only into the master cell's microcontroller and the duty ratio is transferred to slave cells. Therefore, the method offers an easy implementation. In [20], a centralized control strategy based on a proportional-integral (PI) controller with active damping strategy is proposed for ISOP connected identical phase shift full bridge converters. In this control method common duty ratio is used in all cells. Thus, IVS and OCS are naturally achieved. In [21], the input-voltage and output-current equalization performance of a boost LLC-based ISOP converter under the condition of inconsistent submodule parameters is analyzed. The cells operated with the same phase shift. The dynamic voltage-sharing performance depends on the mismatch between capacitances used in cells while the steady-state performance only depends on the mismatch between the transformer's turn ratios. It is reported that the mismatch between the transformer's turn ratio is within $\pm 1\%$. The common duty ratio technique shows excellent IVS and OCS performance for identical cells.

The applicability of the common duty ratio technique is limited due to the parameter mismatch between the cells. However, the parameter mismatch between the transformer's turn ratio is very small in practical applications thanks to the improvement of transformer manufacturing technology as reported in [21]. Also, with the modern transformer manufacturing techniques, such as planar transformers with precise printed circuit-board windings, the mismatch in turn ratios, and, hence, the mismatch in the input-voltage and load-current sharing, can be made negligible [18].

In this paper, a centralized control method is proposed for input series output parallel connected isolated current source topology in [8]. The features and contributions of the proposed control strategy are listed as follows:

- The ISOP connection and super twisting sliding mode control of the isolated current source topology in [8] are introduced first time in this paper.
- Compared to [15], [16], [18], and [20], fewer sensors are used for implementing the proposed control method. Thus, the sensing mismatches are eliminated, and reliability is improved.
- The method only transfers the phase shift ratio generated by ST-SMC to slave cells, hence, the reliability of the system is improved by preventing the large number of data transfer. Moreover, the proposed technique doesn't need to transfer cell's variables to each other. Therefore, the proposed method is more convenient than the technique in [16].
- Compared to [15] and [16], the modularity is not restricted due to the use of individual microcontrollers for generating PWM signals of each cell.

II. MODELING OF CSC AND ISOP CONFIGURATION

Modeling of the current source converter (CSC) and input series output parallel configuration of the CSC is described in this section. Fig. 1. depicts the circuit model of the isolated CSC that's key advantage is requiring a very small output capacitor. The primary side of the high-frequency transformer is connected to the CSC which includes six switches. The voltage source converter (VSC) at the secondary side provides the power transfer from the transformer to the load. The power transfer from the primary to the secondary side depends on the phase shift between the switching signals of the CSC and VSC switches. Furthermore, the primary side power depends on the phase shift value between the switching signals of CSC switches. Therefore, a phase shift modulation strategy is used to generate the switching signals of both CSC and VSC switches.

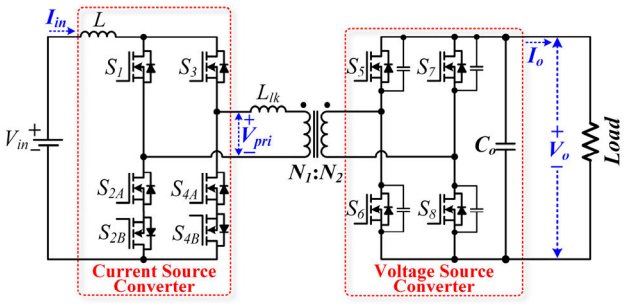

FIGURE 1. Schematic diagram of the isolated CSC.

Fig. 2. depicts the phase shift modulation scheme of the isolated CSC cell. D_a and D_b denote the duty ratio of CSC and VSC side switches, respectively. The duty ratios are constant values that are determined by the defined instructions in [8]. This means that the power flow ratio from the primary side to the secondary side of the transformer is constant. Therefore, only the phase shift value (θ) regulates the power. The input power of the converter varies depending on θ that determines the phase shift ratio between the switching signals of upper and lower switches of CSC as shown in Fig. 2. The switching signals are generated by using the switching logic defined in the modulation scheme.

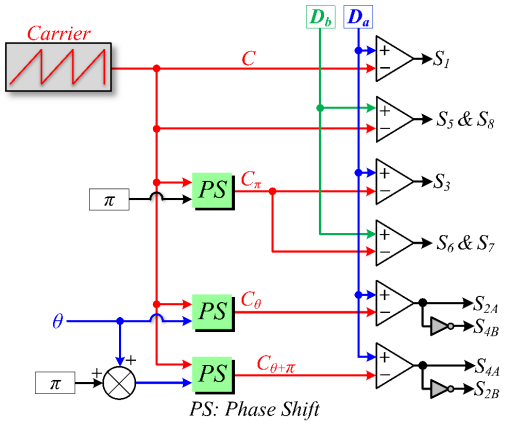

FIGURE 2. Modulation scheme of the isolated CSC.

A. MODELING OF ISOLATED CURRENT SOURCE CONVERTER

The modeling of the isolated CSC is derived to be used in the design of the control method which is presented in the next section. Since the control objective is to regulate the input current (I_{in}) of the converter, the analyzes are done based on the input inductor (L). There are six switching states based on the modulation strategy as given in Table 1. Fig. 3 shows the equivalent circuits used to modeling of the converter.

TABLE 1. Switching states of the isolated CSC.

Switching State	S_1	S_{2A} & $\overline{S}_{4B}$	S_3	S_{4A} & $\overline{S}_{2B}$	S_5&S_8	S_6&S_7
1	ON	OFF	OFF	ON	ON	OFF
2	ON	ON	OFF	ON	ON	OFF
3	ON	ON	OFF	OFF	OFF	OFF
4	ON	ON	ON	OFF	ON	OFF
5	ON	ON	ON	OFF	OFF	OFF
6	OFF	ON	ON	OFF	OFF	ON

Switching State 1: Since S_1, S_{4A} and S_{4B} are ON in the first switching state (Fig. 3(a)), the inductor is discharging through the primary winding of the transformer. Hence, the inductor voltage (v_L) is equal to the difference between input voltage (V_{in}) and primary voltage (V_{pri}) as follows

$$v_L = V_{in} - V_{pri} \tag{1}$$

Since S_5 and S_8 are ON on the VSC side, the secondary current of the transformer (i_s) flows through the output capacitor (C_o) and load as shown in Fig. 3(a).

Switching State 2: The equivalent circuit of the 2nd switching state is shown in Fig. 3(b). This transient interval between

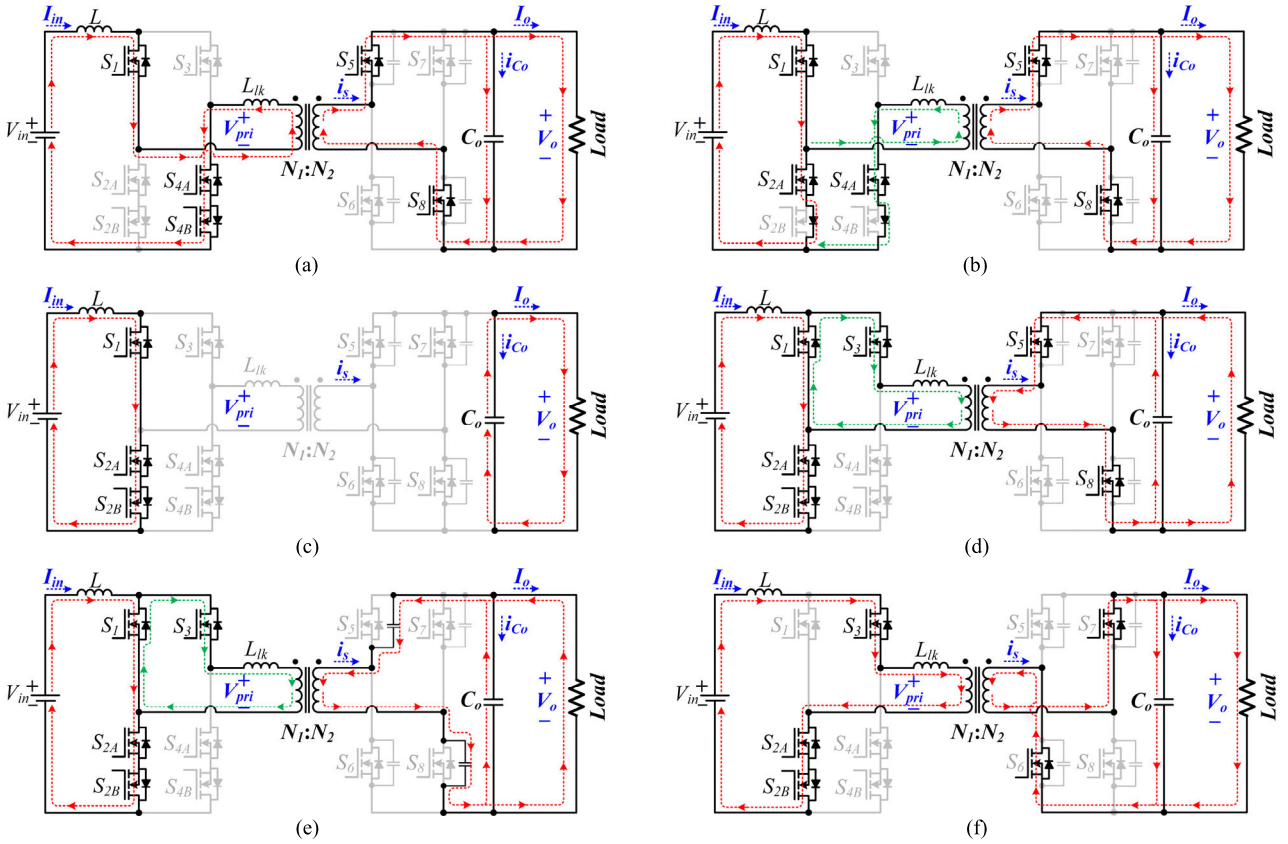

FIGURE 3. Equivalent circuits of the CSC based on the switching states in Table 1. (a) State: 1, (b) State: 2, (c) State: 3, (d) State: 4, (e) State: 5, (f) State: 6.

the first and third states provides ZCS operation [8]. Since S_1 and S_{2A} are ON, the inductor is charged with I_{in} through these switches and body diode of S_{2B}. Therefore, the inductor voltage is equal to the input voltage as follows

$$v_L = V_{in} \tag{2}$$

Similar to the first switching state, i_s flows through C_o and the load at the VSC side.

Switching State 3: Fig. 3(c) shows the equivalent circuit of the 3rd switching state. The transformer is not energized due to all switches in one leg of the CSC are OFF. On the other hand, all switches in the first leg of the CSC are ON. Similar to the 2nd state, the inductor charges with the I_{in} and v_L can be obtained with (2). Since the transformer is not energized, C_o discharges through the load at the VSC side.

Switching State 4: The inductor is charging with I_{in} during this switching state due to the switches in the first leg of CSC are ON, as shown in Fig. 3(d). Therefore, the inductor voltage equals the input voltage as given in (2). In addition, the primary winding of the transformer is short-circuited through S_3 and the body diode of S_1. The leakage inductance of the transformer limits the *di/dt* slope. Therefore, the transformer current's peak value depends on the duration of this state [8].

Switching State 5: Fig. 3(e) shows the equivalent circuit of this switching state. The positions of switches on the CSC side are the same as with the 4th state. However, all the switches on the VSC side are turned OFF. The snubber capacitances of S_5 and S_8 and leakage inductance create a small resonant tank. Therefore, a resonant current flows through the same path. Since the positions of the switches on CSC side are still the same with the 4th state, the inductor is still charging with I_{in} and v_L equals the input voltage as given in (2).

Switching State 6: Fig. 3(f) depicts the circuit model of this switching state. Similar to 1st switching state, I_{in} flows through the primary winding of the transformer and the inductor is discharging. However, the direction of the current flown in transformer winding is opposite compared to 1st state. Therefore, inductor voltage can be written as follows

$$v_L = V_{in} + V_{pri} \tag{3}$$

Also, the secondary current of the transformer flows using the same path as 1st state.

As a consequence of the analysis based on switching states, the inductor charges during the four states (2nd, 3rd, 4th and 5th) while discharging in 1st and 6th states. The general equation of inductor voltage can be obtained by combining (1), (2), (3) and switching states as follows:

$$v_L = L\frac{dI_{in}}{dt} = V_{in} + V_{pri}S_a \tag{4}$$

where S_a denotes the switching pattern as follows

$$S_a = (S_{2A} - S_1) \tag{5}$$

The inductor voltage depends on the position of S_1 and S_{2A}. As mentioned earlier, the position of S_1 is determined by D_a which is a constant value. Therefore, the charge and discharge duration of L depends on the phase shift (θ) between the switching signals of S_1 and S_{2A} as shown in Fig. 2. It is worth noting that the same analysis can be done based on the positions of the switches in the second leg (S_3, S_{4A} and S_{4B}) of CSC. In this case, the charge and discharge duration of L will depend on the θ between the switching signals of S_3 of S_{4A}. Consequently, the inductor current can be controlled by providing appropriate θ.

The voltage gain of the isolated CSC can be obtained as follows

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)}, D = 2\,(D_a - \theta) \tag{6}$$

where D is the duty ratio. As mentioned, D_a is a constant value, hence, the voltage gain is dependent on θ.

B. INPUT-SERIES OUTPUT-PARALLEL CONFIGURATION OF ISOLATED CSC

Fig. 4 shows the input series output parallel configuration of the isolated CSC. The typical feature of such a connection is to share the input voltage (V_{in}) between the cells for high-voltage applications as follows

$$V_{in} = V_{in-m} + V_{in-S1} + \ldots + V_{in-Sn} \tag{7}$$

where m and n denote the number of master and slave cells, respectively. The total system power is also shared to cells by the output parallel feature of such a connection. Therefore, the load current is equal to sum of all cell's current as follows

$$I_L = I_{o-m} + I_{o-S1} + \ldots + I_{o-Sn} \tag{8}$$

In general, all the cells are identically designed for modularity. Therefore, the cells share the input voltage and load current equally in ideal conditions. However, each cell should allow flowing the same current for regulating the input current to its reference. Otherwise, the input current cannot be controlled and the input voltage sharing cannot be provided. Therefore, the cells should operate with the same θ which is generated by the control method.

A decentralized control strategy can be implemented into each cell. In the decentralized strategy, the current reference should be sent from the master cell to the slave cells. Thus, the control method implemented in all cells can regulate the input current to the reference. However, a current sensor should be used in all cells and the input current should be measured accurately in all cells. The control methods can be affected by faults, measurement errors and noises in the slave cell's current sensor. Instead of this method, θ can be sent from master cell to slave cells. In any case, information has to be sent from master to slave cells. However, the current sensor requirement of slave cells can be eliminated by implementing the control method into only the master cell's microcontroller. In this paper, the control method is implemented into the master cell's microcontroller and θ is sent to the slave cell via a frequency-modulated signal. Thus, the self-equalization of input voltages and output current is achieved for the identical cells.

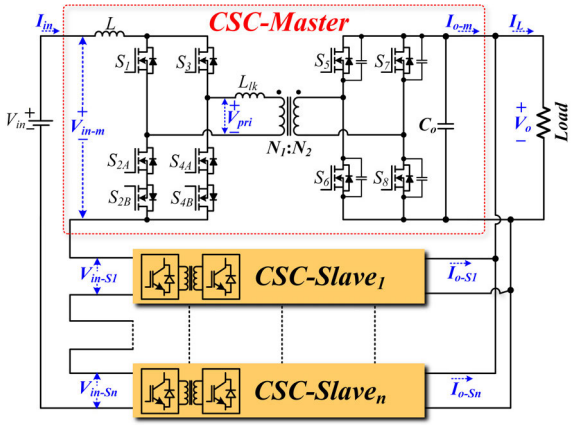

FIGURE 4. Input series output parallel configuration of the isolated CSC.

III. DESIGN OF PROPOSED CONTROL METHOD

The super twisting algorithm-based sliding mode control (ST-SMC) strategy is proposed for the input current control of ISOP-CSC. Since the control algorithm works only in the master cell, the design is presented considering a single cell shown in Fig. 1. SMC can be designed in discrete-time or continuous-time [22], [23], [24], [25], [26], [27], [28], [29]. Both discrete time and continuous time design focus on the distinct features of SMC. However, their design procedures as well as stability analysis and controller gains are different. Discrete-time SMC methods are more efficient regarding computational complexity than continuous SMC due to the microcontrollers working in discrete time. However, designing discrete-time SMCs needs more effort. Therefore, especially in power electronics, the SMC methods are designed in continuous time and implemented into the microcontrollers and sufficient results are obtained [27], [28], [29] with the help of massive improvements in microcontroller technologies.

SMC theory is based on forcing the control error to be around the sliding surface. The sliding surface function is determined based on the required control variables for the stable operation of power converters. Since the control objective is to regulate the input current of ISOP-CSC, the sliding surface function is defined as the control error

$$\sigma = x = I_{in}^* - I_{in} \tag{9}$$

where I_{in}^* denotes the reference of input current. As mentioned before, the phase shift (θ) value determines the time shift between the switching signals in Fig. 2. Therefore, θ should be generated by the control method to achieve current control. Since the sliding surface function is the

error between input current and its reference, it may include high frequency oscillations that is known as chattering. This phenomenon causes high variations in the controller output. Therefore, the suppression of the chattering is essential to prevent high frequency variations in the θ. Different approaches depending on the system's order are proposed to eliminate the effect of perturbations and chattering [30]. The super twisting differentiator is not sensible to perturbation [31] and the chattering problems are also minimized compared to first-order sliding-mode control [32]. The super-twisting SMC approach is an effective method for reducing chattering. The ST-SMC function can be defined by

$$\begin{aligned} \theta &= u_1 + u_2, \\ u_1 &= -\alpha \left|\sigma\right|^{0.5} sign\left(\sigma\right), \\ \dot{u}_2 &= -\beta sign\left(\sigma\right) \end{aligned} \tag{10}$$

where α and β are positive coefficients that determine the controller performance. α affects the dynamic response while β is effective in eliminating the steady-state error. The controller gains are tuned by following procedure: (1) β is increased step by step until the steady-state error is eliminated, (2) thereafter a consecutive step change is applied, and α is increased step by step until eliminating the overshoots and undershoots. It is worth noting that the controller performance can slightly be deviated for different step changes. Therefore, considering the most possible dynamic transition case during the tuning may lead to better controller performance. Besides the controller performance, the stability of ST-SMC should be checked. The stability is checked based on the analysis in [33]. The stability of SMC is guaranteed if the Lyapunov function satisfies the following conditions [34]:

$$\begin{aligned} &\bullet\ V > 0 \text{ for } (\sigma \neq 0) \\ &\bullet\ V \to \infty \text{ for } (\sigma \to \infty) \\ &\bullet\ \dot{V} < 0 \text{ for all } (\sigma \neq 0). \end{aligned} \tag{11}$$

The first and second conditions are satisfied due to the squared definition of the Lyapunov function candidate as follows

$$V = 2\beta \left|\sigma\right| + \frac{1}{2}u_2^2 + \frac{1}{2}\left(\alpha \left|\sigma\right|^{0.5} sign\left(\sigma\right) - u_2\right)^2 \tag{12}$$

where $u_2 = -\beta \int sign(\sigma)dt$. The quadratic form of (12) can be written as follows [33]

$$\begin{aligned} V = \xi^T P \xi = &\begin{bmatrix} \left|\sigma\right|^{0.5} sign\left(\sigma\right) u_2 \end{bmatrix} \\ &\times \begin{bmatrix} 2\beta + 0.5\alpha^2 & -0.5\alpha \\ -0.5\alpha & 1 \end{bmatrix} \begin{bmatrix} \left|\sigma\right|^{0.5} sign\left(\sigma\right) \\ u_2 \end{bmatrix} \end{aligned} \tag{13}$$

Now, the derivative function can be obtained as follows

$$\dot{V} = \dot{\xi}^T P \xi + \xi^T P \dot{\xi} = -\frac{1}{\left|\sigma\right|^{0.5}} \xi^T Q \xi \tag{14}$$

where Q is defined as follows

$$Q = \begin{bmatrix} \alpha\beta + 0.5\alpha^3 & -0.5\alpha^2 \\ -0.5\alpha^2 & 0.5\alpha \end{bmatrix} \tag{15}$$

To satisfy the third condition in (11), $\xi^T Q \xi$ in (14) should be positive. It is proved in [33] that $\xi^T Q \xi$ will be positive when $\alpha > 0$ and $\beta > 0$. Since all the conditions in (11) are satisfied, the ST-SMC method is stable.

Fig. 5 depicts the block diagram of the proposed control method and ISOP-connected two CSC cells. Clearly, the proposed method can be implemented by measuring only the input current. Also, the ST-SMC method is implemented only into the master cell's microcontroller. The controller generates θ and shares it with the slave cell. The modulation strategy in Fig. 2 is implemented into the slave cell's microcontrollers. Thus, all the cells in ISOP-CSC are operated with the same θ. Therefore, the system can be operated independently from the number of slave cells. This feature provides flexibility for the ISOP connection.

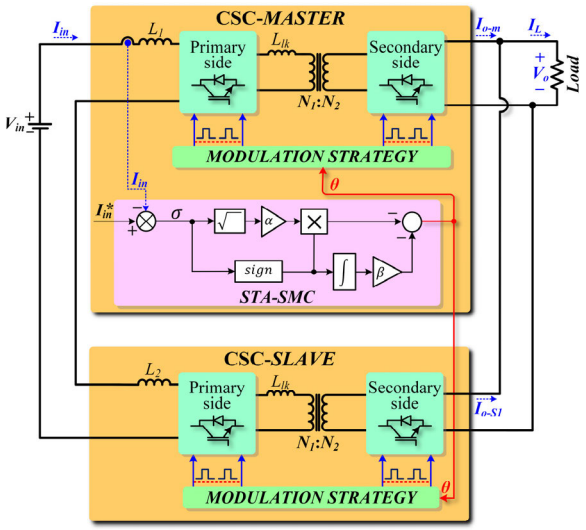

FIGURE 5. Control scheme of the ISOP-CSC.

IV. EXPERIMENTAL VERIFICATION

The performance of the proposed control method is investigated by experimental studies. The experimental prototype was built by input series output parallel connection of two CSC shown in Fig. 6. The complete experimental setup is shown in Fig. 7.

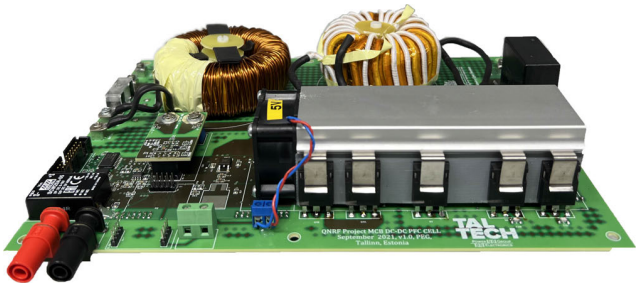

FIGURE 6. One cell isolated CSC prototype.

The system and control parameters are given in Table 2. TMS320F28379 from Texas Instruments microcontroller is

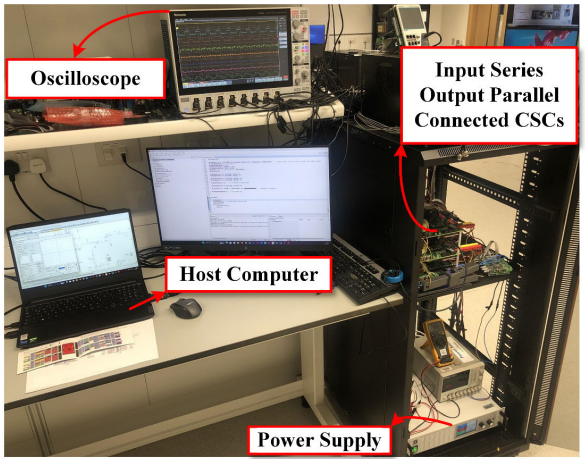

FIGURE 7. Experimental setup.

used to run the developed control algorithm and generate switching signals. The control algorithm is designed in PSIM software. The control algorithm is implemented only into the master cell's microcontroller. In addition, the phase shift value produced by the ST-SMC method is transferred from the master cell to slave cells via an IO pin of the microcontroller. The switching signals of the slave cells are generated based on the received phase shift value. Thus, each cell (both master and slave) operated with the same phase shift. The performances of the ISOP-CSC converter and control algorithm are investigated by four different experimental scenarios given in Table 3.

TABLE 2. System and control parameters.

Parameters	Symbol	Value
Input voltage (3 cells)	V_{in}	440 V_{rms}
Inductance (1 cell)	L	1.35 mH
Leakage inductance	L_{lk}	5 µH
Output capacitance (1 cell)	C_o	30µF
Transformer turns ratio	N_1:N_2	1:1.47
Duty ratios	D_a and D_b	0.506 and 0.45
ST-SMC coefficients	α, β	0.01, 240
Switching frequency	f_{sw}	50kHz

TABLE 3. List of experimental scenarios.

Operating condition	Result	Variation
Steady-state	Fig. 8 and 9	N/A
Step change in I^*_{in}	Fig. 10	1.5A to 2.5A
Step change in the load resistance	Fig. 11	400Ω to 200Ω
Step change in V_{in}	Fig. 12	150V to 200V

Fig. 8 shows the steady-state voltage and currents of ISOP-CSC converter. The reference current was set to 2.5A and load resistance was 200Ω during these tests. Since the

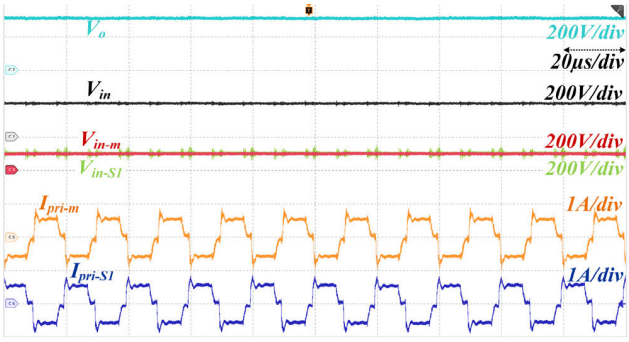

FIGURE 8. ISOP-CSC voltages and transformer currents.

cells are connected in series, the RMS value of transformer currents (I_{pri-m} and I_{pri-S1}) are the same. Also, the cell voltages (V_{in-m} and V_{in-S1}) are equal to half of the total input voltage (V_{in}) due to two cells are connected in series. Fig. 8 verifies that the voltage stress of cells is equal to $V_{in}/(n+1)$.

Fig. 9 shows the input and output currents of ISOP-CSC. The input current includes high-frequency ripples due to the charging and discharging of the inductor in each switching period. Although the output current of each cell (I_{o-m} and I_{o-S1}) includes oscillations, the load current has less oscillations. On the other hand, the average value of I_{o-m} and I_{o-S1} are equal. Therefore, it can be concluded that the total power is shared between the master and slave cells. Like the output currents, each cell's input current waveforms are very similar due to the same phase shift value used in both master and slave CSCs. It can be concluded that the current sharing between the cells and proper operation of ISOP-CSC in steady-state can be successfully achieved by using the same phase shift value in each cell.

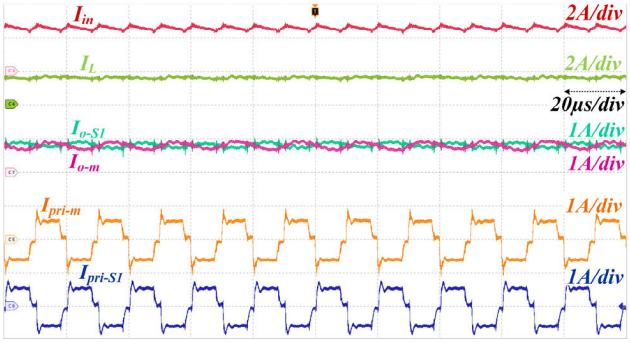

FIGURE 9. ISOP-CSC currents.

The dynamic response of the proposed control method is investigated under step change in the reference current. The reference current value in the control software is increased from 1.5A to 2.5A and reduced to 1.5A again as shown in Fig. 10. The input voltage and load resistance are kept constant during this test as 200V and 300Ω, respectively. The magnified part of the step change from 1.5A to 2.5A shows that the input current is regulated to its new reference in *10ms*. Since the input power is increased from 300W

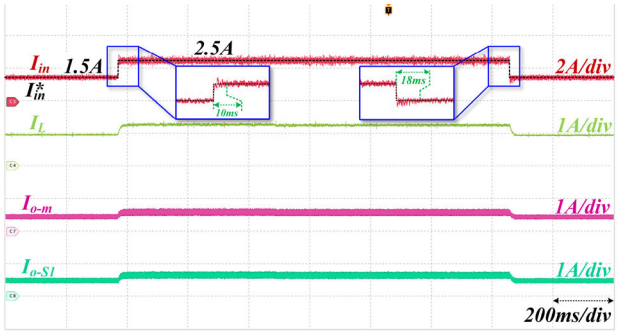

FIGURE 10. Dynamic responses under step change in reference current.

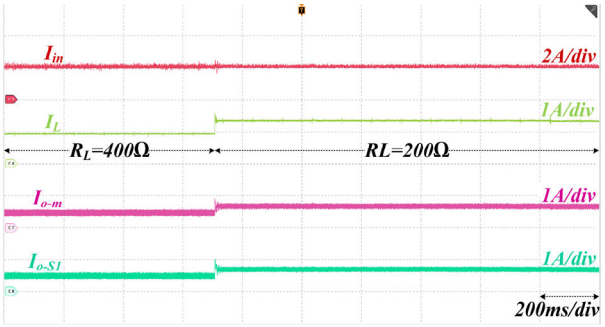

FIGURE 11. Dynamic responses under step change in load resistance current.

to 500W, I_L is also increased. Also, I_L is shared between the master and slave cells before and after the step change. Thereafter, the reference current is reduced to the initial value. The input current is regulated to 1.5A in *18ms* as shown in Fig. 10. The result proves that the output current sharing of the ISOP-CSC is successfully achieved under different input current conditions.

The dynamic performance of the proposed control method is further investigated under step change in the load resistance from 400Ω to 200Ω while the reference current is 2A as shown in Fig. 11. The input current is regulated to 2A, and output current is shared between the cells before the step change. An overshot occurs in the load and cell currents when the load resistance is reduced. However, the deviations in the input current are very small compared to output currents due to the control method designed based on input current control. Nevertheless, the input current is regulated to its reference and the output current is shared between the cells after the transition time as shown in Fig. 11.

Fig. 12. shows the dynamic performance of the proposed control method under step change in the input voltage from 150V to 200V. The reference current and load resistance are kept constant during this test as 2A and 200Ω, respectively. As clearly shown in Fig. 12, the input current is successfully regulated to its reference before and after the step change. Also, the results reveal that neither undershoot nor overshoot occurred during the transition time. Since the input power is increased from 300W to 400W, the output current also increases after the step change. Like the previous step change tests, the output current is shared between the cells.

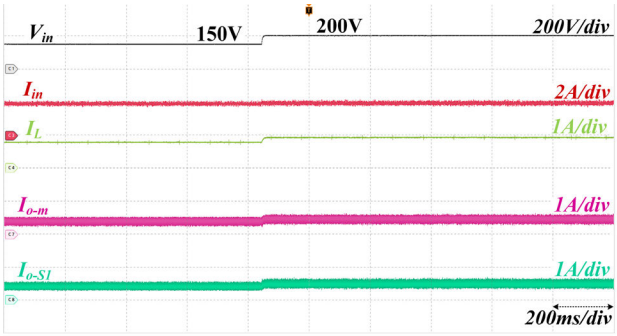

FIGURE 12. Dynamic responses under step change in the input voltage.

TABLE 4. Comparison of ISOP converter control strategies.

Description	[15]	[16]	[18]	[20]	Proposed
Topology	DAB	DAB	Forward Converter	Phase-shifted Full-bridge Converter	Current Source Converter
Control approach	PI Controller (Decentralized)	PI Controller (Centralized)	Common-Duty-Ratio Control (Centralized)	Active Damping Control (Centralized)	ST-SMC (Centralized)
Number of required data/signal transfer	Not needed	Not needed (due to implementation into one microcontroller)	1	1	1
Required sensor number	*2n* voltage sensors	*n*+1 voltage sensors	1 voltage and 1 current sensors	2 voltage sensors	1 current sensor
Robustness to sensing mismatch between the cells	Not robust	Not robust	Robust	Robust	Robust
Simultaneous measurement of each cell's variables	Needed	Needed	Not needed	Not needed	Not needed
Reliability	Medium	Medium	High	High	High
Modularity	Restricted	Restricted	High	High	High

n: Number of slave cells

The results reveal that the proposed method successfully regulates the input current under different input voltage conditions without using voltage sensors.

The comparison of the proposed strategy with four existing studies is given in Table 4. Since the decentralized control techniques require individual sensing of each cell's variables, the technique in [15] is not robust against sensing mismatches. Similarly, the centralized technique in [16] needs to sense the input voltage of each cell and output voltage. Therefore, these techniques require a lot of sensors compared to other studies. On the other hand, the reliability of these two techniques is improved by eliminating data/signal transfer between the cells. However, the reliability is restricted due to the measurement of voltages simultaneously. Since the control techniques in [15] and [16] are implemented into one microcontroller, modularity is also restricted due to the limited number of microcontroller channels. Centralized techniques with one data/signal transfer are used in [18], [20] and the proposed technique. Since these techniques only need sensing of the master cell's variables, [18], [20] and the proposed technique are robust against sensing mismatches. Eliminating sensing mismatches and a low number of data/signal transfers improves the reliability of these centralized techniques. Compared to [18] and [20], the proposed technique requires fewer sensors.

V. CONCLUSION

This paper proposes the ST-SMC method for an ISOP-CSC with master and slave cells. The proposed control method is designed to the input current control of ISOP-CSC. The control method works on the master cell's microcontroller and sends the phase shift value to the slave cell. The switching of the master and slave cells with the same phase shift value allows flowing the same currents on the cells. The results reveal that the input current control of ISOP-CSC is provided under steady-state and dynamic conditions. Furthermore, the input voltage and output current are shared by the master and slave cells under both operating conditions. Thus, the expectations of the ISOP converter are satisfied by controlling only the input current. Since the proposed method is implemented in the master cell, only one current sensor is required. Thus, the sensing issues between the cells are eliminated.

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