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RESEARCH ARTICLE

Internal Model Control Scheme-Based Voltage and Current Mode Control of DC–DC Boost Converter

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ABSTRACT In this work, a current mode control has been proposed for output voltage regulation of DC–DC boost converter. The proposed controller has a cascade control structure with two feedback loops. And the internal model control scheme has been used in both the control loops. The advantageous feature lies in so as to adjust the performance and robustness of the closed-loop system as it has only one tuning parameter. The performance of the proposed internal model control based current mode control of DC–DC boost converter has been evaluated in hardware setup for set point as well as load disturbance response. The load disturbance response has been analyzed by considering random changes in input voltage and load. The faster transient response with a low-rise time and settling time has been observed in the proposed current mode control in comparison with voltage mode control as well as recently reported work. The robustness analysis of the proposed schemes has also been conducted using the small gain theorem and is further validated through hardware experiment. The proposed scheme is robustly stable up to 23% simultaneous change in inductance, capacitance and resistance.

INDEX TERMS DC/DC boost converter, internal model control, voltage mode control, current mode control.

I. INTRODUCTION

DC-DC boost converter (BC) are used in various applications such as switched mode power supplies, energy conversion systems, electric vehicles, etc. In these applications, the BC is required to provide a regulated output voltage despite of changes in load and input voltage. The output voltage regulation of BC is a challenging task due to switched non-linear behavior, parametric uncertainty, and unmodeled dynamics, like parasitic resistance, uncertain values of capacitance, inductance, and voltage drop across the switch and diode [1].

For the BC, the generalized control approach involves the model obtained through averaging in different modes of operation and linearizing around the steady-state operating point [2], [3]. The resulting model consists of non-minimum phase (NMP) zero in the control signal-to-output voltage transfer function model, which poses an additional control challenge due to limitations on achievable performance [4]. In these systems, a zero is present on the right-hand side (RHS) of the s-plane and by increasing the gain in the conventional controller, the closed-loop system pole will be attracted towards RHS zero. This ultimately limits the controller gain and makes the controller design difficult. And also, the location of RHS zero is directly related to the load and inversely proportional to the voltage gain. It creates difficulty in the controller design for high voltage gain and heavy load applications [5].

To address these issues, two control modes for BC are available in the literature, namely, voltage mode (VM) and

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current mode (CM) control. In VM control, the output voltage is compared to the reference voltage command and the error is sent to the controller, which changes the duty cycle to reach the reference voltage.

In CM control, an additional current sensor is used and the output voltage as well as the inductor current are controlled. This mode is implemented as a cascade control structure consisting of two control loops. Cascade control makes use of two or more measurements with a single manipulated input to improve the response of the primary (outer) loop output. When the primary process has a considerably greater time constant with a time delay or RHS zero and, the secondary (inner) process has a smaller time constant with little to no dead time or NMP behaviour, cascade control can be utilised to successfully reject secondary process disturbances. If the secondary loop dynamics is not much faster than the dynamics of the primary loop, no benefit lies in adopting the cascade control [6], [7], [8].

Various control strategies have been recently proposed for the control of BC in the VM as well as in CM. A few popular control strategies used in these modes are fractional order control [9], predictive control [10], stepping control [11], sliding mode control [12], [13], [14], robust control [15], [16] and observer based control [17], [18], [19]. The performance of any control scheme is greatly affected by the dynamic model of the system. With improved modeling accuracy, better control performance can be achieved. In the above-mentioned schemes, few methods use the dynamical model to derive the control law [12], [13], [14], [15], whereas in other methods, the dynamical model is directly used as an integral part of the control scheme, like model predictive control (MPC), the Smith predictor scheme, and internal model control (IMC).

The control schemes consisting model of the system as an integral part of the controller are better suited for systems having NMP zero, like, MPC [20], [21] and the IMC scheme [22], [23], [24]. The MPC uses the internal model of the system for online prediction and involves extensive offline computations. The IMC structure is an unconstrained form of MPC, and its design procedure is very simple. Being a robust control scheme, it utilizes the advantages of an open-loop control structure in terms of stability. Stability of the overall system is guaranteed in the open-loop control system for stable systems if controlled by a stable controller. Utilizing these IMC scheme features, Ahmad and Ali [25] have also exploited the characteristics of the IMC scheme to design an active disturbance rejection controller for the output voltage regulation of the BC. Kobaku et al. [26] used a two degree of freedom IMC which significantly reduce the effect of disturbance leading to computational burden. A closed loop test-based modeling technique of BC is used by Jha et al. [27] in which they controlled BC using IMC and direct synthesis (DS) based approach. According to their observation, IMC based approach performs satisfactorily better than conventional proportional-integral based DS approach. Similarly, a test-based modeling is also performed in [28] for controlling of BC using characteristics of two degree of freedom IMC.

TABLE 1. Abbreviation summary.

Description	Abbreviation
Boost converter	BC
Non minimum phase	NMP
Right-hand side	RHS
Voltage mode	VM
Current mode	CM
Internal model control	IMC
Direct synthesis	DS
Integral absolute error	IAE

The above-mentioned literature has used the IMC scheme for the VM control of BC. The CM control using cascade control strategy has been adopted by several researchers in the literature [29], [30], [31], [32], [33]. Kim and Lee [29] have proposed cascade control structure for output voltage regulation of BC. They have used robust feedback linearization technique for the controller design. Kim and Son [30] has obtained improved performance using a new cascade control structure by combining Integral Proportional-Proportional Integral cascade control and nested reduced order observer. A multivariable approach-based output voltage tracking method is proposed by [31]. A non-linear disturbance observer is used to identify the disturbances and performance recovery output voltage controller is derived which exponentially eliminates the tracking error. Kim and Ahn [32] has obtained the improvement over [31] by forcing the output voltage to track the desired target trajectory guided by a low-pass filter. They have proposed a self-tuning algorithm incorporating disturbance observers. In the aforementioned discussed CM strategies, BC model is not used as a part of the controller.

Approaches that include model as part of the controller, for CM control of BC such as IMC, MPC etc., are less investigated in the literature. With this, Verma and Anwar [33] have proposed CM and VM control-based IMC scheme of BC in simulation only. This article is an extended version of [33].

In this work, an IMC based CM control structure for BC has been proposed. In CM, the inner loop is the current control loop, where the inductor current is regulated, and the outer loop is the voltage control loop. In both loops, IMC structures have been used and the controllers are designed by considering faster inner loop dynamics than outer loop dynamics. This facilitates the load-disturbance rejection performance by mitigating the effect of disturbance on the outer loop. The controller tuning parameter is obtained using minimizing the cost function in the form of integral absolute error (IAE). The abbreviation used in this manuscript are summarized in Table 1.

The performance of the proposed CM scheme has been evaluated in hardware setup for both the set-point and the load-disturbance rejection response. The load-disturbance rejection response has been analyzed by considering random changes in the input voltage and load. The proposed control scheme has also been compared with recently reported work and improved performance has been observed. The robustness analysis has been studied using the small gain theorem. The main contribution of this work is summarized as follows:

- The CM control is proposed where both the inner and outer loops are controlled through the IMC structure. It maintains the average inductor current value within the limits.
- The suggested CM scheme is also validated through a hardware set-up of the BC and improved results are found as compared to the recently reported methods.
- The robustness of the proposed CM scheme has been analyzed using small gain theorem. The control scheme is robustly stable up to 23% change in parametric uncertainty.

Rest of the manuscript is organized as follows: In Section II, state-space averaged modeling of BC has been discussed, followed by a brief discussion of the IMC scheme. The proposed CM scheme is also discussed in this section. Robustness analysis is carried out in Section III. The performance of the proposed CM scheme is experimentally evaluated in Section IV. Section V concludes the paper.

II. STATE SPACE AVERAGED MODELING AND CONTROLLER DESIGN FOR BC

In this section, the model of the BC has been derived through state space averaging technique. Further, the IMC scheme for VM control of BC is discussed in brief followed by discussion of the proposed CM controller.

A. MODELING OF DC-DC BOOST CONVERTER

A circuit diagram of a BC is shown in Figure. 1. V_{in} is the input voltage, and V_o is the output voltage of the BC. L, C, S, and R_o are inductor, capacitor, switch, and load resistance, respectively. i_L is the inductor current and v_c is the voltage across the capacitor. Here, the pulse width modulation (PWM) switching technique is considered with duty ratio D. The switch is ON for a period of DT and OFF for a period of $(1-D)T$, where, T is the time period of the PWM signal.

Considering the BC operating in continuous conduction mode (CCM), the averaged state space model is obtained as:

$$\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-D)}{L} \\ \frac{(1-D)}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{V_C}{L} \\ 0 & \frac{-I_L}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{d} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \hat{i}_L \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_o \end{bmatrix}. \quad (2)$$

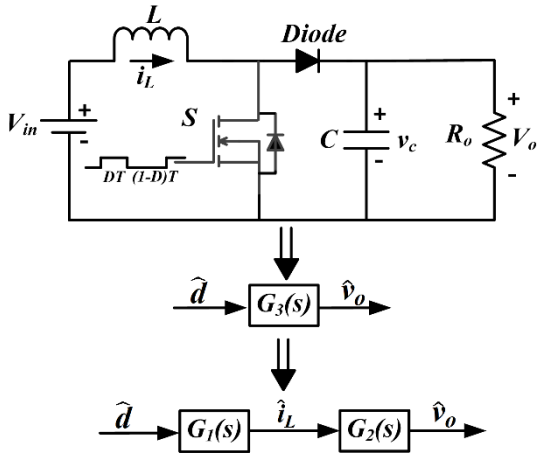

FIGURE 1. Boost converter circuit and its model representation.

where, $\hat{i}_L$, $\hat{v}_o$, $\hat{v}_{in}$ and $\hat{d}$ are the perturbed values of inductor current, output voltage, input voltage, and duty cycle, around their steady state counterparts I_L, V_o, V_{in} and D, respectively. The transfer function from inductor current-to-output voltage is obtained as:

$$G_1(s) = \frac{\hat{v}_o(s)}{\hat{i}_L(s)} = \frac{-LI_L s + (1-D)V_o}{V_o C s + 2(1-D)I_L}. \quad (3)$$

The transfer function from duty ratio-to-inductor current is derived as:

$$G_2(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_o C s + 2(1-D)I_L}{LCs^2 + \frac{L}{R}s + (1-D)^2}. \quad (4)$$

And, the transfer function from duty ratio-to-output voltage of the BC can be derived as:

$$G_3(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-LI_L s + (1-D)V_o}{LCs^2 + \frac{L}{R}s + (1-D)^2}. \quad (5)$$

In the VM control, the transfer function, $G_3(s)$ is utilized in the controller design, where the output voltage, V_o is regulated by controlling the duty ratio of the BC.

For the CM, an additional sensor is used to monitor and control the inductor current along with the output voltage of the BC. Thus, the BC model,$G_3(s)$ is represented as a cascade of transfer functions $G_1(s)$ and $G_2(s)$ as shown in Figure 1. The oscillatory dynamics of the BC make it difficult to control, and the existence of RHS zero in the transfer functions, $G_1(s)$ and $G_3(s)$ further complicates the control issue. This is successfully eliminated in this manuscript with the use of the IMC scheme to control the BC in VM as well as in CM control.

B. VOLTAGE MODE CONTROL OF BOOST CONVERTER USING IMC SCHEME

The IMC scheme is a tried-and-true robust control scheme that has solved numerous control problems in a variety of fields, including process control [22], [23], [24], drive applications [34], [35], servo systems [36], [37] chemical

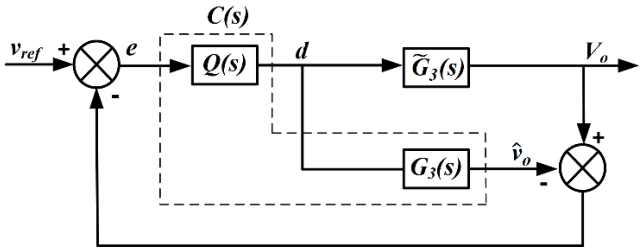

FIGURE 2. Basic IMC structure.

reactor plants [38]. Its simplicity in design (as it has only one adjustable parameter) and lower computational burden are its main attractions. In addition to this, the guaranteed stability of open loop stable systems makes this scheme popular and suitable for low-cost simple applications such as water pumping systems.

The IMC structure is shown in Figure 2, where, $\tilde{G}_3(s)$and $G_3(s)$ are the BC and its model, respectively. In the IMC scheme, the model of the system is an integral part of the controller. In the case of perfect modelling (i.e., $\tilde{G}_3(s) = G_3(s)$), the difference between the output voltage of BC (V_o) and its model $(\hat{v}_o)$ for the same controlling signal d is zero. Thus, the IMC structure behaves like an open loop control system. The controller $Q(s)$ is designed in such a way that the output voltage V_o tracks the reference voltage v_{ref} in open loop. However, in the event of a modelling error, which is unavoidable in a practical scenario, the feedback path is activated, and V_o tracks the v_{ref}.

The controller design procedure of the IMC scheme is discussed here in brief. For this, the system model is divided into two parts as follows:,

$$G_3(s) = G_3^+(s)\, G_3^-(s) \tag{6}$$

where, $G_3^-(s)$ is the invertible part and $G_3^+(s)$ is its non-invertible part. The invertible part is generally composed of the zero and the pole in the left half of s-plane, whereas the non-invertible part is composed of RHS zeros. The IMC controller is designed as follows:

$$Q(s) = [G_3^-(s)]^{-1} \times f(s) \tag{7}$$

where,

$$f(s) = \frac{1}{(\lambda s + 1)^n}.$$

Here, λ is a user specified tuning parameter and n is the order of filter. A lower value of λ will give a faster response,

whereas a higher value results in sluggish response [39]. The order of the filter, n is chosen in order to make the IMC controller, $Q(s)$ proper.

The schematic diagram for the implementation of IMC structure to VM control of BC is shown in Figure 3. Using BC model from (5), the IMC controller is obtained as:

$$Q(s) = \frac{LCs^2 + \frac{L}{R}s + (1-D)^2}{(1-D)\,V_o} \times \frac{1}{(\lambda s + 1)^n}. \tag{8}$$

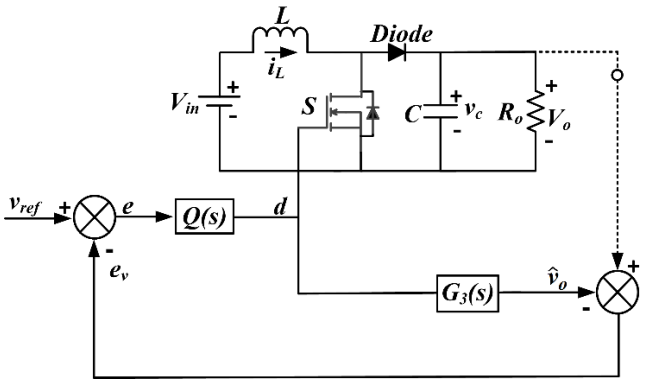

FIGURE 3. Voltage mode control of boost converter with IMC structure.

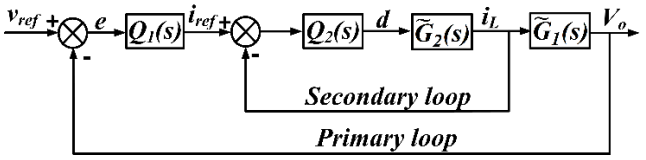

FIGURE 4. Conventional cascade control scheme.

C. CURRENT MODE CONTROL OF BOOST CONVERTER USING IMC SCHEME

The CM scheme for BC is implemented using cascade control configuration. Cascade control offers an advantage when inner loop senses the inductor current and makes an effort to maintain either the average current value or the peak current value within the limits over the course of one switching cycle. With this, internal current feedback is used in the cascade control approach to improve response speed and limit overcurrent. To increase the closed loop bandwidth, a current programmed control is usually required. Also, the order of the system is decreased by one, which makes the outer control loop design much simpler [40], [41].

To apply cascade control scheme, the plant is segregated into two cascaded subsystems, and with the use of an additional sensors, two control loops are constructed. The conventional cascade control configuration is shown in Figure 4. Here, the BC model ($\tilde{G}_3(s)$) is represented as cascaded $\tilde{G}_1(s)$ (primary plant) and $\tilde{G}_2(s)$ (secondary plant). The output of primary controller is the reference command for the inner loop, where the inner loop controller controls the inductor current. For this reason, the inner loop is also known as the ''secondary loop,'' whereas, the outer loop is known as the ''primary loop.''

In this work, both the inner and the outer loops are controlled using the IMC scheme as shown in Figure 5 and its implementation in BC circuit is shown in Figure 6. In this Figure, the inner loop error is the difference between the inductor current of the BC and its model (i.e., $e_i = i_L - \hat{i}_L$). This error is compensated using the inner loop IMC controller, $Q_2(s)$. The inner loop is however, used to circumvent the effect of disturbances before it reaches the

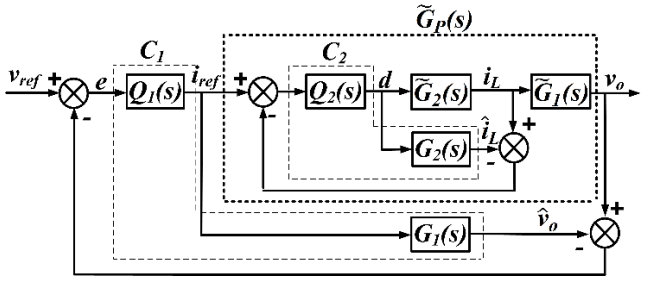

FIGURE 5. Current mode cascade control with IMC structure.

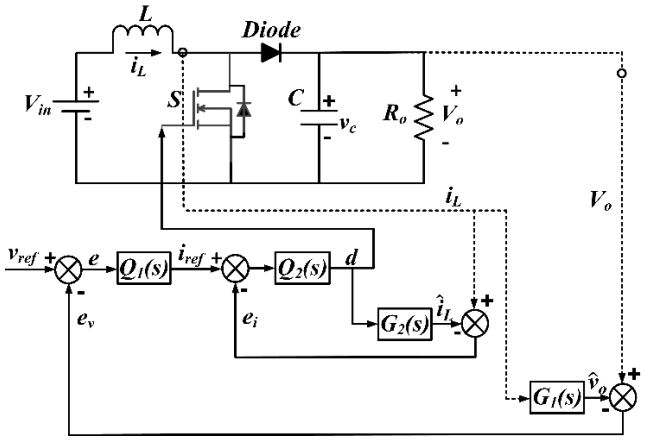

FIGURE 6. Current mode cascade control of boost converter with IMC structure.

outer loop which also helps in reducing the overshoots. The outer loop error (i.e., e_v) is the difference between the output voltage, V_o from the BC and output voltage, $\hat{v}_o$ of its model.

The outer loop is also controlled using the IMC controller, $Q_1(s)$. Output of the outer loop controller, i_{ref} act as a remote reference command to the inner loop.

The inner loop controller $Q_2(s)$ is designed first, followed by the design of the outer loop controller $Q_1(s)$ using the IMC principle discussed in subsection II-B. To design inner loop controller, the inner loop plant model $G_2(s)$ given in (4) is divided into two parts as given by:

$$G_2(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = G_2^+(s)\, G_2^-(s) \tag{9}$$

where,

$$G_2^-(s) = \frac{V_o Cs + 2(1-D) I_L}{LCs^2 + \frac{L}{R}s + (1-D)^2}, \quad G_2^+(s) = 1.$$

The inner loop controller is designed as:

$$Q_2(s) = [G_2^-(s)]^{-1} f_2(s) \tag{10}$$

where,

$$f_2(s) = \frac{1}{(\lambda_2 s + 1)^{n_2}}.$$

λ_2 is the tuning parameter of the inner loop filter and n_2 is the order which is selected so as to make the IMC controller proper. The inner loop controller is written as:

$$Q_2(s) = \frac{LCs^2 + \frac{L}{R}s + (1-D)^2}{V_o Cs + 2(1-D) I_L} \times \frac{1}{(\lambda_2 s + 1)^{n_2}} \tag{11}$$

Here, n_2 should be greater than or equal to 1 to fulfill the design requirement of the controller.

After designing the inner loop controller, the outer loop controller is designed by considering the tuned inner loop as a part of overall plant. By assuming a perfect model of the inner loop ($\tilde{G}_2(s) = G_2(s)$), the inner loop is obtained from (9) and (11):

$$\frac{\hat{i}_L(s)}{i_{ref}(s)} = Q_2(s) \times G_2(s) = \frac{1}{(\lambda_2 s + 1)^{n_2}} \tag{12}$$

To design the outer loop controller, the overall plant including inner loop, is represented as:

$$\begin{aligned} \tilde{G}_p(s) &= Q_2(s)\, G_2(s)\, G_1(s) \\ &= \frac{1}{(\lambda_2 s + 1)^{n_2}} \times \frac{-LI_L s + (1-D) V_o}{V_o Cs + 2(1-D) I_L} \end{aligned} \tag{13}$$

This overall plant $\tilde{G}_p(s)$ is divided into two parts, as given below:

$$\tilde{G}_p(s) = \tilde{G}_p^+(s)\, \tilde{G}_p^-(s), \tag{14}$$

where,

$$\tilde{G}_p^-(s) = \frac{1}{(\lambda_2 s + 1)^{n_2}} \times \frac{(1-D) V_o}{V_o Cs + 2(1-D) I_L},$$

and

$$\tilde{G}_p^+(s) = \frac{-LI_L s}{(1-D) V_o} + 1$$

The outer loop controller is now designed as:

$$Q_1(s) = [\tilde{G}_p^-(s)]^{-1} f_1(s) \tag{15}$$

where,

$$f_1(s) = \frac{1}{(\lambda_1 s + 1)^{n_1}}$$

λ_1 is the tuning parameter for the outer loop and n_1 is the order of the filter.

Thus, the outer loop controller becomes:

$$\begin{aligned} Q_1(s) = \frac{(\lambda_2 s + 1)^{n_2}}{1} &\times \frac{V_o Cs + 2(1-D) I_L}{(1-D) V_o} \\ &\times \frac{1}{(\lambda_1 s + 1)^{n_1}}. \end{aligned} \tag{16}$$

Again here, n_2 should be greater than or equal to 2 to meet design requirements of the outer loop controller. Thus, the controllers have been designed for CM scheme for BC. Next section discusses about the guidelines for the selection of tuning parameters of both the control loops.

TABLE 2. Specifications of BC.

Parameters	Values
Input Voltage (V_{in})	12V
Output Voltage (V_o)	18V
Load resistance (R_L)	50Ω
Capacitor (C)	1100μF
Inductor (L)	5mH
Duty ratio (D)	0.33
Switching frequency (f_s)	20kHz

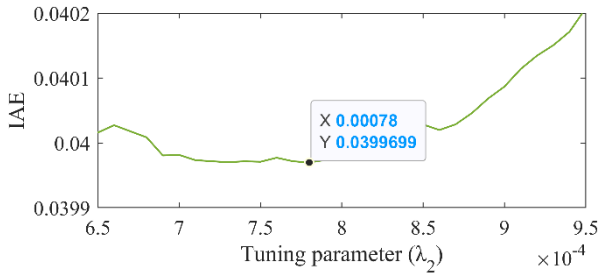

FIGURE 7. Plot of IAE vs tuning parameter λ_2 for the inner loop of proposed CM control.

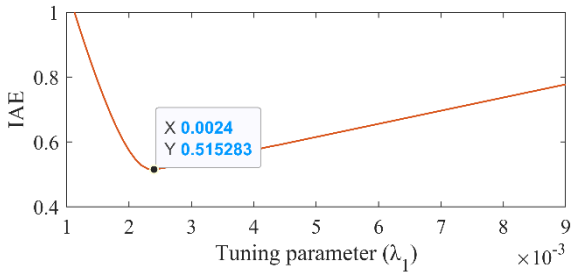

FIGURE 8. Plot of IAE vs tuning parameter λ_1 for the outer loop of proposed CM control.

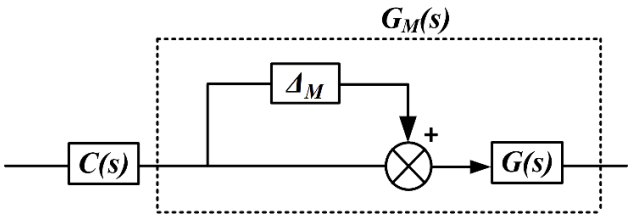

FIGURE 9. Loop gain with multiplicative uncertainty.

D. GUIDELINES FOR CONTROLLER DESIGN

Selection of tuning parameters (λ_1 and λ_2) plays an important role in the performance enhancement of closed-loop control system. So, it should be properly selected in the control of BC using the IMC scheme in proposed structure (Figure 5).

Here, these tuning parameters are selected in such a way to have minimum integral of absolute error (IAE) [42] defined as:

$$IAE = \int_0^\infty |e(t)|dt \tag{17}$$

To demonstrate it, a BC with parameter given in Table 2 has been considered. The inner loop tuning parameter, λ_2 is varied from 0.00065 to 0.00095 with $n_2 = 1$ and IMC based control scheme has been implemented. The IAE values have been recorded and is plotted against tuning parameter, λ_2. This plot is shown in Figure 7. From this figure, minimum IAE value is 0.0399 which is corresponding to the tuning parameter λ_2 = 0.0078, thus, it is used for the inner loop controller design.

To select the outer loop controller, the optimum inner loop controller along with secondary plant is considered as a part of primary plant. Subsequently, the outer loop tuning parameter, λ_1 is varied from 0.001 to 0.009 and IAE value is noted. The plot of IAE value with λ_1 is shown in Figure 8. For this Figure, the minimum value of IAE is 0.515 for $\lambda_1 = 0.0024$.

The proposed CM scheme can be implemented for voltage regulation of BC by following the procedure given below:

Step 1. Obtain the cascaded model of BC, $G_1(s)$ and $G_2(s)$ in terms of circuit parameter information using (3) and (4).

Step 2. To design inner loop controller $Q_2(s)$, divide the inner plant $G_2(s)$ into invertible and non-invertible part as per IMC design procedure.

Step 3. Obtain optimal λ_2 by varying its value and computing IAE value as discussed in subsection II-D.

Step 4. Design inner loop controller using (11) with optimal λ_2 from Step 3.

Step 5. Outer loop controller is designed by following the Step 2 and Step 3 by considering inner loop as a part of the plant. The controller $Q_1(s)$ can be designed using (16).

III. ROBUSTNESS ANALYSIS

The robustness analysis of the control system is important as it ensures satisfactory performance under plant model uncertainty. These modelling uncertainties may arise due to (i) the linearization of non-linearities, (ii) imperfection in measurement devices, and (iii) a reduction of model order for simplicity in controller design [43].

Also, the implemented controller may vary from the one obtained by solving the controller design problem. Here, the robustness analysis is being done using small gain theorem [44], [45].

With multiplicative uncertainty shown in Figure 9, the open loop gain of a single input single output (SISO) feedback control system is given as,

$$G_M(j\omega) = G(j\omega)(1+\Delta_M(j\omega)) \tag{18}$$

Thus, the requirement for the system to be robustly stable in case with multiplicative uncertainty which gives an upper bound on the complementary sensitivity function, $T(j\omega)$ is:

$$|T(j\omega)| < 1/|\Delta_M(j\omega)| \forall\omega(-\infty,\infty) \tag{19}$$

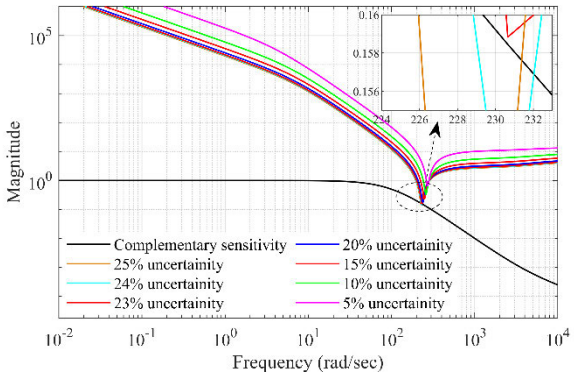

FIGURE 10. Frequency response of complementary sensitivity and parametric uncertainty of voltage mode control.

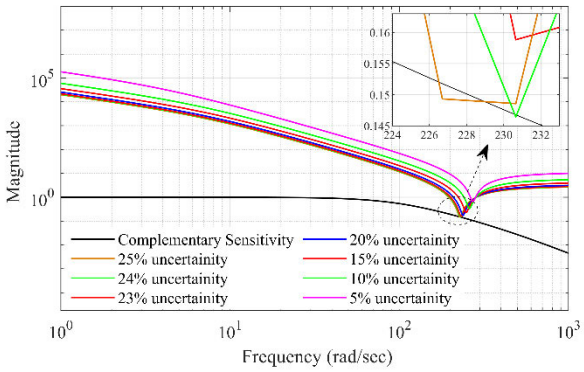

FIGURE 11. Frequency response of complementary sensitivity and parametric uncertainty of current mode control.

where, $T\ (j\omega)$ is written as:

$$T\ (j\omega) = \frac{C(j\omega)G(j\omega)}{1 + C(j\omega)G(j\omega)} \tag{20}$$

where, $C(j\omega)$ and $G\ (j\omega)$ is the controller and system model of the SISO unity feedback configuration.

For VM control, the basic IMC structure as shown in Figure 2, is simplified to SISO feedback control system, with the controller $C\ (j\omega)$ as:

$$C\ (j\omega) = \frac{Q\ (j\omega)}{1 - Q\ (j\omega)\ G_3(j\omega)} \tag{21}$$

The complementary sensitivity function for VM control of BC is given below:

$$T_{VM}\ (j\omega) = Q(j\omega)G_3\ (j\omega) \tag{22}$$

In case of proposed CM control, the equivalent inner loop controller $C_2\ (j\omega)$ as seen from Figure 5 is obtained as:

$$C_2\ (j\omega) = \frac{Q_2\ (j\omega)}{1 - Q_2\ (j\omega)\ G_2(j\omega)} \tag{23}$$

And the complementary sensitivity function, $T_{in}\ (j\omega)$ for inner loop is obtained as:

$$T_{in}\ (j\omega) = C_2\ (j\omega)\ G_2(j\omega) \tag{24}$$

The equivalent outer loop controller $C_1\ (j\omega)$ can be derived by considering primary plant and is written as:

$$C_1\ (j\omega) = \frac{Q_1\ (j\omega)}{1 - Q_1\ (j\omega)\ G_1(j\omega)} \tag{25}$$

Further, the complementary sensitivity function, $T_{out}\ (j\omega)$ for outer loop is attained by considering inner loop as a part of the primary plant, which is obtained as:

$$T_{out}\ (j\omega) = \frac{C_1(j\omega)T_{in}\ (j\omega)\ G_1\ (j\omega)}{1 + C_1(j\omega)T_{in}\ (j\omega)\ G_1\ (j\omega)} \tag{26}$$

For the robustness analysis, uncertainty is considered only in the system model while keeping the controller fixed. The parametric uncertainty in L, C and R is considered simultaneously and it is varied up to 25%. The frequency responses of complementary sensitivity and uncertainty bound for VM and CM control are shown in Figure 10 and 11, respectively. It is observed that both the schemes is equally robust for parametric uncertainty up to 23% in L, C, and R.

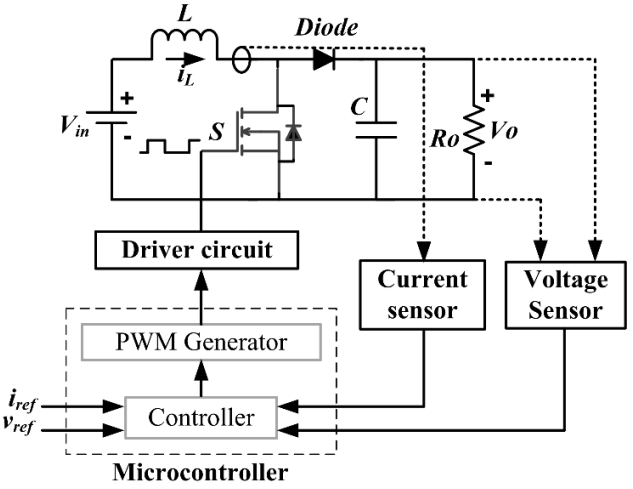

FIGURE 12. Schematic diagram of control scheme.

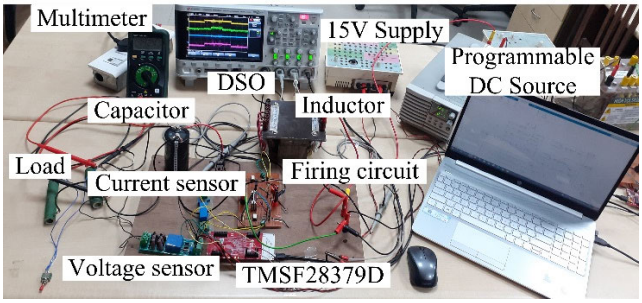

FIGURE 13. Hardware prototype of boost converter.

IV. HARDWARE VALIDATION

A schematic diagram of the control scheme of the BC is shown in Figure 12. The performance of the proposed CM control of BC using the IMC scheme has been evaluated in the hardware experimental setup (Figure 13). A hardware prototype of BC with specification given in Table 2 has

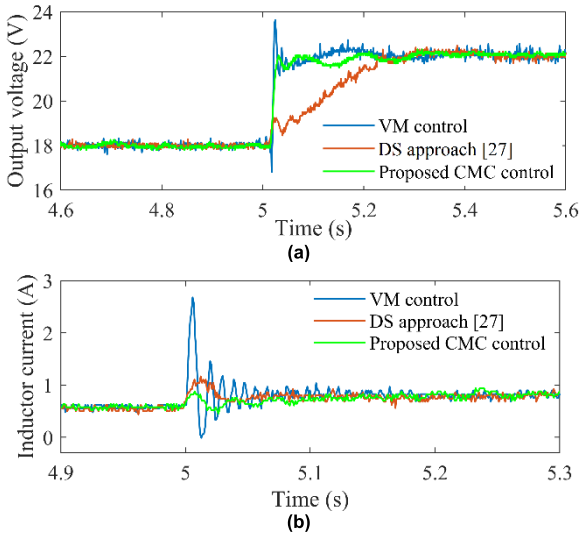

FIGURE 14. Dynamic response under set point change from V_{ref}= 18V → 22V (a) Output voltage (b) Inductor current.

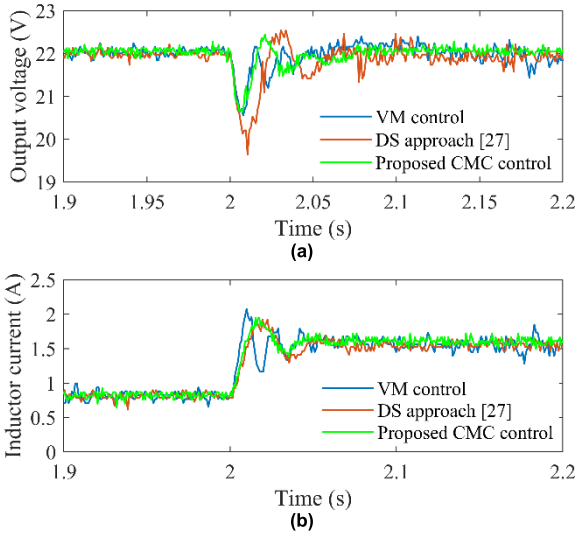

FIGURE 15. Dynamic response under resistance change from R_L= 50 Ω →25Ω (a) Output voltage (b) Inductor current.

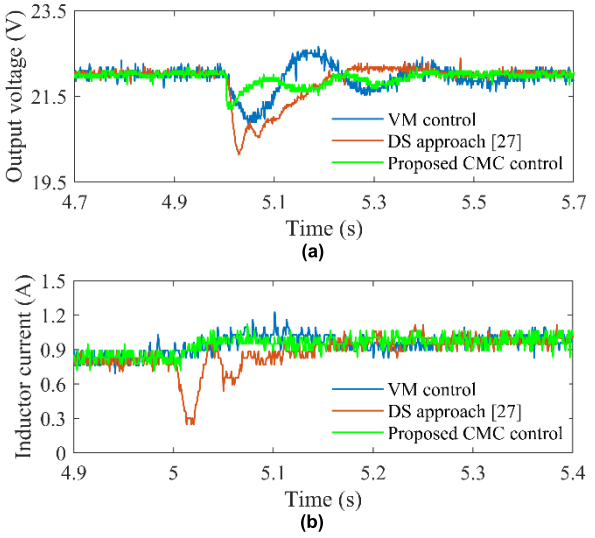

FIGURE 16. Dynamic response under input voltage change from V_{in} =12V → 10V (a) Output voltage (b) Inductor current.

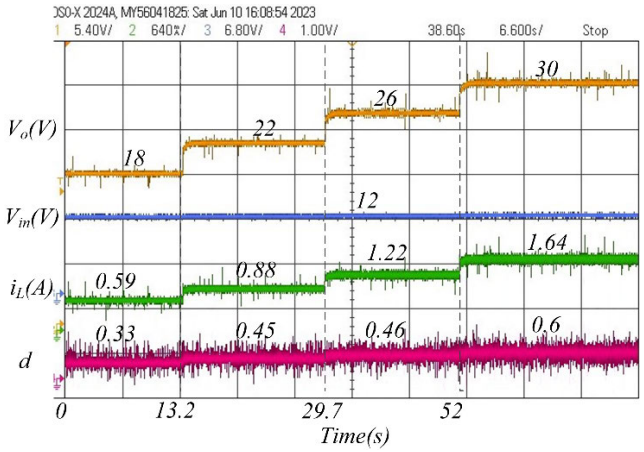

FIGURE 17. Dynamic response under reference set point voltage variation with proposed CM controller.

been developed. The output voltage and inductor current of BC are sensed using sensors LV25-P and LA55-P, respectively. Microcontroller TMS320F28379D is used to provide the output voltage and inductor current feedback which also acts as an interface between simulation and real-time implementation. The PWM frequency for the designed BC is set to 20kHz which is used for the switching of MOSFET (IRFP460). The diode used is MUR3060PT. A programmable DC supply Gwinstek PSW 80-27 is used to provide input to BC. To record the required waveforms of the BC, DSOX2024A is used. A ±15V supply is required in order to provide biasing in the sensors and firing circuit of MOSFET.

The control performance of the proposed CM has been investigated for the set-point and the load-disturbance rejection response (change in input voltage and the load). The transient as well as steady performance are analysed. Further, the robustness of proposed scheme is tested in hardware setup by perturbing the circuit parameter of the BC. Additionally, the obtained results are compared with VM control discussed in Section II and recently reported work of Jha et al. mentioned as DS approach [27].

A. TRANSIENT RESPONSE FOR NOMINAL VALUES

The set point tracking is analysed by introducing a step change from 18V→22V at 5s. During this, the input voltage and load resistance is kept at its nominal value of 12V and 50Ω, respectively. The comparative output voltage response of the proposed CM, VM control and DS approach is shown in Figure 14(a). It is observed from Figure 14(a), that no overshoot is experienced in case of the proposed CM controller and in [27]. However, the proposed scheme offers

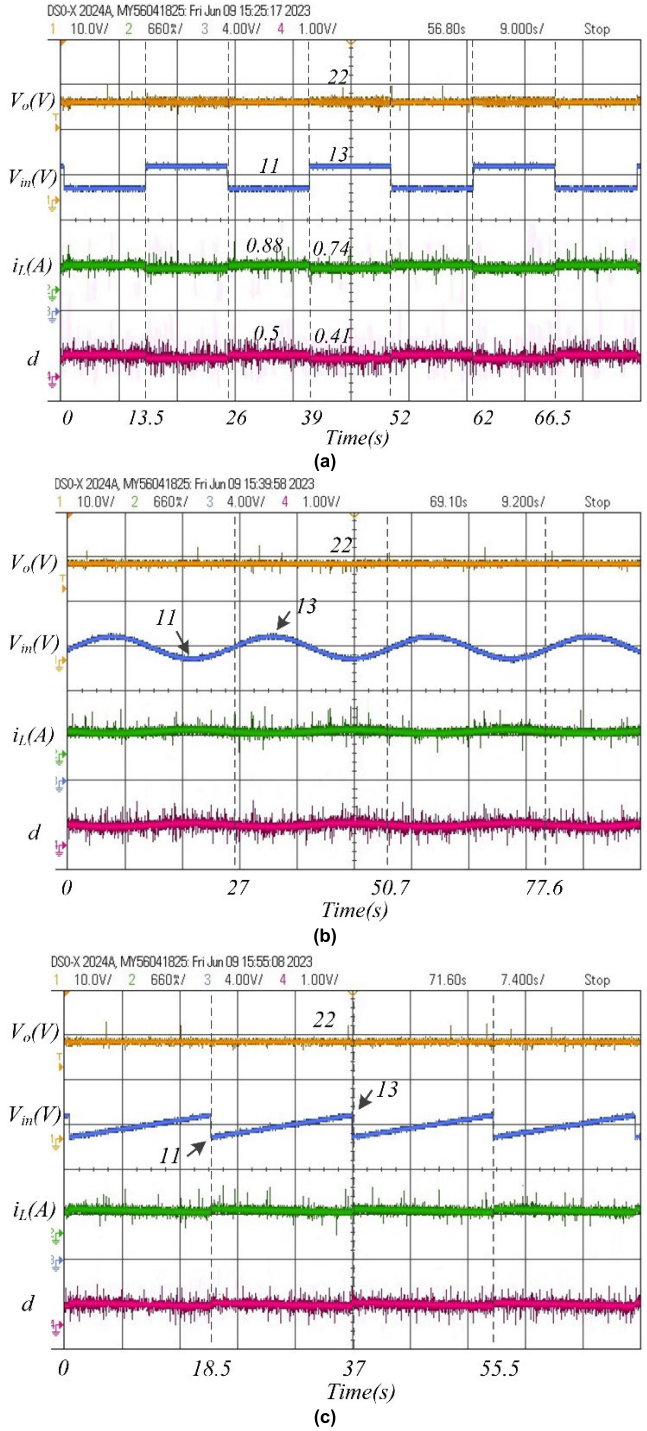

FIGURE 18. Dynamic response under input voltage disturbance with proposed CM controller (a) Periodic square step variation (b) Periodic sinusoidal variation (c) Periodic ramp/sawtooth variation.

a faster settling time whereas sluggish response is found in the method of [27]. The inductor current is shown in Figure 14(b). Maximum deviation in the inductor current of 2.671A is observed in case of VM control. The values of performance measures for these control strategies are tabulated in Table 3. From Figures and Table, it is evident that proposed

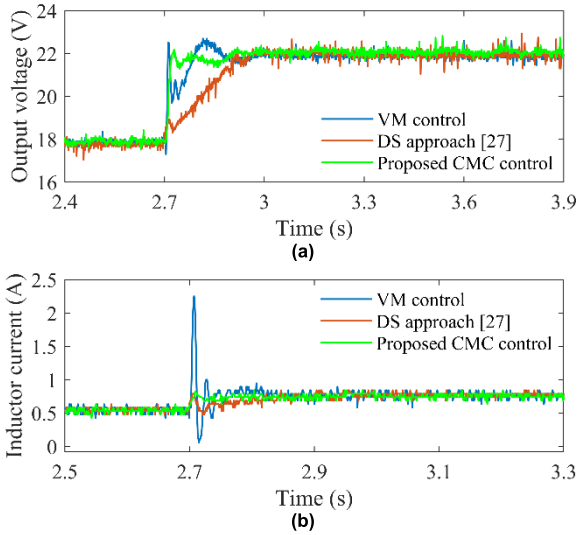

FIGURE 19. Dynamic response under set point change from V_{ref} =18V→ 22V for perturbed values of L and C (a) Output voltage (b) Inductor current.

CM scheme is performing better than VM control and DS approach.

To test the dynamic load disturbance rejection performance, the load is increased to twice the nominal value (i.e., load resistance is changed from 50Ω →25Ω) at 2s while maintaining the input voltage constant at 12V. The comparative output voltage and inductor current are shown in Figure 15. The response of the proposed CM scheme settles fast within 0.04s with less oscillation in the response. The deviation in output voltage is maximum (2.36V) shown in case of DS approach [27].

Dynamic load disturbance rejection response is further investigated by introducing step change in the supply voltage. A change in input voltage i.e., 12V→10V at 5s is applied while keeping the load resistance constant at 50Ω and corresponding response is shown in Figure 16. The proposed CM controller takes 0.23s to reject input voltage disturbance. The output voltage of VM controller strategy experiences a sluggish response with a settling time of 0.47s and a maximum inductor current of 1.05A as noticed from Figure 16 (a) and (b). The maximum deviation in the output voltage is observed by the method of [27]. From the above discussion of dynamic responses, it is noticed that the proposed controller outperforms the control technique in DS approach [27] and VM control strategy, ensuring better voltage regulation.

B. STEADY STATE RESPONSE OF PROPOSED CM CONTROLLER

The steady state tracking performance of the proposed CM controller is tested under set point reference variations with V_{ref} = 18V→22V→26V→30V at t = 13.2s, 29.7s and 52s, respectively. The corresponding output voltage, input voltage, inductor current and duty cycle are shown in Figure 17. The proposed CM controller tracks the reference

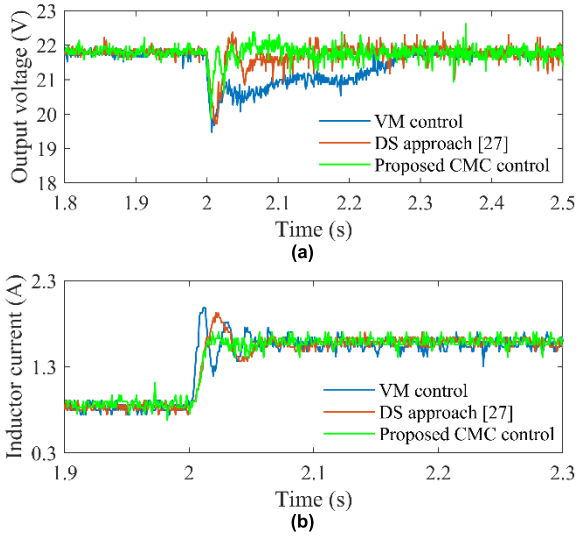

FIGURE 20. Dynamic response under resistance change from $R_L = 50\ \Omega \rightarrow 25\Omega$ for perturbed values of L and C (a) Output voltage (b) Inductor current.

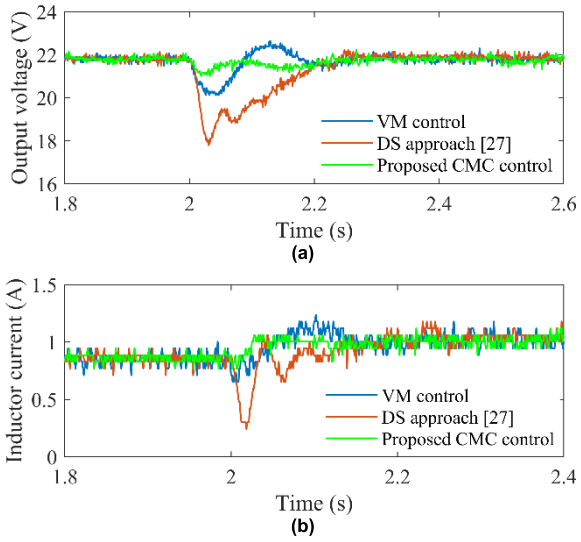

FIGURE 21. Dynamic response under input voltage change from $V_{in} = 12\text{V} \rightarrow 10\text{V}$ for perturbed values of L and C (a) Output voltage (b) Inductor current.

command by manipulating the duty cycle of the BC. The proposed scheme tracks the output voltage command up to 30V by manipulating the duty cycle to 0.6 ($D > 0.5$). It is also worth noting that the proposed CM control scheme does not exhibit subharmonic oscillation in duty cycle.

To demonstrate the effectiveness of the proposed controller, the output response has been examined and the constant input voltage is replaced with periodic supplies such as periodic square wave, sinusoidal wave, and sawtooth wave. The responses under these cases are shown in Figure 18. The reference command is given as 22V and the input voltage is changed periodically between 11V to 13V. The corresponding response is shown in Figure 18(a). Here, the output voltage of BC is maintained constant at 22V

TABLE 3. Comparison of controller performances.

	Parameters	VM control	DS approach [27]	Proposed CM control
For nominal values				
Set point change (18V → 22V)	i_{Lmax}(A)	2.671	1.10	0.814
	t_s(s) of output voltage	0.31	0.33	0.19
	Deviation (V) of output voltage	1.53	-	-
Load resistance change (50Ω→25Ω)	i_{Lmax}(A)	2.074	1.945	1.945
	t_s(s) of output voltage	0.13	0.1	0.04
	Deviation (V) of output voltage	1.27	2.36	1.25
Input voltage change (12V→10V)	i_{Lmax}(A)	1.05	0.25(dip)	0.98
	t_s(s) of output voltage	0.47	0.45	0.23
	Deviation (V) of output voltage	1.1	1.82	0.62
For perturbed values				
Set point change (18V → 22V)	i_{Lmax}(A)	2.25	0.82	0.82
	t_s(s) of output voltage	0.27	0.26	0.16
	Deviation (V) of output voltage	0.69	-	-
Load resistance change (50Ω→25Ω)	i_{Lmax}(A)	1.98	1.87	1.63
	t_s(s) of output voltage	0.3	0.18	0.81
	Deviation (V) of output voltage	2.56	2.33	1.7
Input voltage change (12V→10V)	i_{Lmax}(A)			
	t_s(s) of output voltage	0.23	0.25	0.09
	Deviation (V) of output voltage	1.88	3.97	0.98

irrespective of input voltage behaviour. Further, sinusoidal and sawtooth variations (11V to 13V) have been applied and corresponding responses are shown in Figure 18(b) and (c), respectively. From these figures, it is evident that the proposed CM scheme performs well in the presence of perturbed input voltage.

C. ROBUSTNESS ANALYSIS-PERTURBATION IN L AND C VALUES

To study the robustness of the controllers, against plant parametric variation, the value of L and$C$ are changed to 7mH and 1500μF, respectively. With these perturbed values, the three controllers are experimentally tested under changes in the set point, load resistance and input voltage. The corresponding experimental results are shown in Figure 19 to Figure 21. The performance measures for the same are illustrated in Table 3. It can be seen from the figures and table that the proposed scheme outperforms the schemes of VM control and DS approach [27] in case of system parametric perturbation also.

V. CONCLUSION

This work presents a cascade mode control structure for the output voltage regulation of dc/dc boost converter. Using the advantageous feature of internal model control scheme, conventional cascade control structure is modified to obtain

desired dynamic response. Also, a step-by-step procedure is presented to design the proposed controller. The performance parameters in VM as well as in the proposed CM control are evaluated by considering same level of performance requirement. The proposed CM scheme performs better in comparison with the recently reported work. The IMC structure is based on classical control technique so it is applicable to the linearized model of converters. However, this structure may be applied to non-linear system model in state space domain which is the future prospect of this work. Also, the utility of fractional order controller in the IMC scheme for the boost converter may explore in future. The robustness analysis of the suggested scheme is carried out using small gain theorem and also validated through hardware experiments. The proposed CM scheme is robust and give stable performance up to 23% simultaneous change in L, C, and R. Also, the proposed CM control structure avoids sub-harmonic oscillations for duty cycle above 0.5.

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