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RESEARCH ARTICLE

# A Complementary Low Schottky Barrier Nonvolatile Bidirectional Reconfigurable Field Effect Transistor Based on Dual Metal Silicide S/D Contacts

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**ABSTRACT** In this work, a high-performance nanoscale complementary low Schottky barrier (CLSB) nonvolatile bidirectional reconfigurable field effect transistor (NBRFET) based on dual metal silicide source/drain (S/D) contacts (CLSB-NBRFET) is proposed. It is designed with Source floating gate (SFG) and drain floating gate (DFG) and adopts two kinds of metal silicide contacts to form complementary low Schottky barrier both between the S/D electrodes and the conduction band of silicon and between the S/D electrodes and the valence band of silicon at the same time. Instead of a program gate (PG) of conventional BRFET which needs independent power supply, the SFG and DFG of the proposed CLSB-NBRFET can be programmed by the CG itself. Thereafter, the interconnection can be simplified. The nonvolatile reconfigurable function is also realized. The type of charge stored in both SFG, and DFG decides the conduction type of the CLSB-NBRFET. Due to that there is a coupling effect between the effective voltages of SFG /DFG and the control gate (CG) voltage ($V_{CG}$), the effective voltages of SFG and DFG can be decreased in the reverse biased state, and the reverse leakage current can be reduced. Besides, the dual metal silicide S/D contacts help to largely improve the forward current in both N mode and P mode comparing to conventional BRFET. Therefore, the scale of CLSB-NBRFET simplify the interconnection complexity and improve the characterization of BRFET. The scale of CLSB-NBRFET can be reduced to nanoscale while maintain high performance. The physical mechanism of the proposed CLSB-NBRFET has been analyzed in detail. The device performance has been compared with conventional BRFET. The influence of the amount of charge to the device performance has also been discussed in detail.

**INDEX TERMS** Nanoscale, nonvolatile, complementary low Schottky barrier, bidirectional, RFET.

## I. INTRODUCTION

Nowadays, the physical size of the basic element of integrated circuits (ICs) is getting closer to the physical limit. Therefore, instead of reducing the scale of the basic elements, increasing the functional density of a single element of ICs becomes a new way to ''softly'' improve the density of the ICs. The reconfigurable field effect transistor (RFET) and bidirectional RFET (BRFET) are proposed. Different from conventional transistors, the conduction mode of RFET or BRFET can be reconfigured as n-type or p-type by changing the polarity of the voltage applied on the program gate (PG) [1], [2]. RFET and BRFET can realize various simpler logic gates than conventional MOSFET based logical gates [3], [4], [5], [6], [7]. High Schottky barrier on the source side between the metal source and the conduction band of the semiconductor and the valence band of the semiconductor are formed at the same time for realizing

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the reconfigurable function. Nickel Silicide (NiSi) is typical material for the formation of Schottky barrier in RFET and BRFET. Because the Schottky barrier height formed between NiSi and semiconductor conduction band is like that formed between NiSi and semiconductor valence band [8]. Similar as the high Schottky barrier based bidirectional tunnel field effect transistor (TFET) [9], [10], [11], [12], by adjusting the voltage of the program gate (PG), the electron-hole pairs on the source side in the silicon can be generated through band to band tunneling to overcome the Schottky barrier which prevents the carriers from flowing between the source electrode and the semiconductor region. By adjusting the polarity of the voltage of the PG, the carriers can be controlled to flow in the conduction band or in the valence band of the semiconductor region. Therefore, the polarity of PG voltage determines the type of carriers that the source can provide and determines the conduction type of RFET. The magnitude of the voltage applied to the PG determines the intensity of band bending and the corresponding generation rate of the number of carriers by band to band tunneling. However, Because the generation rate of the number of carriers by band to band tunneling effect is extremely limited, its forward conduction current is often much smaller than the mainstream technology, which is a congenital disadvantage of Schottky barrier based RFET. Besides, the scales of RFET and BRFET involved in the reports are much larger than that achieved by today's mainstream technology [13], [14], [15], [16]. RFET and BRFET actually generate carriers and form current through band to band tunneling phenomena to conquer the Schottky barriers which form on the interface between the source electrode and silicon [17], [18]. However, to reconfigure the device, two independent gate electrodes are required. Compared with single gate FETs, the extra PG of RFET or BRFET increases the complexity of metal interconnection. More than this, when RFET or BRFET works in the off state or reversely biased state, the local electric field enhancement caused by the PG which is always works at high voltage will enhance the band bending and lead to the band to band tunneling effect and increase the power consumption. This effect is particularly significant for highly integrated RFET. When the PG and the control gate (CG) are applied to voltages with opposite polarity, the band to band tunneling effect in the region between these two gates will be significantly strengthened. To simplify the metal interconnection and realize a high-performance nanoscale RFET, in this paper, we propose a complementary low Schottky barrier source/drain (S/D) contacts based nonvolatile bidirectional reconfigurable field effect transistor (CLSB-NBRFET). Unlike conventional BRFET which adopt one kind of metal (such as NiSi) to form high Schottky barrier both between the S/D electrodes and the conduction band of silicon and between the S/D electrodes and the valence band of silicon, the CLSB-NBRFET adopts two kinds of metal silicide to form low Schottky barrier both between the S/D electrodes and the conduction band of silicon and between the S/D electrodes and the valence band of silicon at the same time. The height of Schottky barrier formed between the first kind of metal (ErSi) and silicon for electrons in conduction band $\phi_{bn1}$ is much smaller than the one for holes in valence band $\phi_{bp1}$.The height of Schottky barrier formed between the first kind of metal (PtSi) and silicon for holes in valence band $\phi_{bp2}$ is set to be much smaller than the one for electrons in conduction band $\phi_{bn2}$. The low $\phi_{bn1}$ formed on the interface between ErSi is about 0.25V [19], and the low $\phi_{bp2}$ formed on the interface between PtSi and silicon is about 0.25V [20], [21]. Therefore, when the source floating gate (SFG) and the drain floating gate (DFG) are positively charged, the electrons from source electrode can easily flow into the semiconductor region through the low $\phi_{bn1}$ Schottky barrier due to thermionic emission in the conduction band, while when the SFG and the DFG is negatively charged, the holes from semiconductor can easily flow into the source electrode through the low $\phi_{bp2}$ Schottky barrier due to thermionic emission in the valence band. Therefore, the forward current in both N mode and P mode are largely improved comparing to unique Schottky barrier based conventional BRFET. Because charge can be stored between dielectric layers by trapping phenomena [22], [23], source floating gate (SFG) and drain floating gate (DFG) are designed which can simplify the gate interconnection of RFET and realize the nonvolatile reconfigurable function. The type of charge stored in both SFG, and DFG decides the conduction type of the CLSB-NBRFET. Due to that there is a coupling effect between the effective voltages of SFG/DFG and the control gate (CG) voltage ($V_{CG}$), the effective voltages of SFG and DFG can be reduced in the reverse biased state, the reverse leakage current can be reduced. Therefore, the scale of CLSB-NBRFET can be reduced to nanoscale while maintain high performance. Instead of a program gate (PG) of conventional BRFET which needs independent power supply, the SFG and DFG of the proposed CLSB-NBRFET can be programmed by the CG itself. Thereafter, the interconnection can be simplified. The physical mechanism of the proposed CLSB-NBRFET has been analyzed in detail. The device performance has been compared with conventional BRFET. The influence of the amount of charge to the device performance has also been discussed in detail.

## II. DEVICE STRUCTURE

Figure 1 (a) is the top view of the proposed CLSB-NBRFET, figure 1(b), figure1(c), figure 1(d) and figure 1 (e) are the cross views along cut line A, cut line B, cut line C, and cutline D of figure 1 (a), respectively. Figure 1 (f) is the cross view along cut line A of figure 1 (b). Figure 1 (g) is a cross view of a conventional Schottky barrier based BRFET. $L_{si}$ is the length of silicon. $L_{CG}$ is the length of CG. $L_{FG}$ is the length of SFG or DFG. $L_{SP}$ is the length of spacer either between CG and the SFG/DFG, or between S/D and SFG/DFG. $t_{si}$ is the thickness of silicon, $t_{ox1}$ is the thickness of the first $HfO_2$ gate oxide layer between SFG/DFG and silicon. $t_{ox2}$ is the thickness of the second $HfO_2$ gate oxide layer between SFG/DFG and CG. $W_{si}$ is the width of silicon.

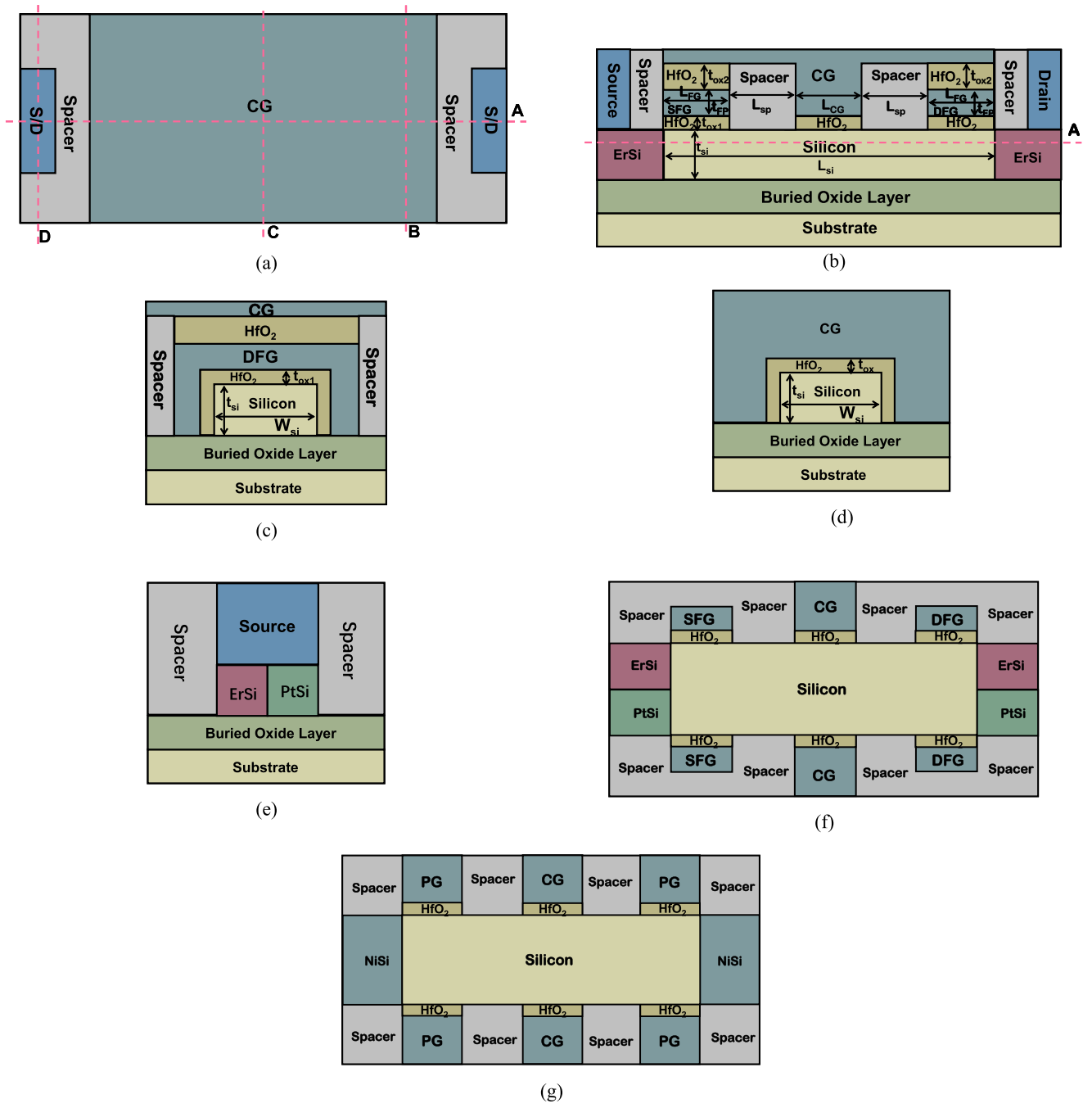



**FIGURE 1.** (a) The top view of the proposed CLSB-BRFET, (b) the cross views along cut line A of figure 1 (a), (c) the cross views along cut line B of figure 1 (a), (d) the cross views along cut line C of figure 1 (a), (e) the cross views along cutline D of figure 1 (a), (f) the cross view along cut line A of figure 1 (b), (g) a cross view of a conventional unique Schottky barrier based BRFET.

$\varepsilon_{HfO2}$ is the relative permittivity of $HfO_2$, $\varepsilon_{spacer}$ is the relative permittivity of Spacer. $q\phi_{bn1}$ is the barrier height between the first kind of metal (ErSi) of the S/D electrodes and the conduction band of silicon. $q\phi_{bp1}$ is the barrier height between the first kind of metal (ErSi) of S/D electrodes and the valence band of silicon. $q\phi_{bn2}$ is the barrier height between the second kind of metal (PtSi) of the S/D electrodes and the conduction band of silicon. $q\phi_{bp2}$ is the barrier height between the second kind of metal (PtSi) of S/D electrodes and the valence band of silicon. $q\phi_{bn0}$ is the barrier height between NiSi S/D electrodes and the conduction band of silicon. $q\phi_{bp0}$ is the barrier height between NiSi S/D electrodes and the valence band of silicon. The parameter selection for CLSB-NBRFET is shown in Table 1. The parameters of the conventional BRFET are selected as consistent as possible with the parameter of CLSB-NBRFET.

**TABLE 1. Parameters selection for CLSB-NBRFET and BRFET.**

| Symbol | Parameters | Values |
|---|---|---|
| $L_{si}$ | length of silicon | 20nm |
| $L_{CG}$ | length of CG | 4nm |
| $L_{PG}$ | the length of PG | 4nm |
| $L_{sp}$ | length of spacer between CG and PG | 4nm |
| $t_{ox1}$ | the first layer of $HfO_2$ gate oxide thickness | 1nm |
| $t_{ox2}$ | the second layer of $HfO_2$ gate oxide thickness | 2nm |
| $t_{FP}$ | The thickness of SFG/DFG | 3nm |
| $T_{si}$ | the thickness of silicon | 5nm |
| $W_{si}$ | the width of silicon | 6nm |
| $\varepsilon_{HfO2}$ | the relative permittivity of $HfO_2$ | 21.976 |
| $\varepsilon_{spacer}$ | the relative permittivity of SiO2 Spacer | 3.89 |
| $q\phi_{bn0}$ | the barrier height between NiSi S/D electrodes and the conduction band of silicon | 0.56eV |
| $q\phi_{bp0}$ | the barrier height between NiSi S/D electrodes and the valence band of silicon | 0.52eV |
| $q\phi_{bn1}$ | the barrier height between the first kind of metal (ErSi) of the S/D electrodes and the conduction band of silicon | 0.25eV |
| $q\phi_{bp1}$ | the barrier height between the first kind of metal (ErSi) of S/D electrodes and the valence band of silicon | 0.83eV |
| $q\phi_{bn2}$ | the barrier height between the second kind of metal (PtSi) of the S/D electrodes and the conduction band of silicon | 0.83eV |
| $q\phi_{bp2}$ | the barrier height between the second kind of metal (PtSi) of S/D electrodes and the valence band of silicon | 0.25eV |

## III. ANALYSIS AND DISCURSSIONS

The characteristics of the proposed CLSB-NBRFET are verified by device simulation using SILVACO tools [24]. Physical models such as Fermi distribution model, Auger recombination model, band gap narrowing model, dielectric tunneling model and band to band tunneling model are all turned on. Figure 2 (a) shows the relationship between $Q_{SFG}$ / $Q_{DFG}$ and programming time under different negative $V_{CG}$ s. and figure 2 (b) shows the relationship between $Q_{SFG}$ / $Q_{DFG}$ and erasing time under different positive $V_{CG}$ s with an initial positive $Q_{SFG}$ / $Q_{DFG}$. When the SFG and the DFG is being programming, the S/D electrode are both grounded, and the CG is applied to be a high voltage. The $Q_{SFG}$ / $Q_{DFG}$ stored in the SFG/DFG are roughly proportional to the programming time, and the programming time is inversely proportional to $V_{CG}$. After programming by a negative $V_{CG}$, positive charges are stored in the SFG/DFG and the proposed CLSB-NBRFET works in N-mode. The positive $Q_{SFG}$ / $Q_{DFG}$ should be erased by applying a relatively high positive $V_{CG}$. The erasing time is also inversely proportional to the $V_{CG}$.

Figure 3 (a) shows the relationship between $V_{CG}$ and the $V_{SFG}$/ $V_{DFG}$ with different $Q_{SFG}$s/ $Q_{DFG}$ s. For a certain $V_{CG}$, $V_{SFG}$/ $V_{DFG}$ increases with the increase of $Q_{SFG}$s/ $Q_{DFG}$ s. For a certain $Q_{SFG}$s/ $Q_{DFG}$s, $V_{SFG}$/ $V_{DFG}$ shows obvious coupling effect with $V_{CG}$, and $V_{SFG}$/ $V_{DFG}$ is generally proportional to $V_{CG}$. This makes $V_{SFG}$/ $V_{DFG}$ of the proposed CLSB-NBRFET different from the $V_{PG}$ of conventional BRFET. It is not fixed at a certain value, but a variable function which changes with the changing of $V_{CG}$. The positive $Q_{SFG}$s/ $Q_{DFG}$s and the positive $V_{CG}$ can both increase the $V_{SFG}$/ $V_{DFG}$. $V_{SFG}$/ $V_{DFG}$ can achieve an effective value that higher than $V_{CG}$ when CG is positively biased. $V_{SFG}$ and $V_{DFG}$ also decrease with the decreasing of $V_{CG}$. Figure 3 (b) shows the relationship between $V_{CG}$ and the voltage difference between $V_{SFG}$/ $V_{DFG}$ and $V_{CG}$ ($V_{SFG-CG}$/ $V_{DFG-CG}$) with different $Q_{SFG}$s/ $Q_{DFG}$ s. $V_{SFG-CG}$/ $V_{DFG-CG}$ can be reduced by reduce the $Q_{SFG}$s/ $Q_{DFG}$s. The coupling effect makes the $V_{SFG-CG}$/ $V_{DFG-CG}$ smaller than the voltage difference between the PG and CG when CG is reverse biased. Therefore, the band bending can be minimized in the reverse biased state, and the leakage current can be reduced.

Figure 4 shows the comparison of transfer characteristics between CLSB-NBRFET and conventional BRFET. According to Figure 3(a), the effective $V_{SFG}$/ $V_{DFG}$ is about 1.2V/1.4V in the forward biased state, not larger than voltage

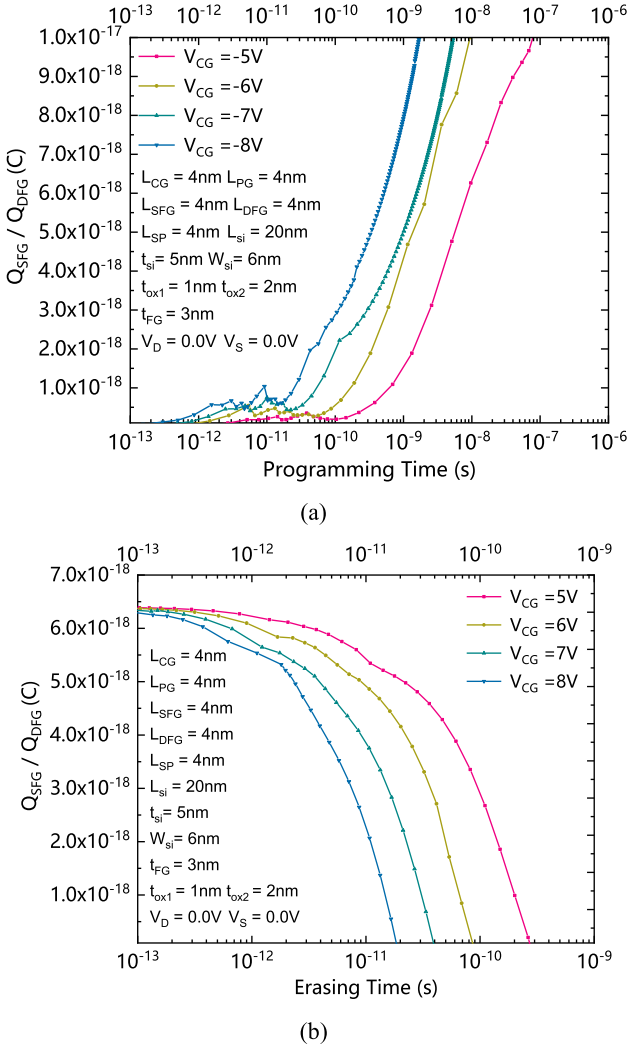
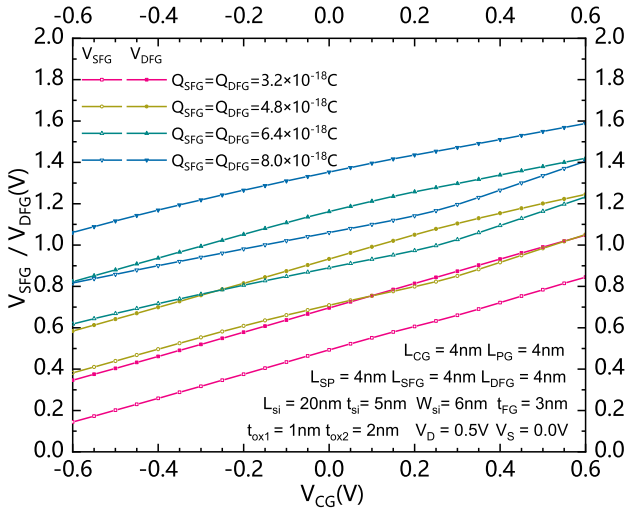
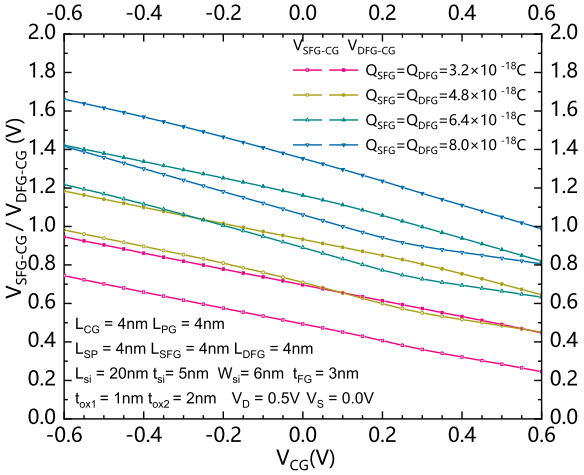



**FIGURE 2. (a) The relationship between $Q_{SFG}$ / $Q_{DFG}$ and programming time under different negative $V_{CG}$ s. (b) The relationship between $Q_{SFG}$ / $Q_{DFG}$ and erasing time under different positive $V_{CG}$ s with an initial positive $Q_{SFG}$ / $Q_{DFG}$.**




(a)




(b)

**FIGURE 3.** (a) The relationship between $V_{CG}$ and the $V_{SFG}$/ $V_{DFG}$ with different $Q_{SFG}$s/ $Q_{DFG}$ s. (b) The relationship between $V_{CG}$ and $V_{SFG-CG}$/ $V_{DFG-CG}$ with different $Q_{SFG}$s/ $Q_{DFG}$ s.

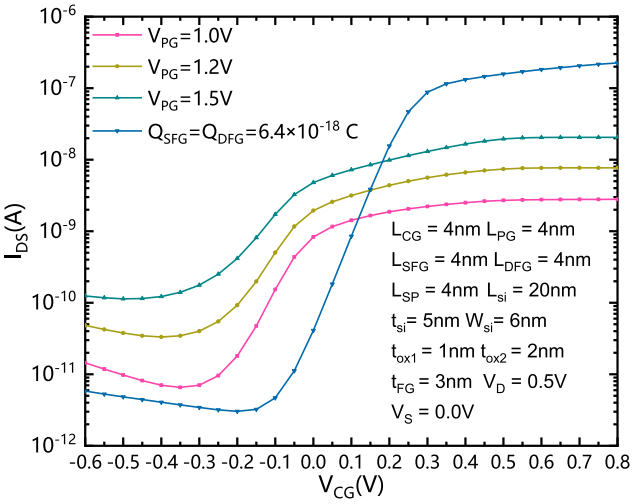



**FIGURE 4.** Comparison of transfer characteristics between CLSB-NBRFET and conventional BRFET.

of PG of conventional BRFET given in Figure 4, however, the proposed CLSB-NBRFET achieves much larger forward current than conventional NBRFET. The reverse leakage current is also reduced at the same time.

The principle of the proposed CLSB-NBRFET can be interpreted through the energy band theory. Figure 5 (a) shows the band energy distribution of the two structures under forward biased conditions in n mode. The CG of both CLSB-NBRFET and conventional BRFET is forwardly biased. The SFG/DFG of CLSB-NBRFET is written with a mount of positive charge. The PG of the conventional BRFET is positively biased. As shown in Figure 5 (a), $E_{FMS}$ is the Fermi energy level of the source electrode, while $E_{FMD}$ is the Fermi energy level of the drain electrode. $E_C$ is the bottom energy level of the conduction band, and $E_V$ is the top energy level of the valence band. Both the band energy of CLSB-NBRFET and the band energy of conventional BRFET in silicon are pulled down from the source electrode to the drain electrode under the combination of CG and SFG/DFG or PG. The overall trends of the energy band distribution of both CLSB-NBRFET and conventional BRFET are consistent with each other. However, due to that the Schottky barrier heights are different. The dominate carrier generation mechanism for these two devices is different from each other. Figure 5 (b) shows the comparison of carrier concentration distributions between CLSB-NBRFET and conventional BRFET in the forward state. In most of the corresponding regions, the concentrations of electrons and holes are almost the same, however, in the region near the interface between the source/drain electrodes and SFG/DFG of the proposed CLSB-NBRFET or PG of conventional BRFET, the electron concentration is largely different. The electron concentration of CLSB-NBRFET is much larger than the one of conventional BRFET. Due to that the barrier height of the proposed CLSB-NBRFET is largely reduced by selecting ErSi as the first kind of metal which forms a lower Schottky barrier between S/D electrodes and the conduction band of silicon comparing to conventional BRFET.

Figure 6 (a) shows the band energy distribution diagram of the two structures under reverse biased conditions in n mode. Figure 6 (b) shows the carrier concentration distributions of the two structures under reverse biased conditions in n mode. The CG of both CLSB-NBRFET and conventional BRFET is reversely biased. The SFG/DFG of CLSB-NBRFET is written with a mount of positive charge. The PG of the conventional BRFET is positively biased. As shown in Figure 6 (a), both the band energy of CLSB-NBRFET and the band energy of conventional BRFET in the central region of silicon are pulled up by CG. For the conventional BRFET, the band energy near both the source electrode and drain electrode regions under the control of PG are pull down. Therefore, a large band bending can be

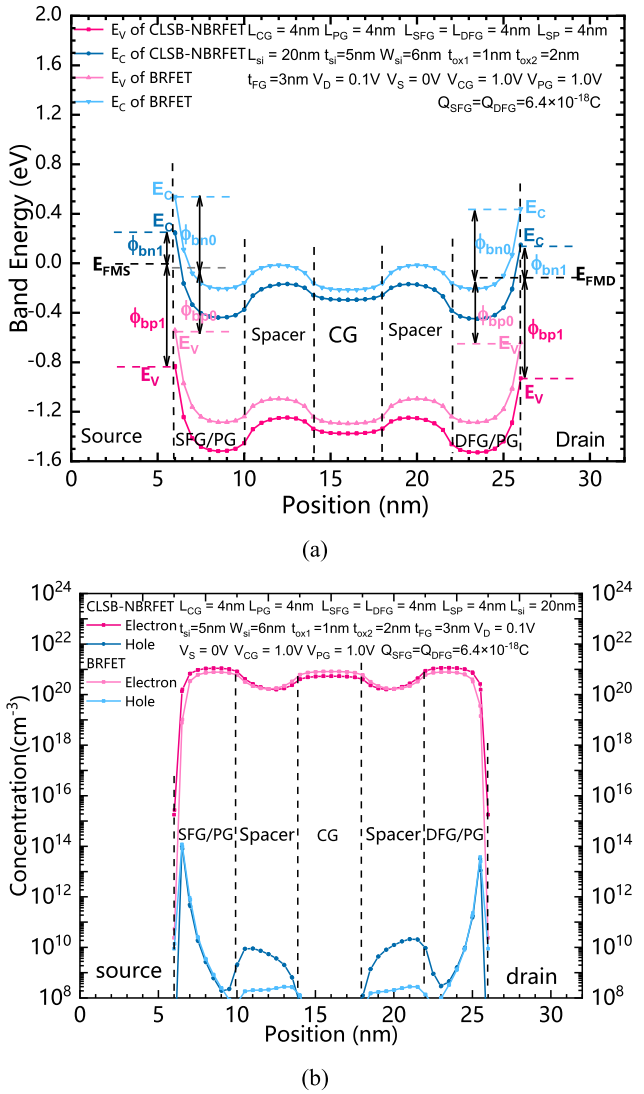



**FIGURE 5.** The comparison of band energy distribution and (b) carrier concentration distributions between CLSB-BRFET and the conventional BRFET in the forward state.

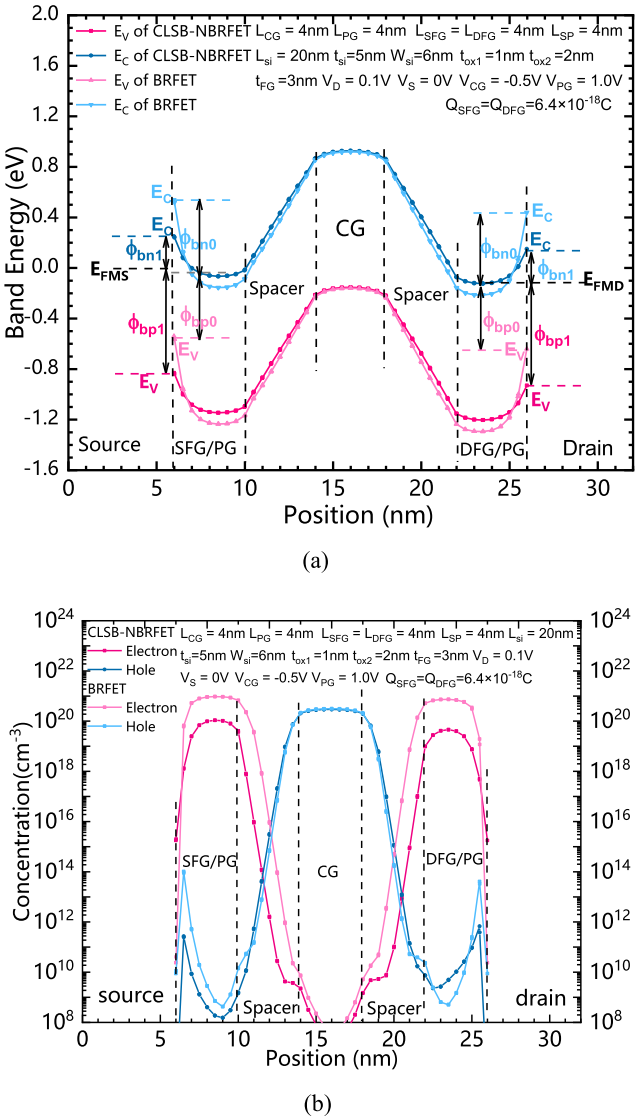



**FIGURE 6.** (a) The dependence between $V_{FG}$ and $V_G$ with positive $Q_{FG}$s. (b) the dependence between $V_{FG}$ and $V_G$ with negative $Q_{FG}$s.

formed in the spacer regions between PG and CG. The only way to reduce the intensity of band bending for conventional BRFET is to prolong $L_{SP}$. However, this is unfavorable for the improvement of integration. For CLSB-NBRFET, unlike the conventional BRFET, due to the coupling effect, $V_{SFG}$ / $V_{DFG}$ can be also decreased with the decreasing of $V_{GS}$. Thus, the band energy in the region under the control of SFG/ DFG can also be pull up to some extent. Thereafter, the band bending in the silicon near to the source / drain electrodes can be largely reduced. This leads to the weakening of the band to band tunneling effect near the source region, thus preventing the generation of enormous number of electron hole pairs. As Figure 6 (b) shows, comparing to the conventional BRFET, the electron concentration near the source /drain electrodes is reduced. The band bend of CLSB-NBRFFET shown in figure 6 (a) is also weaker than that of conventional BRFET. Therefore, reverse leakage current of the proposed CLSB-NBRFET can be reduced comparing to conventional BRFET.

Figure 7 shows the transfer characteristics of CLSB-NBRFET with different $Q_{SFG}$s/ $Q_{DFG}$ s. To determine the conduction mode and provide $V_{SFG}$ / $V_{DFG}$ high enough, the SFG/DFG should be programmed with sufficient charges. The increased $Q_{SFG}$/ $Q_{DFG}$ are helpful to improve the effective voltage of the SFG and DFG when the gate electrode is reversely biased. It should be noted that the amount of charge needs to be optimized, because excessive charge will cause the effective voltage of the SFG/DFG to be too high, thus increasing the energy band bending in the silicon region between CG and the SFG/DFG and the corresponding increase of the reverse leakage current. The optimize value of $Q_{SFG}$/ $Q_{DFG}$ for the selected structural parameters is about $6.4 \times 10^{-18}$C.

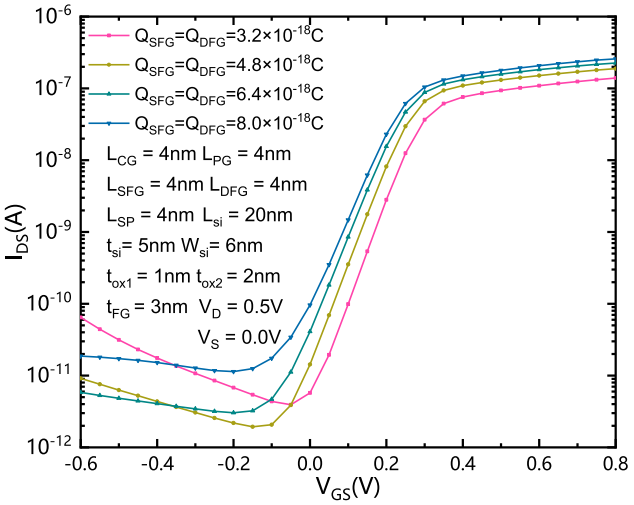



**FIGURE 7. Comparison of transfer characteristics of CLSB-BRFET with different $V_{PG}$s.**

Figure 8 (a) shows the output characteristics of the proposed CLSB-NBRFET with different $V_{CG}$s. Figure 8 (b) shows the comparison of output characteristics between the proposed CLSB-NBRFET and conventional BRFET. The forward on state saturation current is strictly restricted by the $V_{CG}$. The output characteristic enters from the linear region into the saturation region as $V_{DS}$ increases. The saturation $I_{DS}$ increases with the increase of the gate voltage. The saturation current of the proposed CLSB-NBRFET is much larger than the one of conventional BRFET.

Figure 9 shows the reconfigurable characteristics of the proposed CLSB-NBRFET. Charge type stored in SFG/DFG determines the conduction mode of the proposed CLSB-NBRFET. When the SFG/DFG is positively charged and the CG and the drain electrode are positively biased, electrons flow from ErSi source into the conduction band to form the forward current. And the proposed CLSB-NBRFET operates in the turn-on state of N mode. Similarly, when the SFG/DFG is negatively charged and the CG and the drain electrode are negatively biased, the holes flow from PtSi source into the valence band to form the forward current. And the proposed CLSB-NBRFET operates in the turn-on state of P mode. In both modes, the proposed CLSB-NBRFET has good on state conduction characteristics, low static power consumption, and the $I_{on}$ / $I_{off}$ ratio achieves about $10^5$.

Figure 10 show a brief method to produce the proposed CLSB-NBRFET. As figure 10 (a) shows, etch the upper regions on both sides of the silicon film on the surface of the SOI wafer, and deposit the first type of metal (Er) to form an ErSi alloy and flatten the surface till expose the silicon film through chemical mechanical polishing (CMP) process, then as figure 10 (b) shows, etch the lower part of the silicon film on both sides, and form a PtSi alloy by depositing the second type metal (Pt), and flatten the surface till expose the silicon film through chemical mechanical polishing (CMP) process, then the complementary low Schottky barrier on both source/drain sides are formed. As figure 10 (c), figure 10(d) and figure 10 (e) shows, in order to reserve the space for HfO2

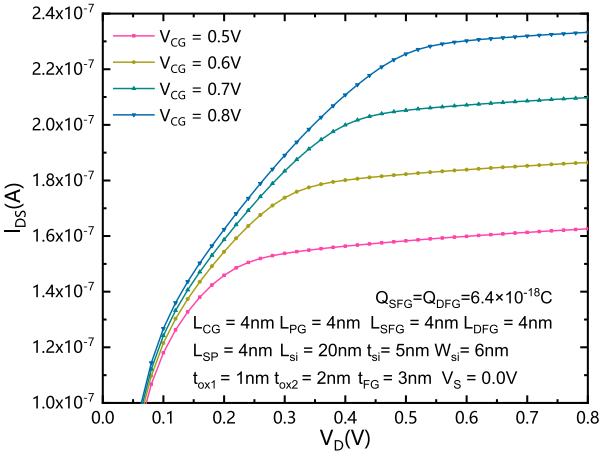



**FIGURE 8. (a) The output characteristics of the proposed CLSB-NBRFET with different $V_{CG}$s. (b) comparison of the output characteristics between the proposed CLSB-NBRFET and BRFET.**

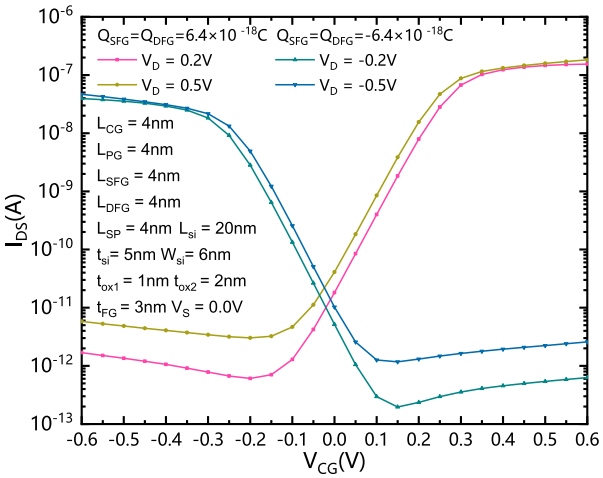



**FIGURE 9. The reconfigurable characteristics of the proposed CLSB-BRFET.**

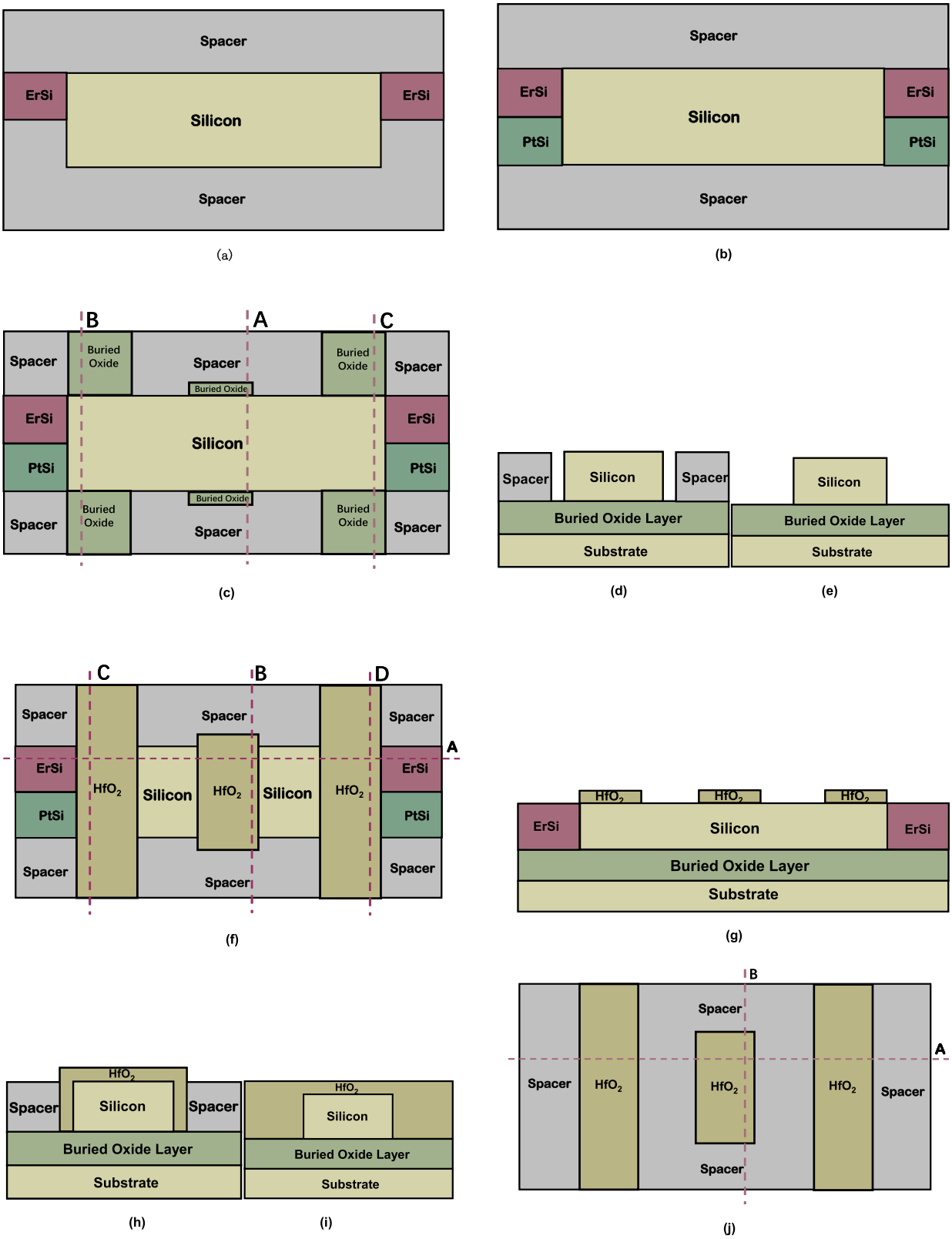



**FIGURE 10.** (a) Top view of step 1, (b) top view of step 2, (c) top view of step 3, (d) cross view of figure 10 (c) along cutline A, (e) cross view of figure 10 (c) along cutline B or C, (f) top view of step 4, (g) cross view of figure 10 (f) along cutline A, (h) cross view of figure 10 (f) along cutline B, (i) cross view of figure 10 (f) along cutline C or D, (j) top view of step 5, (k) cross view of figure 10 (j) along cutline A, (l) cross view of figure 10 (j) along cutline B, (m) top view of step 6, (n) cross view of figure 10 (m) along cutline A, (o) cross view of figure 10 (m) along cutline B or C, (p) top view of step 7, (q) cross view of figure 10 (p) along cutline A, (r) cross view of figure 10 (p) along cutline B, (s) cross view of figure 10 (p) along cutline C or D, (t) top view of step 8, (u) cross view of figure 10 (t) along cutline A, (v) cross view of figure 10 (t) along cutline B or C.

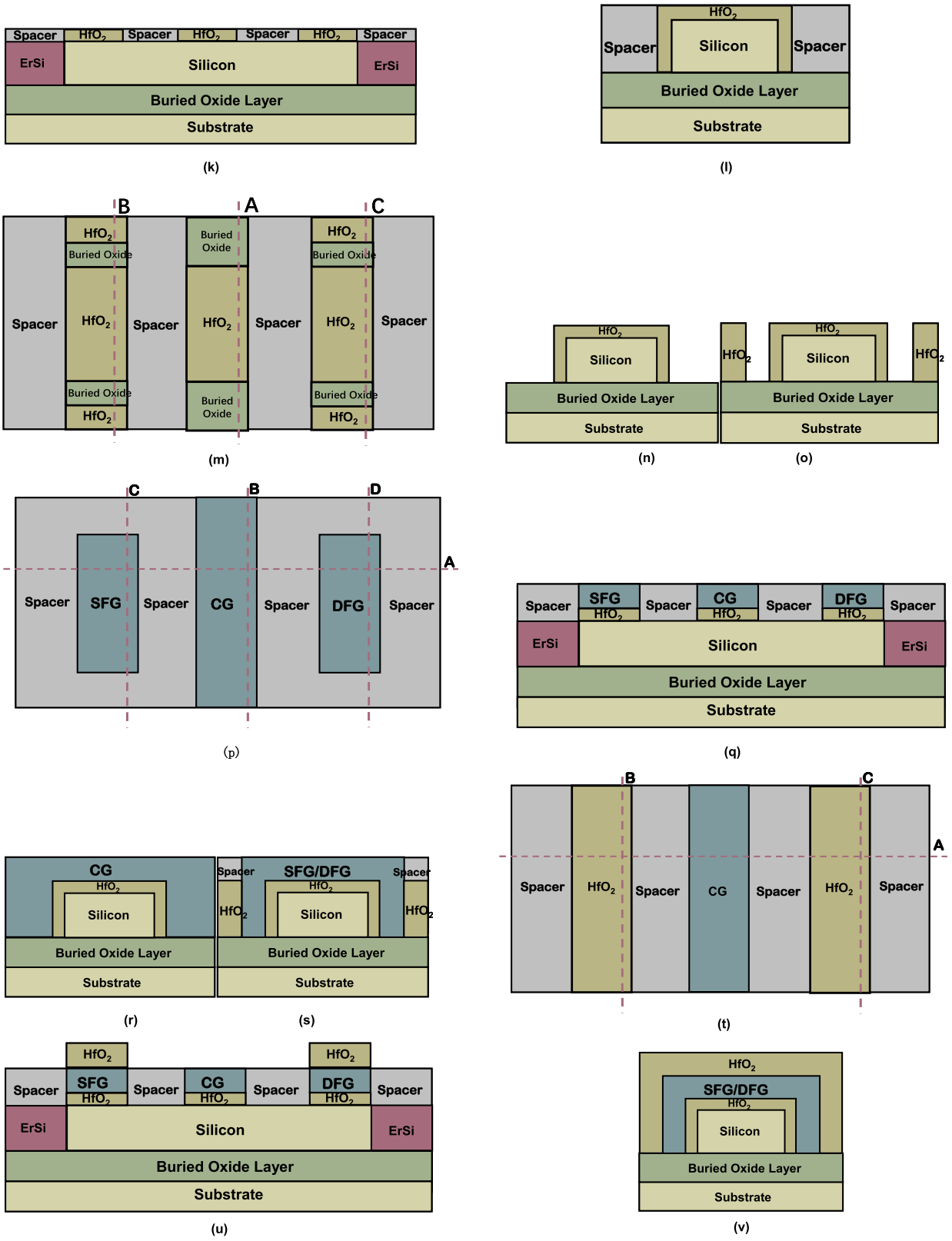



**FIGURE 10.** *(Continued.)* (a) Top view of step 1, (b) top view of step 2, (c) top view of step 3, (d) cross view of figure 10 (c) along cutline A, (e) cross view of figure 10 (c) along cutline B or C, (f) top view of step 4, (g) cross view of figure 10 (f) along cutline A, (h) cross view of figure 10 (f) along cutline B, (i) cross view of figure 10 (f) along cutline C or D, (j) top view of step 5, (k) cross view of figure 10 (j) along cutline A, (l) cross view of figure 10 (j) along cutline B, (m) top view of step 6, (n) cross view of figure 10 (m) along cutline A, (o) cross view of figure 10 (m) along cutline B or C, (p) top view of step 7, (q) cross view of figure 10 (p) along cutline A, (r) cross view of figure 10 (p) along cutline B, (s) cross view of figure 10 (p) along cutline C or D, (t) top view of step 8, (u) cross view of figure 10 (t) along cutline A, (v) cross view of figure 10 (t) along cutline B or C.

layer and SFG/DFG, remove some parts of the spacer till that the buried oxide of SOI wafer is exposed by photolithography. As figure 10 (f) to figure (i) shows, the first $HfO_2$ layer is formed by deposition process, after flattening the surface through CMP process to adjust the thickness of the $HfO_2$ layer, etch some parts of the $HfO_2$ layer to expose the surfaces of silicon and ErSi /PtSi regions. As figure 10 (j) to figure (l) shows, the spacer region is further formed by deposition CMP processes. As figure (m) to figure (o) shows, remove some parts of the $HfO_2$ layer and spacer to reserve space for SFG/DFG layer and CG by photolithography. As figure (p) to figure (s) shows, deposit metal or polysilicon and flatten the surface by CMP. Then remove some parts of this layer to form part of the CG and SFG/DFG layers, then deposit the insulator layer and flatten the surface to expose the CG and SFG/DFG layer to further form the spacers. As figure (t) to figure (v) shows, form the second layer of $HfO_2$ by deposition and etching processes. Finally, as figure 1(a) to figure 1(f) shows, etch some parts of the spacer till expose the surface of CG, then deposit metal to further form the CG, etch some parts of the spacer till expose the surface of ErSi/PtSi layer on both source/drain sides to reserve space for source and drain electrodes.

## IV. CONCLUSION

In this work, a CLSB-NBRFET based on dual S/D contacts is proposed. It is designed with SFG/ DFG and adopts two kinds of metal silicide contacts to form CLSB both between the S/D electrodes and the conduction band of silicon and between the S/D electrodes and the valence band of silicon at the same time. The proposed CLSB-NBRFET can be programmed by the CG itself. The interconnection can be simplified. The nonvolatile reconfigurable function is also realized. The type of charge stored in both SFG, and DFG decides the conduction type of the CLSB-NBRFET. The $Q_{SFG}$ / $Q_{DFG}$ stored in the SFG/DFG are roughly proportional to the programming time, and the programming time is inversely proportional to $V_{CG}$. It works in N or P-mode after programming by a negative or positive $V_{CG}$, positive or negative charges are stored in the SFG/DFG and can be erased by applying a relatively high positive or negative $V_{CG}$. The erasing time is also inversely proportional to the $V_{CG}$. The coupling effect makes the $V_{SFG-CG}$/ $V_{DFG-CG}$ smaller than the voltage difference between the PG and CG when CG is reverse biased. Therefore, the band bending can be minimized in the reverse biased state, and the leakage current can be reduced. Besides, the dual metal silicide S/D contacts help to largely improve the forward current in both N mode and P mode comparing to conventional BRFET. The $I_{on}$ / $I_{off}$ ratio achieves about $10^5$. The physical mechanism of the proposed CLSB-NBRFET has been analyzed in detail. The optimize value of $Q_{SFG}$/ $Q_{DFG}$ for the selected structural parameters is about $6.4 \times 10^{-18}$C. The amount of charge in SFG/DFG is sensitive to the erasure time and voltage. During the data reading process, it is necessary to avoid reading the voltage too high to affect the retention of the data.

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