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RESEARCH ARTICLE

A MPCC-Based Variable Sampling Time Interleaving Method for a Two-Phase Totem-Pole Bridgeless Boost PFC Converter

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ABSTRACT This paper proposes a Model Predictive Current Control (MPCC) based variable sampling time interleaving method to improve the current shaping ability, power conversion efficiency, power density and current ripple reduction of a two-phase totem pole bridgeless boost power factor correction (PFC) converter. The proposed method is based on the Finite Control Set-Model Predictive Control (FCS-MPC) technique, which has the advantage of easily including nonlinear constraints among Model Predictive Control (MPC). However, since ON/OFF of the switch is determined through model-based cost function comparison, the switching frequency is variable and a separate modulator is not used. As a result, it is difficult to apply an interleaving method using a phase shift of a Pulse Width Modulation (PWM) carrier wave in each phase using an existing inductor and switch in two phases. Accordingly, in order to reduce the current ripple, a method of making the switching states of the two phases independent by varying the MPCC sampling time of one phase was proposed.

INDEX TERMS Model predictive current control (MPCC), two-phase totem-pole bridgeless boost PFC converter, variable sampling time interleaving control method.

I. INTRODUCTION

Due to the development of the electrical industry, AC-DC power conversion devices are widely used in many applications, including Energy storage systems (ESS), On-board chargers (OBC) for electric vehicles, power supply devices for communication, and Uninterruptible power supplies (UPS). Accordingly, various studies have been conducted [1], [2], [3], [4], [5], [6], [7]. In general, when using only diode bridge rectifier circuit for AC-DC converters, harmonics are generated, causing distortion of voltage and current, which can lead to problems such as malfunction and shortened lifespan of surrounding circuits. Additionally, a significant amount of reactive power is generated due to the low input power factor. The occurrence of these harmonics and reactive power leads to inefficient use of active power, resulting in economic losses. Therefore, it is necessary to comply with the standards for each class according to IEC-61000-3-2 for harmonics and power factor, and power factor correction (PFC) converters are used for this purpose [8]. PFC converters consist of Buck, Boost, and Buck-Boost converters [9].

A. EXISTING RESEARCH ON BOOST PFC CONVERTER

Above mentioned converters, the Boost PFC converter is widely used in medium to high power (400W to a few kilowatts) applications, operating in continuous conduction mode to minimize the level of harmonic distortion and achieve a single input power factor, due to its good Electromagnetic interference (EMI) characteristics [10], [11].

The bridgeless PFC converter has been proposed as an approach to increase power density, reduce conduction losses,

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and improve the efficiency of conventional diode bridge PFC converters [12], [13], [14], [15].

However, early versions of this technology had poor EMI characteristics due to the common mode (CM) noise with switching components when the input voltage is in a negative state [13]. To solve this problem, various topologies have been proposed, and among them, the totem-pole bridgeless boost PFC converter solves the problem of CM interference issues because the output is fixed to the input by slow diodes or switches during each grid half cycle. Therefore, this converter has excellent CM noise characteristics [16], [17].

For this reason, there is a trend to eliminate the diode bridge and switch to a bridgeless architecture, and the totem-pole bridgeless PFC converter is currently gaining popularity [18].

B. CONTROL FOR CURRENT SHAPING IN BOOST PFC CONVERTERS

Using an inductor and a switching device in parallel while producing pulse width modulation (PWM) to phase-shift carrier waves and reduce current ripple, a control method known as interleaving is used in power converters to decrease the size of inductor and increase efficiency [19], [20], [21], [22]. This technique lowers the Total Harmonic Distortion (THD) by increasing switching frequency while simultaneously minimizing ripple due to an offset effect between currents. As a result, this method achieves both miniaturization and high efficiency of the power converter. On the other hand, the common method for current shaping in power electronics control technology is to use average current mode control. However, this method has the drawback of a complex control structure and slow dynamic response due to multiple feedback loops and Pulse Width Modulation (PWM). Additionally, it is vulnerable to input power distortion and difficult to implement the controller by adjusting the parameters. Therefore, in recent years, new and fast microprocessors have been used for power converter control, and the development of new control strategies has been studied. Model Predictive Control (MPC) techniques are one of the control techniques that are used for almost all power converter controllers [23], [24].

Among MPC techniques, Finite Control Set Model Predictive Control (FCS-MPC) is attracting increasing interest due to its ability to achieve optimal control, fast dynamic response, easy inclusion of nonlinear constraints of the system, and flexibility to incorporate different system requirements into the controller [25], [26], [27], [28].

FCS-MPC predicts the future value from the discrete-time model, compares the cost function, and selects the switching state with the small error between the reference value and the predicted value to perform control. Thus, in FCS-MPC, the manipulated variables selected by the controller are discrete and are the switches of the converter limited to a finite set. Additionally, unlike conventional control methods, control gain design and adjustment are not required [29], [30].

In addition, since FCS-MPC does not perform switching at each sampling time, which is the cost function comparison time, the switching frequency is lower than the sampling frequency, so it is suitable as a control method for improving efficiency [31]. Above mentioned features and advantages, in this paper, FCS-MPC-based Model Predictive Current Control (MPCC) was used for current shaping control of the PFC converter. However, FCS-MPC has a variable switching frequency and does not use a modulator. As a result, it is difficult to implement the conventional interleaving method described above.

Therefore, the paper proposes a variable sampling time interleaving method implemented in MPCC based on FCS-MPC. The proposed method uses two MPCCs for the two-phase inductor current shaping control, and the two MPCCs use the same cost function. Adjust one of the two MPCCs by assigning a weighting factor to the sampling time, which is the cost function comparison time. This adjustment allows the switching states of the two phases to operate independently, achieving an effect similar to conventional interleaving methods. As a result, the proposed method achieves both robustness of current shaping capability and increased power density due to interleaving effect.

C. PAPER ORGANIZATION

The rest of the paper is organized as follows: Section II provides the derivation of the cost function for the MPCC to control the current of a single-phase totem-pole bridgeless boost PFC converter. Section III proposes an interleaving control method based on MPCC for a two-phase totem-pole bridgeless boost PFC converter to reduce inductor size and current ripple and performs a theoretical analysis. Section IV verifies the validity of the proposed method through experimental results using the 3.3kW totem-pole bridgeless boost PFC converter prototype, its power factor and input current ripple are also analyzed. Finally, Section V concludes the paper.

II. ANALYSIS OF CIRCUIT OPERATION PRINCIPLE FOR MPCC

A. ANALYSIS OF TOTEM-POLE BRIDGELESS BOOST PFC CONVERTER

Fig. 1 shows one of the bridgeless PFC converters, the totem-pole bridgeless boost PFC converter circuit. This converter has a switching device on one leg and a low-frequency diode on the other leg. It operates during both the positive and negative half cycles of the AC input voltage, and the current flow is determined by the switching method. Fig. 2 shows the direction of current flow during the positive half cycle of the AC input voltage for the totem-pole bridgeless PFC converter.

Fig.2(a) shows Q_2 is in the ON state while Q_1 is OFF complementarily, and in Fig. 2(b), the operation is reversed.

Therefore, the equivalent circuits of the input voltage during the positive and negative half cycles are shown in Fig. 3 (a) and (b). The equivalent circuit creates a synchronous boost converter, where Q_2 operates as the control switch and Q_1 operates as the synchronous switch during

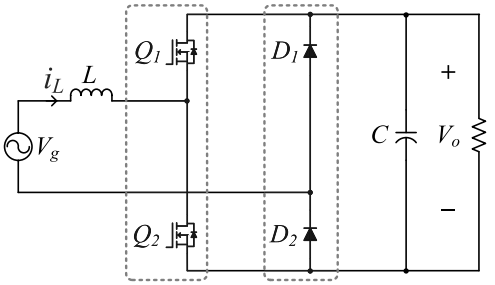

FIGURE 1. The circuit of the totem-pole bridgeless boost PFC converter.

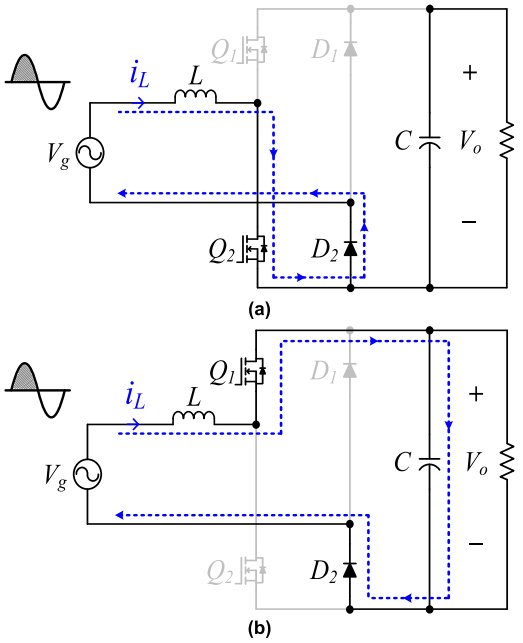

FIGURE 2. The totem-pole bridgeless boost PFC converter operating at CCM in the positive half cycle of input voltage (a) Q_1 is turned OFF; (b) Q_1 is turned ON.

the positive half cycle. Conversely, during the negative half cycle, Q_1 operates as the control switch and Q_2 operates as the synchronous switch.

B. DESIGNING A MODEL PREDICTIVE CURRENT CONTROL COST FUNCTION FOR TOTEM-POLE BRIDGELESS BOOST PFC CONVERTER

The MPCC for current control predicts the current of the next period under different switching state conditions within the sampling time, and selects a switching state with a smallest error by comparing the current value of the predicted variable $i_L(k+1)$ and the reference value i_{L_ref} through cost function comparison. The MPCC cost function is derived from the circuit equations of the equivalent circuit shown in Fig. 3.

The circuit equations according to Kirchhoff's laws for the positive and negative half cycles with the control switches ON and OFF are expressed as (1) and (2), respectively.

$$L\frac{di_L}{dt} = V_g \tag{1}$$

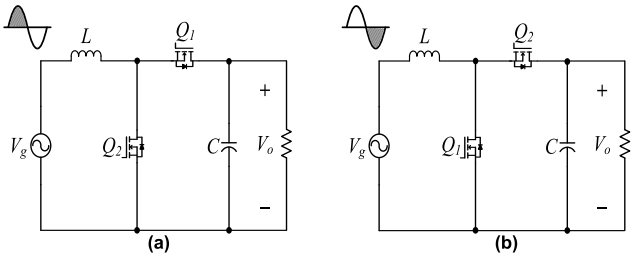

FIGURE 3. Equivalent circuit of totem-pole bridgeless boost PFC Converter. (a) Positive half line cycle (b) Negative half line cycle.

$$L\frac{di_L}{dt} = V_g - V_o \tag{2}$$

where V_g is the input voltage, V_o is the output voltage, L is the value of inductor and i_L is the inductor current.

(1) and (2) are organized into (3) depending on the switch ON/OFF state. In addition, when Euler's law is applied to the current change expression di/dt for the sampling time t_s, it is expressed as a discrete-time model such as (4).

Through (3) and (4), the inductor current of the next cycle is expressed as (5). Where t_s is the sampling time of system, 'k' represents the current cycle and '$k+1$' represents the next cycle.

$$\frac{di_L}{dt} = \begin{cases} \dfrac{V_g}{L}, & Q_1 \text{ is on} \\ \dfrac{V_g - V_o}{L}, & Q_1 \text{ is off} \end{cases} \tag{3}$$

$$\frac{di_L}{dt} = \frac{i_L(k+1) - i_L(k)}{t_s} \tag{4}$$

$$i_L(k+1) = \begin{cases} i_{L\_on}(k+1) = i_L(k) + \dfrac{V_g}{L}t_s \\ i_{L\_off}(k+1) = i_L(k) + \dfrac{V_g - V_o}{L}t_s \end{cases} \tag{5}$$

Using the above equations, the ON/OFF cost function of MPCC is expressed as:

$$g = \left| i_{L\_ref}(k+1) - i_L(k+1) \right| \tag{6}$$

III. THE PROPOSED CONTROL METHOD

A. PROPOSED INTERLEAVING CONTROL METHOD OF TWO-PHASE TOTEM-POLE BRIDGELESS BOOST PFC CONVERTER

Fig. 4 shows a circuit that consists of a two-phase totem-pole bridgeless boost PFC converter, which is controlled using a proposed method. As shown in the Fig. 4, there are two MPCC blocks to control the switching elements of two phases. The output voltage V_o tracks the reference V_{o_ref} and is controlled through a voltage compensator (G_v) to scale the AC input current reference. Each phase's inductor current (i_{L1}, i_{L2}) is individually controlled through each MPCC control block to form a sinusoidal inductor current. In order to implement the interleaving effect of the two phases, the sampling time of one MPCC is varied and controlled.

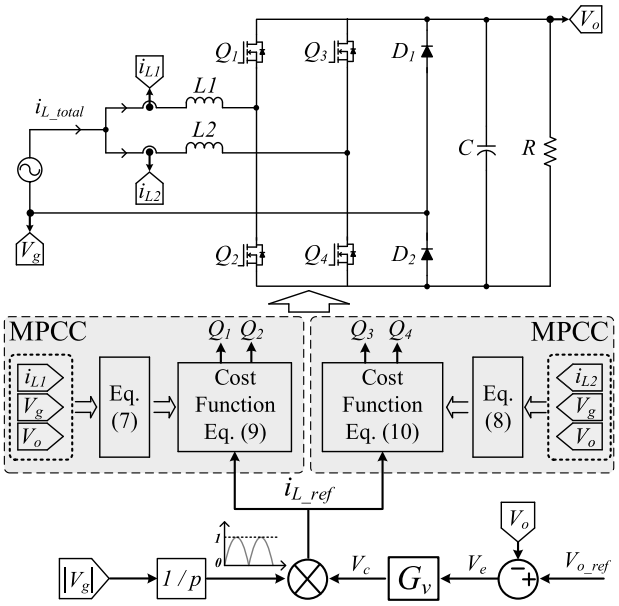

FIGURE 4. Diagram of the proposed control method for a two-phase totem-pole bridgeless PFC converter.

To explain the proposed method, the cost functions for the two MPCCs are derived first. When expressed according to the switching ON/OFF state of inductor $L1$, it is as shown in (7). Where t_{s_L1} is the sampling time of the $L1$ phase MPCC, 'k_1' represents the current cycle when the inductor current i_{L1} is expressed as discrete time and 'k_1+1' represents the next cycle.

$$i_{L1}(k_1+1) = \begin{cases} i_{L1\_on}(k_1+1) = i_{L1}(k_1) + \dfrac{V_g}{L1} t_{s\_L1} \\ i_{L1\_off}(k_1+1) = i_{L1}(k_1) + \dfrac{V_g - V_o}{L1} t_{s\_L1} \end{cases} \tag{7}$$

When expressed according to the switching ON/OFF state of inductor $L2$, it is as shown in (8). Where t_{s_L2} is the sampling time of the $L2$ phase MPCC, 'k_2' represents the current cycle when the inductor current i_{L2} is expressed as discrete time and 'k_2+1' represents the next cycle.

$$i_{L2}(k_2+1) = \begin{cases} i_{L2\_on}(k_2+1) = i_{L2}(k_2) + \dfrac{V_g}{L2} t_{s\_L2} \\ i_{L2\_off}(k_2+1) = i_{L2}(k_2) + \dfrac{V_g - V_o}{L2} t_{s\_L2} \end{cases} \tag{8}$$

Through the above equations, the MPCC cost function equations g_{L1} and g_{L2} of the inductors $L1$ and $L2$ phases are expressed as follows:

$$g_{L1} = \left| i_{L\_ref}(k_1+1) - i_{L1}(k_1+1) \right| \tag{9}$$

$$g_{L2} = \left| i_{L\_ref}(k_2+1) - i_{L2}(k_2+1) \right| \tag{10}$$

Fig. 5 shows the inductor current waveforms of two phases when the proposed interleaving method is applied. Where

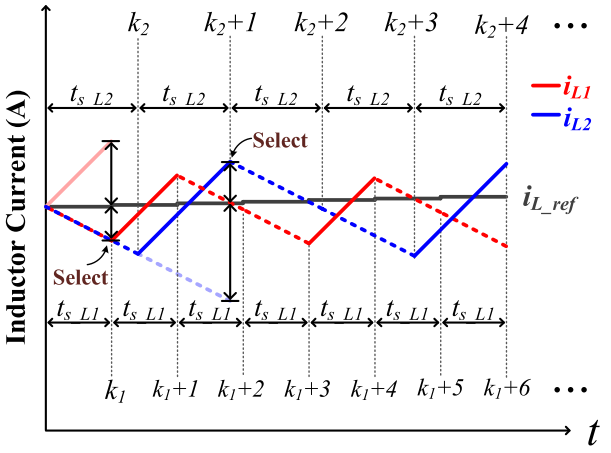

FIGURE 5. Proposed MPCC-based interleaving control method.

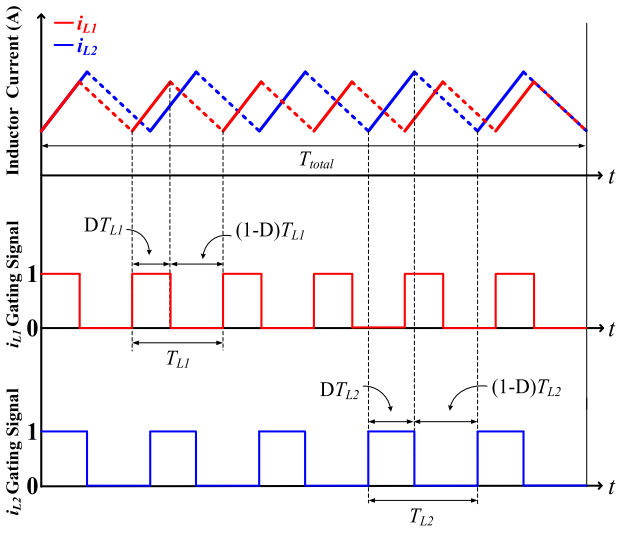

FIGURE 6. Inductor current switching period waveform of the proposed interleaving control method.

the red and blue solid lines represent the slope of ON, and the dashed line represents the slope of OFF. The Inductor currents $i_{L1}(k_1)$ and $i_{L2}(k_2)$ of the two phases predict future values from discrete-time models at predetermined sampling times and select switching states with small error compared to the reference i_{L_ref}. Therefore, the moment of comparison between the cost function and the reference is changed by varying the sampling time. As a result, the switching state of each phase is changed independently and an interleaving effect is implemented.

Fig. 6 shows the inductor current waveforms according to the switching period of the inductor current according to the sampling time variation of the proposed interleaving method. T_{total} is one period in which the inductor current switching periods of the two phases overlap at the beginning and end. T_{L1} and T_{L2} represent one switching period of the inductor currents i_{L1} and i_{L2} of the two phases, respectively, and D represents the duty ratio.

B. VARIABLE SAMPLING TIMED INTERLEAVING CONTROL METHOD INDISPENSABLE CONDITION

The following assumptions are made for convenience of analysis.

1) The converter operates in Continuous Conduction Mode.
2) The Output Voltage V_o contains only the DC component.
3) The sampling time t_s according to the variable constant and the switching period of the inductor current are proportional.
4) The sampling frequency is very high, so that voltage is constant during on period T_{total}.

Fig. 7 shows the case where the sampling time is set using the variable constant $1 + \delta$ for the sampling time of the $L2$ phase, where δ is the positive variable constant. The reference switching period of the phase having the longer switching period among the two phases is T_{std}, and the switching period of the other phase is T_{comp}. As shown in the figure, the difference between the switching period T_{std} and T_{comp} is equal to δT_{comp} and is expressed as (11).

$$T_{std} = T_{comp} + \delta T_{comp} \tag{11}$$

Using this similarity, the rise and fall of the current is expressed as follows:

$$\frac{V_g \times D \cdot \delta T_{comp}}{L} \tag{12}$$

$$\frac{(V_g - V_o) \times (1 - D)\delta T_{comp}}{L} \tag{13}$$

Thus, by varying the sampling time using a variable constant of $1 + \delta$ in one of the two phases, the components of (12) and (13) are included in the reference switching period T_{std}, which results in an increase in ripple. When the currents of two-phase inductors overlap in a circuit, the resulting ripple is defined as the ratio between the height caused by the rising and falling edges and the height caused by their cancellation. The ripple reaches 100% when the variable constant of δ is 0.25. Therefore, the maximum value of δ is set to 0.25 when a positive variable constant δ is substituted into the sampling time of one phase, as the inductor current may become saturated by the increased sampling time. Furthermore, considering the corresponding switching loss, the minimum value of δ is set to -0.25 when a negative variable constant δ is substituted, as the switching frequency increases. As a result, the conditions for the value of δ to realize the interleaving effect are selected as $|\delta| < 0.25$, $\delta \neq 0$.

C. CALCULATION OF INTERVAL LENGTH FOR EACH SWITCHING STATE BASED ON VARIABLE SAMPLING TIME

When δ is selected according to the previous conditions, it satisfies the relationship expressed in (14). Where constant A is the length of the base of T_{total}, constant B is the length of the base of T_{std}, constant C is the length of the base of T_{comp},

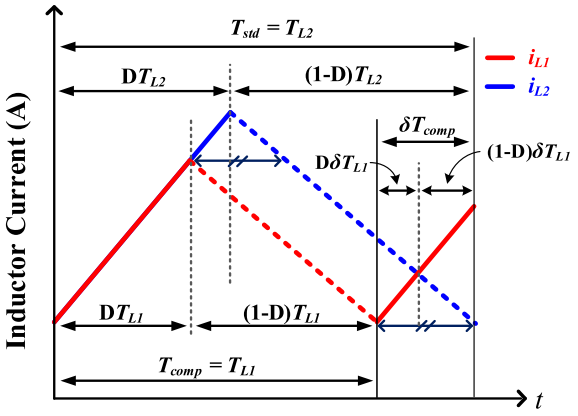

FIGURE 7. One switching cycle of two-phase inductor current when the sampling time of i_{L2} is increased Based on i_{L1}.

n is the number of T_{std}, within T_{total} and is the inverse of the variable constant δ.

$$A = \sum_{m=1}^{n} B = \sum_{m=1}^{n} (C + \delta C)$$

$$= \sum_{m=1}^{n} \{C - (m-1)\delta C\} + \sum_{m=1}^{n} (m\delta C) \tag{14}$$

The B, C and δC generated by varying the sampling time have the same duty ratio D and inductor current slope. Therefore, using the similarity relationship, A is expressed as a base for each interval according to the switching state of the two phases in terms of the duty ratio D. According to the (14) relationship, the basic formula for one period of B is expressed as follows;

"Interval 1" is the interval of D based on subtracting δC of the previous period from C within one period of B, and is expressed as (15)

$$D\,(C - (m-1)\delta C) \tag{15}$$

"Interval 2" is the interval of $(1 - D)$ based on subtracting δC of the previous period from C within one period of B, and is expressed as (16)

$$(1 - D)\,(C - (m-1)\delta C) \tag{16}$$

"Interval 3" is the interval of D based on $m\delta C$ within one period of B and is expressed as (17)

$$D\,(m\delta C) \tag{17}$$

"Interval 4" is the interval $(1 - D)$ based on $m\delta C$ within one period of B and is expressed as (18)

$$(1 - D)\,(m\delta C) \tag{18}$$

When considering the increasing $m\delta C$ and DB(duty ratio of B), the interval is divided within B. This is represented by "Interval 1 to 4" by case from "# 1 to 7", as shown in Table 1.

TABLE 1. The interval of *B* one period according to the switching state of the two phases in *A*.

One period of B (15) ~ (18)								
Case	**Interval 1**		**Interval 2**		**Interval 3**		**Interval 4**	
#1	$\{D-(m-1)D\delta\}C$		$Dm\delta C$	$\begin{Bmatrix}1-D-D\delta\\-(m-1)\delta\end{Bmatrix}C$	$Dm\delta C$		$(1-D)m\delta C$	
#2	$\{D-(m-1)\delta\}C$	$\begin{Bmatrix}(m-1)\delta\\-(m-1)D\end{Bmatrix}C$	$Dm\delta C$	$\begin{Bmatrix}1-D-D\delta\\-(m-1)\delta\end{Bmatrix}C$	$Dm\delta C$		$(1-D)m\delta C$	
#3	$\{D-(m-1)\delta\}C$	$\begin{Bmatrix}(m-1)\delta\\-(m-1)D\end{Bmatrix}C$	$Dm\delta C$	$\begin{Bmatrix}1-D-D\delta\\-(m-1)\delta\end{Bmatrix}C$	$Dm\delta C$		$(D-Dm\delta)C$	$(m\delta-D)C$
#4	$\{D-(m-1)D\delta\}C$		$Dm\delta C$	$\begin{Bmatrix}1-D-D\delta\\-(m-1)\delta\end{Bmatrix}C$	$Dm\delta C$		$(D-Dm\delta)C$	$(m\delta-D)C$
#5	$\{D-(m-1)\delta\}C$	$\begin{Bmatrix}(m-1)\delta\\-(m-1)D\end{Bmatrix}C$	$\{(1-D)-(m-1)(1-D)\delta\}C$		$\begin{Bmatrix}D\delta+D\\+(m-1)\delta-1\end{Bmatrix}C$	$\begin{Bmatrix}1+D(m-1)\delta\\-D-(m-1)\delta\end{Bmatrix}C$	$(1-D)m\delta C$	
#6	$\{D-(m-1)\delta\}C$	$\begin{Bmatrix}(m-1)\delta\\-(m-1)D\end{Bmatrix}C$	$\{(1-D)-(m-1)(1-D)\delta\}C$		$\begin{Bmatrix}D\delta+D\\+(m-1)\delta-1\end{Bmatrix}C$	$\begin{Bmatrix}1+D(m-1)\delta\\-D-(m-1)\delta\end{Bmatrix}C$	$(D-Dm\delta)C$	$(m\delta-D)C$
#7	$\{D-(m-1)D\delta\}C$		$\{(1-D)-(m-1)(1-D)\delta\}C$		$\begin{Bmatrix}D\delta+D\\+(m-1)\delta-1\end{Bmatrix}C$	$\begin{Bmatrix}1+D(m-1)\delta\\-D-(m-1)\delta\end{Bmatrix}C$	$(D-Dm\delta)C$	$(m\delta-D)C$
#8	$\{D-(m-1)D\delta\}C$		$\{(1-D)-(m-1)(1-D)\delta\}C$		$\begin{Bmatrix}D\delta+D\\+(m-1)\delta-1\end{Bmatrix}C$	$\begin{Bmatrix}1+D(m-1)\delta\\-D-(m-1)\delta\end{Bmatrix}C$	$(1-D)m\delta C$	

Cases according to specific conditions of B are divided into 8 categories, respectively, as follows:

The intervals of B's first period is referred to as #1.

The intervals of B's when $DB < m\delta C$ is referred to as #2.

The intervals of B's where C of the current period and C of the next period exist in B are referred to as #3, when $D < 0.5$ and $m\delta C$ and DC are not in a common multiple relationship.

The interval of B's when $D < 0.5$ and $DB < m\delta C < (1-D)B$ is referred to as #4.

The intervals of B's where C of the current period and C of the next period exist in B are referred to as #5, when $D > 0.5$ and $m\delta C$ and DC are not in a common multiple relationship.

The interval of B's when $D > 0.5$ and $DB < m\delta C < (1-D)B$ is referred to as #6.

The interval of B's when $(1-D)B < m\delta C$ is referred to as #7.

The interval of B's end period is referred to as #8.

Where DC is duty ratio of C.

In conclusion, the length of the base of A for each interval according to the switching state of the two-phase is obtained. Accordingly, the ratio of the offset interval according to the value of the variable constant δ and the duty ratio D in A can be obtained.

IV. RESULT OF VERIFICATION

A. SELECTING THE OPTIMAL CONSTANT OF VARIABLE SAMPLING TIME

To verify the performance of the proposed method, a 3.3kW converter was used, and the circuit parameters for verification are shown in Table 2.

Fig. 8 shows the peak-to-peak ripple and average ripple in A (T_{total}) one period near the peak voltage. As shown in figure, when δ is 0, there is no interleaving effect. When $|\delta|$ is 0.001, the variable constant is very small, and the interleaving effect is insignificant. In addition, it can be seen that the current ripple decreases due to the interleaving effect as the $|\delta|$ increases. However, when a positive variable constant δ of 0.1 or more is applied, the ripple increases. Therefore, in this paper, the negative variable constant -0.2 with the lowest current ripple was selected.

Fig. 9 (a) and (b) show the waveform of the input current i_{L_total} and input voltage V_g when the proposed interleaving method is without applied and with applied, respectively. Compared to the case where it is not applied, the average current ripple during the entire one cycle near peak voltage A has decreased by 49.09% and the peak-to-peak current ripple has decreased by 25.58%. In addition, when the proposed control method is with applied, the power factor of input voltage and current is 0.99.

TABLE 2. Electrical parameter of the PFC converter.

Symbol	Quantity	Value
V_g	Input voltage	220 V_{rms}
f_{line}	Line frequency	60 Hz
V_o	Output voltage	380 V_{dc}
R	Load resistance	46 Ω
f_{samp}	Sampling frequency	50 kHz
L_1, L_2	Input inductance	2.5 mH
C	Output capacitance	1000 μF

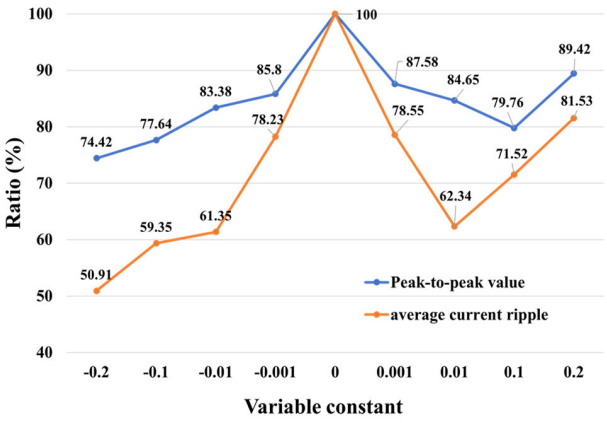

FIGURE 8. Comparison of peak-to-peak ripple in $A(T_{total})$ One Period near the Peak Voltage according to Variable Constant.

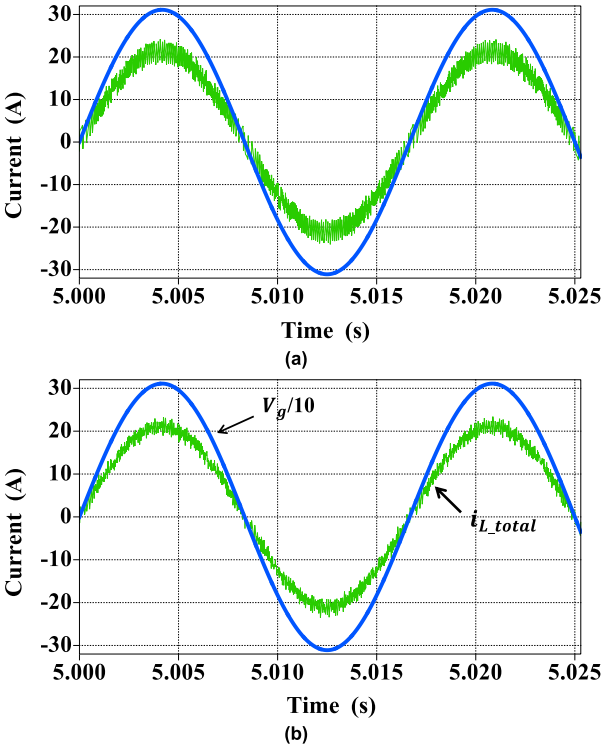

FIGURE 9. Waveform of the input voltage and input current (a) Without Applying the proposed interleaving method (b) With applying the proposed interleaving method.

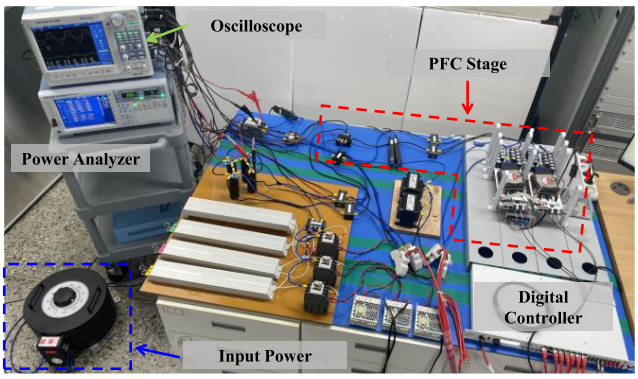

FIGURE 10. Experimental setup of totem-pole bridgeless boost PFC converter prototype.

B. EXPERIMENTAL RESULTS

To verify the simulation result and the performance of the proposed control method, experiments were conducted by using the 3.3 kW totem-pole bridgeless boost PFC converter prototype as shown in Fig. 10.

The parameters used in the experiment were the same as in the simulation, and the optimal variable constant selected through the simulation was applied to the experiment. The experimental results were measured and analyzed using an oscilloscope to evaluate the performance of the proposed control method. In addition, in order to compare the performance of the proposed control method, a comparative analysis was performed with the conventional PI control method with a switching frequency of 50 kHz that implements an interleaving effect through the phase shift of the PWM carrier wave.

Fig. 11(a) and (b) show input current i_{L_total} and the current waveform results of two-phase inductor i_{L1} and i_{L2} without and with applying the proposed control method.

In Fig. 11(a), the inductor currents of both phases, i_{L1} and i_{L2}, have the same current waveform, resulting in i_{L_total} being the sum of i_{L1} and i_{L2}.

On the other hand, Fig. 11(b) shows the results of with applying the proposed method to the inductor current i_{L1}. The results of with applying the proposed method shows that the ripple of the input current i_{L_total} is reduced compared to Fig. 11 (a).

Fig. 12(a), (b) and (c) show the waveform results of input current i_{L_total}, input voltage V_g, and output voltage V_o without and with applying the proposed control method and with applying the conventional control method.

The input current ripple rate analysis result for Fig. 12 is shown in Table 3. As a result of comparison between the proposed control and the conventional PI control methods, the peak-to-peak value of the current ripple rate was 3.6% higher. Conversely, the average value was measured to be 2.1% lower. The peak-to-peak value was higher, while the average value was measured lower, confirming the

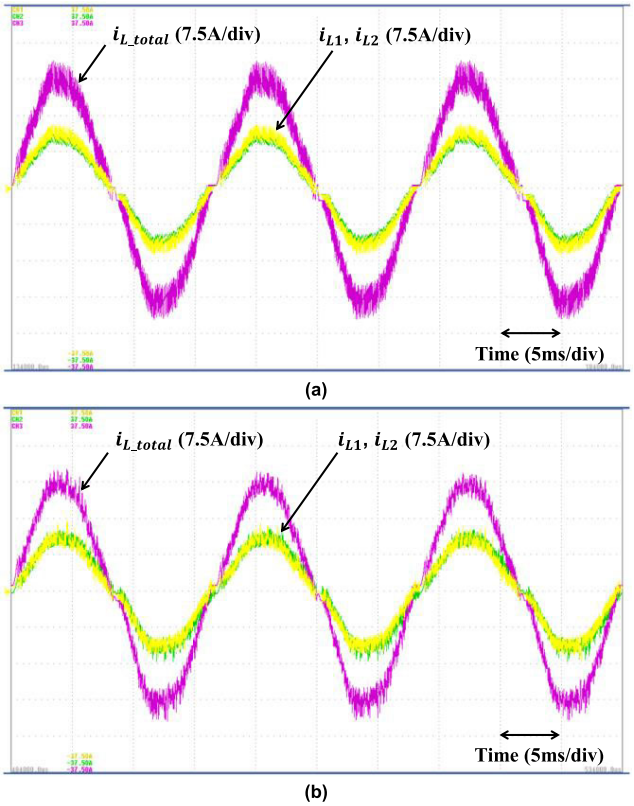

FIGURE 11. Waveform of model predictive current control PFC. (a) Without applying the proposed interleaving method (b) With applying the proposed interleaving method.

TABLE 3. Ripple rate of input current.

Conditions	Without interleaving	Proposed method	Conventional method
Peak-to-peak Value rate	100%	76.1%	72.5%
Average Value rate	100%	51.3%	53.4%

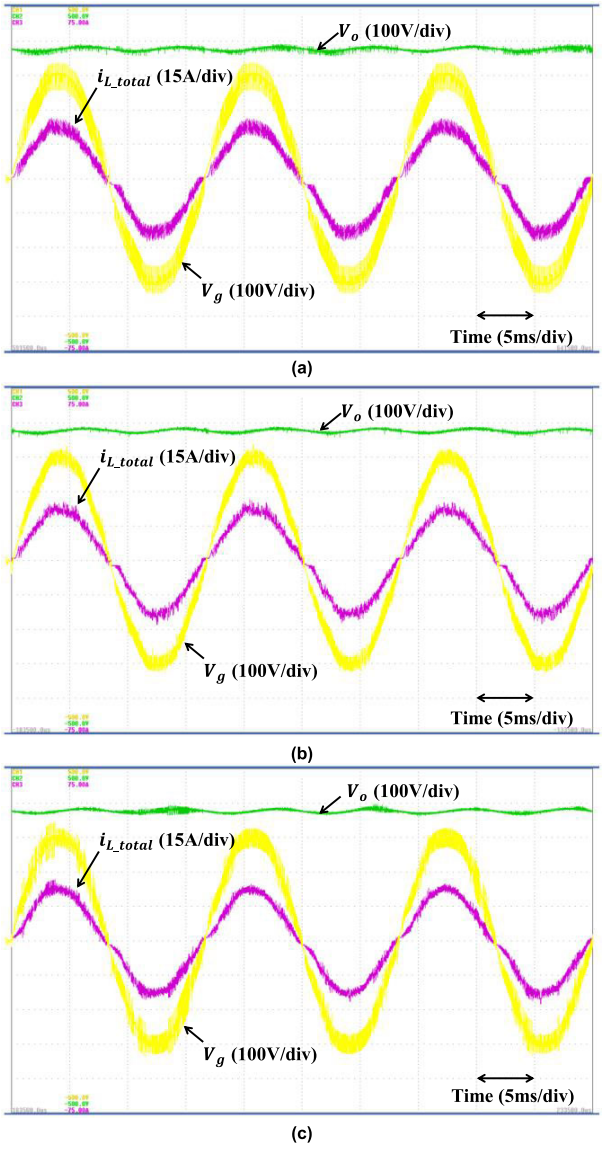

FIGURE 12. Waveform of comparison between the proposed control method and the conventional control method (a) Without applying the proposed interleaving method (b) With applying the proposed method (c) Conventional interleaving method.

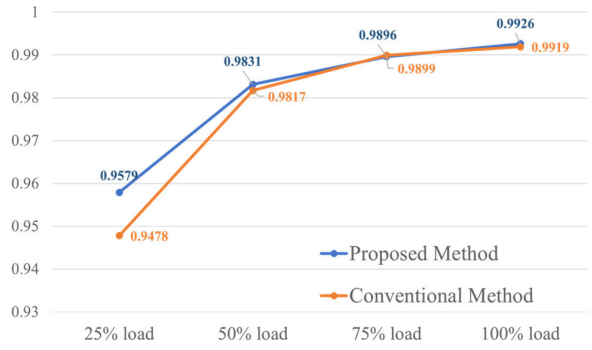

FIGURE 13. Power factor measurements at different load condition.

validity of the proposed method. In addition, the THD of the proposed method satisfies the IEC-61000-3-2 Class A standard.

Fig. 13 shows the measured power factor of the proposed method and the conventional method. As a result of power factor comparison, the proposed control method has a higher or similar power factor in entire load conditions compared to the conventional PI control method. In particular, at 100% load, both control methods showed a high-power factor of 0.99 or more. However, the power factor of the proposed method was measured as 0.9926, showing a higher power factor than the conventional method. These results mean that the proposed control method is suitable for current shaping control of the input current.

Fig. 14 shows the waveform of the transient response characteristics of the load change with applying the proposed interleaving control method. Experiments were conducted on load changes from 75% to 100%, and the figure

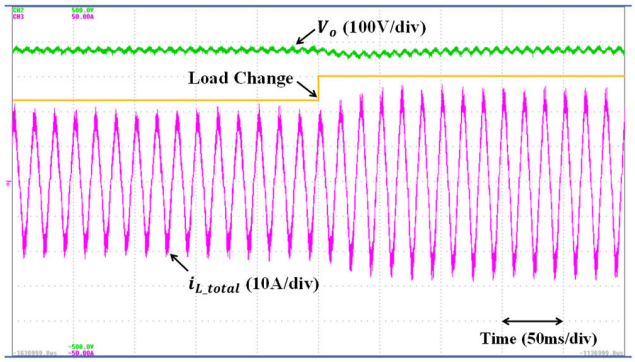

FIGURE 14. Transient response of input current i_{L_total} and output voltage V_o under load change from 75% to 100% load.

shows that the proposed method is robust against load changes.

V. CONCLUSION

A MPCC-based variable sampling time interleaving control method for current shaping and current ripple reduction was proposed in this paper. Since the proposed method is based on the MPCC of FCS-MPC technology, the switching frequency is variable and does not require a separate modulator. Accordingly, it is difficult to implement the conventional interleaving method using the carrier wave phase shift of PWM. Therefore, a method is proposed to change the switching period by weighting factor it at the sampling time, which is the comparison point between the predicted future values from the discrete-time model and the cost function. As a result, the interleaving effect was implemented by allowing the switching states of the two phases to operate independently, and the validity of the proposed method was verified through real experiments. The verification results showed that the proposed method had the effect of reducing the input current ripple, and in particular, the power factor at 100% load showed a high-power factor of 0.99 or more. In addition, it was confirmed that it was robust against load fluctuations.

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