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RESEARCH ARTICLE

# 103.1-dB DR Switched-Resistor Delta-Sigma Modulator With Chopped Negative-R for Suppressing Low-Bandwidth Noise

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**ABSTRACT** This paper presents a high-resolution, low-bandwidth, continuous-time delta-sigma modulator (CTDSM). Although continuous-time integrators are popular for implementing power-efficient DSMs, the coefficient of conventional RC integrators depends on the clock frequency and requires excessively large resistance and capacitance for implementation in low-bandwidth CTDSMs. The high resistance causes thermal noise, limiting the overall performance of the modulator. Accordingly, the CTDSM presented herein incorporates a switched resistor (SR) integrator that overcomes the thermal noise issue and enables high-resolution CTDSM to be used in low-bandwidth applications. The proposed integrator also adopts a chopped negative-R technique to reduce the flicker noise in the amplifier while simultaneously enhancing linearity. The proposed 3rd-order CTDSM is successfully fabricated in a 0.18-$\mu$ m CMOS process and achieves the following measurement results: a peak signal-to-noise and distortion ratio of 98.8 dB, dynamic range of 103.1 dB, total power consumption of 20.3 $\mu$ W, and signal bandwidth of 200 Hz.

**INDEX TERMS** Analog-to-digital converter (ADC), switched resistor (SR) integrator, continuous-time delta-sigma modulator (CTDSM), chopped negative R, low bandwidth.

## I. INTRODUCTION

Recently, the demand for low-bandwidth sensors has increased significantly for applications such as biomedical [1], [2], [3], battery-monitoring current [4], and temperature [5], [6], [7]. Sensor systems demand low power and high resolution, especially mobile sensors with a signal bandwidth of several hundred Hertz.

Conventional switched-capacitor delta-sigma modulators (DSMs) exhibit extremely stable performance [8]. However, their power efficiency is poor owing to the requirement of high-speed operational amplifiers (op amps) [9]. In contrast, continuous-time (CT) DSMs can be implemented with relatively low-speed op amps and are becoming popular in many applications.

The active RC (A-RC) integrator has excellent linearity and can achieve a high dynamic range (DR) because the feedback loop enforces a strong virtual ground at the input of the op-amp [10], [11]. Therefore, A-RC integrators are

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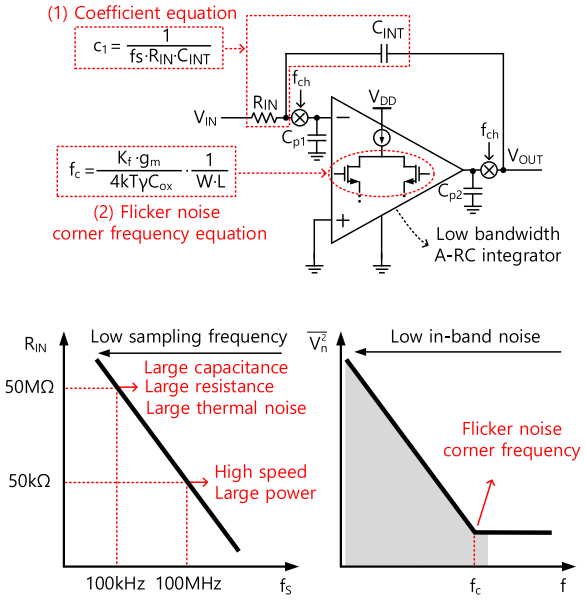


**FIGURE 1.** Resistance value and flicker noise issues of a conventional A-RC integrator in low-bandwidth.

used in many CTDSMs [12], [13]. Although CTDSMs exhibit high performance, the A-RC integrator has limitations in achieving a high signal-to-noise ratio (SNR) and distortion ratio (SNDR) for signal bandwidths of several hundred Hertz. The RC time constant must be excessively large to implement the integrator coefficients. However, the thermal noise of large input resistors makes it difficult to implement high-SNDR CTDSMs in low-bandwidth applications.

Two issues must be addressed in low-bandwidth CTDSMs, as shown in Fig. 1. The most important is the thermal noise from the resistor, which determines the coefficient using two other parameters. For example, if we assume an integrator coefficient ($c_1$) of 0.2 (which is common in high-order DSMs), the RC value can be determined once the sampling frequency ($f_s$) is known, which can be 100 MHz (or higher) for high-speed CTDSMs. Then, values of 50 kΩ and 1 pF can respectively be selected for the resistance and capacitance, occupying a reasonable chip area and generating low thermal noise. Hence, thermal noise of the resistor is not a critical issue for high-speed CTDSMs. However, with an $f_S$ of 100 kHz for low-bandwidth applications, the RC value would increase significantly for the same coefficient of 0.2. For example, if a 1 pF capacitor is selected, resistor $R_{IN}$ becomes 50 MΩ. The thermal noise would increase significantly, and the expected improved performance would be unachievable owing to the resulting excessively high thermal noise.

Another important type of noise to consider is shown in Fig. 1. Flicker noise is a low in-band noise that degrades resolution and performance [14]. Because the corner frequency ($f_c$) of the flicker noise is inversely proportional to the size of the op-amp, increasing the size of the op-amp can reduce its effect of flicker noise. However, because increasing the size inevitably increases the parasitic capacitance and reduces the speed of the op amp, a higher power consumption is required to recover the speed.

In this study, we focused on overcoming the limitations of the conventional A-RC integrator to enable high resolution at low sampling frequencies. To achieve this, we introduced the proposed switched-resistor (SR) integrator, which maintains the advantages of CTDSM while achieving a dynamic range (DR) of over 100 dB with typical RC sizing. Additionally, by applying the chopped negative-R technique to the SR integrator with lower power consumption compared to its application in the A-RC integrator, we effectively suppressed the op-amp's input-referred noise and improved linearity. As a result, we obtained a dynamic range (DR) of over 100 dB.

The remainder of this paper is organized as follows. In Section II, we review the low-bandwidth integrator for noise reduction. Section III presents the circuit implementation. Section IV provides the measurement results of the designed CTDSM. Section V presents the conclusions.

## II. LOW-BANDWIDTH INTEGRATOR FOR NOISE REDUCTION

For a low-bandwidth A-RC integrator to achieve a DR higher than 100 dB, area and noise limitations must be overcome. Fig. 2 displays three DSM loop filters based on the conventional A-RC, switched-capacitor (SC) integrators, and the proposed SR integrator. Here, H(s) and H(z) represent the remaining parts of the loop filter, while R-DAC and C-DAC denote resistive and capacitive feedback digital-to-analog converters (DACs). Furthermore, $R_{IN}$ is an input resistor, $C_{IN}$ denotes an input capacitor, $C_{INT}$ is an integrating capacitor, and $f_S$ is the sampling frequency. Term $f_S = 2f_B$OSR (OSR=256) is the oversampling ratio and $f_B$ is the signal bandwidth frequency. The coefficient of the first integrator ($c_1$) of 0.2 is achieved, where $c_1$ is generally between 0.1 to 0.2 [12], [15], [16].

Fig. 2(a) displays the CTDSM loop filter, where the first integrator is implemented by an A-RC integrator. In an A-RC integrator with a low-sampling frequency ($f_S$), the values of resistor $R_{IN}$ and capacitor $C_{INT,A-RC}$ increase significantly. In particular, the capacitor $C_{INT,A-RC}$ area issue becomes more serious because the increase in resistor $R_{IN}$ is restricted to avoid thermal noise. The $C_{INT,A-RC}$ value of the conventional A-RC integrator can be expressed as follows [17]:

$$C_{INT,A-RC} = \frac{1}{R_{IN} \cdot f_S \cdot c_1}. \tag{1}$$

Fig. 2(b) shows the SCDSM loop filter. The SC integrator performs integration by charging and discharging capacitors. Fig. 2(c) displays the proposed CTDSM loop filter, in which the first integrator is implemented by an SR integrator and two switches operate at a duty cycle of 50% of the signal. The first integrator's $C_{INT,SR}$ value can be expressed

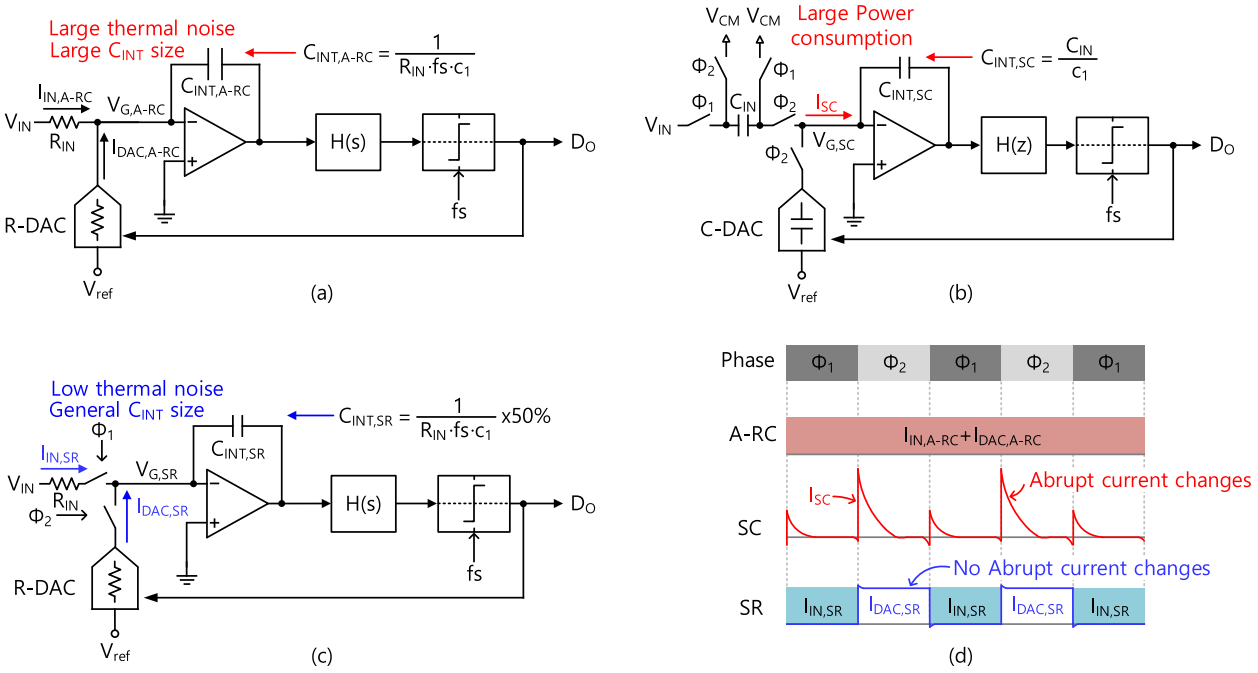


**FIGURE 2.** Depiction of the DSM loop filters, where the first integrator is implemented respectively by (a) an A-RC integrator, (b) an SC integrator, (c) an SR integrator, accompanied by (d) a timing diagram including the input node currents of each integrator.

as follows:

$$C_{INT,SR} = \frac{1}{R_{IN} \cdot f_S \cdot c_1} \times 50\%. \tag{2}$$

Here, the proposed SR integrator, which switches at the input like the SC integrator, also lacks an anti-aliasing filter structure. Nevertheless, it is clear that the SR integrator can generate the same coefficient and input resistance with smaller values for the integrating capacitance when compared to an A-RC integrator.

Fig. 2(d) displays the timing diagram and current waveforms of each integrator. In the conventional A-RC integrator, the input signal and DAC feedback signal are integrated simultaneously. In contrast, the proposed SR integrator integrates the input signal during the $\phi_1$ phase and the DAC feedback signal during the $\phi_2$ phase. In addition, while the SC integrator exhibits abrupt current changes, the SR integrator shows no abrupt current changes. Consequently, even when using an amplifier with the same speed as the A-RC integrator, the proposed SR integrator performs with sufficient linearity.

The thermal noise of the resistor and capacitor for the 1st integrator basically decides the target DR. To achieve a high resolution, a smaller-value integrator resistor $R_{IN}$ is preferred. Moreover, as the input resistance decreases, the input current increases, and the transconductance of the op-amp increases; hence, the current consumption also increases. Therefore, using a conventional A-RC integrator in a CTDSM for low-bandwidth applications would render it difficult to achieve high resolution.

As displayed in Fig. 2(a), the thermal noise of the A-RC integrator can be calculated as follows [15]:

$$\begin{aligned} v_{n,A-RC}^2 &\cong 8kTf_B(R_{IN} + R_{DAC}\frac{R_{IN}^2}{R_{DAC}^2}) \\ &\cong 16kTf_BR, \end{aligned} \tag{3}$$

where $R_{IN}$ and $R_{DAC}$ are the input resistance and the DAC resistance, respectively ($R = R_{IN} = R_{DAC}$). The formula for the value of capacitor $C_{INT,A-RC}$ according to the target thermal noise power $v_{n,A-RC}^2$ in the A-RC integrator is as follows:

$$C_{INT,A-RC} = \frac{8kT}{c_1 \times v_{n,A-RC}^2 \times OSR}. \tag{4}$$

In (4), k is the Boltzmann constant and T is the absolute temperature. The capacitor $C_{INT,A-RC}$ of the A-RC integrator is inversely proportional to the target thermal noise $v_{n,A-RC}^2$. Therefore, capacitor $C_{INT,A-RC}$ of the A-RC integrator targeting low thermal noise is significantly increased.

Regarding the noise analysis, while the DTDSM operates in a sample-and-hold manner, the proposed SR integrator continuously integrates over the entire period, as shown in Fig. 2(d). Therefore, we have assumed the possibility of continuous noise analysis for the proposed SR integrator. Using a similar principle, the input thermal noise of the proposed SR integrator in Fig. 2(b) can be expressed as follows:

$$\begin{aligned} v_{n,SR}^2 &\cong 8kTf_B(R_{IN} + R_{DAC}\frac{R_{IN}^2}{R_{DAC}^2}) \times 50\% \\ &\cong 8kTf_BR. \end{aligned} \tag{5}$$

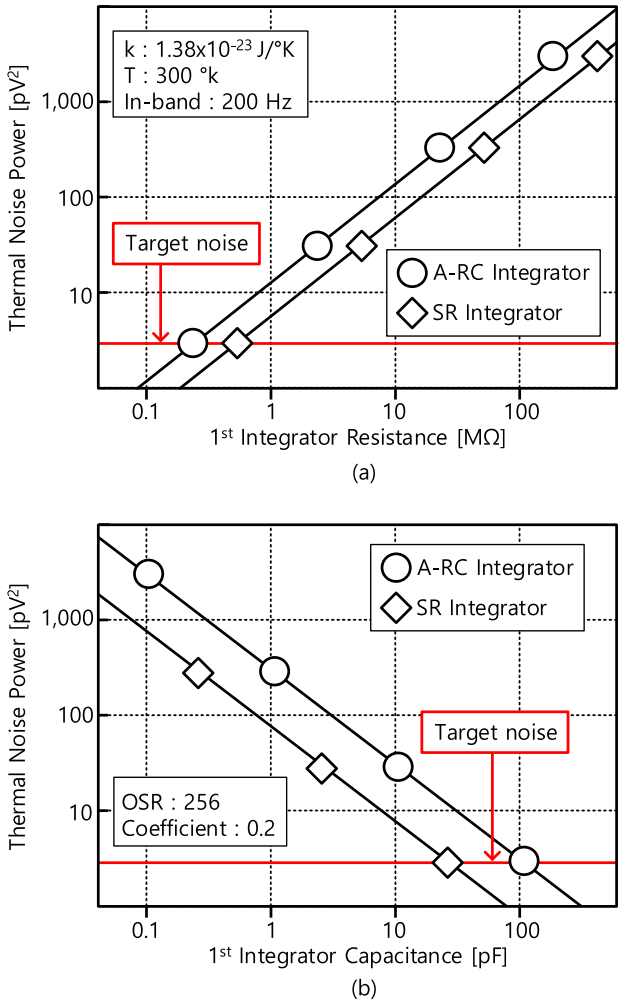


**FIGURE 3.** Comparison of thermal noise power versus an increasing 1$^{st}$ integrator (a) resistance and (b) capacitance.

It is evident that the thermal noise of the integrator is halved because the $R_{IN}$ and $R_{DAC}$ resistors operate at 50% duty in different cycles. Therefore, in the proposed SR integrator, the value of $C_{INT,SR}$ according to the target thermal noise $v^2_{n,thermal}$ can be expressed as follows:

$$C_{INT,SR} = \frac{2kT}{c_1 \times v^2_{n,SR} \times OSR} \tag{6}$$

Fig. 3(a) displays resistor value versus thermal noise for the A-RC and SR integrators. Comparing (3) and (5), the thermal noise $v^2_{n,SR}$ of the SR integrator is twice as small as the thermal noise $v^2_{n,A-RC}$ of the conventional A-RC integrator. In particular, comparing (4) and (6), the capacitor value according to the target thermal noise of the SR integrator becomes four times smaller than that of the A-RC integrator.

Fig. 3(b) displays the integrator capacitor value according to the thermal noise of the A-RC integrator and SR integrator. Here, it is evident that the thermal noise decreases with increasing integrating capacitance. When the SR integrator target thermal noise power is close to 5 p$V^2$, the integrator

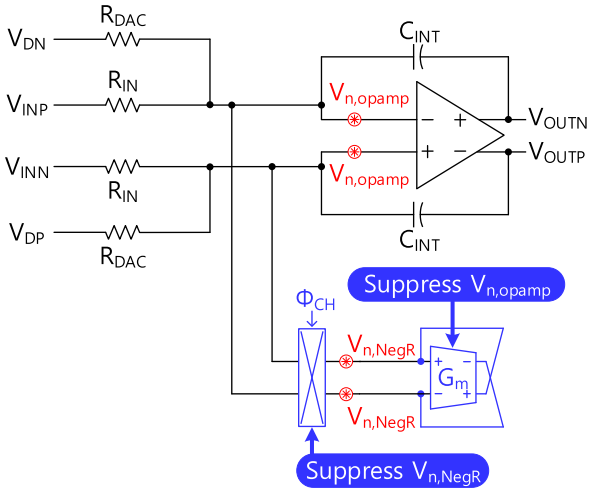


**FIGURE 4.** Simplified schematic of the active-RC integrator with a chopped negative-R [13].

capacitance is 32 pF, which is a general size that can be implemented in an integrated circuit (IC). However, when the target thermal noise power is approximately 5 p$V^2$, the A-RC integrator capacitance increases to 128 pF, which is too large to be implemented in an IC. Furthermore, if the SR integrator duty cycle is less than 50%, the integrator's area and thermal noise effect can be further reduced. However, the first integrator is very important for the CTDSM's performance, and considering the linearity of the integrator, a 50% duty cycle was selected in this study.

In addition to thermal noise, low in-band flicker noise also limits the signal-to-noise ratio (SNR) of the CTDSM. Therefore, the total noise power thermal noise and flicker noise according to the target SNR can be expressed as follows [15]:

$$v^2_{n,tot} = v^2_{n,thermal} + v^2_{n,flicker} = v^2_s \cdot 10^{-\frac{SNR_{target}}{10}}, \tag{7}$$

where $v^2_{n,tot}$ is the sum of thermal noise and flicker noise. If the input signal power $v^2_s$ is 0.4 and the target SNR is 90 dB, the total noise power $v^2_{n,tot}$ must be less than 400 p$V^2$. Using the capacitance in (1) and the thermal noise in (3), if the first integrating capacitance is 40 pF, the thermal noise power of the A-RC integrator is 16 p$V^2$. Therefore, there is no thermal noise problem, even if the capacitance of the conventional A-RC integrator is just several tens of pF. However, when the target SNR is close to 100 dB, the total noise power must be less than 40 p$V^2$. Thermal noise is a large proportion of the total noise value in A-RC integrators. The proposed SR integrator obtains 4 p$V^2$ thermal noise power using the same capacitance as the A-RC integrator through (2) and (5). Overall, the proposed CTDSM, in which the first integrator is implemented by an SR integrator, requires only 25% of the integrated capacitance of a conventional A-RC integrator to achieve a similar target thermal noise power.

Fig. 4 shows a simplified circuit of the A-RC integrator with applied chopped negative-R. A negative-R is commonly employed in conventional A-RC integrators, which serves

to compensate for the loss current of the resistor by generating an equal compensation current. The loss of current compensation improves the linearity of the op-amp [16]. Furthermore, although using a negative-R can effectively suppress $V_{n,opamp}$, the 1/f noise of the negative-R, $V_{n,NegR}$ becomes the dominant 1/f noise source in the CTDSM. Adding chopping to the virtual ground where the negative-R is connected, as shown in Fig. 4, effectively reduces the in-band 1/f noise. Hence, the remaining in-band noise consists only of thermal noise [13].

The proposed circuit successively integrates different signals in phases $\phi_1$ and $\phi_2$. Fig. 5 depicts the operation of the proposed SR integrator with a chopped negative-R. The proposed circuit consists of a switched-resistor circuit and a chopped negative-R. In general, when designing a switch and a resistor together, it is necessary to consider $R_{on}$.

In the designed CTDSM, the maximum input swing is a $V_{pp}$ of 1.15 V. In addition, the switches $S_{1-4}$ are only connected to the input of the amplifier. Hence, the complementary switches were sufficient to ensure linear operation. We did not use bootstrapped switches as they would lead to a larger area and higher power consumption. Resistors $R_{IN}$ and $R_{DAC}$ of a low-bandwidth SR integrator are hundreds of kΩ, whereas the on-resistances of switches $S_{1-4}$ are only hundreds of ohms. Therefore, since $R_{on,S_{1-4}} \ll R_{IN,DAC}$, it is not necessary to consider the on-resistance of the switches when configuring the circuit.

As shown in Fig. 5(a), as switches $S_1$ and $S_2$ are turned on in $\phi_1$, the input signals are integrated, and switches $S_3$ and $S_4$ are turned off to block DAC feedback signals. Conversely, in $\phi_2$, as switches $S_3$ and $S_4$ are turned on, the DAC feedback signals are integrated, and switches $S_1$ and $S_2$ are turned off to block the input signals. Therefore, for the entire period, the proposed SR integrator works in the same way as an A-RC integrator composed of the equivalent resistance $R_{eq}(= R_{IN} = R_{DAC})$ and $C_{INT}$. In addition, a chopped negative-R was applied in the proposed SR integrator, since it has the same continuous-time operation as the A-RC integrator in $\phi_1$ and $\phi_2$. The total current loss generated in the SR integrator is equal to the input current loss in $\phi_1$ or the DAC feedback current loss in $\phi_2$. Therefore, a chopped negative-R can be designed with less power than that applied to a conventional A-RC integrator.

Fig. 5(c) shows the chopping operation when all switches are open for a short period. Chopping operates in dead-time without input current and feedback DAC current. Thus, when the chopping of the negative-R circuit is operating, there is no interference between the DAC path with a large step of single-bit feedback and the input signal path, thereby effectively minimizing harmonic distortion of the CTDSM. The results of noise simulation showed that the proposed SR integrator structure effectively suppressed the previous input-referred total noise from 76 $pV^2$/Hz to 22.7 $pV^2$/Hz by applying the chopped negative-R technique.

Fig. 5(d) display the timing diagram of the SR integrator. Although the dead-time has a short period of 1.2 nS, this is a sufficient period for the chopping operation. Furthermore, since the dead-time of 1.2 nS is much shorter than the 4.9 $\mu$S at which the signal is integrated, the dead-time period is very short compared to the entire period.

## III. CIRCUIT IMPLEMENTATION

The proposed CTDSM was designed with a single-bit, third-order, CIFF CTDSM structure. The output voltage swing of each integrator was reduced due to the feedforward path of the modulator. Therefore, this alleviated the slew rate and voltage headroom constraints of the op-amp [17], obtaining good power efficiency.

To ensure stability of the proposed CTDSM, a noise transfer function (NTF) peak gain of 1.5 was used. Moreover, with a signal bandwidth of 200 Hz and a sampling frequency of 102.4 kHz, the coefficients of the proposed CTDSM were determined through MATLAB/Simulink modeling.

Fig. 6 displays the circuit implementation of the proposed CTDSM. Here, $V_{ref}$ is set to the same value as the supply voltage, which is 1.8 V. The first integrator was designed with an SR integrator and the second and third integrators were designed with A-RC integrators. The open-loop structure of the negative-R is directly subjected to PVT variations. Significant variations in the negative-R suggest that the input-referred noise and the linearity of the first op-amp cannot be effectively compensated to match these changes. Thus, negative-R was implemented with a cross-coupled inverter amplifier source-degenerated structure to improve linearity and reduce matching issues. With respect to resistance PVT variations, the source degeneration and target resistors were implemented with the same type of resistor. The large $G_m$ of the source degeneration negative-R is given by

$$G_m = \frac{2g_m}{(1 + g_m R_D)}. \tag{8}$$

In negative-R, PMOS and NMOS have the same transconductance of 1.64 $\mu$S and the degeneration resistor was designed as 610 kΩ.

The designed CTDSM has an input impedance of 1.22 MΩ due to its 50% duty cycle. Additionally, switch $S_B$ is designed to prevent the input node from floating during $\phi_2$ phase and to provide a constant input current at the input loading [18].

Fig. 7 presents the matching error between the implemented negative-R and the target resistance according to PVT variations. Fig. 7(a) displays the simulation results of matching error under different CMOS process corners (SS, SF, TT, FS, and FF) with different temperatures (–40 and +120 °C). It is evident that the mismatch was within ±10% in all cases. Fig. 7(b) displays the simulation results of matching error under different corners when the 1.8 V supply voltage had variations of −10% and +10%. Here, it can be observed that the worst matching error of 7% was obtained when the supply voltage had a variation of −10% at the SS process corner. In comparison, the mismatch was within 2% for all

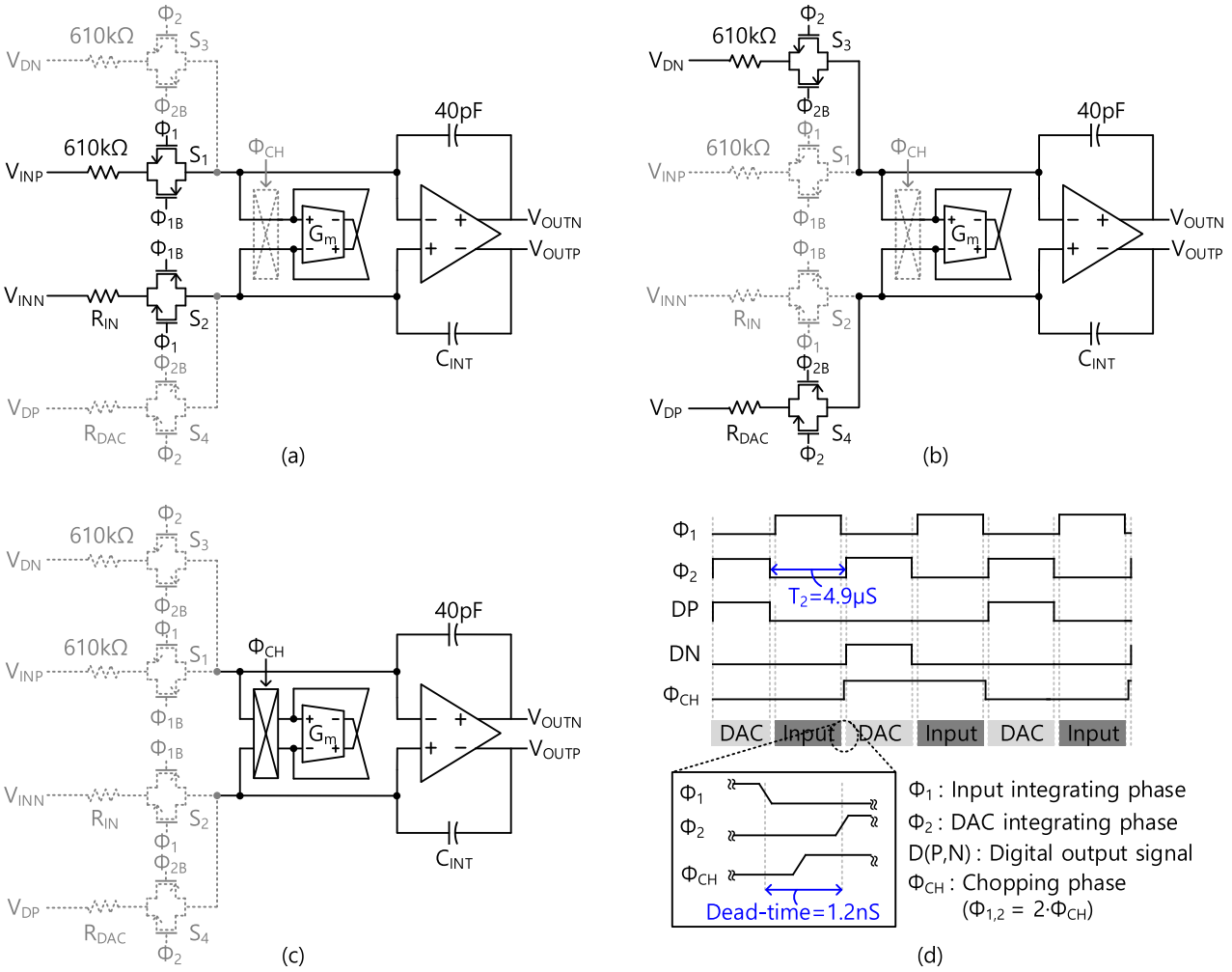


**FIGURE 5.** Operation of the proposed SR integrator (a) $\phi_1$: analog input integration mode, (b) $\phi_2$: DAC feedback integration mode, (c) $\phi_{ch}$: dead-time for the negative-R chopping region, (d) timing diagram.

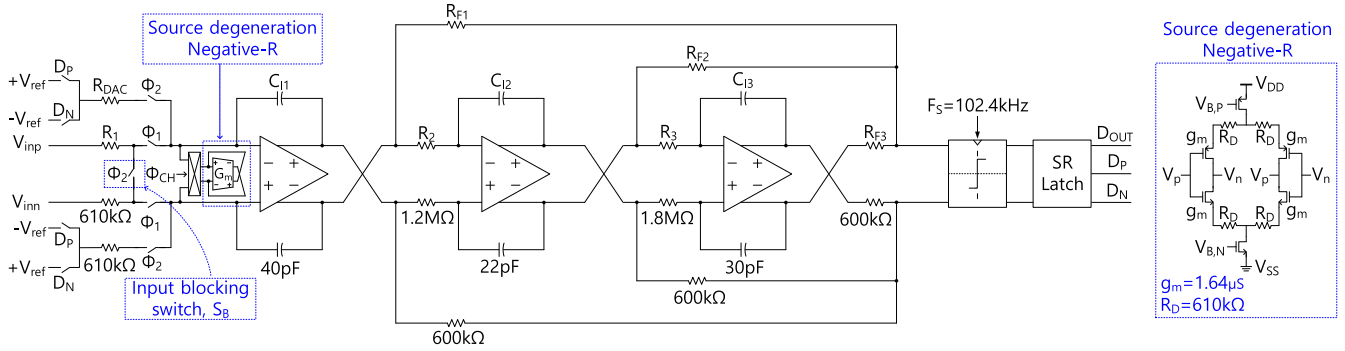


**FIGURE 6.** Switched-resistor CT schematic.

the other cases. Thus, the mismatch problem due to PVT variation was minimized.

The DC-gain of the SR integrator according to the matching coefficient $\alpha$ is as follows [16]:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{\alpha}{\alpha - 1}\right) \times A_v \tag{9}$$

where $\alpha$ represent the matching between the target resistance ($R_{eq} = R_1 = R_{DAC}$) and negative-R of the SR integrator in Fig. 6. If the matching coefficient $\alpha \approx 1$, the integrator DC-gain becomes infinite. Fig. 8 displays the simulation results of DC-gain according to the ±30% variation in the source degeneration resistance of negative-R and the target resistance.

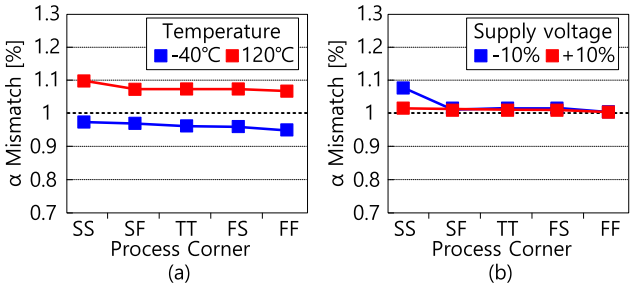


**FIGURE 7.** Simulated negative-R with (a) temperature variations, and (b) supply voltage variations.

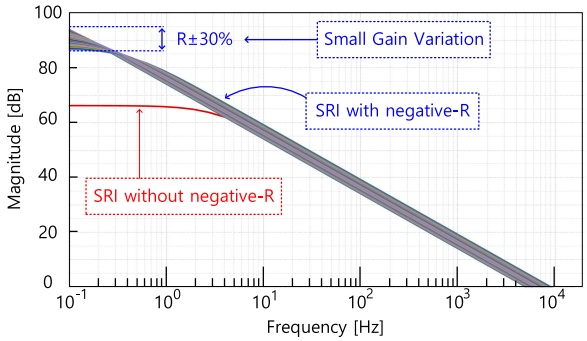


**FIGURE 8.** DC-gain according to resistance variation of the SR integrator with negative-R.

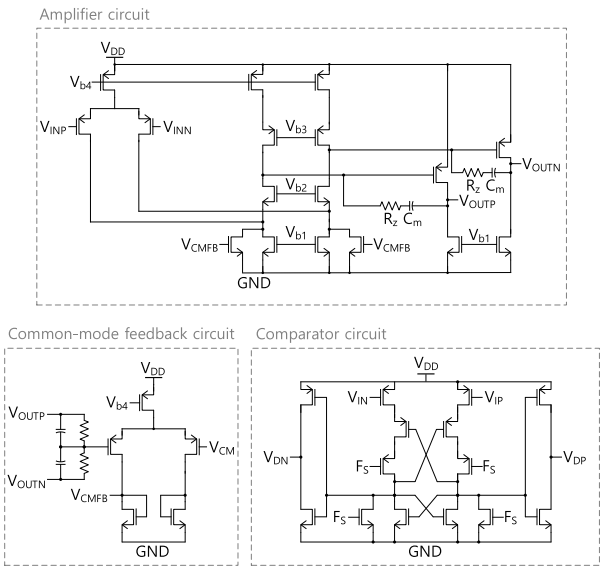


**FIGURE 9.** Schematic of the amplifier and comparator circuit.

Fig. 9 displays the circuit diagrams of the used op-amp and comparator. The designed CTDSM used a 1-bit quantizer [15] and a two-stage folded cascode amplifier structure. By applying chopped negative-R, we can achieve sufficient optimization for low power consumption in the first op-amp since chopping is not performed during the input and output stages.

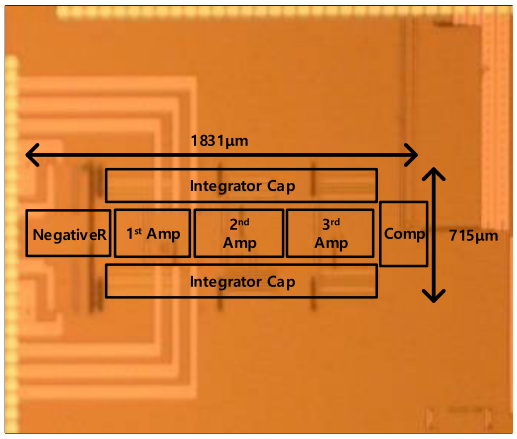


**FIGURE 10.** Chip microphotograph.

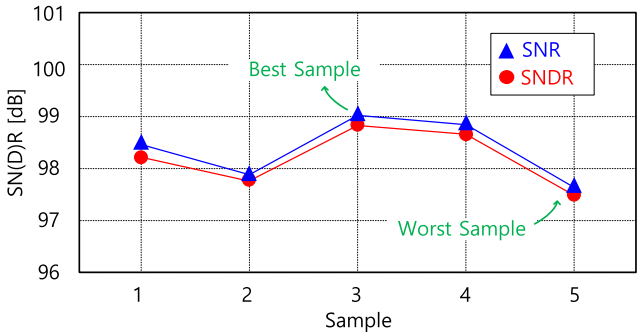


**FIGURE 11.** Measured peak SNR and SNDR of five samples.

The DC-gain of the SR integrator without negative-R was 65 dB. In comparison, the DC-gain of the SR integrator with negative-R was 96 dB, and 30 dB was compensated through negative-R compensation. Even in the worst-case scenario (resistance changes at the rate of ±30%), the integrator DC-gain was 86 dB and the error was 10 dB. Hence, the rate of change of the DC gain was small.

## IV. MEASUREMENT RESULTS

Fig. 10 displays a microphotograph of the proposed CTDSM, which was fabricated using a standard 0.18 $\mu$m CMOS process. The proposed CTDSM consumed 20.3 $\mu$W with a supply voltage of 1.8 V. The first integrator consumed 58% of this total power, dominating the total power consumption.

Fig. 11 shows the measured SN(D)R of five samples. The performance differences between the best and the worst samples are 1.3 dB for SNR and 1.2 dB for SNDR.

Fig. 12 presents the measurement results of the designed CTDSM. The measured SNR and SNDR for different amplitudes of the input signal are displayed in Fig. 12(a). With an input signal amplitude of −3.8 dB, a peak SNR of 99.1 dB and a peak SNDR of 98.8 dB are achieved. Consequently, Fig. 12(a) displays the measured DR of 103.1 dB for the proposed CTDSM at a signal bandwidth of 200 Hz. Fig. 12(b) displays a 524 k-point Fast Fourier Transform (FFT) spectrum of the proposed CTDSM's output,

**TABLE 1. Comparison of the low-bandwidth delta-sigma modulators.**

| Parameter | [20]ASSC'19 | [21]JSSC'21 | [22]VLSI'18 | [23]JSSC'19 | [2]TCASI'22 | [24]VLSI'19 | [12]TCASII'22 | This work |
|---|---|---|---|---|---|---|---|---|
| Structure | A-RC | VCO | $G_m$-C | $G_m$-C | SC | $G_m$-C | A-RC+$G_m$-C | SR+A-RC |
| Topology | 3rd order CTDSM | VCO-based with DPCM | 3rd order CTDSM | 2nd order CTDSM | 3rd order DTDSM | 1st order CTDSM | 3rd order CTDSM | 3rd order CTDSM |
| Process | 65-nm | 65-nm | 0.18-$\mu$m | 0.18-$\mu$m | 90-nm | 0.18-$\mu$m | 0.18-$\mu$m | 0.18-$\mu$m |
| Area (mm$^2$) | 0.23 | 0.08 | 1.1 | 0.69 | 0.39 | 0.14 | 0.29 | 1.31 |
| Supply voltage (V) | 1 | 1.2 | 0.6 | 1.8 | 1.2 | 0.3 | 1.8 | 1.8 |
| BW (Hz) | 150 | 500 | 300 | 250 | 250 | 62 | 250 | 200 |
| $F_S$ (kHz) | 38.4 | 32 | 12.8 | 640 | 250 | *2.64 | 64 | 102.4 |
| Power ($\mu$W) | 5.4 | 3.2 | 6.5 | 23.04 | 30 | 0.037 | 2.16 | 20.3 |
| SNR/SNDR (dB) | -/84.2 | -/89.2 | -/84.3 | -/78 | 93/91 | 54.7/53.3 | 80.1/78.4 | 99.1/98.8 |
| DR (dB) | 99.3 | 94.2 | 92.3 | 90 | 95.6 | 53.8 | 81.4 | 103.1 |
| **FoM (dB) | 158.6 | 171.2 | 160.9 | 148.4 | 160.2 | 145.5 | 159.0 | 168.7 |

* Center frequency of asynchronous DSM
**FoM = SNDR+10log(BW/Power)

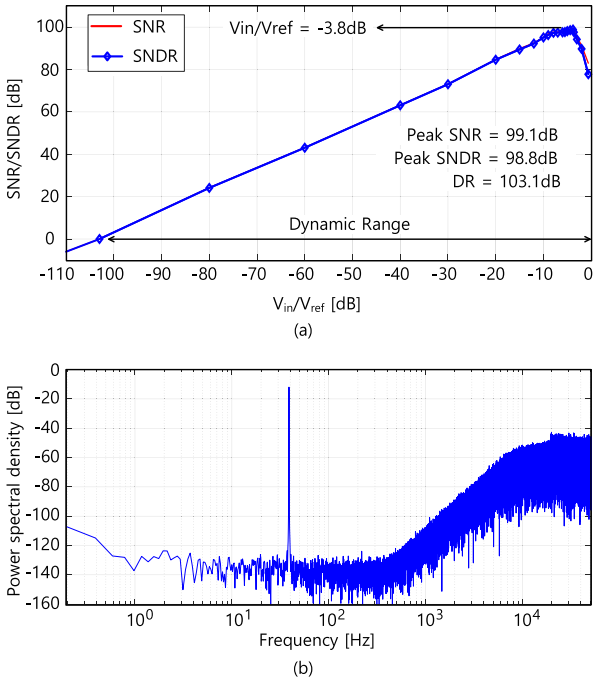


**FIGURE 12. Measured (a) dynamic range and (b) output spectrum.**

where the peak SNDR of 98.8 dB was achieved at a −3.8 dB sinusoidal input amplitude.

Table 1 presents a performance comparison of the proposed CTDSM with other signal bandwidth DSMs. Here, FoM was used to evaluate the performance of all the DSMs [19]. As shown in Table 1, the CTDSMs with a low-signal bandwidth that are suitable for sensor applications used $G_m$-C or A-RC integrators. These low-bandwidth integrators suffer from linearity limitations, large RC values and noise issues. This is why they exhibit lower performances (FoM, DR, SNR, and SNR) compared to DSMs for audio-band applications. Therefore, we proposed a CTDSM whose first integrator is implemented by an SR integrator with a chopped negative-R, which solved the issues of thermal noise and flicker noise.

Nonetheless, the chip area still remains larger in comparison to other similar works. Unlike these comparative studies, our target DR exceeds 100 dB. Therefore, we require capacitors on the order of tens of pF and resistors with values in the several MΩ range. The measured results indicate that the proposed CTDSM achieved higher DR and SNR/SNDR values than those reported in the referenced papers. Notably, it also achieved the highest DR, as shown in Table. 1.

## V. CONCLUSION

A single-bit third-order CTDSM was presented with a low power of 20.3 $\mu$W for low-bandwidth applications. Moreover, the proposed CTDSM achieved effective noise suppression and high linearity for several hundred Hz of signal bandwidth. The proposed SR integrator overcame the limitations of resistor and capacitor area that occur due to the sampling frequency of several hundred kHz. It also suppressed flicker noise without degrading linearity due to chopping operation using dead-time. The measurement results indicated an SNR of 99.1 dB, an SNDR of 98.8 dB, and a DR of 103.1 dB for a 200 Hz signal bandwidth. The proposed CTDSM also had the highest DR, SNR, and SNDR performance among hundreds of Hz signal bandwidth ADCs. Finally, the proposed CTDSM is expected to be applied in various ways in high-resolution, low-power low-bandwidth applications.

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