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RESEARCH ARTICLE

Common-Mode Voltage Mitigation for Dual Three-Phase Three-Level ANPC Inverters Using Dynamic Phase-Shift PWM

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ABSTRACT In this study, a common-mode voltage (CMV) reduction scheme based on carrier-based pulse-width modulation (PWM) is proposed for asymmetric dual three-phase hybrid active neutral-point-clamped (ADTP-HANPC) inverters. The fundamental concept is that the alignment sequence of multi-level gating signals is adjusted to produce zero CMV or ones with equal magnitude and opposite polarities in the two individual loads. To achieve this objective, dynamic phase-shift PWM (DPSPWM) is implemented between the switches of the DTP-HANPC inverter. The DPSPWM outperforms existing CMV elimination methods in terms of efficiency, with a 20 % improvement. This is primarily owing to the lower number of switching transitions. Furthermore, the current and voltage THDs are reduced compared with the existing zero CMV space vector PWM (SVPWM). The effectiveness of the proposed method has been validated through simulations and experiments. These demonstrated a significant reduction ($\geq$ 75.9 %) in maximum CMV peaks.

INDEX TERMS Common-mode voltage (CMV), dual three-phase (DTP), hybrid active neutral point clamped (HANPC), pulse-width modulation (PWM).

I. INTRODUCTION

Over the past few decades, multiphase (MP) drive systems have been proposed as effective alternatives to their three-phase counterparts. The use of these systems is imminent in applications that require robust power and torque sharing capabilities. Another significant characteristic of these drives is their capability to withstand faults. Consequently, a wide range of applications including naval propulsion systems, more electric aircraft (MEA) technologies, and military traction applications are increasingly adopting MP drive systems to fulfill their requirements [1], [2], [3], [4].

The dual three-phase (DTP) configuration, specifically the asymmetric DTP (ADTP) with a 30° phase shift, is the most extensively studied MP structure. Its similarity to conventional three-phase systems combined with the additional advantages of MP drives has made it a subject of continued research [5].

Multi-level (ML) inverters (rather than two-level topologies) have been demonstrated to be a better solution for high-power, medium-voltage applications. The multi-level multi-phase (MLMP) drives can reduce the voltage stress and ratings of switches, and provide additional paths that impart fault endurance to the system [3], [6]. In [7], a highly robust and fault-tolerant system for electric aircrafts, utilizing three-level neutral-point-clamped (NPC) inverters with MP generators was introduced.

Active neutral-point-clamped (ANPC) inverters provide more advantages than NPC inverters. These include a larger number of redundant switching states for fault-tolerance and a uniform distribution of thermal stress across the entire inverter. However, these advantages come at the cost of a larger number of switches than NPC inverters [7], [8]. When used in MP drives, the ANPC inverter causes an increased total loss.

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Advancements in wide-bandgap (WBG) devices have provided solutions to this problem [9]. A hybrid ANPC (HANPC) structure was developed earlier. Herein, silicon carbide (SiC) MOSFETs and Si IGBT were used to reduce the inverter losses [8], [9], [10], [11], [12].

When evaluating DTP structures, two critical aspects to consider are the cost and operational losses. As the number of phases increases, these factors tend to increase. Therefore, the advantages of HANPC inverters such as enhanced efficiency, cost-effectiveness, and increased fault-tolerant capability make them highly suitable for DTP inverters.

However, the discrete characteristic of all advanced inverters results in an undesirable voltage potential between the load-neutral point and neutral point of the inverter. It is known as common-mode voltage (CMV). Pulse variations in voltage (dv/dt) cause a common-mode current (CMC). It is a significant factor that causes issues such as the deterioration of motor bearings and degradation of stator winding insulation. These effects shorten the motor lifetime. Higher switching frequencies for inverters using WBG devices yield higher CMV peaks. Thus, the effect of the CMV is more significant [13], [14], [15].

Several CMV mitigation methods have been implemented to overcome these challenges. Among the solutions presented, only software-based methods are discussed in this study. Solutions pertaining to the modification of PWM can be categorized as SVPWM or carrier-based one. SVPWM determines the appropriate voltage vectors that either reduce or eliminate the CMV.

In general, carrier-based CMV suppression methods offer significant advantages compared to SVPWM suppression methods, as referenced in [13], [14], [15], and [16]. These advantages include straightforward scalability to a higher number of levels, lower offline and online complexity, and a potential decrease in real-time execution speed. Carrier-based PWM remains unaffected by the number of phases, enabling its extension to multiphase systems without complexities [13], [14], [16].

Modified SVPWM methods adopt vector state decomposition (VSD) to obtain MP vectors. In [17], VSD was applied to a three-level five-phase NPC inverter to eliminate the CMV by exclusively using vectors that produce zero CMV. Similarly, the utilization of virtual voltage vectors for CMV mitigation has been recommended [18]. However, this method is limited to an odd number of phases and cannot be applied to ML inverters. Other switching combinations for CMV reduction have also been recommended [19].

A general algorithm that can be applied to any MLMP drive based on an understanding of multidimensional conversions was proposed in [20]. Transformation matrices are required to convert voltage references into gating signals that can eliminate the CMV. In general, SVPWM methods become more complex as the numbers of levels and phases increase.

Carrier-based techniques have been studied extensively. Phase-shift PWM has been utilized on many occasions to eliminate or reduce the CMV. A phase shift of 180° between the two inverters (180°) was recommended for CMV elimination and reduction [21], [22], [23], [24]. For a symmetric DTP, opposite carriers or a 180° phase shift between the two inverters can straightforwardly produce an opposite CMV in both the loads. The effects of phase shift are compared in [23] and [24]. The use of two opposite sawtooth carriers for both the inverters to reduce the CMV in symmetrical DTP inverters was recommended in [25].

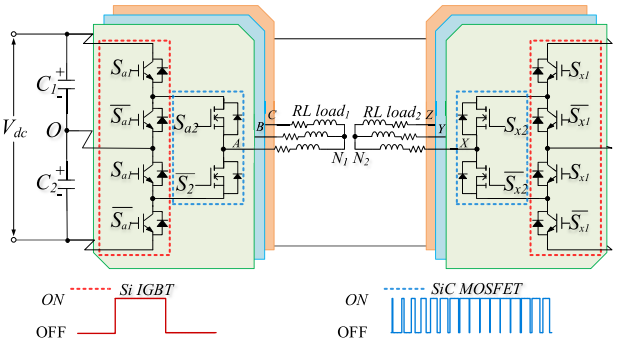

FIGURE 1. Dual three-phase hybrid ANPC inverter.

TABLE 1. Switching states for HANPC.

Switching state	S_{a1}	S_{a2}	*Phase voltage* (V_{AO})
P	ON	ON	$+V_{dc}/2$
O^+	ON	OFF	0
O^-	OFF	ON	0
N	OFF	OFF	$-V_{dc}/2$

The aforementioned carrier-based methods were applied to two-level inverters. However, these can be extended conveniently to MLMP typologies [13], [14]. A generalized CMV elimination method for all MLMP configurations was introduced in [26]. The core concept focuses on employing switching functions and a virtual voltage-source inverter (VSI) to determine all the feasible switching states. This method relies on calculations contingent on whether the inverter levels are even or odd. However, this method does not consider the variation in the switching frequencies between switches as in the case of HANPC inverters. Separate switching functions should be considered in the hybrid topologies.

End-to-end alignment in a two-level configuration was utilized for CMV cancellation of ADTP inverters [27], [28], [29], [30]. The rising and falling edges of the inverter switches are aligned such that all the CMV components add up to zero. This could be achieved by using phase-shifted sawtooth carriers.

This study introduces a novel technique called as dynamic phase-shift PWM (DPSPWM). It is an extension of end-to-end alignment for three-level HANPC inverters. The proposed method involves the generation of a variable-phase carrier wave for each switch following the criteria for cancelling the CMV. Simulation and experimental results are provided to demonstrate the effectiveness of the proposed technique. As a carrier-based technique, DPSPWM provides

advantages such as lower voltage and current THDs and reduced switching losses.

II. DYNAMIC PHASE-SHIFT FOR HANPC INVERTERS

A. DTP HANPC INVERTERS

The extension of a typical three-phase structure to any multiphase configuration offers similar attributes and characteristics [20], [26]. This is also applicable to HANPC inverters. DTP HANPC inverters inherit the advantages of HANPC such as efficiency, equal thermal distribution, lower cost, and fault tolerance. A simplified topology of the DTP HANPC inverter is illustrated in Fig. 1. In this structure, the conventional ANPC inverter is modified by employing two types of switches: Si IGBTs and SiC MOSFETs. The inverters are connected to two three-phase loads (denoted as ABC and XYZ). These have separate neutrals (N_1 and N_2, respectively). The switching states and pole voltages are listed in Table 1.

In conventional carrier-based PWM techniques, Si IGBT devices operate at the fundamental frequency. That is, the IGBT switches are turned on or off with the zero crossing of the reference wave, as shown in Fig. 1. In contrast, SiC MOSFETs operate at switching frequency based on the carrier signal reference [9].

The sinusoidal reference signal for the HANPC inverter can be expressed as

$$V_i = m \cdot \cos(\omega t + \theta^\circ) \tag{1}$$

where V_i, m, and θ are the phase-voltage references for the modulation, modulation index, and phase angle for a particular phase, i, respectively. The modified reference signal, D_i, is given by

$$D_i = V_i + 1. \tag{2}$$

Equation (2) can be normalized and modified further into a piecewise reference (V_{refi}) (varying from zero to one) for phase i as follows:

$$V_{refi} = \begin{cases} D_i - 1: & D_i \geq 1 \\ D_i: & D_i < 1. \end{cases} \tag{3}$$

The switching states of the Si IGBTs (S_{a1} and $\overline{S_{a1}}$) operating at the fundamental frequency are given by

$$S_{i1} = \begin{cases} 1: & D_i \geq 1 \\ 0: & D_i < 1. \end{cases} \tag{4}$$

Those of SiC MOSFETs (S_{a2} and $\overline{S_{a2}}$) with a switching frequency are expressed as

$$S_{i2} = \begin{cases} 1: & V_{refi} \geq \textit{dynamic carrier} \\ 0: & V_{refi} < \textit{dynamic carrier}. \end{cases} \tag{5}$$

Dynamic carrier is a variable high-frequency triangular wave adapted for gating signal alignment.

TABLE 2. Switching States for HANPC inverter.

CMV	*Voltage vectors*
$+V_{dc}/2$	[PPP]
$-V_{dc}/2$	[NNN]
$+V_{dc}/3$	[POP][OPP][PPO]
$-V_{dc}/3$	[NON][NNO][ONN]
$+V_{dc}/6$	[OOP][OPO][POO][PNP][NPP][PPN]
$-V_{dc}/6$	[ONO][NOO][OON][NNP][NPN][PNN]
0	[OOO][PNO][ONP][NOP][NPO][OPN][PON]

B. ANALYSIS OF DPSPWM FOR HANPC INVERTERS

In a three-phase system, the CMV is defined as the voltage difference between the load-neutral point (N_1 or N_2) and DC-link neutral point (O). This is shown in Fig. 1. In the case of DTP inverters with separate load neutrals, the CMV is specified as the average of the two individual voltages.

The switching vectors and the corresponding CMVs for an individual three-phase structure are listed in Table 2. SVPWM techniques can reduce or mitigate the CMV by selecting appropriate voltage vectors. In carrier-based techniques, it is crucial that both the inverters produce opposite CMV polarities for effective CMV cancellation.

The CMV for dual three-phase inverters with separate neutrals can be extended from conventional three-phase equations [13], [14]:

$$\begin{cases} CMV_{abc} = (V_{AN1} + V_{BN1} + V_{CN1})/3 \\ CMV_{xyz} = (V_{XN1} + V_{YN1} + V_{ZN1})/3 \end{cases} \tag{6}$$

The total CMV, CMV_{total}, is the average of CMV_{abc} and CMV_{xy} in (6). It is expressed as follows:

$$CMV_{total} = (CMV_{abc} + CMV_{xyz})/2. \tag{7}$$

This signifies that the CMV can be eliminated under the following conditions:

$$\begin{aligned} CMV_{abc} &= CMV_{xyz} = 0 \; or \\ CMV_{abc} &= -CMV_{xyz}. \end{aligned} \tag{8}$$

The fundamental requirement for gating signal shifting and alignment is that the sum of all the reference voltages should be zero. This can be expressed as

$$\begin{aligned} \sum_{i=a,b,c} V_i + V_{ZS1} &= 0 \text{ and} \\ \sum_{i=x,y,z} V_i + V_{ZS2} &= 0. \end{aligned} \tag{9}$$

It is highlighted in (9) that both V_{ZS1} and V_{ZS2} (injected zero-sequence voltage offsets) should be zero to achieve DPSPWM. This limits the utilization of all third-order harmonic offset injections.

HANPC inverters provide three distinct pole voltages as listed in Table 1. For the positive pole voltage of $+V_{dc}/2$, the duty cycles of S_1 and S_2 are denoted as "positive voltage ON time." Conversely, for the negative pole voltage of $-V_{dc}/2$, these are referred to as "negative voltage

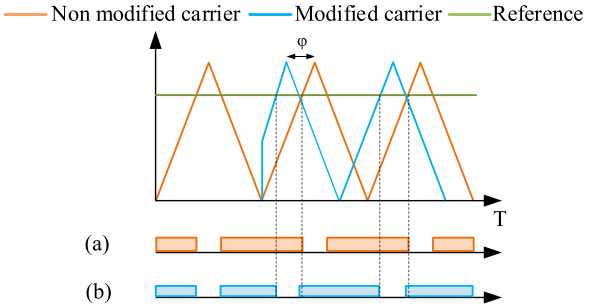

FIGURE 2. Effect of phase shift on turn-on and turn-off characteristics of S_x. (a) Conventional LS-PWM. (b) DPSPWM with phase shift (φ).

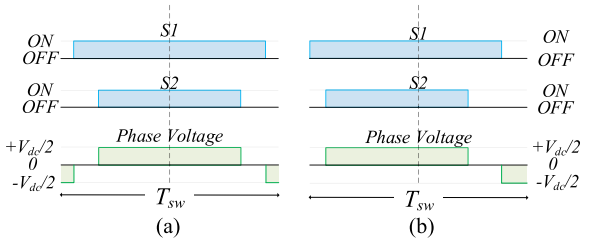

FIGURE 3. Gating signal and pole voltage. (a) Symmetric LS-PWM. (b) Asymmetric DPSPWM.

ON time." DPSPWM utilizes these voltage-magnitude durations rather than single-switch duty cycles. The significance of this approach is emphasized further in Section III.

III. PROPOSED DYNAMIC PHASE-SHIFT FOR COMMON-MODE VOLTAGE MITIGATION

A. NOVEL DYNAMIC PHASE-SHIFT FOR DTP HANPC INVERTERS

The dynamic carrier enables the adjustment of switch turn-on and turn-off timings. Fig. 2(a) and (b) show the gating signals for level-shift PWM (LS-PWM) and DPSPWM, respectively. In Fig. 2(b), it is evident that the change in the phase shift of the carrier signal results in asymmetric duty cycles for the switches (S_x). This individual effect on the switches can be combined in the form of a phase response to the carrier shift, as shown in Fig. 3.In conventional LS-PWM, as shown in Fig. 3(a), the triangular carrier waves can be considered as without phase shift or 0° phase shift. Consequently, the switching signals denoted by S_1 and S_2 are aligned at the center, adhering to conventional alignment principles. This alignment is mirrored in the phase voltage, evident from the symmetrical distribution along the dashed centerline in Fig. 3(a).

Modifying the phase shift of the carrier wave produces asymmetric turn-on times, as shown in Fig. 3(b). It can be noticed that the turn-on and turn-off times of the switches have changed with the carrier wave. In this specific case, a negative phase shift is implemented to advance the turn-on time of S_1 and S_2 within the switching period. The change in switching instants produces modified pole voltage waveforms, which are asymmetrical in the case of DPSPWM.

Similarly, dynamic phase shifting enables the alteration of all the six-phase voltages. Accordingly, the duty cycle of each switch should be considered for shifting. However, for an improved implementation, it is more effective to consider the shifting of the phase voltages rather than the duty cycles of individual switches.

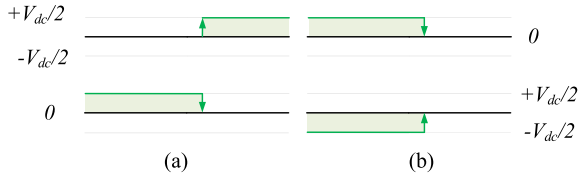

FIGURE 4. Voltage edge alignment. (a) Both positive. (b) Positive and negative.

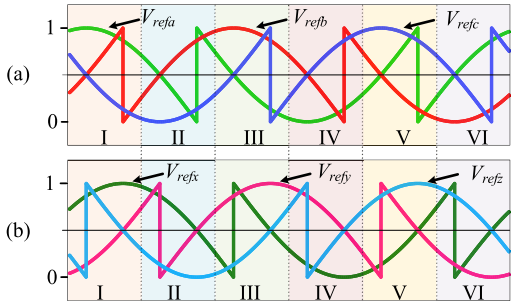

FIGURE 5. Reference voltages and region selection. (a) Phase ABC. (b) Phase XYZ.

Fig. 4 illustrates the concept of aligning the pole voltages. Fig. 4(a) shows the rising and falling edges of two arbitrary pole voltages, both of which are $+V_{dc}/2$. Fig. 4(b) shows the alignment property of the proposed PWM when one of these has a voltage magnitude of $-V_{dc}/2$. This approach helps combine the effects of all the single-phase switches although these are considered to have different duty cycles.

For CMV mitigation, the precursor uses switching combinations that yield opposite polarities of CMV values for each load. This is achieved by dynamically shifting the phase voltages in each switching cycle to align these in a specific manner.

B. DETERMINATION OF REGION

Fig. 5 illustrates the division of the fundamental period into six distinct regions with a specific alignment order. In the proposed scheme, the instantaneous highest or lowest references, V_{refi}, are used for an effective region assessment process. Equation (2) determines the phase voltage polarity $+V_{dc}/2$ or $-V_{dc}/2$, whereas (3) determines the positive or negative voltage on time for each phase. In each region, the selection process involves the use of two voltage references (V_{refi}). Considering region I as an example, both V_{refa} and V_{refx} with positive polarities ($+V_{dc}/2$) and the highest positive voltage over time are selected. Conversely, in region II, V_{refc} and V_{refz} exhibit negative polarities ($-V_{dc}/2$) and the highest negative voltages on time. As shown in Fig. 5, the fundamental period is divided into odd regions (where $+V_{dc}/2$ references are used) and even regions (where the selections are based on $-V_{dc}/2$). These assessments can effectively reduce the number of possibilities for switching sequences.

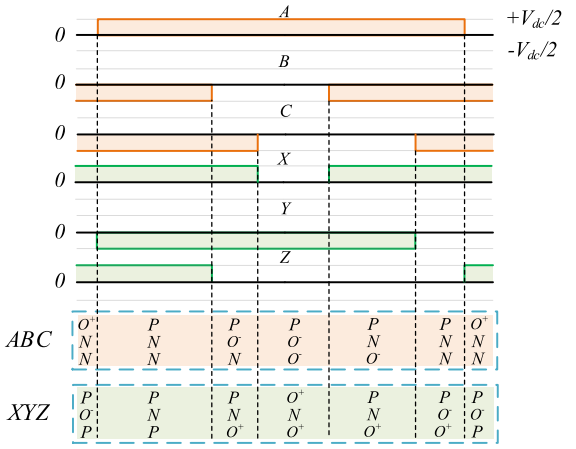

FIGURE 6. Switching state representation for fully-aligned phase voltages (with DPSPWM).

This will be explained in the following subsections. The region selection can be altered in numerous ways, the selection of the opposite polarity of V_{refi}. However, for achieving the optimal voltage and current THDs, it is recommended to adhere to the proposed region configuration.

C. DETERMINATION OF SWITCHING SEQUENCES

The determination of the switching sequences can be simplified by selecting the highest phase voltage as a reference. For this particular reference phase, maintaining the phase shift stationary or providing it with a constant shift would simplify the proposed method. As explained earlier, in odd sectors, the highest positive voltage on time is selected. This is because the on time for $+V_{dc}/2$ is longer than that for $-V_{dc}/2$, whereas the converse is true in even sectors.

Fig. 6 shows an example of a switching period in region I. In this case, the phase-A voltage exhibits the highest positive time, thereby making it the initial reference. Notably, phase A remains center-aligned throughout this duration.

Two methods of selecting sequences can be adopted: intra- and inter-load approaches [29]. Intra-load addresses the alignment of both the phases separately. For example, phase A is aligned with phase B, after which phase B is aligned with phase C. Similarly, for the other three phases, phase X is aligned with phase Y, and phase Y is aligned with phase Z. The final sequence becomes A→B→C→X→Y→Z. In contrast, in the inter-load approach, all the six phases are considered in an alternating manner, e.g., A→Y→C→X→B→Z. In multi-level inverters, the alignment sequences yield different results. This is primarily because the timing of the negative-phase voltage peaks should also be considered, and these timings vary depending on the total number of levels in the multi-level inverters.

A shortcoming of the intra-load alignment is the excessive use of medium-voltage vectors. This is because intra-load configuration avoids the same-polarity overlapping within the three phases. Multi-level inverters tend to produce zero CMV with the appropriate use of existing space vectors.

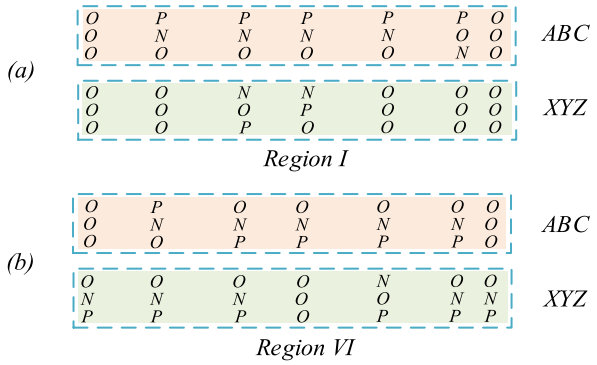

FIGURE 7. Switching state representation for fully-aligned phase voltages with DPSPWM(I) (a) Region I (b) Region VI.

TABLE 3. Switching alignments of DPSPWM.

Region	Alignment order		
	DPSPWM(1)	DPSPWM(2)	DPSPWM(3)
I	A→C→B→X→Z→Y	A→X→Z→C→B→Y	A→Z→B→X→C→Y
II	C→B→A→Z→Y→X	C→Z→X→A→B→Y	Z→B→X→C→Y→A
III	B→A→C→Y→X→Z	B→Y→X→A→C→Z	B→X→C→Y→A→Z
IV	A→C→B→X→Z→Y	A→X→Z→C→B→Y	X→C→Y→A→Z→B
V	C→B→A→Z→Y→X	C→Z→Y→B→A→X	C→Y→A→Z→B→X
VI	B→A→C→Y→X→Z	B→Y→X→A→C→Z	Y→A→Z→B→X→C

Thus, DPSPWM naturally produces zero CMV in three phases when applied in an intra-load manner. This characteristic of DPSPWM results in a higher THDs for voltage and current.

Another factor that contributes to the alignment order is the varying polarity of the phase voltages $+V_{dc}/2$ and $-V_{dc}/2$. In addition to the reference phase, the other five phases alter the voltage polarity in each region. As shown in Fig. 5, each region exhibits two polarity transitions. These transitions should be considered while selecting an appropriate alignment order and switching state.

The difference between the SVPWM and proposed method is shown in Fig. 6. Unlike conventional SVPWM, DPSPWM is directed by asymmetric gating signals. Consequently, unequal divisions can be observed. Fig. 6 shows that the use of the inter-load configuration provides a wider range of switching vectors, as opposed to only medium-voltage vectors.

In Fig. 6, the phase-alignment transitions are shown in the following order: A→Z→B→X→C→Y. As mentioned earlier, the alignment begins with the reference phase (phase A), which is center-aligned without phase shift. During this specific switching period, the phases A, X, and Z exhibit positive phase voltages, whereas the remaining phases have negative polarities. The phases ABC produce a CMV opposite to that for the phases XYZ. The vector [O^+NN] produces a CMV of $-V_{dc}/3$. To counteract this effect, $+V_{dc}/3$ is applied by the other three-phase inverter, [PO^-P]. The constraints imposed to ensure cancellation of the CMV significantly constrain the available options for switching combinations. This limits the number of feasible alignment combinations.

TABLE 4. Parameters for simulation.

Rated power	1 MW
V_{dc}	3 kV
IGBT switching frequency	50 Hz
SiC switching frequency (f_{sw})	40 kHz
Load resistance	6.1 Ω
Load inductance	6 mH
DC-link capacitance	2000 μF
IGBT	DIM400GCM33
SiC MOSFET	CAS310M17BM3

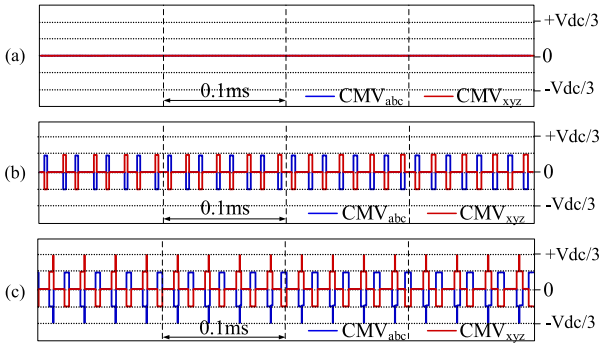

FIGURE 8. CMV_{abc} and CMV_{xyz} under different DPSPWM alignments. (a) DPSPWM(1). (b) DPSPWM(2). (c) DPSPWM(3).

Three combinations of the DPSPWM alignments are introduced. These are listed in Table 3. DPSPWM(1) demonstrates intra-load alignment. Fig. 7(a) and (b) illustrate the switching state representation in regions I and VI for DPSPWM (1), highlighting the extensive utilization of zero and medium voltage vectors. As a result, the individual CMVs are reduced to zero. DPSPWM (2) considers reducing the individual CMVs to $V_{dc}/6$, and DPSPWM (3) maintains $V_{dc}/3$ in the individual loads. The combined CMV for all the proposed switching alignments is zero. However, the voltage and current THDs are deteriorated depending on the alignment order.

IV. SIMULATION RESULTS

A. ANALYSIS FOR DPSPWM

To verify the proposed PWM scheme, simulations have been conducted in PLECS using the parameters listed in Table 4. These parameters were selected to align with existing high-power MLMP applications [7]. Fig. 8 shows the instantaneous values of the individual CMVs, CMV_{abc} and CMV_{xyz}. DPSPWM (1), (2), and (3) are shown in Fig. 8(a), (b), and (c), respectively. All the DPSPWM alignments produce opposite CMVs for both the loads. DPSPWM (1) considers intra-load alignment. Thus, the individual CMVs are zero. Both DPSPWM (2) and (3) use inter-load alignment. However, the alignment of DPSPWM (2) produces an individual maximum CMV of $+V_{dc}/6$. DPSPWM (3) produces the lowest voltage and current THDs while maintaining a combined CMV of zero. Therefore, DPSPWM (3), referred to as DPSPWM, is used for further elaboration.

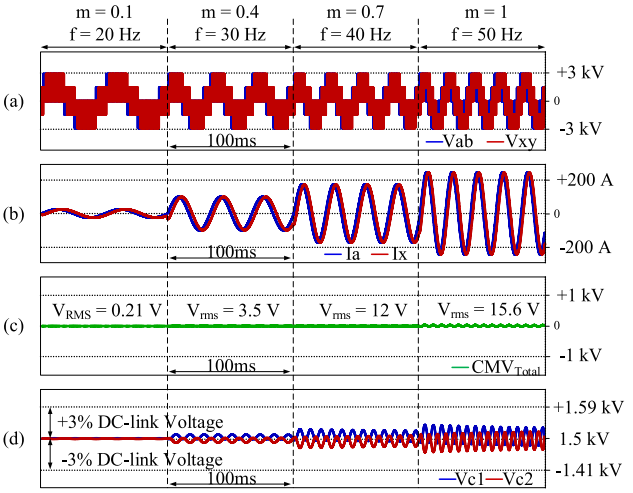

FIGURE 9. Operation of variable voltage and variable frequency. (a) Output voltages (line-to-line). (b) Phase currents. (c) CMV_{rms}. (d) DC-link capacitor voltages.

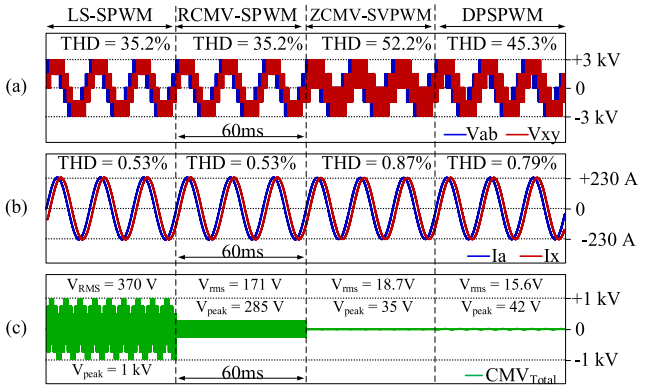

FIGURE 10. DTP PWM methods at m = 1. (a) Output voltages (line-to-line). (b) Phase currents. (c) CMV_{total}.

Fig. 9 shows the waveforms associated with the dynamic behavior of the proposed modulation scheme. Different modulation indices (m = 0.2, 0.4, 0.7, and 1) are tested at different fundamental frequencies (f = 20, 30, 40, and 50 Hz). The output voltages and phase currents of both the inverters are shown in Fig. 9(a) and (b), respectively.

Fig. 9(c) shows the capability of DPSPWM to achieve a negligible CMV. The marginal CMV_{total} values are caused by fluctuations in the neutral-point voltage. Fig. 9(d) illustrates the voltages of the DC-link capacitors. Herein, both V_{c1} and V_{c2} remain balanced and within the permissible limits for all modulation indices and frequencies.

B. COMPARISON WITH EXISTING PWM METHODS

Existing methodologies for CMV mitigation in ANPC inverters are mostly limited to SVPWM. In addition to the higher switching losses, most of these methods are limited to regular ANPC inverters. Hence, special consideration should be given to making these methods uniform with a HANPC topology [31], [32]. The adapted modulation methods analyzed in this study are as follows:

1) LS-SPWM: Level-shift SPWM (no CMV reduction)

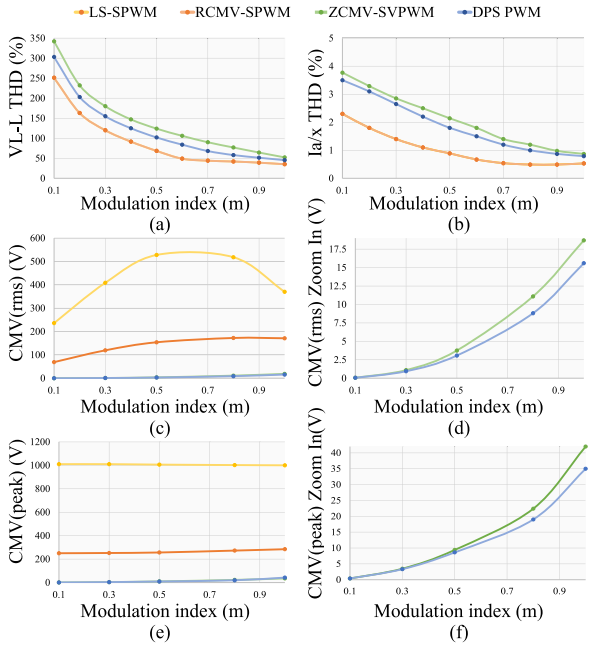

FIGURE 11. Metrics for DTP PWM methods at different modulation indices. (a) Voltage THD. (b) Current THD. (c) CMV_{rms}. (d) Zoomed-in CMV_{rms}. (e) Max CMV peak. (f) Zoomed- in max CMV peak.

2) RCMV-SPWM: Reduced CMV SPWM (180° phase shift) [20], [21], [22], [23].
3) ZCMV-SVPWM: Zero-CMV SVPWM
4) DPSPWM: Dynamic phase-shift PWM (proposed).

Fig. 10 shows the performance of these methods at unity modulation index with a fundamental frequency of 50 Hz. Fig. 10(a) and (b) shows the output voltages and phase currents with comparable THD values. Fig. 10(c) shows the CMV_{total} waveform in conjunction with V_{rms} and V_{peak}. Both LS-SPWM and RCMV-SPWM provide identical distortion levels since these do not modify the intra-load dynamics of the three-phase inverters. In RCMV-SPWM, the phase shift between ABC and XYZ varies to 180°. Therefore, the line-to-line voltages and phase currents are equal to those in LS-SPWM. Consequently, these values represent the lowest feasible THDs. Both the methods yield high V_{rms} and V_{peak} values. Meanwhile, ZCMV-SVPWM and DPS-PWM provide negligible CMV rms and peak values. However, this comes at the cost of increased voltage and current THDs, as illustrated in Fig. 10(a) and (b), respectively. An assessment of DPSPWM and ZCMV-SVPWM reveals that DPSPWM provides lower THDs owing to the inter-phase alignment rather than the intra-phase approach. The negligible CMV is owing to the marginal ripples in the DC-link voltages.

Fig. 11(a) and (b) illustrate the THDs of the output voltage and phase current, respectively. The proposed method consistently exhibits a lower THD than ZCMV-SVPWM across different modulation indices. Specifically, in Fig. 11(a), a reduction of approximately 24 % in the voltage THD is observed at a modulation index of 0.8, whereas the smallest reduction of approximately 11 % is observed at a modulation index of 0.1. Similarly, Fig. 11(b) shows comparable results, with the highest reduction in the current THD of approximately 16 % at a modulation index of 0.8 and the lowest reduction of approximately 5.7 %.

TABLE 5. Parameters for experiments.

Rated power	3.3 kW
V_{dc}	300 V
IGBT switching frequency	50 Hz
SiC switching frequency(f_{sw})	40 kHz
Load resistance	20 Ω
Load inductance	6 mH
DC-link capacitance	2000 μF
IGBT	IHW50N65R5
SiC MOSFET	SCTWA50N120

Two of the key metrics used to understand the effectiveness of the proposed method are the RMS and maximum peak of the CMV. A comparison of the CMV_{rms} is illustrated in Fig. 11(c) and (d). Both LS-SPWM and RCMV-SPWM produce significantly high CMV_{rms} compared with the CMV elimination methods. The maximum peak CMV are shown in Fig. 11(e). These reveal no significant differences in the maximum peak variations. ZCMV-SVPWM and DPSPWM produce negligible CMV peaks, and comparable results are evident in Fig. 11(f).

An increasing trend of CMV is evident in Fig. 11(d) and (f), and this can be attributed to the increasing DC-Link capacitor voltage ripple. As modulation increases, there is a corresponding rise in the capacitor voltage ripple, resulting in elevated values for both the maximum CMV peak and its rms value.

The exclusive use of medium and zero vectors in ZCMV-SVPWM results in a higher neutral-point current, consequently leading to a more pronounced capacitor voltage ripple. On the contrary, DPSPWM employs small voltage vectors that incorporate both positive and negative neutral-point currents. This unique characteristic of including negative neutral-point current contributes to a reduction in the overall neutral-point current [33]. Consequently, this decrease leads to a lower voltage ripple.

An issue with SVPWM-based CMV reduction or elimination methods is the increase in switching losses. Fig. 12 shows the switching losses of the HANPC inverter with ZCMV-SVPWM and DPSPWM. All the carrier-based PWM methods result in losses similar to those for DPSPWM. This is because phase shift alone does not alter the number of switching instants within the switching period. Unlike the proposed method, ZCMV-SVPWM incurs higher losses since it employs more switching transitions within a single switching period. The reduction in losses obtained by using the proposed method consistently exceeds 20 %.

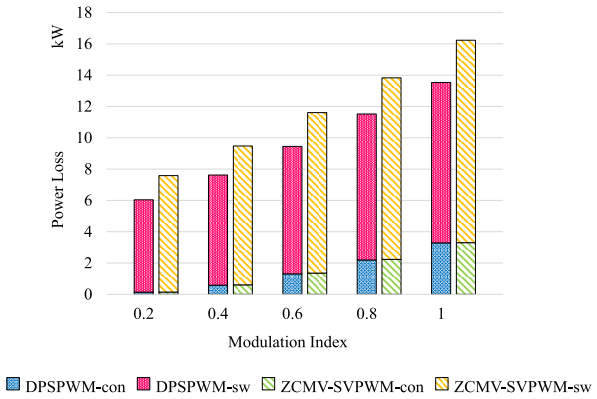

FIGURE 12. Switching losses for DTP PWM methods at different modulation indices.

V. EXPERIMENTAL VERIFICATION

A downscaled prototype of the three-level HANPC inverter was constructed in the laboratory, as shown in Fig. 13. The experimental parameters are listed in Table 5.

The algorithm for the DSP implementation is summarized in Fig. 14. The reference generation block computes the conventional HANPC inverter control references that fulfill the conditions stated in (3) - (5). The typical carrier-based control of HANPC inverters generates references for SiC MOSFET, whereas the polarity of the reference voltage determines the switching state of IGBT. These references are fed into a dynamic carrier generation block.

The dynamic carrier-generation block requires a region information as shown in Fig. 5. The switching sequences are selected based on the data in Table 3. The alignment of the gating signals requires accurate knowledge of the turn-on and turn-off timings. The timings are calculated by using the reference voltage provided by the reference generation block. Considering the initial phase shift to be center-aligned, a half of the voltage timing can be regarded as the initial falling or rising voltage position. This also depends on the polarity of the reference voltage, thereby implying that the transition can occur from $+V_{dc}/2$ to zero, $-V_{dc}/2$ to zero, or vice versa.

After the alignment of the six phase voltages, phase shift in DSP is performed by modifying the time base phase shift (TBPHS) and phase direction (PHSDIR) registers in each sampling period [34].

The sampling frequency for the experiment is 80 kHz, and the dead-time selected for both types of switches is 1 μs. The alignment of gating signals is a highly precise process. Hence, the implementation of dead time may deteriorate the CMV [27], [28]. When dead time is introduced, unique behaviors emerge since both complementary switches are in off state during transition. As shown in Fig. 1, either both S_{a1} and $\overline{S_{a1}}$ or S_{a2} and $\overline{S_{a2}}$ are in the off state. During this transition period, the current flow determines the polarity of the pole voltage. As previously established, the cumulative CMV is linked to the sum of pole voltages (6) and (7). Consequently, a sudden change in pole voltage results in a corresponding abrupt change in CMV. Any unintended increase or decrease

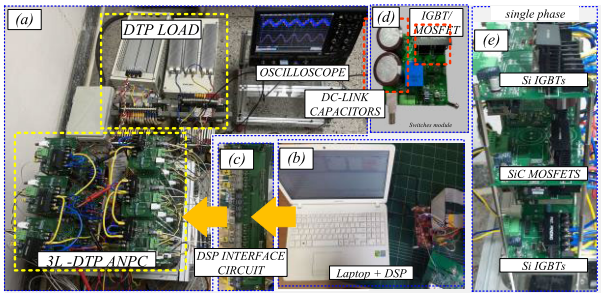

FIGURE 13. Experimental setup. (a) DTP inverter and loads. (b) Laptop and DSP controller. (c) Interface circuit. (d) Sub-module. (e) Single-phase HANPC inverter.

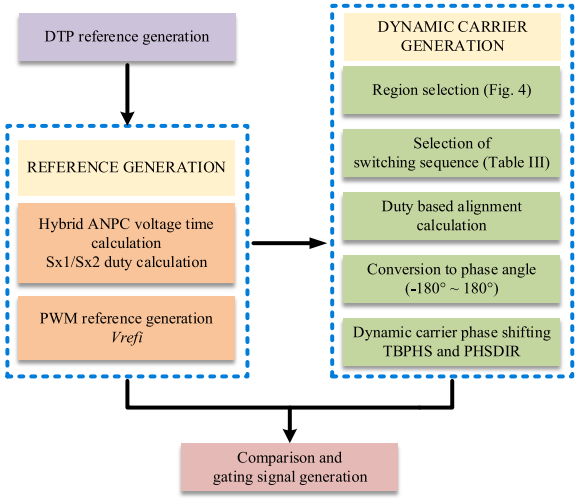

FIGURE 14. Implementation of DPSPWM in DSP.

in the magnitude of any phase voltage will consequently alter the CMV. The impact of dead time on LS-PWM is relatively minor due to the inherently high CMV, which can reach levels as high as $V_{dc}/3$. In contrast, when dead time is introduced to any zero CMV method, peaks in the CMV become noticeable. CMV consistently remains zero until deadtime occurs; therefore, CMV spikes due to deadtime effect are inevitable. To measure the individual CMVs, the load neutrals (N_1 and N_2) are connected to the neutral point of the DC-link capacitors (O) via a differential probe. The effect varies based on the phase current polarity.

Fig. 15(a) and (b) show the output voltages and phase currents at modulation indexes of 0.5 and 1. The corresponding CMV waveforms are shown in Fig. 15(c), illustrating reduced peaks well within the $V_{dc}/12$ range. These minor CMV peaks can be attributed to the switching transitions and dead-time effects.

Fig. 16(a) shows the measured CMVs. It reveals that CMV_{abc} and CMV_{xyz} are opposite or zero at any instant. DPSPWM produces individual peaks of $V_{dc}/3$. However, a combined peak with negligible magnitude is obtained. Fig. 16(b) shows the presence of transients resulting from the switching transitions and the inherent dead time of the inverter.

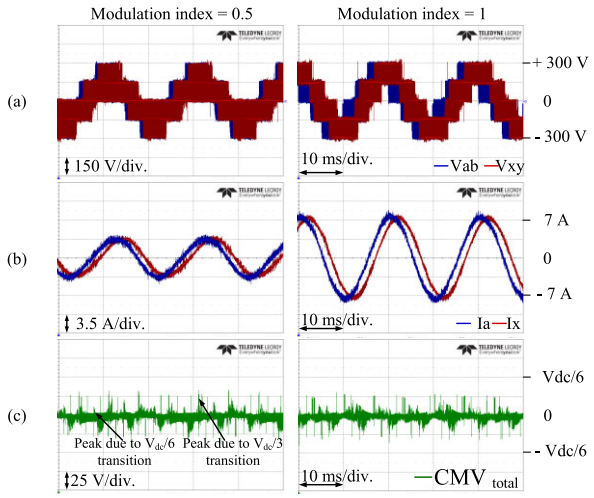

FIGURE 15. DPSPWM output at m = 0.5 and 1 at f = 50 Hz. (a) Output voltages. (b) Phase currents. (c) CMV_{total}.

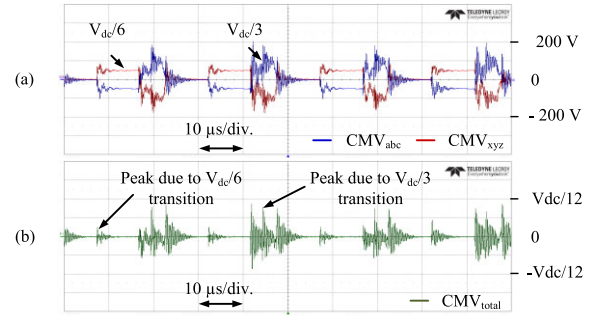

FIGURE 16. Zoomed-in CMVs. (a) Individual CMVs. (b) CMV_{total}.

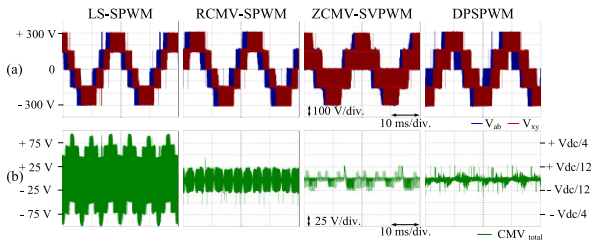

FIGURE 17. Comparison of DTP PWM methods. (a) Phase voltages. (b) CMV_{total}.

The output voltages and CMVs of the existing and proposed methods are shown in Fig. 17. Notably, the proposed method exhibits a significant reduction in both the peak and RMS of the total CMV compared with LS-SPWM and RCMV-SPWM. Similar CMV results are observed for ZCMV-SPWM and DPSPWM. However, these methods exhibit minor CMV peaks, as shown in Fig. 17(b).

The FFT analysis shown in Fig. 18 represents that LS-SPWM and RCMV-SPWM have a high switching harmonic content at multiples of 40 kHz. In contrast, with ZCMV-SVPWM and DPSPWM, the harmonic contents are almost eliminated from the total CMV waveform.

The CMV_{rms} and CMV_{peak} values are summarized in Table 6. ZCMV-SVPWM and DPSPWM provide equal CMV_{peak} and similar CMV_{rms} values.

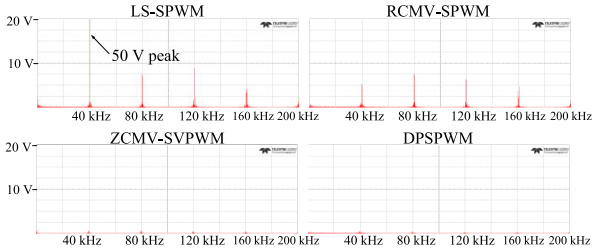

FIGURE 18. FFT analysis of CMV_{total} for different PWM methods.

TABLE 6. Evaluation of CMV metrics.

PWM Method	CMV_{rms} (V)	CMV_{peak} (V)
LS-PWM	42 (V_{dc}/7)	108
RCMV-SPWM	16 (V_{dc}/18)	45
ZCMV-SVPWM	4.9 (V_{dc}/61)	26
DPSPWM (Proposed)	4.7 (V_{dc}/64)	26

VI. CONCLUSION

In this study, a carrier-based PWM method dedicated to the ADTP HANPC inverter was proposed. Its main aim was to eliminate the CMV for asymmetric DTP loads. The region selection process, switching sequences, and alignment orders were described. Three alignment orders were discussed based on the individual CMV magnitudes. The experimental investigations demonstrated that the use of DPSPWM (compared with LS-PWM) caused significant reductions in CMV_{rms} (by 88.8 %) and CMV_{peak} (by 75.9 %). The advantages of DPSPWM compared with ZCMV-SVPWM is evident. It has achieved a 20 % reduction in switching losses, demonstrated lower voltage, and current THDs, with reductions of at least 11 % and 5.7 %, respectively.

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