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RESEARCH ARTICLE

Proportional–Resonant Controller Based on Virtual Impedance for Harmonic Suppression of ESS-UPS System

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ABSTRACT A proportional–resonant controller based on the output impedance is proposed for a single-phase full-bridge inverter offering harmonic suppression of uninterruptible power supply with an energy storage system. In order to design the voltage transfer function and output impedance independently, the proposed controller properly places a virtual impedance loop within the output voltage controller, and control gains are selected according to the proposed design rules. To secure a high power quality, the virtual impedance is designed to have low output impedance characteristics in all frequency bands. In addition, some practical issues are analyzed and readily compensated such as parametric error and the performance of output voltage tracking respectively. Mathematical and theoretical analyses are presented to validate the proposed controller, and experiments were conducted to verify its performance.

INDEX TERMS Proportional–resonant (PR) controller, virtual impedance, energy storage system (ESS), uninterruptible power supply (UPS), harmonic suppression.

I. INTRODUCTION

To ensure that renewable energy sources such as small-scale generation of photovoltaics and wind provide a stable power supply, an energy storage system (ESS) is needed to store energy for end users, and an uninterruptible power supply (UPS) system is needed to ensure that the grid has power during emergencies. A UPS system has three different operating modes: bypass, grid-connected, and islanded. During islanded operation with an ESS, a UPS system uses a single-phase full-bridge inverter that regulates the output voltage to be close to a sinusoidal wave. However, nonlinear load conditions can cause voltage perturbations due to output impedance, which results in harmonic distortion [1]. Standards such as IEEE STD 51 specify that the harmonic distortion must be less than a threshold value (<5%) under different load conditions. Thus, harmonic suppression is an important issue for power applications [2]. Conventionally, most studies have focused on solving the voltage distortion caused by nonlinear loads by designing different control structures or controller types [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23].

In [3], a control structure was proposed for capacitor voltage feedback that compensates for the voltage distortion of a grid-connected inverter. The feedback transfer function includes a derivative component, which enables active damping without the need for a sensor of the capacitor current. However, a low-pass filter (LPF) is inevitably required to ensure that the entire frequency range can be fully controlled. In addition, issues with noise amplification need to be considered for digital implementation.

Multiple resonant harmonic compensators can be added to the control loop for selective harmonic suppression [4]. However, the control structure becomes complicated as the number of compensating harmonic orders is increased. In addition, the separate control loops need to be tuned to harmonic frequencies independently and can require a band-pass filter for each, which increases the computational load and execution time [5].

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According to the internal model principle (IMP), if a closed-loop system is asymptotically stable and the controller contains a mathematical model that describes the reference input, then the system can perfectly track its reference without a steady-state error [6]. Studies on IMP-based repetitive control (RC) [7], [8] have shown that this approach has a good harmonic rejection capability against periodic error. To achieve a fast response time, odd-harmonic RC schemes [8] have been proposed to avoid redundant compensation of even harmonic frequencies. This reduces the internal model delay, increases the error convergence rate, and saves data space, though at the cost of the tracking performance of partially periodic signals [9].

Nonlinear control methods such as model predictive control and deadbeat control can secure high dynamic characteristics and reduce harmonics under nonlinear load conditions [4], [10]. However, these methods are sensitive to parametric errors and are greatly affected by the sampling frequency. In addition, high-resolution current and voltage sensors are required for multiple state variables to achieve dynamic stiffness [7].

Droop-controlled systems based on the output impedance are widely used to minimize the tradeoff between the accuracy of the output voltage regulation and the power-sharing ratio in the case of unbalanced line impedances. A virtual impedance can be used with droop control [11] to constrain the phase angle of the output impedance between $-\pi/2$ and $+\pi/2$ rad, which enables accurate distribution of active and reactive powers under different loads. Most studies on virtual impedance have focused on using parallel-connected inverters to achieve equivalent power sharing in UPS systems [11], [12], [13]. The proposed methods often control the system by using the resistance to equalize the output impedance. However, a high virtual resistance along the current path degrades the voltage regulation performance [14].

In a study on a DC microgrid system [15], a resistive–capacitive output impedance shaping method was proposed to reduce the output capacitance. This is called integral droop control [16] for hybrid ESSs or virtual inertia control [17], [18] for DC grid systems and provides a virtual output impedance to damp the system during load step changes. However, the previous studies on output impedance shaping [11], [12], [13], [14], [15], [18] mainly applied parallel operation of inverters based on droop control. Therefore, they were more focused on using the virtual impedance to match the phase angle of the output impedance within the system, which is more suitable for power-sharing and fast response functions in the case of transient events.

The scope of the present study was focused on the harmonic suppression of a single-phase full-bridge inverter in an ESS-UPS system during islanded operation. The objective was to match the magnitude rather than the phase angle of the output impedance, which causes output voltage perturbations according to the load current. A proportional–resonant (PR) controller was designed based on the output impedance for a single-phase full-bridge inverter to realize harmonic suppression under all load conditions. A virtual impedance is constructed so that the voltage transfer function and output impedance can be designed independently. Mathematical and theoretical analyses were performed to develop design guidelines with a flowchart. In addition, parametric errors and degradation of the voltage-tracking ratio were considered, and simple solutions were developed. The proposed design is more intuitive than conventional approaches and does not require including an additional filter in the control loop.

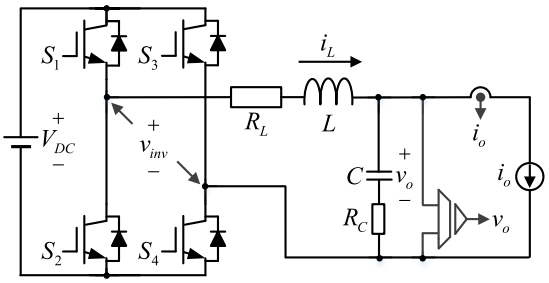


FIGURE 1. Configuration of a single-phase full-bridge inverter with an LC filter.

II. SYSTEM MODEL WITH VIRTUAL IMPEDANCE

A. SYSTEM CONFIGURATION AND BASIC TRANSFER FUNCTIONS

Fig. 1 shows a single-phase full-bridge inverter for the UPS system, where the input voltage is modeled as a voltage source provided by the ESS and the output current is modeled as a current source so that all load conditions can be considered. The parasitic inductor resistance R_{L} is included in the inductance–capacitance (LC) filter, and the output voltage, and current are sensed for feedback control. The parasitic capacitor resistance R_{C} is described in this configuration and the following system equations; however; it is excluded from the design procedure because of its negligible value.

The equivalent model of Fig. 1 is given by

$$v_o(s) = \frac{1}{LCs^2 + R_L Cs + 1} \cdot v_{inv}(s) - \frac{Ls + R_L}{LCs^2 + R_L Cs + 1} \cdot i_o(s) \quad (1)$$

The bridge output voltage v_{inv} of the inverter is assumed to follow the pulse-width modulation (PWM) reference voltage v^*_{inv}. The output voltage v_{o} comprises the output response of v_{inv} with a voltage transfer function and the voltage perturbation caused by the load current i_{o}. According to (1) and under the assumption of no i_{o}, the open-loop voltage transfer function G_{vo} is derived as follows:

$$G_{vo}(s) = \left.\frac{v_o(s)}{v_{inv}(s)}\right|_{i_o=0} = \frac{1}{LCs^2 + R_L Cs + 1} \quad (2)$$

The transfer function of the output impedance Z_{vo}, which perturbs the output voltage according to i_{o}, can similarly be derived from (1) as follows:

$$Z_{vo}(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_{inv}=0} = \frac{Ls + R_L}{LCs^2 + R_L Cs + 1} \quad (3)$$

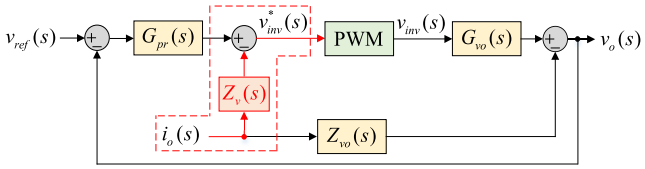


FIGURE 2. Control block diagram of the proposed closed-loop voltage feedback control comprising a PR controller and virtual impedance control loop.

B. PROPORTIONAL–RESONANT VOLTAGE CONTROLLER AND VIRTUAL IMPEDANCE LOOP

Fig. 2 shows the control block diagram of the closed-loop voltage feedback control, which comprises an open-loop voltage controller $G_{\rm vo}$, PR controller $G_{\rm pr}$, output impedance $Z_{\rm vo}$, virtual impedance $Z_{\rm v}$, and PWM block. $G_{\rm vo}$ provides the benefits of not requiring a coordinate transformation and the ability to track the sinusoidal reference with minimal error. The transfer function of $G_{\rm pr}$ can be expressed as

$$G_{pr}(s) = k_p + \frac{k_i\omega_c(s+\omega_c)}{s^2+2\omega_c s+\omega_o^2} \tag{4}$$

where ω_c is the internal bandwidth, ω_o is the fundamental frequency, k_p is the proportional gain, and k_i is the resonance gain respectively.

In this study, the virtual impedance was treated as an active damper to adjust the output impedance of the system. The virtual impedance Z_v comprises the virtual resistance R_v and virtual inductance L_v:

$$Z_v(s) = R_v + sL_v \tag{5}$$

III. PROPOSED CONTROLLER

The proposed controller allows the voltage transfer function and output impedance of a closed-loop system to be designed independently. To decouple these two components, the virtual impedance loop should be engaged with the output current feedback so that the characteristic equation is not influenced by virtual impedance parameters, while the impedance loop should be placed as an inner loop before the PWM block. As given in (1), the output voltage is perturbed by the output current in the form of the output impedance. Thus, the virtual impedance does not affect the stability of the entire system. On the other hand, the virtual impedance does affect the characteristic equation of the system and the stability in the case of inductor current feedback.

To analyze the closed-loop dynamics of the proposed system, both the voltage equation for the power stage and the control equation for the output voltage of the inverter bridge need to be derived. First, (1) is divided by the open-loop voltage transfer function $G_{vo}(s)$ and is rearranged as follows:

$$v_{inv}(s) = \frac{1}{G_{vo}(s)}\cdot v_o(s) + \frac{Z_{vo}(s)}{G_{vo}(s)}\cdot i_o(s) \tag{6}$$

In addition to the bridge output voltage v_{inv}, the control equation includes the PR voltage control and virtual impedance loops, which are derived as follows:

$$v^*_{inv}(s) = G_{pr}(s)\cdot\{v_{ref}(s) - v_o(s)\} - Z_v(s)\cdot i_o(s) \tag{7}$$

Assuming that v_{inv} and v^*_{inv} are equalized by PWM normalization, the closed-loop dynamics of the inverter system are derived as follows:

$$v_o(s) = G_{vc}(s)v_{ref}(s) - Z_{vc}(s)i_o(s) \tag{8}$$

$$\begin{aligned}
G_{vc}(s) &= \frac{b_3s^3+b_2s^2+b_1s+b_0}{a_4s^4+a_3s^3+a_2s^2+a_1s^1+a_0} \\
a_4 &= LC \\
a_3 &= 2\omega_cLC + (R_L+R_C)C + k_pR_CC \\
a_2 &= \omega_o^2LC + 1 + k_p + \omega_cR_CC(2k_p+k_i) \\
&\quad + 2\omega_cC(R_L+R_C) \\
a_1 &= \omega_o^2C(R_L+R_C) + 2\omega_c + R_CC(k_p\omega_o^2 + k_i\omega_c^2) \\
&\quad + (2k_p+k_i)\omega_c \\
a_0 &= \omega_o^2 + k_p\omega_o^2 + k_i\omega_c^2 \\
b_3 &= k_pR_CC \\
b_2 &= k_p + \omega_cR_CC(2k_p+k_i) \\
b_1 &= (2k_p+k_i)\,\omega_c + R_CC(k_p\omega_o^2 + k_i\omega_c^2) \\
b_o &= k_p\omega_o^2 + k_i\omega_c^2 \\
Z_{vc}(s) &= \frac{c_4s^4+c_3s^3+c_2s^2+c_1s+c_0}{a_4s^4+a_3s^3+a_2s^2+a_1s^1+a_0} \\
c_4 &= R_CC(L+L_v) \\
c_3 &= (L+L_v)(1+2\omega_cR_CC) + R_CC(R_L+R_V) \\
c_2 &= (L+L_v)(2\omega_c+\omega_o^2R_CC) + (R_L+R_V) \\
&\quad \times (1+2\omega_cR_CC) \\
c_1 &= (L+L_v)\omega_o^2 + (R_L+R_V)(2\omega_c+\omega_o^2R_CC) \\
c_0 &= \omega_o^2(R_L+R_V)
\end{aligned} \tag{9, 10}$$

where $G_{vc}(s)$ is the closed-loop voltage transfer function, $Z_{vc}(s)$ is the closed-loop output impedance, and v_{ref} is the reference output voltage of the inverter system.

A. DESIGN OF THE CLOSED-LOOP VOLTAGE TRANSFER FUNCTION

As given in (9), the design parameters of the closed-loop voltage transfer function $G_{vc}(s)$ include only parameters of the PR controller and power stage without the virtual impedance parameters. This implies that $G_{vc}(s)$ can be designed independently from the closed-loop output impedance $Z_{vc}(s)$.

During this design procedure, the magnitude response of the voltage transfer function should be 0 dB at ω_o while the poles of the characteristic equations are placed in left-half plane (LHP). Accordingly, the first design rule for $G_{vc}(s)$ is proposed as follows:

$$|G_{vc}(s=j\omega_o)| \approx 0\ \text{dB} = 1 \tag{11}$$

$$v_o(s) = v_{ref}(s) - Z_{vc}(s)i_o(s) \tag{12}$$

Thus, the closed-loop dynamics in (8) becomes (12) because $G_{vc}(s)$ ideally has a gain of unity at ω_o. Fig. 3 shows an example Bode diagram for $G_{vc}(s)$.

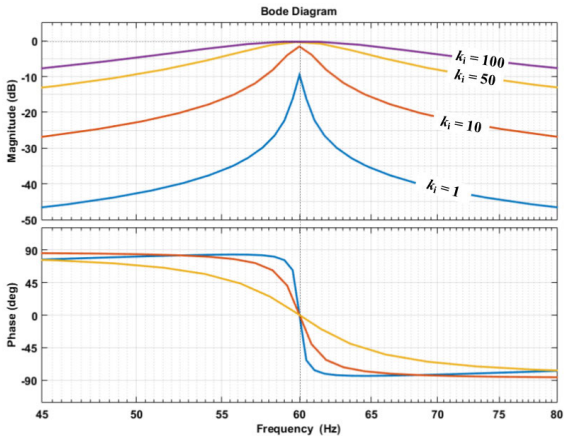


FIGURE 3. Bode diagram of the closed-loop voltage transfer function $G_{vc}(s)$ according to the variation in k_i.

The magnitude response at ω_o approaches 0 dB as k_i increases from 1 to 100 ($k_p = 0.001$ and $\omega_c = 1$) while it has a relatively low magnitude response at other frequencies. The magnitude response at ω_o can be linearly approximated as follows:

$$|G_{vc}(s = j\omega_o)| \approx \frac{1}{1 + \frac{2}{2k_p + k_i}} \tag{13}$$

(Base assumption is that $\omega_r = 1/\sqrt{LC} \gg \omega_o \gg \omega_c$)

Here, ω_r is a resonant frequency of the LC filter.

A high magnitude for the term $2k_\mathrm{p} + k_\mathrm{i}$ is required to achieve $|G_{vc}(s = j\omega_o)|$ with a magnitude close to unity. Thus, the controller gains of k_p and k_i can be selected a priori by (13). However, increasing the gains is not simple because not only the effects on the system stability but also the sensitivity to the input error need to be considered. Therefore, a stability analysis using pole-zero maps should be conducted simultaneously, as described in Section III-B.

B. STABILITY ANALYSIS OF THE PROPOSED CONTROLLER

Fig. 4 shows the pole-zero maps of the closed-loop system according to variations in the control gains k_p, k_i, and ω_c. According to (9) and (10), the four poles should comprise two complex conjugates: ω_o and close-loop system ω_r. All four poles should be placed in the LHP for the system to operate in the stable region.

Fig. 4(a) shows the pole-zero map when k_p is changed to 0, 0.1, 0.5, 1, and 2 while $k_i = 50$ and $\omega_c = 1$. For example, the poles are in the stable region at $\omega_o = -26 \pm \mathrm{j}376$ and $\omega_r = -25 \pm \mathrm{j}8170$ when $k_\mathrm{p} = 0.001$. As k_p increases, the two poles of ω_r move to the LHP (i.e., stable region) while the two poles of ω_o initially on the LHP gradually move to the right-half plane (i.e., unstable region). Fig. 4(b) shows the pole-zero map when k_i is changed from 0 to 100 while k_p and ω_c are fixed. With increasing k_i, the poles of ω_o gradually move to the stable region and the poles of ω_r move to the unstable region. Fig. 4(c) shows the pole-zero map when ω_c is increased from 0 to 2 rad/s. Similar to the case

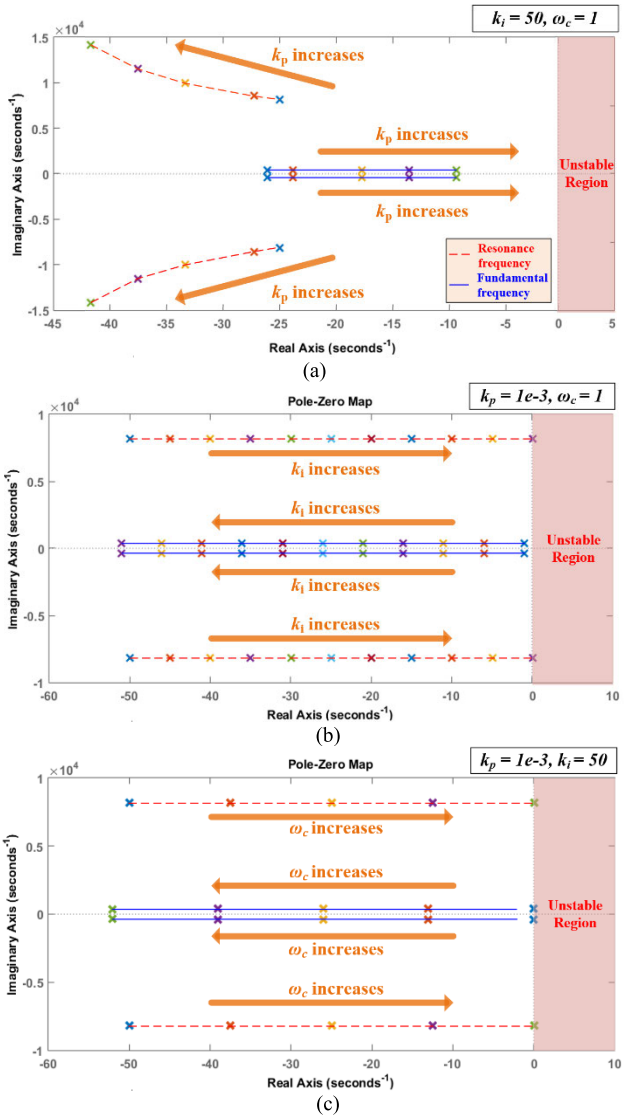


FIGURE 4. Pole-zero maps for the variations in the (a) proportional gain k_p, (b) resonance gain k_i, and (c) cutoff frequency ω_c.

of k_i, increasing ω_c has the same effect on system stability, but increasing ω_c affects the bandwidth of the magnitude response around ω_o.

Even if the gain of k_p has a low value, the poles of ω_r are already in the stable region, while the poles of ω_o are also in the stable region. Considering that the term $2k_\mathrm{p} + k_\mathrm{i}$ in (13) should be a high value, the gain of k_i should be set to a high value so that the first design rule is satisfied.

C. DESIGN OF THE CLOSED-LOOP OUTPUT IMPEDANCE

The closed-loop output impedance Z_vc(s) affects the voltage perturbation caused by the output current when the feedback loop of the control structure is considered. Therefore, if the load is assumed purely resistive, this impedance should be designed so that the magnitude is minimized at ω_o:

$$|Z_{vc}(s = j\omega_o)| \approx -\infty\,\mathrm{dB} = 0 \tag{14}$$

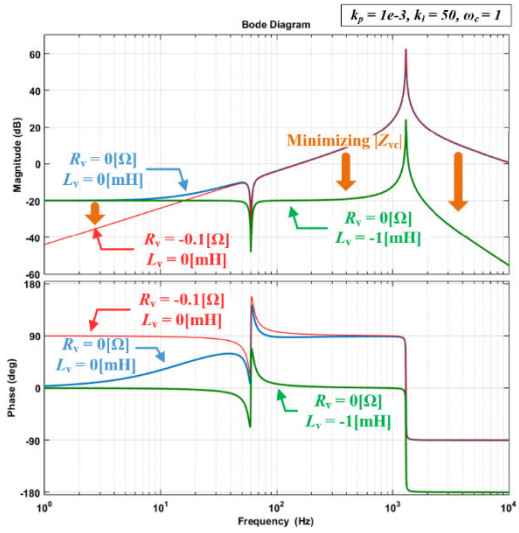


FIGURE 5. Bode diagram of Z_{VC} with the proposed closed-loop impedance design using R_V and L_V independently.

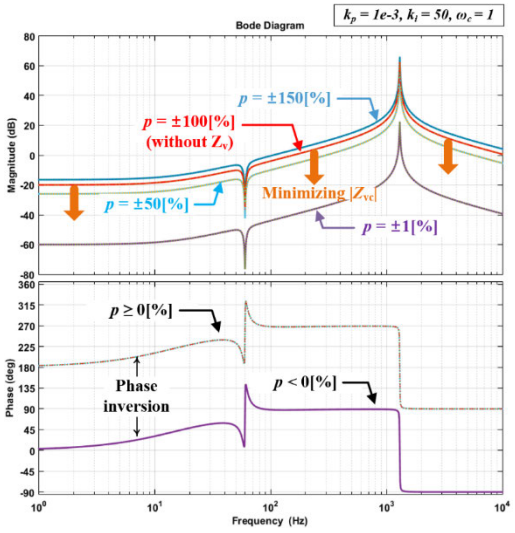


FIGURE 6. Bode diagram of Z_{VC} considering parametric errors.

Then, the closed-loop dynamics are obtained as follows:

$$v_o(s = j\omega_o) = v_{ref}(s = j\omega_o) \tag{15}$$

Considering all the load conditions for (12), the second design rule for minimizing Z_{vc} at all frequency bands is proposed as follows:

$$|Z_{vc}(s)| \approx -\infty\,\mathrm{dB} = 0 \tag{16}$$

Consequently, if the proposed controller satisfies the two design rules of (11) and (16), the output voltage ideally follows the reference voltage under all load conditions:

$$v_o(s) = v_{ref}(s) \tag{17}$$

The coefficients a_n $(n = 1, 2, 3, 4)$ in the denominator of (10) come from a characteristic equation that cannot be controlled to satisfy (16). However, the coefficients c_n $(n = 1, 2, 3, 4)$ in the numerator of (10) are affected by the virtual impedance parameters. To cancel the output impedance, the virtual impedance should be designed to satisfy (16) as

$$R_V = -R_L, \quad L_V = -L \tag{18}$$

Fig. 5 shows the Bode diagram when the proposed closed-loop impedance design is applied to the output impedance considering R_v and L_v independently. Regarding the magnitude of Z_{vc}, especially in (10), L_v should have a larger effect than R_v on the high-frequency region due to the higher-order coefficients and vice versa. The solid blue line represents Z_{vc} without the virtual impedance ($R_v = 0$, $L_v = 0$), and the solid red line represents Z_{vc} when it is purely compensated by R_V ($R_v = -0.1$, $L_v = 0$), which can be confirmed when the phase response around ω_o becomes capacitive. The magnitude response of Z_{vc} decreases in the low-frequency band because of the low-order coefficients of c_n. The solid green line represents when Z_{vc} is compensated by L_V($R_v = 0$, $L_v = -1$ mH) to be resistive. Compared to the solid red line, the magnitude response of Z_{vc} decreases in the high-frequency region because L_V minimizes the high-order coefficients of c_n.

IV. PRACTICAL CONSIDERATIONS

A. FREQUENCY RESPONSE OF THE CLOSED-LOOP OUTPUT IMPEDANCE CONSIDERING PARAMETRIC ERRORS

During practical implementation, compensating Z_{vc} completely as in (18) will be impossible because of parametric errors. Therefore, the virtual impedance including the parametric error rate p% is defined as $Z_{v,e}$, and the effect of p% on (5) can be expressed as follows:

$$Z_{v,e} = (R_v + sL_v) \times (1 + \frac{p}{100}) \tag{19}$$

By substituting (19) into (10), the closed-loop output impedance $Z_{vc,e}(s)$ is defined as

$$Z_{vc,e}(s) \approx Z_{vc}(s) - \frac{pZ_{vc,o}(s)}{100} \tag{20}$$

Here, $Z_{vc,o}(s)$ represents the closed-loop output impedance without the virtual impedance ($R_v = 0$, $L_v = 0$), which is equivalent to the solid red line in Fig. 6. Based on (16), if $Z_{vc}(s)$ converges to 0 dB in (20), the magnitude of $Z_{vc,e}$ does not exceed $Z_{vc,o}(s)$ when $p < 100\%$. This implies that the proposed method is robust against parametric errors. Fig. 6 indicates that the proposed virtual impedance can reduce $Z_{vc}(s)$ as long as $p\%$ is within 100%. The phase response can differ by 180° inversion depending on the sign of $p\%$.

B. VOLTAGE REFERENCE COMPENSATION

Because of the simplified controller characteristics according to the proposed controller design, the output voltage-tracking ratio $v_{o(RMS)}/v_{ref\,(RMS)}$ is affected by other specifications such as the stability and dynamic characteristics, so it may not reach unity so that both bandwidth and stability are sufficient. Theoretically, a high resonance gain is required for the

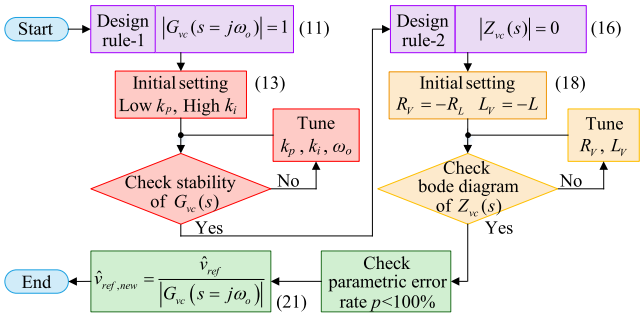


FIGURE 7. Flowchart of the design procedure.

voltage-tracking ratio to come close to 100%, but a higher resonance gain greatly affects the system stability and peak resonance. In this study, this problem was solved by simply scaling the voltage reference with a voltage compensation as follows:

$$\hat{v}_{ref,new} = \frac{\hat{v}_{ref}}{|G_{vc}(s=j\omega_o)|} \tag{21}$$

C. DESIGN PROCEDURE

Fig. 7 shows a flowchart for better visualization of the design procedure. Two design rules are established to minimize the output impedance for harmonic suppression, as given in (11) and (16). Based on the simplified relationship given in (13) and the conclusion in Section III-B, a low gain value for k_p and high gain value for k_i are initially selected to satisfy the first design rule. Next, the stability should be checked because increasing or decreasing the gains have opposite effects on the fundamental and resonant frequencies on the pole-zero maps, as shown in Fig. 4. Once $G_{vc}(s)$ achieves a magnitude of almost unity, the second design rule is followed to minimize the effect of the output impedance. The proposed design can be used to initially determine the virtual impedance. Then, the Bode diagram needs to be checked for whether the magnitude of $Z_{vc}(s)$ is suppressed well at all frequencies without a significant phase delay. After R_v and L_v are tuned, $p\%$ should be carefully examined to ensure that it does not exceed 100%. Finally, based on the magnitude of $G_{vc}(s)$, the compensated voltage reference $v_{ref,new}$ should be applied to the control block diagram shown in Fig. 2.

V. COMPARISON WITH CONVENTIONAL STUDIES

In [19], impedance shaping methods are reviewed for disturbance rejection and damping of voltage-source and current-source converters. Based on the classification used in [19], the proposed controller can be categorized as an LC filter voltage-source converter that uses an inner virtual impedance controller. Inner loop structure is directly applied to the PWM block, while the outer loop structure is linked to the grid side (either ac voltage or current). Table 1 summarizes existing virtual impedance-based controls that are the most similar to the proposed controller.

In [20], a similar method is used to that of the proposed controller, but the resistive impedance is only considered in the outer loop, and the inductor current needs to be sensed for a dual-loop structure so that the circulating currents of UPS modules can be suppressed under different output impedances.

A proportional–integral (PI) controller in [21] includes the LPF in the virtual inductive part to avoid high-frequency noise. Although their Bode diagram shows that the output impedance has more resistive behavior in the high-frequency region, the high-order harmonics of the circulating current are difficult to suppress with nonlinear loads because of the LPF.

In [22], a proportional–integral–derivative (PID) controller is used, but its limitations introduce output voltage distortion with nonlinear loads. This limitation can be mitigated by using multiple loops, but this makes the controller more complicated. Unfortunately, they did not include detailed Bode diagrams with regard to setting the controller gain and the design procedure.

In [23], the output impedance loop cannot be designed independently of the closed-loop current transfer function, and a high-pass filter (HPF) is added to avoid a drop in the phase margin. Because the system loop gain includes the virtual impedance, the design parameters of the controller gain, impedance of the inductance–capacitance–inductance (LCL) filter, and the virtual parameters cannot be decoupled.

In terms of using either a LPF or HPF, the parameter variation (a cutoff frequency of filter has a dependency on the initial set-value regardless of its inequality) introduces an intrinsic damping issue in the control loop. In contrast to the above methods, the proposed controller can ensure harmonic suppression in all frequency bands without a filter. The outer loop could be struggled with the low bandwidth of grid side voltage/current control loop to mitigate harmonic instability; however, the inner control loop is suitable to compensate the harmonic distortions with the better dynamic performance. In addition, the inner control loop can effectively decouple the system from the virtual impedance.

TABLE 1. Existing virtual impedance-based controls.

Ref.	System Control	Loop Structure	Feedback Type	Additional Filter	Control Independency	Application	Grid Filter	Purpose
[20]	PR	Outer	Voltage	No	No	UPS	LC	Parallel operation
[21]	PI	Outer	Voltage	LPF	No	UPS	LC	Parallel operation
[22]	PID	Inner	Voltage	No	Yes	UPS	LC	Parallel operation
[23]	PR	Inner	Current	HPF	No	Grid-connected inverter	LCL	Passivity enhancement
Proposed	PR	Inner	Voltage	No	Yes	UPS	LC	Harmonic suppression

Based on the comparison study, the proposed controller has similar features to [22]. But the different points are that the system control is based on the PID controller and the target topology is the half-bridge inverter. It is well-known that this PID controller is not appropriate to track the sinusoidal reference and rarely used in practice because of amplified signal resulted from time-derivative approach. To obtain the high-quality output voltage waveform, the voltage controller in [22] uses high gain and it leads to excluding the output impedance (reduced its influence) in the closed loop. But, this practice (high gain) should be proven its stability by drawing polo-zero map as Fig. 4. In this study, the output impedance Z_{vo} is included in the control loop (see Fig. 2) since the gain is not always set to high value.

It can be noted that the virtual impedance-based controls aim for parallel operation [20], [21], [22] and passivity enhancement [23]. Therefore, those articles do not precisely analyze both fast Fourier transform (FFT) and total harmonic distortion (THD) in their experimental sections. This study could contribute to showing experimental results of the FFT and THD for harmonic suppression through the proposed PR controller based on virtual impedance in the Section VI.

VI. EXPERIMENTAL RESULTS

Various experiments were performed to verify the proposed controller design for islanded operation of a single-phase full-bridge inverter. The experimental setup is shown in Fig. 8. A three-phase AC/DC converter and ESS-UPS module were connected to an AC grid and DC power supply, respectively. Measurements were taken by using an oscilloscope and power analyzer WT-3000. The linear and nonlinear loads were prepared by using three 37.3 Ω resistors, two 330 μF capacitors, and a diode rectifier. The experimental details are presented in Table 2, including both system and control parameters.

Significant differences according to the control method were only observed under nonlinear loads. Therefore, the experimental results under linear loads are not described in this study. Fig. 9 compares the experimental waveforms of the proposed PR controller and conventional PI and PR controllers under a nonlinear load at 2.3 kVA without voltage compensation as given in (21).

The nonlinear load was constructed by using a diode rectifier with one resistance (37.3 Ω) and two capacitors (330 μF each) in series. Figs. 9(a)-(c) show the performances of the conventional PI controller, conventional PR controller, and the proposed PR controller with output impedance design respectively. The proposed PR controller reduced the voltage perturbation caused by the output impedance and current harmonics. Furthermore, FFT analysis showed that it reduced the voltage harmonic components. In particular, it almost completely suppressed the 3rd order harmonic component even though the 3rd order harmonic currents were similar in magnitude for conventional PI and PR controllers.

Figs. 10 and 11 illustrate the effects of the virtual resistance R_v and virtual inductance L_v on the closed-loop input

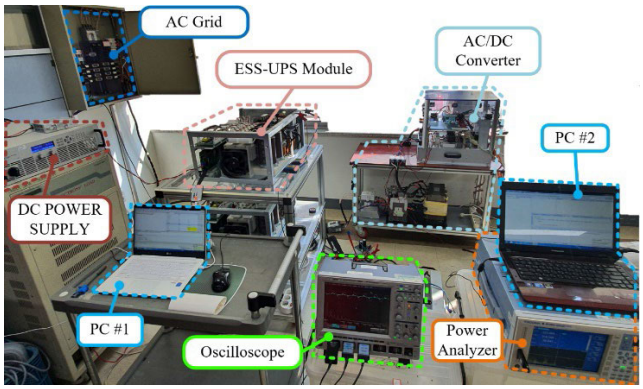


FIGURE 8. Experimental setup with the ESS-UPS system.

TABLE 2. System and control parameters of the experiment.

Parameters	Value	Unit
Maximum active power P	4000	W
Maximum reactive power Q	1000	VAR
DC input voltage V_{DC}	350	V_{dc}
AC output voltage v_o	220	V_{rms}
AC grid frequency	60	Hz
Filter inductance L	1	mH
Filter capacitance C	15	μF
Filter resistance R_L (measured)	100	mΩ
Switching frequency f_{sw}	12	kHz
Proportional gain k_p	0.001	-
Resonance gain k_i	50	-
Cutoff frequency (PR controller) ω_c	1	rad/s
Fundamental frequency ω_o	377	rad/s
Resonance frequency ω_r	8170	rad/s
Reference voltage with compensation v_{ref}	228.75	V_{rms}
Virtual resistance R_v	−121	mΩ
Virtual inductance L_v	−1	mH
Linear load (Resistive: 3 R-in-parallel)	12.43	Ω
Nonlinear load (Capacitive: Rectifier+R+2 C-in-series)	(Rectifier + 37.3 + 165)	-, Ω, μF

impedance, as described in Fig. 5. Fig. 10 shows that $Z_{vc}(s)$ in a low-order frequency region (e.g., 3rd and 5th orders) increased as R_v was decreased to −1, −1.5, and −2 Ω when L_v was fixed at 0 mH. Thus, the voltage harmonics increased at lower frequencies. This confirmed that R_v has a large effect at lower frequencies because of the lower-order related coefficients in (10). Similarly, Fig. 11 illustrates that higher-order harmonic components were more affected and increased rather than low-order harmonics when L_v was increased to −1, −5, and −10 mH while R_v was fixed to 0.1 Ω. This confirmed that the coefficients of the higher-order related components in (10) are more influenced by L_v.

To calculate the voltage-tracking ratio, the voltage output $v_{o(RMS)}$ was measured by the power analyzer WT-3000 during tests while the voltage reference $v_{ref(RMS)}$ was set to 220 V_{rms}.

Fig. 12(a) shows the experimental waveform of the conventional PI controller, which has the advantage of a high voltage-tracking ratio (218.9/220 = 99.5%) but inevitably

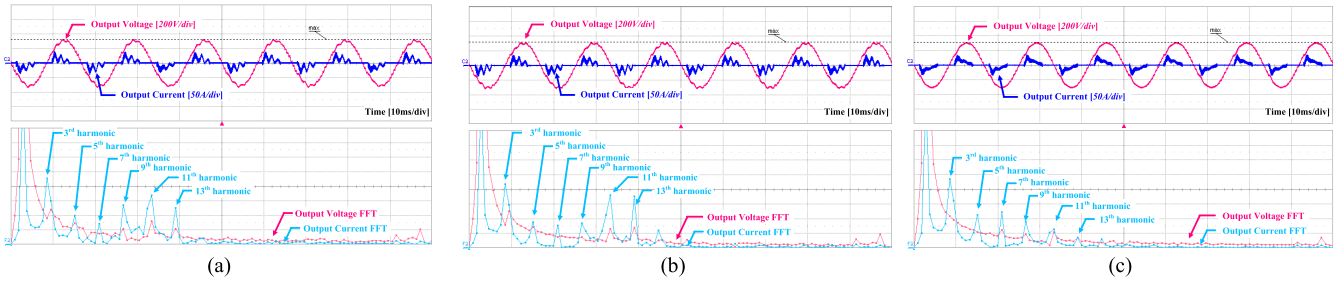


FIGURE 9. Experimental waveforms under nonlinear loads: (a) conventional PI controller, (b) conventional PR controller, (c) proposed PR controller with output impedance design.

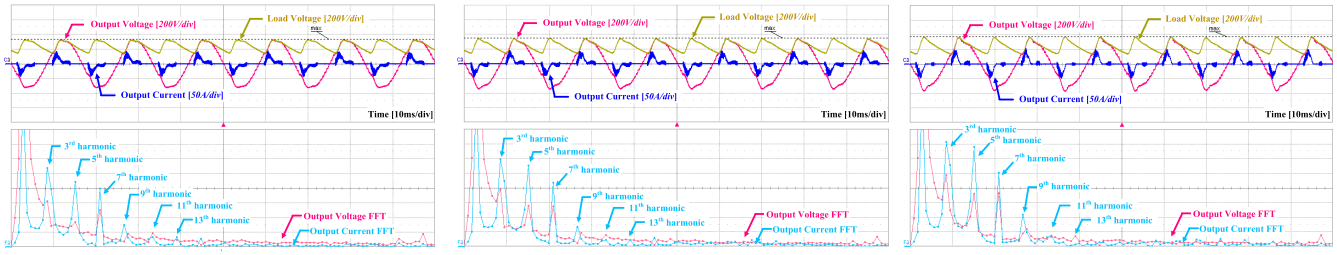


FIGURE 10. Effects of the output impedance on the output voltage with different R_V: −1, −1.5, and −2 Ω.

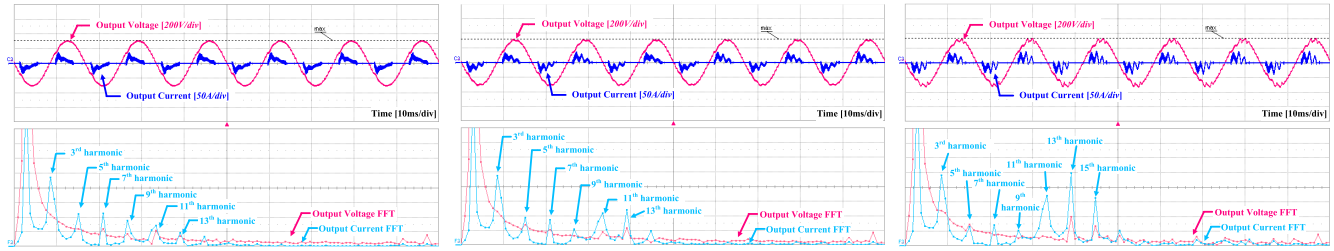
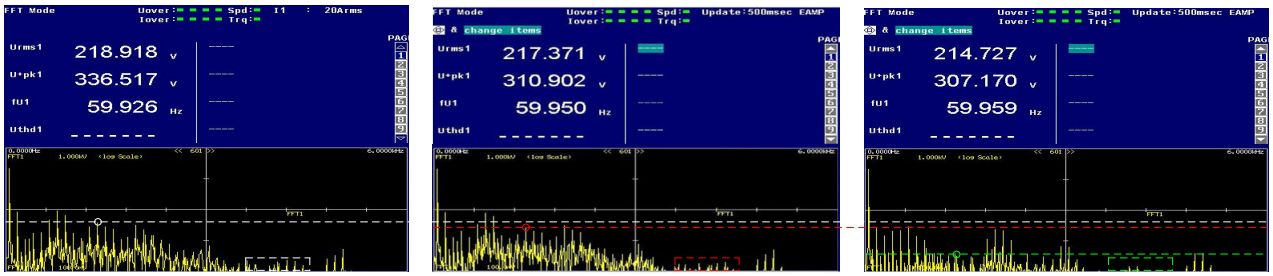


FIGURE 11. Effects of the output impedance on the output voltage with different L_V: −1, −5, and −10 mH.



(a) (b) (c)

FIGURE 12. FFT analysis: (a) conventional PI controller, (b) conventional PR controller, and (b) proposed PR controller.

includes a number of harmonic components in various frequency bands under nonlinear loads because of the simple control structure. Fig. 12(b) shows the experimental results of the conventional PR controller with slightly suppressed harmonic spectrum at the expense of lower voltage-tracking ratio. Fig. 12(c) shows the experimental waveform of the proposed PR controller with virtual impedance (R_V: −121mΩ, L_V: −1mH). The harmonic spectrum was significantly improved in various frequency bands compared to that shown in Fig. 12(a) despite the lower voltage-tracking ratio (214.7/220 = 97.6%).

The harmonic spectrum and the THD results of output voltage with conventional PI controller, conventional PR controller, and proposed PR controller are compared in Fig. 13. These results are obtained from Fig. 12 and summarize the odd harmonics at low-frequency band (from 3rd to 21st),

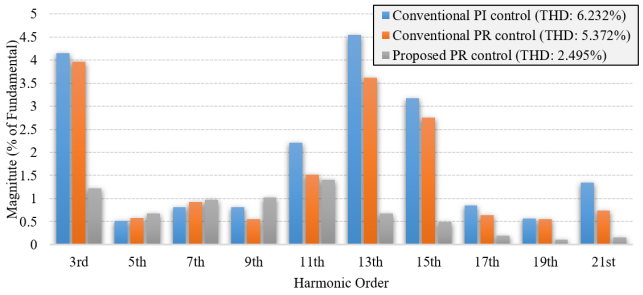
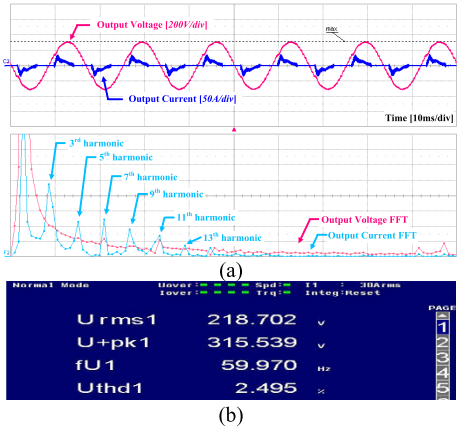


FIGURE 13. Harmonic spectrum and the THD of output voltage: conventional PI, PR controllers, and proposed PR controller.



(a)

(b)

FIGURE 14. Proposed design approach with voltage compensation: (a) experimental waveforms and (b) THD result.

which is dominant in the spectrum of output voltage of single-phase inverter [24]. It can be noted that the FFT analysis of the log scale in Fig. 12 (obtained by WT-3000) is converted to the linear scale in Fig. 13.

The THD can be improved a lot in the proposed PR controller with output impedance design as 2.495% compared to other controllers, for example, conventional PI controller as 6.232%, and conventional PR controller as 5.372% respectively. For fair comparison in terms of THD, the PR-based controllers for harmonic suppression in single-phase full-bridge inverters [25], [26] are investigated. In [25], the THD is improved to 4.03% (conventional PR controller) compared to 6.37% (conventional PI controller). Based on the THD tendency, it can be noted that the coherent results are found for conventional studies in Fig. 13.

Thanks to the combination of a state-feedback controller with a disturbance observer for the PR controller, the THD can be even more suppressed to 3.6% [26]. However, it is only considered the 3^{rd} and 5^{th} order harmonic components to prevent increasing design complexity. In the proposed control, the THD is 2.495% by significant reductions of harmonic voltage at the 3^{rd}, 13^{th}, and 15^{th} compared to conventional PI and PR controllers as shown in Figs. 13. The harmonic components at high-frequency band (over 21^{st}) are also suppressed as Fig. 12. While the harmonics at over 5^{th} order frequency could not be effectively suppressed in [26] since it is the form of multiple resonant controllers with the particular selection of harmonic components.

The voltage-tracking ratio can be improved by voltage compensation using (21) in Fig. 14. The voltage-tracking ratio was improved from 97.60% to 218.7/220 = 99.41% under same virtual impedance.

Figs. 9–14 demonstrate the feasibility of the proposed design and verify that it is intuitive and simple to implement. An excellent THD of 2.495% was obtained even under nonlinear load conditions, which meets the requirement of <5% under IEEE STD 519 as shown in Fig. 14(b).

VII. CONCLUSION

A PR controller design based on the output impedance is proposed for a single-phase full bridge inverter. The main contributions can be summarized as follows.

1) A theoretical analysis is presented on how the output impedance affects voltage perturbations under nonlinear loads. To support this analysis, the transfer functions and closed-loop dynamics of the inverter system are well-derived. This model can be effectively used for other controllers.

2) Based on the analysis, a simple voltage feedback control using the virtual impedance is presented that minimizes the closed-loop output impedance and allows the voltage transfer function and output impedance to be designed independently. To apply this proposed control to any system under different specification, the general design rules and procedure are provided.

3) To validate the stability, this study presents proper pole-zero maps but also Bode diagrams. The mathematical analysis has been proven that the proposed method is robust against parametric errors within 100%.

Experimental results have verified the effectiveness of the analysis on the proposed PR controller with output impedance. The results confirmed that the proposed PR controller suppressed harmonic components significantly in all frequency bands compared with conventional PI and PR controllers. The proposed controller achieved a voltage-tracking ratio of 99.41% and THD of 2.495% under nonlinear loads while maintaining a simple control structure.

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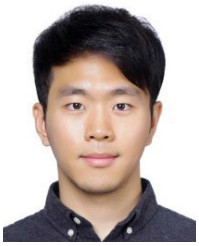

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