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RESEARCH ARTICLE

Full-Bridge Diode-Clamped Four-Level Symmetric Switching Converter

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ABSTRACT In this paper, we propose a novel full-bridge (FB) diode-clamped four-level symmetric switching converter. Multi-neighboring reference vector discontinuous PWM (MNRV DPWM) for FB topology was implemented using a symmetric half-bridge (HB)-based control approach that incorporates an offset voltage addition method. A diode-clamped four-level symmetrical switching circuit with pulse-amplitude-modulation (PAM) was proposed and its working principle was explained in detail. Voltage gain, duty loss factor, and zero-voltage-switching (ZVS) condition were derived by analyzing the steady-state operating characteristics of the proposed converter. The required input and output capacitance values were also calculated explicitly. The voltages across the series-connected input DC-link capacitors were well balanced and the output voltage was controlled in a simple linear manner by PAM. The proposed method offers the advantage of reducing circulating current when compared to the existing phase-shift method, thanks to the inclusion of an additional power delivery period. The effectiveness of the proposed converter was verified through simulation and prototype experiments. The power conversion efficiency exceeded 91.44% at an output power (P_O) of 250W or higher, with a peak efficiency of 95.23% achieved at $P_O = 750$W.

INDEX TERMS Full-bridge, diode-clamped converter, four-level, symmetric switching, DC-link voltage balancing, pulse-amplitude-modulation, multi-neighboring reference vector discontinuous PWM.

I. INTRODUCTION

Multilevel converters are popular in high-voltage applications because of their advantages such as the use of low rated voltage switches, low harmonic distortion generation, and reduced electromagnetic interference (EMI) [1], [2], [3], [4], [5]. Among many multilevel converters such as diode-clamped topology, flying capacitor method, and cascaded H-bridge type, diode-clamped type is widely used in the industry such as renewable energy systems and motor drives because of its simple power stage configuration [6], [7]. The diode-clamping topology is particularly useful in applications with limited power supply lines, such as rail vehicles where a single extra-high voltage power line is fed from an overhead catenary.

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However, the diode-clamped method suffers from the voltage deviation problem of series-connected DC-link capacitors as the multilevel dimension increases [8]. DC voltage imbalances can impact the performance of the converter. They can lead to increased losses, reduced efficiency, and distortion in the output voltage waveform. In extreme cases, severe imbalances can trigger fault conditions or overvoltage events. To solve this problem, many studies have been conducted in the literature, including the use of auxiliary circuit [9], [10], predictive control [11], [12], fault detection and protection [13]. Auxiliary circuits for DC voltage balancing offer simplicity, reliability, and cost-effectiveness, but can have limited control capabilities, energy losses, slow response times, and issues related to component size and scalability. Using model predictive control for DC voltage balancing in diode-clamped multilevel inverters provides benefits such as optimal control, flexibility, fast response, and reduced

harmonics. However, it raises issues related to computational complexity, parameter tuning, implementation complexity, and robustness. Fault detection and protection mechanisms offer significant benefits in terms of reliability, safety and reduced maintenance costs. However, there are challenges associated with complexity, cost, potential for false alarms, response time, and compatibility.

Meanwhile, virtual-vector PWM (VVPWM) and carrier-overlapped PWM (COPWM) are successfully applied to multi-phase multilevel PWM inverters [14], [15], [16], [17], [18], [19], [20], [21]. VVPWM quickly eliminates capacitor voltage deviations within a carrier period by extending the reference vector to a virtual space vectors whose associated current sum is zero. Thus, the voltage ripple is greatly reduced. COPWM effectively eliminates the voltage deviation across the capacitors and preserves the *volt·time* product by using multiple geometrically elaborately designed overlapping carriers with a single command voltage. However, for full closed-loop control, laborious control such as zero-sequence voltage calculations or rather complex duty compensation designs are required. In addition, these two methods have a problem in that switching loss is increased compared to the general phase-deposition PWM method. Both methods are suitable for multi-phase multilevel inverters, but are difficult to apply to DC/DC converters with high switching frequencies.

A lot of research has been conducted on multi-phase multilevel modular converters such as input-series/output-parallel (ISOP) converters, and cascaded converters based on a two-level topology [22], [23], [24], [25], [26], [27]. These topologies can be easily scaled to accommodate varying system capacities, making them particularly advantageous for constructing high-capacity power systems. However, each sub-module requires additional passive components, and the number of secondary diodes or switches increases proportionally with the number of sub-modules, making the overall system bulky, complex, and low power density. A separate voltage balancing algorithm between sub-modules is also essential. The modular multilevel converter (MMC) is a promising technology in the high-voltage and high-power fields [5], [28], [29]. Like other modular converters, it offers advantages in terms of system scalability and high power quality. However, the system configuration is complex, involving a large number of power semiconductors along with multiple leveling capacitors, and it also requires an advanced sorting algorithm for voltage balancing between sub-modules.

Multi-neighboring reference vector discontinuous PWM (MNRV DPWM) applicable to full-bridge (FB) DC/DC converters has been reported recently [30], [31]. It is characterized in that several reference voltage vectors having different charge/discharge characteristics of the capacitors are selected and combined according to the position of the command voltage. With the aid of duty compensators designed to reduce the voltage deviations among DC-link capacitors, voltage balance between capacitors is easily achieved while satisfying the magnitude of the command voltage on average. MNRV DPWM can be applied to any buck derived symmetric converter topology.

FB diode-clamped four-level *LLC* resonant converter using MNRV DPWM controls the output voltage by modulating the amplitude of the switching leg voltage instead of the conventional method of sweeping the switching frequency [30]. Pulse-amplitude-modulation (PAM) allows the switching frequency to be fixed at the resonant frequency, facilitating passive component design. However, since the resonant converter must be designed with a low magnetizing inductance (L_m) to secure zero-voltage-switching (ZVS), there is a problem in that the internal circulating current increases.

On the other hand, a phase-shift FB (PSFB) converter operates by modulating the phase difference between the switching legs [32], [33]. Unlike resonant converters, L_m can be designed to be large, so the circulating current can be greatly reduced. Additionally, both the primary switch and secondary diode are switched smoothly, providing high efficiency over a wide load range. Unlike the resonant converter in which the input/output voltage gain is related to the complex trigonometric values, the output voltage of PSFB converter can be simply controlled by modulating the leg phase difference.

Meanwhile, it has been proven that the MNRV DPWM method for FB topology can be implemented as a symmetric control method of two half-bridges (HBs) constituting the FB [34]. In other words, the FB topology can be easily replaced with two HBs by aligning the symmetry point where the polarity of the command voltage changes and the boundary point where the switching area is divided. Symmetric HB-based control technique can be easily implemented with a well-known offset voltage addition method [35], [36]. This means that MNRV DPWM can be widely applied to two/three or more multi-phase power conversion systems in the future.

In this paper, a symmetric switching converter with offset voltage addition is proposed. The circuit and basic operation principle of the proposed converter are described in Section II. The detailed operating characteristics in steady state are analyzed in Section III, and the design parameters for input and output capacitors are expressed in Section IV. In Section V, the effectiveness of the proposed converter is confirmed and validated by simulations and 500W prototype circuit experiments. Section VI compares the proposed symmetric switching converter with a conventional isolated multilevel converter and elucidates its advantages and disadvantages. In the conclusion section VII, suitable application areas, along with the characteristics and pros and cons of the proposed converter, are outlined.

II. PROPOSED FB DIODE-CLAMPED FOUR-LEVEL SYMMETRIC SWITCHING CONVERTER

A. CIRCUIT STRUCTURE

The circuit of the proposed converter is shown in Fig. 1. The DC-link stage consists of series-connected three capacitors

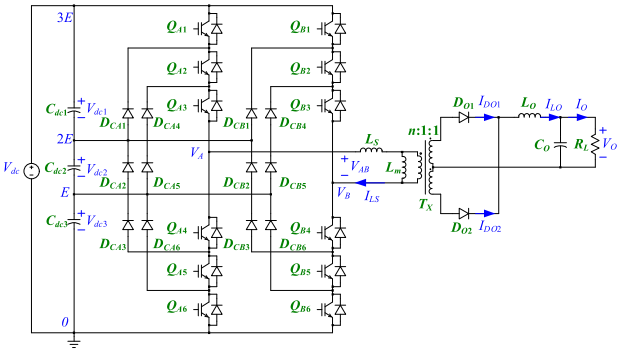

FIGURE 1. Circuit diagram of the proposed FB diode-clamped four-level symmetric switching converter.

C_{dc1}, C_{dc2}, and C_{dc3}. The switching stack consists of A-phase switches Q_{A1} to Q_{A6} and B-phase switches Q_{B1} to Q_{B6}, and clamping diodes $D_{CA1} \sim D_{CA6}$ and $D_{CB1} \sim D_{CB6}$. Here, the four-level topology is represented with three clamp diodes in series, rather than two in series, in order to balance the voltage across the clamp diodes [37]. The series inductor L_S includes the leakage inductance of the transformer T_X having a L_m and a turn ratio of n:1:1. The rectifying stage is comprised of output diodes D_{O1} and D_{O2} and supplies power to the load R through the output smoothing inductor L_O and the output capacitor C_O. According to the complementary rule of the diode-clamped topology, the on/off states of the lower switches are determined inversely to the on/off states of the corresponding upper switches. Q_{A1} and Q_{A4}, Q_{A2} and Q_{A5}, and Q_{A3} and Q_{A6} are complementary switch pairs. The same applies to the phase B.

B. DESIGN PRINCIPLES OF FB MNRV DPWM

Fig. 2 illustrates the principle of symmetric MNRV DPWM for the FB diode-clamped four-level topology with an offset voltage injection method. The FB topology (or more than three phases is also possible) can be equated to the symmetric operation of the two HBs that constitute the FB, and the HB-based diode-clamped topology can be readily implemented by applying the well-known offset voltage injection technique. In this context, V_{cmd} was assumed to be positive, and the offset voltage was applied differently depending on clamp mode (CM). In the symmetric HB-based MNRV, the V_{cmd} is divided into two command voltages corresponding to phases A and B as $V_{cmd\_A} = 0.5V_{cmd}$ and $V_{cmd\_B} = -0.5V_{cmd}$. Then, by adding normalization voltage of $0.5V_{dc}$ and the offset voltage of V_{offset} that varies according to CM, the final command values of V_{CMD_A} and V_{CMD_B} are set as $V_{CMD\_A} = V_{cmd\_A}+0.5V_{dc} + V_{offset}$ and $V_{CMD\_B} = V_{cmd\_B}+0.5V_{dc} + V_{offset}$, respectively. V_{offset} is determined by (1) according to the CM.

$$V_{offset} = \begin{cases} 0.5V_{dc} - \max(V_{cmd\_A}, V_{cmd\_B}), & for\ CM = 1 \\ -0.5V_{dc} - \min(V_{cmd\_A}, V_{cmd\_B}), & for\ CM = -1 \end{cases} \tag{1}$$

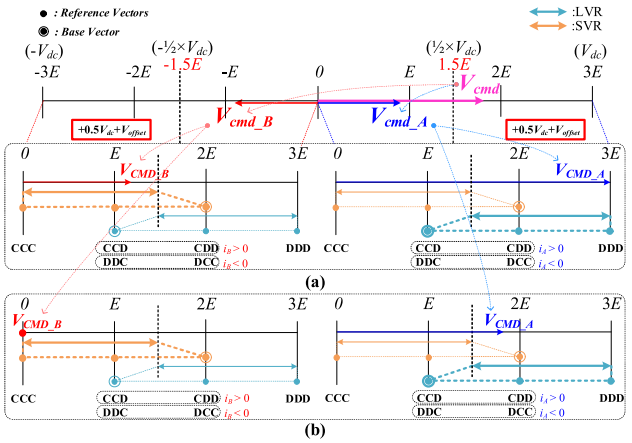

FIGURE 2. Symmetric HB-based MNRV DPWM design rule for FB topology in (a) UCM and (b) LCM when $V_{cmd} > 0$.

Fig. 2a and b represent multiple adjacent reference voltage selection rule according to the upper clamping mode (UCM, CM = 1) and the lower clamping mode (LCM, CM = −1). Based on the virtual neutral point $0.5V_{dc}$, if V_{CMD_A} or V_{CMD_B} is larger than the corresponding virtual voltage, it is classified as large vector region (LVR), and if these command voltages are smaller than the virtual voltage, it is distinguished as small vector region (SVR). According to the position of command voltages, several adjacent reference vectors with different charging/discharging characteristics for DC-link capacitors are selected. In LVR, reference voltage vectors are selected from E to $3E$, and in SVR, they are selected from 0 to $2E$. Here, E is the unit voltage level of the capacitor and means one third of the DC-link voltage V_{dc}. In MNRV DPWM, a ±180° clamped switching state is introduced to reduce switching loss and redundancy [38]. When $V_{cmd} > 0$, in UCM, V_{CMD_A} is clamped to a V_{dc} value and V_{CMD_B} is classified to LVR or SVR according to the magnitude of V_{CMD_B}, and in LCM, V_{CMD_B} is clamped to 0 value and V_{CMD_A} is divided to LVR or SVR depending to the magnitude of V_{CMD_A}. The C or D located at the bottom indicates the charge/discharge state of capacitors at each step voltage. For example, the switching pairs representing $2E$ includes (20) in LCM and (31) in UCM, and the capacitor charge/discharge state at (20) is CDD, which means that C_{dc1} is charged and C_{dc2} and C_{dc3} are discharged. When V_{cmd} is negative, it has a symmetry with the case of positive V_{cmd}.

$$@CM = 1$$

$$(AB) = \begin{cases} \underset{DDD}{(30)} - \underset{DDC}{(31)} - \underset{DCC}{(32)}, & for\ 0.5 \le m \le 1 \\ \underset{DDC}{(31)} - \underset{DCC}{(32)} - \underset{CCC}{(33)}, & for\ 0 \le m < 0.5 \\ \underset{DDC}{(13)} - \underset{DCC}{(23)} - \underset{CCC}{(33)}, & for\ -0.5 \le m < 0 \\ \underset{DDD}{(03)} - \underset{DDC}{(13)} - \underset{DCC}{(23)}, & for\ -1 \le m \le -0.5 \end{cases} \tag{2}$$

$@CM = -1$

$$(AB) = \begin{cases} \underset{DDD}{(30)} - \underset{CDD}{(20)} - \underset{CCD}{(10)}, & for\ 0.5 \le m \le 1 \\ \underset{CDD}{(20)} - \underset{CCD}{(10)} - \underset{CCC}{(00)}, & for\ 0 \le m < 0.5 \\ \underset{CDD}{(02)} - \underset{CCD}{(01)} - \underset{CCC}{(00)}, & for\ -0.5 \le m < 0 \\ \underset{DDD}{(03)} - \underset{CDD}{(02)} - \underset{CCD}{(01)}, & for\ -1 \le m \le -0.5 \end{cases} \tag{3}$$

The switching patterns in the end sag type that adopt either down or up counting carrier depending on the magnitude of modulation index $m = V_{cmd}/V_{dc}$ ($-1 \le m \le 1$) and CM are expressed in (2) and (3) [30]. When V_{cmd} is greater than $0.5V_{dc}$ in UCM, the switching pair (AB) changes as follows: because the A phase is clamped to the positive DC rail, the switching status of A always remains at "3", while the switching status of the B phase changes from "0", "1", and "2" because the B phase is located in SVR. When V_{cmd} is less than $0.5V_{dc}$ in UCM, phase A remains fixed at "3", and phase B is located in LVR, causing it to switch among "1", "2", and "3". This design was intended to have an end sag characteristic, resulting in a staircase-shaped waveform descending from the end. The same principles apply to other cases.

To remove the voltage deviations of capacitors, duty compensators proportional to the capacitor voltage deviation are designed as (4).

$$\begin{aligned} &d_{comp1\_23} \\ &= k_p(V_{dc1} - \frac{V_{dc2} + V_{dc3}}{2}) + k_i \int_0^t (V_{dc1} - \frac{V_{dc2} + V_{dc3}}{2})dt, \\ &d_{comp12\_3} \\ &= k_p(\frac{V_{dc1} + V_{dc2}}{2} - V_{dc3}) + k_i \int_0^t (\frac{V_{dc1} + V_{dc2}}{2} - V_{dc3})dt. \end{aligned} \tag{4}$$

The duty compensation parameters d_{comp1_23} and d_{comp12_3} are proportional to the differences between V_{dc1} and $(V_{dc2} + V_{dc3})/2$ and between $(V_{dc1} + V_{dc2})/2$ and V_{dc3}, respectively. V_{dc1}, V_{dc2}, and V_{dc3} denote the voltages of C_{dc1}, C_{dc2}, and C_{dc3}, respectively. In (4), k_p and k_i refer to the proportional and integral gains of the PI controller. Based on the E vector in LVR and the $2E$ vector in SVR, the duty ratios of each reference vectors are determined according to the CM by (5) and (6), as shown at the bottom of the next page, while satisfying the *volt·time* product.

d_{0_X}, d_{E_X}, d_{2E_X}, and d_{3E_X} ($X = A$ or B) refer to duty ratios of step voltages 0, E, $2E$, and $3E$ vectors, respectively. As seen in (5) and (6), the duty ratios of each step voltages include the duty compensation parameters, so it can be expected that the capacitor voltage deviation will be controlled by these duty combinations.

$V_{cmd} \ge 0$

$@CM = 1$

PWM_CMDs of A leg :

$$\begin{pmatrix} PWM\_CMD\_A1 \\ PWM\_CMD\_A2 \\ PWM\_CMD\_A3 \end{pmatrix} = N_{\max} \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix},$$

PWM_CMDs of B leg :

$$\begin{pmatrix} PWM\_CMD\_B1 \\ PWM\_CMD\_B2 \\ PWM\_CMD\_B3 \end{pmatrix} = \begin{cases} N_{\max} \begin{pmatrix} d_{3E\_B} \\ d_{2E\_B} + d_{3E\_B} \\ 1 \end{pmatrix} @LVR, \\ N_{\max} \begin{pmatrix} 0 \\ d_{2E\_B} \\ d_{E\_B} + d_{2E\_B} \end{pmatrix} @SVR, \end{cases}$$

$@CM = -1$

PWM_CMDs of B leg :

$$\begin{pmatrix} PWM\_CMD\_B1 \\ PWM\_CMD\_B2 \\ PWM\_CMD\_B3 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix},$$

PWM_CMDs of A leg :

$$\begin{pmatrix} PWM\_CMD\_A1 \\ PWM\_CMD\_A2 \\ PWM\_CMD\_A3 \end{pmatrix} = \begin{cases} N_{\max} \begin{pmatrix} d_{3E\_A} \\ d_{2E\_A} + d_{3E\_A} \\ 1 \end{pmatrix} @LVR, \\ N_{\max} \begin{pmatrix} 0 \\ d_{2E\_A} \\ d_{E\_A} + d_{2E\_A} \end{pmatrix} @SVR. \end{cases} \tag{7}$$

$V_{cmd} < 0$

$@CM = 1$

PWM_CMDs of B leg :

$$\begin{pmatrix} PWM\_CMD\_B1 \\ PWM\_CMD\_B2 \\ PWM\_CMD\_B3 \end{pmatrix} = N_{\max} \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix},$$

PWM_CMDs of A leg :

$$\begin{pmatrix} PWM\_CMD\_A1 \\ PWM\_CMD\_A2 \\ PWM\_CMD\_A3 \end{pmatrix} = \begin{cases} N_{\max} \begin{pmatrix} d_{3E\_A} \\ d_{2E\_A} + d_{3E\_A} \\ 1 \end{pmatrix} @LVR, \\ N_{\max} \begin{pmatrix} 0 \\ d_{2E\_A} \\ d_{E\_A} + d_{2E\_A} \end{pmatrix} @SVR, \end{cases}$$

$@CM = -1$

PWM_CMDs of A leg :

$$\begin{pmatrix} PWM\_CMD\_A1 \\ PWM\_CMD\_A2 \\ PWM\_CMD\_A3 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix},$$

PWM_CMDs of B leg :

$$\begin{pmatrix} PWM\_CMD\_B1 \\ PWM\_CMD\_B2 \\ PWM\_CMD\_B3 \end{pmatrix} = \begin{cases} N_{\max} \begin{pmatrix} d_{3E\_B} \\ d_{2E\_B} + d_{3E\_B} \\ 1 \end{pmatrix} @LVR, \\ N_{\max} \begin{pmatrix} 0 \\ d_{2E\_B} \\ d_{E\_B} + d_{2E\_B} \end{pmatrix} @SVR. \end{cases} \tag{8}$$

After determining the duty ratios of each step voltage, the final PWM command values PWM_CMD_X of A and B legs can be calculated according to CM as (7) and (8). Here, N_{max} corresponds to carrier period value. As can be seen from (5)−(8), it can be confirmed that when m is negative, it has a symmetric characteristic as when m is positive. In other words, when the polarity of V_{cmd} changes, $+/-$ m becomes $-/+$ m and A leg's values are interchanged with B leg's values.

C. CONTROL ALGORITHM

The control block diagram of the proposed symmetric switching converter is shown in Fig. 3. First, the CM is determined by comparing the absolute difference values between the reference value ($V_{dc}/3$) and V_{dc1} and between reference value and V_{dc3}. For CM $= -1$, it tends to charge C_{dc1} and discharge C_{dc3}, and vice versa for CM $= 1$. Therefore, CM is selected as -1 if V_{dc1} is lower than V_{dc3}, and vice versa, CM becomes 1. To control the output voltage V_O constantly, PI control is

$$
\begin{aligned}
&V_{cmd} \geq 0 \\
&@CM = 1 \\
&A\ leg's\ reference\ vectors: \\
&\begin{pmatrix} d_{E\_A} \\ d_{2E\_A} \\ d_{3E\_A} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix}, \\
&B\ leg's\ reference\ vectors: \\
&\begin{cases}
@LVR: \\
\begin{pmatrix} d_{E\_B} \\ d_{2E\_B} \\ d_{3E\_B} \end{pmatrix} = \begin{pmatrix} m - \frac{1}{3}d_{comp1\_23} \\ m + \frac{2}{3}d_{comp1\_23} \\ 1 - 2m - \frac{1}{3}d_{comp1\_23} \end{pmatrix}, \\
@SVR: \\
\begin{pmatrix} d_{0\_B} \\ d_{E\_B} \\ d_{2E\_B} \end{pmatrix} = \begin{pmatrix} -1 + 2m - \frac{1}{3}d_{comp12\_3} \\ 1 - m + \frac{2}{3}d_{comp12\_3} \\ 1 - m - \frac{1}{3}d_{comp12\_3} \end{pmatrix},
\end{cases} \\
&@CM = -1 \\
&B\ leg's\ reference\ vectors: \\
&\begin{pmatrix} d_{0\_B} \\ d_{E\_B} \\ d_{2E\_B} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix}, \\
&A\ leg's\ reference\ vectors: \\
&\begin{cases}
@LVR: \\
\begin{pmatrix} d_{E\_A} \\ d_{2E\_A} \\ d_{3E\_A} \end{pmatrix} = \begin{pmatrix} 1 - m + \frac{1}{3}d_{comp1\_23} \\ 1 - m - \frac{2}{3}d_{comp1\_23} \\ -1 + 2m + \frac{1}{3}d_{comp1\_23} \end{pmatrix}, \\
@SVR: \\
\begin{pmatrix} d_{0\_A} \\ d_{E\_A} \\ d_{2E\_A} \end{pmatrix} = \begin{pmatrix} 1 - 2m + \frac{1}{3}d_{comp12\_3} \\ m - \frac{2}{3}d_{comp12\_3} \\ m + \frac{1}{3}d_{comp12\_3} \end{pmatrix}.
\end{cases}
\end{aligned} \tag{5}
$$

$$
\begin{aligned}
&V_{cmd} < 0 \\
&@CM = 1 \\
&B\ leg's\ reference\ vectors: \\
&\begin{pmatrix} d_{E\_B} \\ d_{2E\_B} \\ d_{3E\_B} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix}, \\
&A\ leg's\ reference\ vectors: \\
&\begin{cases}
@LVR: \\
\begin{pmatrix} d_{E\_A} \\ d_{2E\_A} \\ d_{3E\_A} \end{pmatrix} = \begin{pmatrix} -m - \frac{1}{3}d_{comp1\_23} \\ -m + \frac{2}{3}d_{comp1\_23} \\ 1 + 2m - \frac{1}{3}d_{comp1\_23} \end{pmatrix}, \\
@SVR: \\
\begin{pmatrix} d_{0\_A} \\ d_{E\_A} \\ d_{2E\_A} \end{pmatrix} = \begin{pmatrix} -1 - 2m - \frac{1}{3}d_{comp12\_3} \\ 1 + m + \frac{2}{3}d_{comp12\_3} \\ 1 + m - \frac{1}{3}d_{comp12\_3} \end{pmatrix},
\end{cases} \\
&@CM = -1 \\
&A\ leg's\ reference\ vectors: \\
&\begin{pmatrix} d_{0\_A} \\ d_{E\_A} \\ d_{2E\_A} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix}, \\
&B\ leg's\ reference\ vectors: \\
&\begin{cases}
@LVR: \\
\begin{pmatrix} d_{E\_B} \\ d_{2E\_B} \\ d_{3E\_B} \end{pmatrix} = \begin{pmatrix} 1 + m + \frac{1}{3}d_{comp1\_23} \\ 1 + m - \frac{2}{3}d_{comp1\_23} \\ -1 - 2m + \frac{1}{3}d_{comp1\_23} \end{pmatrix}, \\
@SVR: \\
\begin{pmatrix} d_{0\_B} \\ d_{E\_B} \\ d_{2E\_B} \end{pmatrix} = \begin{pmatrix} 1 + 2m + \frac{1}{3}d_{comp12\_3} \\ -m - \frac{2}{3}d_{comp12\_3} \\ -m + \frac{1}{3}d_{comp12\_3} \end{pmatrix}.
\end{cases}
\end{aligned} \tag{6}
$$

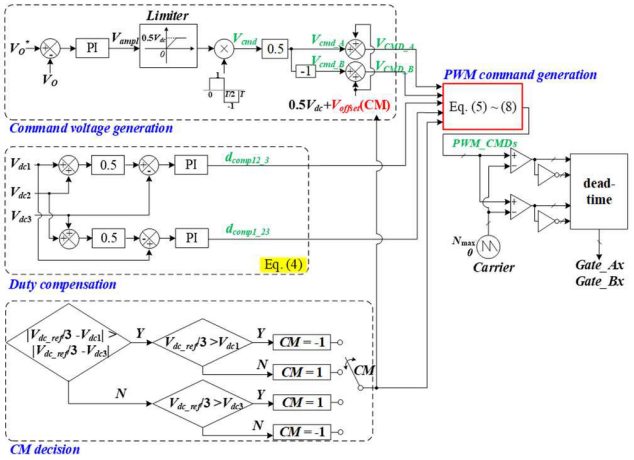

FIGURE 3. Control block diagram for the proposed converter.

performed, and the result is set as V_{ampl}, which corresponds to to the magnitude (amplitude) of the PWM command voltage. V_{ampl} is multiplied by a switching square wave alternating ± 1 to generate a V_{cmd} reference voltage that swings V_{ampl} for half cycle and $-V_{ampl}$ for the next half cycle. As described above, this V_{cmd} is divided into V_{cmd_A} and V_{cmd_B}. After adding the V_{offset} of (1) and the normalization factor of $0.5V_{dc}$, and considering duty compensator values of (4), final PWM commands are generated accordingly. Designing appropriate carrier either down or up types depending to the CM, proper gate signals of the A and B legs are finally output.

III. ANALYSIS

A. OPERATION MODES

The equivalent circuits of the switching states that causes a capacitor voltage fluctuation are shown in Fig. 4. Except for (30), (03), (33), and (00), capacitor voltage deviations occur uniquely in all other switching pairs. In UCM, capacitor voltage charging states becomes DDC or DCC, and in LCM, it becomes CDD or CCD. Therefore, if $V_{dc1} > V_{dc3}$, UCM is selected and vice versa.

To analyze the operating characteristics in steady state, it is assumed that proposed converter operates in LVR as UCM during one cycle and as LCM during the next cycle as shown in Fig. 5. In steady state, it has four distinct modes during each half cycle.

Mode 1 [t_0, t_1]: At t_0, CM changes from LCM to UCM and the polarity of V_{cmd} changes from negative to positive. The switching state at this mode is (30), and all upper switches of phase A are on and all upper switches of phase B are off. All upper switches of phase A turn on ZVS condition due to negative L_S current, I_{Ls}. This mode corresponds to the commutation time period in which both D_{O1} and D_{O2} are conducting with soft commutation. Output inductor current, I_{LO}, is sum of two output diodes currents. The time length of this mode is equal to duty loss period, $d_{loss} \cdot T/2$, and the primary side switching voltage V_{AB} is not applied to the secondary side. Here, T is time period.

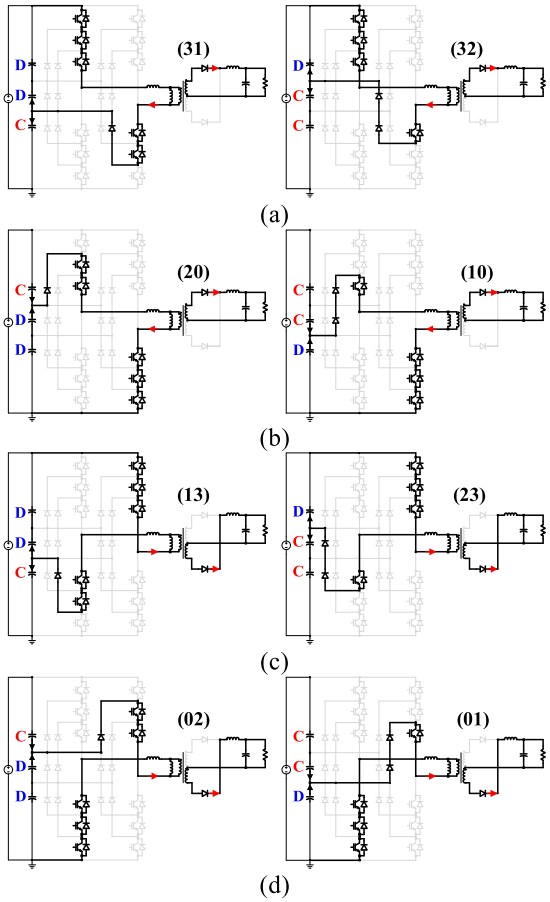

FIGURE 4. Equivalent circuits of switching pairs that produces a voltage variation at (a) UCM, (b) LCM when $V_{cmd} \geq 0$ and (c) UCM, (d) LCM when $V_{cmd} < 0$.

Mode 2 [t_1, t_2]: At t_1, commutation process ends, and the primary current is delivered to the output stage through D_{O1}. Until Q_{B3} is turned on (i.e., Q_{B6} is turned off) at t_2, the switching state is still (30). Assuming that L_m is much larger than L_S and ignoring the voltage drop due to the current flowing through L_S, V_{AB} of V_{dc} is applied to output inductor through D_{O1}. I_{LO} increases with the slope of $(V_{dc}/n - V_O)/L_O$. I_{LO} equals current of diode D_{O1}, I_{DO1}. The length of this mode corresponds to $(d_{3E} - d_{loss}) \cdot T/2$.

Mode 3 [t_2, t_3]: At t_2, Q_{B6} turns off and the switching state becomes (31). The capacitor charge state becomes DDC, which means C_{dc1} and C_{dc2} are discharged with a current of $1/3 \cdot I_{LS}$ and C_{dc3} is charged with a current of $2/3 \cdot I_{LS}$. V_{AB} of $2V_{dc}/3$ is applied to the L_O through D_{O1}, and the slope of I_{LO} changes to $(2V_{dc}/3n - V_O)/L_O$. The length of mode 3 corresponds to $d_{2E} \cdot T/2$. Unlike conventional PSFB converters, this mode corresponds to another powering period. Through this section, the reactive current can be reduced because power is transferred from the primary side to the secondary side of transformer.

Mode 4 [t_3, t_4]: At t_3, Q_{B5} turns off and the switching state becomes (32). The capacitor charge state becomes DCC, and C_{dc1} is discharged with a current of $2/3 \cdot I_{LS}$ and C_{dc2} and

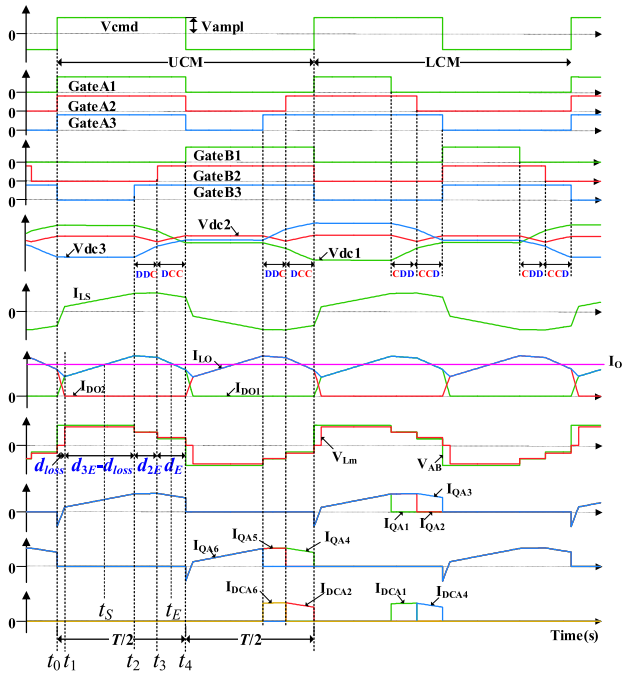

FIGURE 5. Theoretical waveforms of the proposed converter when |m| ≥ 0.5.

C_{dc3} are charged with a current of $1/3 \cdot I_{LS}$. V_{AB} of $V_{dc}/3$ is applied to the L_O through D_{O1}, and the I_{LO} decreases with a negative slope of $(V_{dc}/3n - V_O)/L_O$. This mode continues until all of the upper switches of phase A are turned off and all of the upper switches of phase B are turned on at t_4. The time period of this mode is $d_E \cdot T/2$. This section is also included in the powering period.

Due to the symmetrical operation of the DC/DC converter, the operation of remaining half cycle in UCM can be easily inferred from the previous half cycle. During the next one cycle, LCM operation starts. The operations in LCM are symmetric with UCM. Fig. 5 also includes the switches and clamping diodes currents (I_{QAx}, I_{DCAx}) of phase A. The operating aspect of the proposed converter is similar to the conventional two-level PSFB topology, but the current pattern is symmetric without distinction between leading and lagging legs. Although not shown in the Figure, the current of phase B also has cross-symmetric characteristics with phase A, which means that I_{QAx} has time-shifted symmetry with $I_{QB(7-x)}$. Here, $x = 1, 2, 3, \ldots, 6$.

B. VOLTAGE GAIN

Meanwhile, an analyzing result of the change of I_{LO} during half cycle (Fig. 6) is expressed in (9) and (10) when $|m| \geq 0.5$ and $|m| < 0.5$, respectively.

Using the fact that the *volt·time* product of the inductor preserves as zero, the voltage transfer gain of nV_O/V_{dc} is obtained as (11). The voltage transfer gains in LVR and SVR have a similar relationship.

Because the average of I_{LO} during $T/2$ is equal to output current I_O, $I_{LO}(t_0)$ can be calculated as (12). Using the

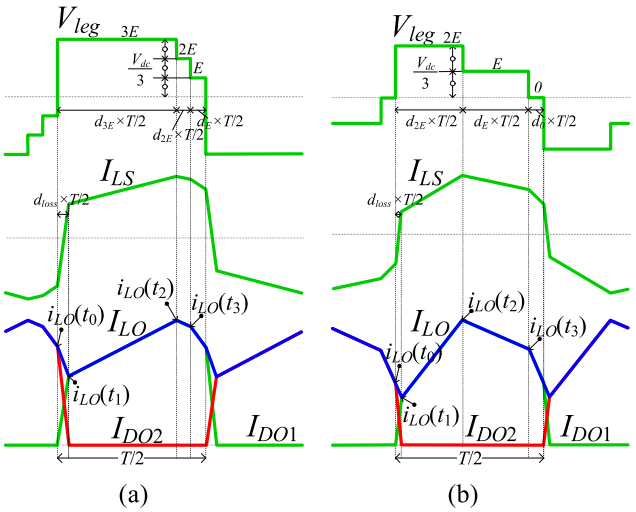

FIGURE 6. V_{leg}, I_{LS}, and I_{LO} waveforms of the proposed converter when (a) |m| ≥ 0.5 and (b) |m| < 0.5.

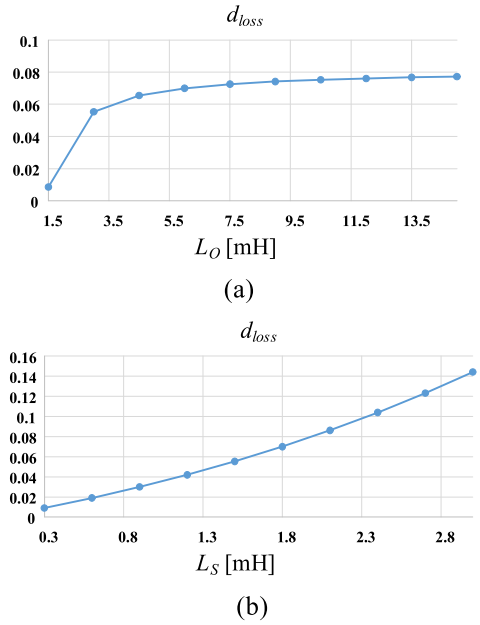

FIGURE 7. d_{loss} dependency according to the inductance variations of (a) L_O and (b) L_S.

geometry of I_{LS} and I_{LO} during the commutation period, d_{loss} can be determined as (13), where **A** and **B** factors are related to circuit parameters as expressed in (14).

$$For\ |m| \geq 0.5:$$

$$i_{LO}(t_1) = i_{LO}(t_0) - \frac{V_O}{2L_O} d_{loss} T,$$

$$i_{LO}(t_2) = i_{LO}(t_1) + \frac{\frac{V_{dc}}{n} - V_O}{2L_O} (d_{3E} - d_{loss}) T,$$

$$i_{LO}(t_3) = i_{LO}(t_2) + \frac{\frac{2}{3} \cdot \frac{V_{dc}}{n} - V_O}{2L_O} d_{2E} T,$$

$$i_{LO}(t_0) = i_{LO}(t_3) + \frac{\frac{1}{3}\cdot\frac{V_{dc}}{n} - V_O}{2L_O} d_E T. \tag{9}$$

For $|m| < 0.5$:

$$i_{LO}(t_1) = i_{LO}(t_0) - \frac{T}{2L_O}\cdot d_{loss} V_O$$

$$i_{LO}(t_2) = i_{LO}(t_1) + \frac{\frac{2}{3}\cdot\frac{V_{dc}}{n} - V_O}{2L_O} T\cdot(d_{2E} - d_{loss})$$

$$i_{LO}(t_3) = i_{LO}(t_2) + \frac{\frac{1}{3}\cdot\frac{V_{dc}}{n} - V_O}{2L_O} T\cdot(d_E)$$

$$i_{LO}(t_0) = i_{LO}(t_3) - \frac{T}{2L_O}\cdot d_0 V_O \tag{10}$$

$$\frac{nV_O}{V_{dc}} = \begin{cases} m - d_{loss}, & for\ |m| \geq 0.5 \\ m - \frac{2}{3}d_{loss}, & for\ |m| < 0.5 \end{cases} \tag{11}$$

$$i_{LO}(t_0) = \begin{cases} I_O - \frac{T}{4L_O}\left\{\begin{pmatrix} -\frac{2}{3}m^2 + d_{loss}^2 - md_{loss} \\ +\frac{7}{3}m - d_{loss} - \frac{2}{3} \end{pmatrix}\cdot\frac{V_{dc}}{n} \right\}, \\ \quad -mV_O \\ for\ |m| \geq 0.5 \\ I_O - \frac{T}{4L_O}\left\{\begin{pmatrix} \frac{1}{3}m^2 + \frac{2}{3}d_{loss}^2 - \frac{4}{3}md_{loss} \\ +m - \frac{2}{3}d_{loss} \end{pmatrix}\cdot\frac{V_{dc}}{n} \right\}, \\ \quad -2mV_O \\ for\ |m| < 0.5 \end{cases} \tag{12}$$

$$d_{loss} = 0.5 \times (-A + \sqrt{A^2 - 4B}) \tag{13}$$

$$A = \begin{cases} -m - 1 + \frac{nV_O}{V_{dc}} + \frac{n^2 L_O}{L_S}, & for\ |m| \geq 0.5 \\ -2m - 1 + \frac{3nV_O}{2V_{dc}} + \frac{n^2 L_O}{L_S}, & for\ |m| < 0.5 \end{cases}$$

$$B = \begin{cases} -\frac{2}{3}m^2 + (\frac{7}{3} - \frac{nV_O}{V_{dc}})m - \frac{2}{3} - \frac{4nL_O I_O}{TV_{dc}}, \\ \qquad for\ |m| \geq 0.5 \\ \frac{1}{2}m^2 + (\frac{3}{2} - \frac{3nV_O}{V_{dc}})m - \frac{6nL_O I_O}{TV_{dc}}, \\ \qquad for\ |m| < 0.5 \end{cases} \tag{14}$$

Referring to Fig. 7, which shows the relationships between d_{loss} and L_O and L_S from (13), d_{loss} increases mainly in proportion to L_S. This is because when L_S increases, the current slopes of I_{DO1} and I_{DO2} decreases during the commutation period, thus d_{loss} period becomes longer. Here, the calculation conditions are $V_{dc} = 700$V, $V_O = 350$V, $I_O = 1.43$A, $n = 1.5$, $L_S = 1.5$mH, $L_O = 3$mH, $T = 0.1$ms, $m = 0.8$.

Fig. 8 shows the calculation and simulation results for the change of gain and d_{loss} according to the m variation. Ignoring the small d_{loss} value, it can be seen that the gain is almost simply proportional to m.

C. ZVS CONDITION

To satisfy the ZVS condition, when the switching state changes from (01) (Fig. 4d) or (23) (Fig. 4c) to (30), the energy stored in L_S must be sufficiently large to charge and discharge the output capacitances C_{OSS} of six switches in A leg and two switches in B leg. Therefore, the L_S value that satisfies the ZVS condition can be determined by (15).

$$L_S \geq \frac{8}{9} n^2 C_{OSS} \left(\frac{V_{dc}}{i_{LO}(t_0)}\right)^2 \tag{15}$$

Since the unit switching voltage level of the four-level converter is reduced by three times compared to two-level topology, L_S for ZVS is reduced compared to the existing two-level converter. The dead-time t_{dead} needed to ensure ZVS can be also calculated as (16) [39].

$$t_{dead} \geq \frac{T_r}{4} = \frac{\pi}{2}\sqrt{L_S C_{OSS,EQ}} = \frac{\sqrt{6}\pi}{3}\sqrt{L_S C_{OSS}} \tag{16}$$

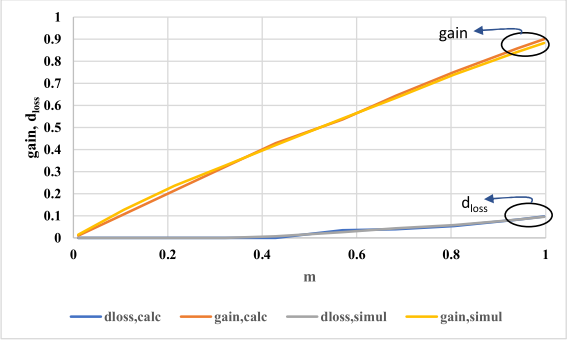

FIGURE 8. Comparison of gain and duty loss between calculation and simulation according to the m.

IV. DESIGN PARAMETERS

As shown in Fig. 5, the amount of charging and discharging of capacitors C_{dc1} or C_{dc3} during a half cycle is determined by the magnitude and duration of I_{LS}. The durations during which the capacitors are charged or discharged correspond to d_{E_X} and d_{2E_X}. A current of 1/3· I_{LS} during d_{E_X} and a current of 2/3· I_{LS} during d_{2E_X} discharges the capacitor C_{dc1}. Therefore, the required input capacitance C_{dc} satisfying the allowable voltage deviation $\Delta V_{dc,target}$ of the input capacitor during a half cycle can be determined as (17).

$$C_{dc} = \frac{1}{\Delta V_{dc,target}}\left[\begin{matrix} \frac{2}{3}\cdot\frac{i_{LS}(t_2) + i_{LS}(t_3)}{2}\cdot d_{2E}\frac{T}{2} \\ +\frac{1}{3}\cdot\frac{i_{LS}(t_3) + i_{LS}(t_0)}{2}\cdot d_E\frac{T}{2} \end{matrix}\right]$$

$$= \frac{1-m}{4nf_{sw}\Delta V_{dc,target}} \cdot\left[2I_O - \frac{T}{2L_O}\left\{\begin{pmatrix} -\frac{2}{3}m^2 + d_{loss}^2 - md_{loss} \\ -\frac{1}{3}m + \frac{2}{3}d_{loss} + \frac{1}{3} \end{pmatrix}\cdot\frac{V_{dc}}{n} \right\}\right.$$

$$\left. + \left(-\frac{2}{3} + \frac{4}{3}m\right)V_O\right] \tag{17}$$

On the other hand, the net incremental charge Q of the output capacitor C_O can be calculated as (18) by integrating

the $I_{LO}-I_O$ during the time between t_S and t_E, the intersection where I_{LO} and I_O meet in Fig 5. Then dividing Q by the allowable voltage deviation of output capacitor, $\Delta V_{O,target}$, the required output capacitance C_O can be computed as (19).

$$\begin{aligned} Q &= \int_{t_S}^{t_E} (i_{LO}(t) - I_O)dt \\ &= \frac{t_2 - t_S}{2} \times \frac{V_{dc}/n - V_O}{L_O} \times (t_2 - t_S) \\ &\quad - \frac{d_{2E}\frac{T}{2}}{2} \times \frac{2V_{dc}/3n - V_O}{L_O} \times d_{2E}\frac{T}{2} - \frac{t_E - t_3}{2} \\ &\quad \times \frac{V_{dc}/3n - V_O}{L_O} \times (t_E - t_3) \end{aligned} \tag{18}$$

$$\begin{aligned} C_O = &\frac{1}{24nL_O\Delta V_{O,target}f_{sw}^2} \\ &\times \left[\begin{array}{c} \frac{\{V_{dc}(-2m^2+3d_{loss}^2-3md_{loss}-5m+3d_{loss}+4)+nV_O(9m-6)\}^2}{12(V_{dc}-nV_O)} \\ -\frac{\{V_{dc}(-2m^2+3d_{loss}^2-3md_{loss}-m+3d_{loss})+3nmV_O\}^2}{4(V_{dc}-3nV_O)} \\ -(2V_{dc}-3nV_O)\cdot(1-m)^2 \end{array} \right] \end{aligned} \tag{19}$$

V. SIMULATIONS AND EXPERIMENTS

A. SIMULATIONS

To verify the feasibility of the proposed converter, several simulations were performed under the conditions listed in Table 1.

TABLE 1. Simulation conditions.

P_O(W)	V_{dc}(V)	V_O(V)	L_S(mH)	L_O(mH)
500	700	350	1.5	3
C_{dc}(μF)	C_O(μH)	n	f_{SW}(kHz)	
100	11	1.5	10	

Figs. 9 and 10 show the simulation results in steady state of the proposed symmetric switching converter for $m = 0.9$ and $m = 0.45$, respectively. From top to bottom, they are *GateA*, *GateB*, V_{dc1}, V_{dc2}, andV_{dc3}, I_{LS}, I_{DO} and I_{LO}, V_{AB} and V_{Lm}, V_O, I_{A_upper}, I_{A_lower}, I_{DCA}, I_{B_upper}, I_{B_lower}, I_{DCB}. It can be seen that the overall operating characteristics are consistent with the above steady-state operation analysis results. Because the proposed converter is designed based on the end sag type, unique gate signals corresponding to end sag can be found depending on the CM [30]. When the polarity of V_{cmd} is changed, a soft commutation period occurs, and the shape of the I_{LS} and I_{LO} changes smoothly according to the step voltages. When V_{cmd} belongs to LVR, the form of step leg voltage changes in the order of 3→2→1, and when it belongs to SVR, the form of step leg voltage changes in the order of 2→1→0. All primary side switches are turned on with ZVS condition and secondary side diodes are turned off by ZCS condition.

As shown in Fig. 11, it can be noted that the currents of phases A and B are symmetrical to each other. Unlike the existing PSFB, a symmetrical current pattern can be seen without distinction between leading and lagging legs. That is why this converter topology is named symmetric switching converter. Due to the additional powering period following the main powering period, the reduced circulating current of the proposed converter can be expected.

Using PLECS' heat loss modeling method, the losses of the switching elements are analyzed in Fig. 12 for an output power of $P_O = 500$W. The analysis was conducted using the actual datasheet of the device referenced in the subsequent Experiments section. The calculation conditions are as shown in Table 1. The thermal resistances and capacitances were set so that the temperature of the heat sink was saturated at 80°C in steady state. Here, $P_{cond,Q}$ represents the conduction losses of the main switches, and $P_{SW,Q}$ represents the switching losses of the main switches. $P_{cond,CD}$ and $P_{SW,CD}$ denote the conduction and switching losses of the clamping diodes. Finally, $P_{cond,OD}$ and $P_{SW,OD}$ are the conduction and switching losses of the output diodes. Switching losses and conduction losses for these switches and diodes are determined using the thermal modeling method within PLECS software. This calculation relies on interpolation and considers operating conditions like on-state current, blocking voltage, and internal device temperature, following the lookup table established from pre-defined electrical specifications of the device.

The switching losses of the main switches were the largest as 24W, followed by the conduction losses of the output diodes as 2.7W and the conduction losses of the main switches as 2.6W. The total loss is about 30W, which corresponds to an expected efficiency of 94%.

B. EXPERIMENTS

To check and verify the operating characteristics and effectiveness of the proposed converter, several experiments were conducted under the same conditions in Table 1. The experimental prototype circuit including DSP, DC-link capacitors, FB switching stack, input and output voltage sensing parts, L_S, L_O and T_X is shown in Fig. 13. The main switches are FGW35N60HD, the clamping diodes are STTH15RQ06-Y, and the output diodes are VS-HFA06TB120S-M3. The center-tapped transformer has three stacked ferrite cores of EE7166S with a turn ratio of 42:28:28. The L_S consists of two stacked ferrite cores of EE4242S with 41 turns. The L_O is made of ferrite core EE6565S with 98 turns. All magnets have air gaps to prevent saturation. The controller was implemented using TMS320F28377D.

Fig. 14 shows the operational waveforms of proposed converter at $P_O = 500$W, 750W, and 250W. It can be seen that the CM alternates every cycle for voltage balancing, and leg voltages change accordingly. Except for parasitic resonances due to parasitic components in transformer winding and circuits, the waveforms of the I_{LS} and I_{LO} agree with the theoretical analysis in Fig 5. From negative values of I_{LS}, ZVS behavior can be observed in all power ranges. Fig. 15 shows the dynamics of voltage balancing when P_O changes from 250W to

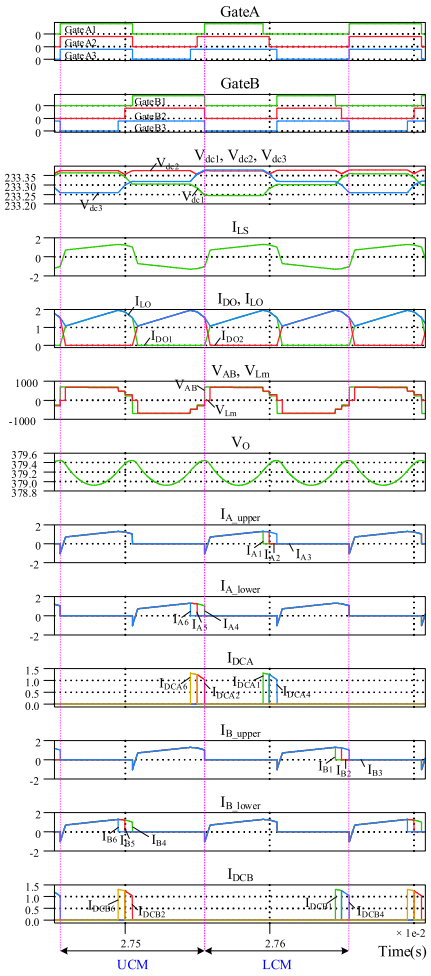

FIGURE 9. Simulation results for m = 0.9.

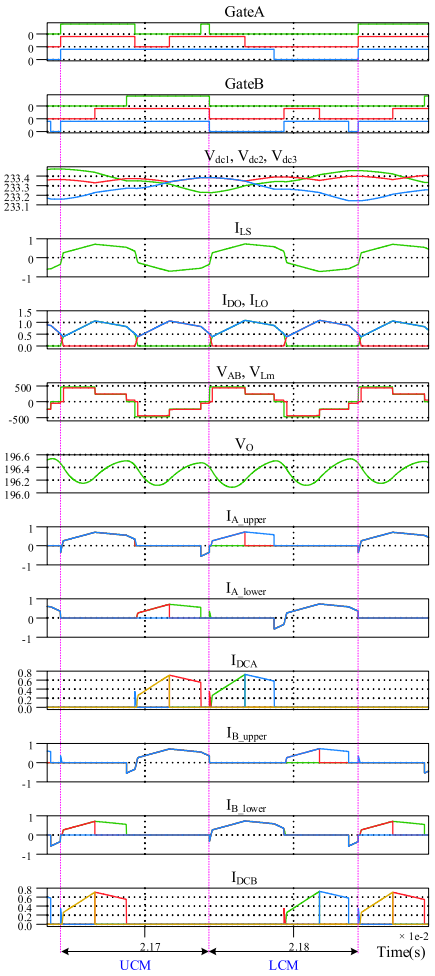

FIGURE 10. Simulation results for m = 0.45.

750W. The DC-link voltages (V_{dc1}, V_{dc2}, and V_{dc3}) maintain a value of $V_{dc}/3$ and are well balanced even with sudden load changes. Fig. 16 shows the load regulation performance when P_O changes from 250W to 750W. The output voltage is well controlled within 45V during transients.

Fig. 17 shows the measuring result of power conversion efficiency η when P_O changes from 250W to 750W using Yokogawa's WT5000 power analyzer. η was calculated as P_O/P_{in}, where P_{in} is product of $V_{dc,rms}$ and $I_{dc,rms}$, and P_O is product of $V_{O,rms}$ and $I_{O,rms}$. At $P_O = 250$W, the η was 91.44%, and as the load increased, the η increased gradually, and the maximum η was measured as 95.23% at $P_O = 750$W.

VI. ADVANTAGES OF THE PROPOSED CONVERTERS

To compare and validate the competitiveness of the proposed converter, we conducted a comparison with existing representative isolated multilevel DC/DC converters in Table 2. Well-known multilevel converters in the literature include the ISOP-structured modular converter [22], [23], [24], [25], the cascaded modular converter [26], [27], and MMC [5], [28], [29].

In the case of ISOP/cascaded converters, to handle high input voltage levels, they are configured with several sub-modules arranged in an input series and output parallel format, based on a two-level isolated converter structure. To operate at relatively high switching frequencies, they have been modularized using low breakdown voltage devices with low $R_{ds,on}$ and fast switching characteristics. Consequently, the number of input switches increased according to the number of sub-modules, and the number of output diodes or switches also increased. The ISOP converter incorporates passive elements such as inductors and transformers within each sub-module. The cascaded method offers the advantage of reducing the number of passive elements by connecting the structure of the input switching stack in a cascading manner. However, it still maintains a parallel structure on the output side, resulting in an increase in the number of transformer output windings. MMCs consist of multiple individual sub-modules connected in series. Each sub-module typically contains one or more power semiconductor devices along with capacitors. MMCs offer excellent waveform quality with low harmonic distortion. This is important in high-power

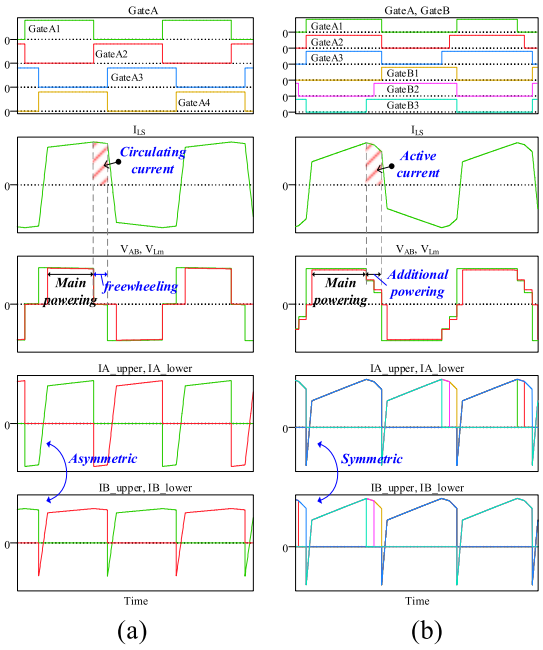

FIGURE 11. Comparison between (a) conventional two-level PSFB converter and (b) proposed four-level symmetric switching converter.

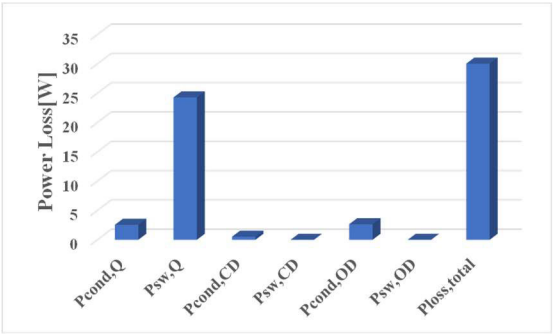

FIGURE 12. Losses analysis results when $P_O = 500W$.

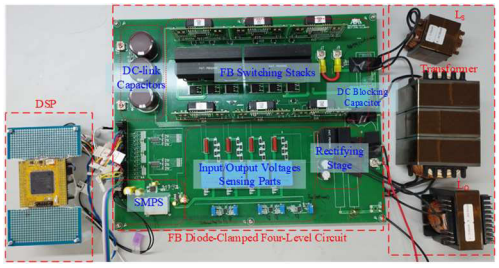

FIGURE 13. Prototype circuit.

applications to minimize interference with the power grid and reduce losses in the connected equipment.

While the ISOP, cascaded, and MMC converter structure boasts high scalability, allowing for flexible adjustment of the number of modules to match the system's capacity, it necessitates a large number of passive components and requires advanced voltage balancing control for each sub-module.

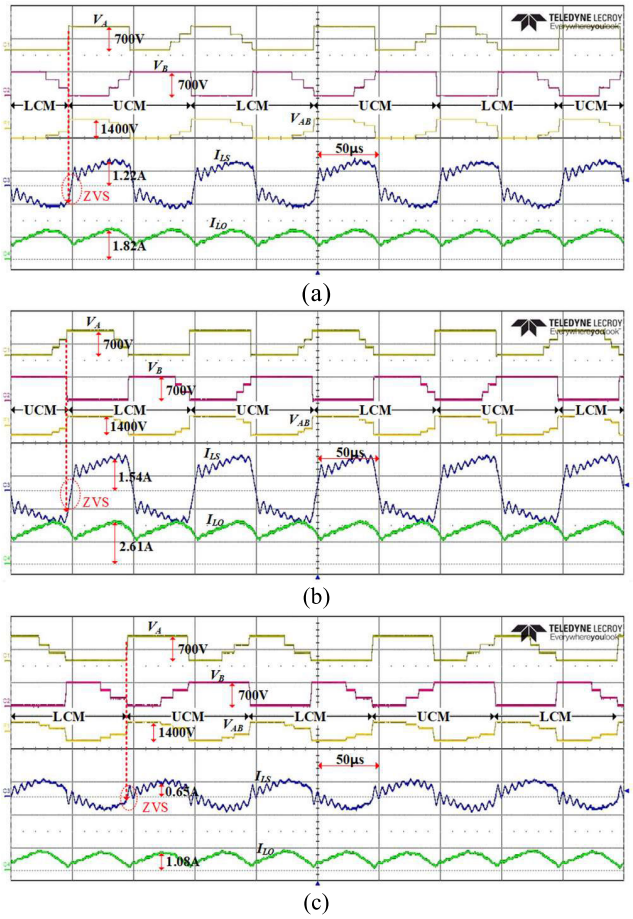

FIGURE 14. Operational waveforms when (a) $P_O = 500W$, (b) $P_O = 750W$, and (c) $P_O = 250W$.

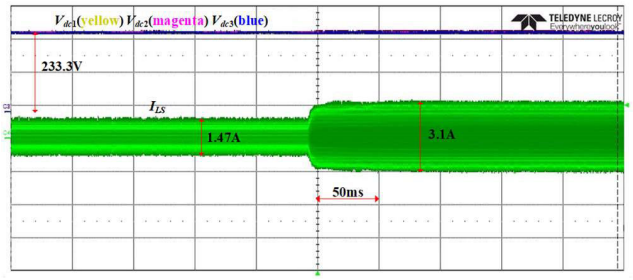

FIGURE 15. Dynamic voltage balancing performance when P_O changes from 250W to 750W.

Furthermore, there is a method of handling high input voltage based on a two-level topology using recently developed high-voltage SiC devices [40], [41]. This configuration, based on the well-known two-level topology, offers the advantage of significantly reducing the number of components compared to other methods. However, these devices are still under development at the laboratory level, are prohibitively expensive, and are not readily available in the market. Additionally, due to the requirement for a single switch to handle very high voltages, it leads to high EMI and imposes limitations on switching frequency.

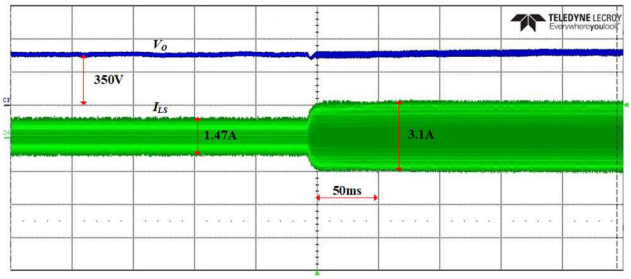

FIGURE 16. Load regulation performance when P_O changes from 250W to 750W.

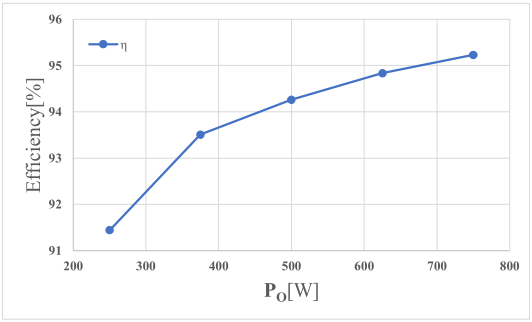

FIGURE 17. Power conversion efficiency (=P_o/P_{in}).

TABLE 2. Comparison of isolated multilevel dc/dc converters.

	ISOP Converter [22]–[25]	Cascaded Converter [26, 27]	MMC [5], [28, 29]	Proposed Converter
# of primary switches	Large	Large	Large	Large
# of secondary diodes (switches)	Large	Large	Small	Small
# of clamping diodes	-	-	-	Large
# of passive components	Large	Medium	Large	Small
Advantages	Modularity/ High power handling capability	Modularity/ High power handling capability/ Reduced harmonics	Modularity/ Bidirectional power flow/ High power handling capability/ High power quality	Simple power configuration (single DC source)/ High power density/ Embedded DC balancing algorithm
Disadvantages	Many passive components/ Separated DC balancing algorithm	Many isolated DC sources/ Separated DC balancing algorithm	Many capacitors/ Separated DC balancing algorithm (Sorting algorithm)	Many clamping diodes/ Scalability

In contrast, the proposed method employs a simple input power supply configuration based on a diode-clamped circuit and achieves high power density by utilizing only one set of passive elements. However, owing to the characteristics of the diode-clamped circuit, the number of clamp diodes increases rapidly with the increase in the multilevel order, resulting in a somewhat complex circuit configuration. Modularization is also more challenging when compared to the ISOP or cascading methods. On the bright side, the voltage balancing algorithm is already integrated into the implementation of the PWM switching pattern, eliminating the need for separate voltage balancing efforts. Moreover, the issue of the large number of clamp diodes in the FB topology can be mitigated by applying the HB method, reducing it by half [34].

The proposed converter offers several advantages over existing resonant converters or PSFB converters. In comparison to resonant converters that rely on trigonometric values [30], [31], the voltage transfer gain in the proposed converter is directly proportional to 'm', simplifying the design and tuning of controller parameters. While resonant converters often face the challenge of requiring a large circulating current and low 'L_m' to meet ZVS conditions, the proposed converter is not constrained by this requirement, allowing for the suppression of circulating current by designing 'L_m' to be large. Additionally, the proposed converter effectively mitigates the circulating current typically associated with the freewheeling section in conventional PSFB converters by introducing an additional powering section in the voltage drop section following the main powering section. This reduction in current flow through switches and magnetic components contributes to its advantages.

VII. CONCLUSION

In this paper, we propose a novel FB diode-clamped four-level symmetric switching converter based on MNRV DPWM. The proposed converter operates in the PAM method with fixed switching frequency. Through the HB-based symmetric switching method, the switching modulation design scheme in the proposed FB topology was easily implemented through the offset voltage addition method. In this study, we have described MNRV DPWM design rules with offset voltage addition and have proposed appropriate control algorithms. A detailed analysis of the operating characteristics of the proposed converter is presented, including voltage transfer gain, ZVS conditions, and circuit design parameters. Furthermore, the proposed converter underwent a comparative analysis with existing representative isolated multilevel converters to validate its effectiveness and competitiveness. The results of this comparison revealed that, while the proposed converter exhibits lower modularity and a somewhat complex circuit configuration when compared to the existing ISOP, cascade-type converters, and MMCs, it offers the distinct advantages of enhancing the power density due to the reduction of passive components and streamlining the power supply configuration. Moreover, the DC-link voltage balancing control is inherently integrated into the PWM switching control, eliminating the need for an additional balancing control algorithm. Furthermore, when compared to existing resonant and PSFB converters, the proposed converter stands out for its simplified controller design and reduced circulating current. The feasibility and effectiveness of the proposed converter were verified through simulations and experiments on a 500W prototype circuit. The proposed converter can be applied in power conversion systems with high input voltage

requirements, such as DC/DC converter stations between MVDC-to-LVDC, electric vehicle (EV) charger, and railway vehicle propulsion systems. The proposed method can also be extended to HB-based multiphase systems consisting of three or more phases by utilizing offset voltage addition methods. As future work, our research plans aim to investigate diode-clamped multilevel multiphase topologies employing MNRV PWM.

APPENDIX

Below we show the source codes for calculating the PWM command values of the proposed symmetric switching converter.

```
Vcmd_A = Vcmd/2;
Vcmd_B = -Vcmd/2;

if (CM== 1) Voffset = 0.5*Vdc - max(Vcmd_A, Vcmd_B);
else Voffset = -0.5*Vdc - min(Vcmd_A, Vcmd_B);

VCMD_A = Vcmd_A + Voffset + 0.5*Vdc;
VCMD_B = Vcmd_B + Voffset + 0.5*Vdc;

//X=A or B
if (VCMD_X <= 0.5*Vdc) CMD_region_X = 2;
else CMD_region_X = 1;

if (CMD_region_X == 1)
{
    if (VCMD_X == Vdc)
    {
        PWM_CMD_X1 = PWM_CMD_X2 = PWM_CMD_X3 = N_max;
    }

    else

    {
        dE_X = -VCMD_X/Vdc - CM*dcomp_1_23/3 + 1.;
        d2E_X = dE_X + CM* dcomp_1_23;
        d3E_X = 1 - dE_X - d2E_X;

        PWM_CMD_X1 = N_max*d3E_X;
        PWM_CMD_X2 = N_max*(d2E_X + d3E_X);
        PWM_CMD_X3 = N_max;
    }
}

if (CMD_region_X == 2)
{
    if (VCMD_X == 0)
    {
        PWM_CMD_X1 = PWM_CMD_X2 = PWM_CMD_X3 = 0;
    }

    else
    {
        d2E_X = VCMD_X/ Vdc - CM*dcomp_12_3/3.;
        dE_X = d2E_X + CM*dcomp_12_3;
        d0_X = 1 - dE_X - d2E_X;

        PWM_CMD_X1 = 0;
        PWM_CMD_X2 = N_max*d2E_X;
        PWM_CMD_X3 = N_max*(dE_X + d2E_X);
    }
}
```

They consist of dividing V_{cmd} into V_{cmd_A} and V_{cmd_B}, calculating V_{offset} according to CM, adding $0.5V_{dc} + V_{offset}$, distinguishing the positions of command values V_{CMD_A} and V_{CMD_B}, calculating duties of reference vectors, and generating PWM_CMDs. Codes that are common to either the *A* or *B* legs are denoted together by the symbol X.

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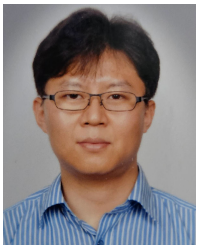

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