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RESEARCH ARTICLE

Optimal Inductor Design Method for GaN-Based PFC

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ABSTRACT The main theme of this paper is to propose an optimal inductor design method for GaN-based PFC. The proposed method is developed based upon the minimization of PFC total losses, which include copper losses, core losses and switching losses of power devices. A systematic design flow chart is proposed to give the optimal turn number and stack number subject to the window area of core and minimization of PFC total losses. The proposed optimization design method is confirmed by analysis results first and then simulation results using ANSYS®. The designed optimized inductor is applied to a GaN-based 1.5 kW Totem-pole PFC for server power and the experimental results show the peak efficiency goes up to 97.5% and 99%, under 115V and 264V of input voltage, respectively. The results fully support the effectiveness of the proposed optimization design method.

INDEX TERMS Totem pole PFC, inductor design, core losses, copper losses, switching losses.

I. INTRODUCTION

It is well known that the performance indexes for high performance two-stage server power include efficiency, size and cost, to give high power density. The two-stage server power consists of the PFC front end and the DC- DC stage. The two-stage efficiency of 94% under 50% load is required by 80 PLUS Titanium efficiency code [1] for 115Vac input voltage. To meet this code, the efficiency for PFC front-end stage should be higher than 97% if the efficiency for DC-DC stage is 97%.

Several PFC topologies [2], [3], [4], [5], [6] have been proposed to meet the concerns, including efficiency and components count. The related component counts for different topologies are summarized in [7]. As presented in [7], the Totem-pole (TTP) PFC topology shown in Fig. 1, is recommended for higher efficiency concern. This topology requires less power devices in the magnetizing and demagnetizing current paths, leading to reduced conduction losses inherently. It utilizes two high frequency power devices (typically wide band gap device) that operate at high switching frequency. Additionally, it employs two low frequency power devices (generally MOSFET) that operate at the line frequency with almost no switching action. As a result, this topology only requires two switching power devices, thereby minimizing switching losses.

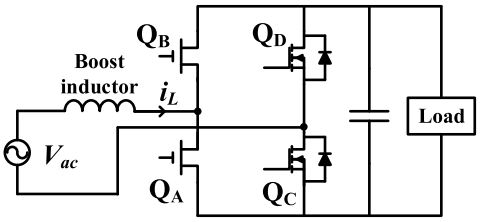

FIGURE 1. Totem-pole PFC.

Moreover, the power devices and boost inductor in PFC contributes to the losses relevantly. More recently development of wide band gap devices, including Silicon Carbide MOSFETs and GaN MOSFETs are used due to low switching losses, especially turn-off losses [8], [9], [10]. For the design of PFC, inductor design is a degree of freedom when the power devices and topology are selected.

For conventional approaches to inductor design includes Area-Product (A_P) and geometric constants (K_g and K_{gac}) [11], [12]. However, these methods require predefined parameters such as maximum flux density (B_{max}) and current density (J). In [13], the inductance is determined based upon

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current ripple. However, the current ripple is decided without any optimization performance index. In [14], [15], and [16] the summation of core and copper losses is considered as the optimization index for the inductor design to reduce the thermal impact.

However, it is important to note that the working point of an inductor vary based on the input voltage for PFC applications. As a result, the inductor ripple current at each working point gives not only the core and copper losses but also the switching losses of the power devices. In [14], [15], and [16], only copper and core losses at a **single working point** are considered. The switching losses are not considered for inductor design in [14], [15], and [16], neither.

Table 1 provides a summary of various inductor design approaches [12], [16], [17], [18], [19], including their power ratings, efficiencies, power device losses, copper losses, core losses, DC bias, inductor volume, and current non-linearity. However, it is worth noting that none of these approaches considers all of these factors comprehensively for the design of inductor.

This paper expands upon the findings presented in [20] and more details of the optimized inductor design is included in this paper. An optimal inductor design method for GaN-based PFC is proposed in this paper. The proposed method is developed based upon the minimization of PFC total losses, which include copper losses, core losses and switching losses of power devices at six working points in a quarter fundamental period. A systematic design flow chart is proposed to give the optimal turn number and stack number subject to the window area of core and minimization of PFC total losses. The proposed optimization design method is confirmed by analysis results first and then simulation results using ANSYS®. The designed optimized inductor is applied to a GaN-based 1.5 kW Totem-pole PFC for server power and the experimental results show the peak efficiency goes up to 97.5% and 99%, under 115V and 264V of input voltage, respectively.

This paper is divided into five sections. Section II introduces loss calculation of inductor and power device for the continuous conduction mode (CCM) PFC. Section III presents the proposed efficiency-optimized inductor design based on the minimization of PFC losses. In Section IV, simulation and test results for of the proposed optimized inductor design method are presented. Finally, Section V gives the conclusions of the study and summarizes the key contributions of this paper.

II. LOSS CALCULATION OF INDUCTOR & POWER DEVICES

Figure 2 shows the loss map of a PFC, including the inductor and power device losses. It is well known that the inductance value of PFC will affect the input current ripple under CCM. The more the inductance value is, the less the ripple will be. The fundamental component of the PFC current depends on the ac voltage and the power delivered, but not from the inductance. Therefore, the conduction losses of power devices is not included in the analysis of this paper.

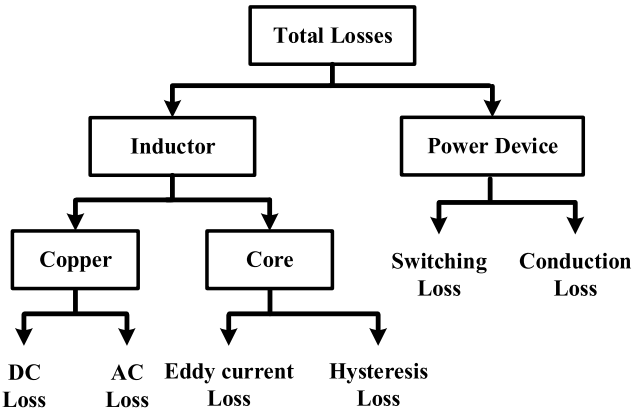


FIGURE 2. Loss map of PFC.

The calculation of core and copper losses of inductor, as well as switching losses of power devices will be presented in this section for the development of the proposed inductor design method to follow.

A. COPPER LOSSES

Both AC and DC losses of copper are considered as shown in (1). The DC copper losses is calculated by multiplying the square of the RMS current with the winding's DC resistance [12]. In contrast, the AC copper losses is dominated by the high frequency current harmonics which can be derived by Fourier analysis results of inductor current as shown in (2). In this paper, up to 11^{th} harmonics of switching frequency are considered and the higher order harmonics are not considered for the trivial contributions. The AC resistance is formulated in (3) [21]. The equivalent N_l layer in (3) is derived by (4), and the maximum turn number $N_{max,Nl}$ in (4) can be found in (5) [19].

Both skin effect and proximity effect contribute to AC copper losses. For the inductor with Litz wire, the skin effect on AC copper losses is reduced.

$$P_{copper} = I_{L,rms}^2 R_{dc} + \sum_{n=1}^{\infty} \left(\frac{I_{L,rms,n}}{p}\right)^2 R_{ac,np} \tag{1}$$

$$i_L(t) = I_{avg} + \sum_{n=1}^{\infty} \frac{\Delta i_L \sin(n\pi D)}{n^2\pi^2 D(1-D)} \sin(n\omega t) \tag{2}$$

$$R_{ac,n} = \left(\frac{4}{\pi}\right)^{\frac{1}{4}} l_T \left(\frac{\rho\mu\pi n f_{sw} \times 10^3}{ds}\right)^{\frac{1}{2}} \left[1 + \frac{2(N_l^2 - 1)}{3}\right] \tag{3}$$

$$N_l = \begin{cases} \dfrac{N}{N_{max,1}}, \text{for} N \le N_{max,1} \\ 1 + \dfrac{N - N_{max,1}}{N_{max,2}}, \text{for } N_{max,1} < N \\ \qquad \le (N_{max,1} + N_{max,2}) \\ \vdots \end{cases} \tag{4}$$

$$N_{max,N_l} = \pi \left(\frac{I.D}{dia._{eff}} - (2N_l - 1)\right), \quad \text{for } N_l = 1, 2\ldots \tag{5}$$

TABLE 1. Survey results for inductor design papers.

Comparison Items	[12]	[16]	[17]	[18]	[19]	Proposed
input/output voltage	5 Vdc 5.45 V_{p-p}	300 Vdc 630 V_{p-p}	75 Vdc 150 Vdc	220 Vac 390 Vdc	187 Vac UNK Vdc	Universal 400 Vdc
output power	10 W	16.5 kW	600 W	3.2 kW	3 kW	1.5 kW
switching frequency	250 kHz	100-350 kHz	40 kHz	50-70 kHz	Not available	65 kHz
volume	Y	Y	N	Y	Y	Y
power device losses	N	N	N	Y	N	Y
copper & core losses	Y	Y	Y	Y	Y	Y
DC bias	N	Y	Y	Y	Y	Y
current non-linearity	N	N	Y	N	N	Y
stack core	N	N	Y	N	N	Y
topology	Inverter	Four-phase Boost converter	DC/DC Boost Converter	Semi-Bridgeless PFC	Three-Level Bridgeless PFC	Totem Pole PFC
peak efficiency	93%	97.2%	97.3%	98.2%	Not available	99%
optimized index	Volume	inductor losses	smooth efficiency curve	inductor losses	inductor losses	Optimal *converter* losses
design approach	AP method	Numbers of turns	different core material	inductance	inductance	Numbers of cores & turns (winding)

where, n: order of harmonics, p: strand number of winding, Δi_L: current ripple (A), D: duty cycle, l_T: winding length (cm), ρ: conductivity of copper (Ω·cm), μ: permeability of copper (H/cm), f_{sw}: switching frequency (kHz), d: diameter of single wire (cm), s: distance between windings (cm), $N_{max,Nl}$: maximum turn can be wounded in each layer, N_l: number of a certain layer of the winding, $I.D$: inner diameter of core (cm), $dia_{.eff}$: equivalent diameter of winding (cm)

B. CORE LOSSES

Powder core has a characteristic that their permeability varies non-linearly under different DC bias conditions [22]. This variation in permeability can result in significant change in inductance and inductor ripple current. Particularly under high DC bias condition, this non-linear behavior can lead to larger ripple current during heavy load operation and complicate the estimation of core losses. Many methods have been proposed in previous literature to estimate core losses [23], [24], [25], but most of them focus on a specific operating point by ignoring the non-linear behavior. The Steinmetz Equation (SE) with parameters from the powder core datasheet has been widely adopted to consider the non-linear behavior.

The core losses include by eddy current loss and hysteresis loss. Since the radius of powder particles is smaller than the skin depth in general, the eddy current loss can be neglected as addressed in [26]. As shown in [27], the hysteresis loss based upon Steinmetz Equation (SE) for the square wave excitation signal is shown by (6). The core losses are therefore calculated by (6) and denoted by $P_{core,square}$.

$$P_{core,square} \approx C_m \left[\frac{B_{pk}^{y} T_{ON}}{(2T_{ON})^{x} T_{sw}} + \frac{B_{pk}^{y} T_{OFF}}{(2T_{OFF})^{x} T_{sw}} \right] V_e SN \tag{6}$$

where, C_m, x, y are Steinmetz parameters from the datasheet of core, T_{sw}: switching period (s), T_{ON}: magnetizing time (s), T_{OFF}: demagnetizing time (s), V_e: volume of core (cm^3), SN: stack core number.

In (6), B_{pk} = Half variation of flux density (Tesla) = 0.5 ΔB which denotes the variations of flux density (Tesla). Figure 3 shows the B-H curve in the first quadrant to explain the relationship among B_{pk},ΔB and inductor current. As shown in Fig. 3, smaller inductance gives larger current ripple which results in the bigger B_{pk} and ΔB. The core losses will be increased as shown in (6). In contrast, the larger inductance which requires more turns (N), will reduce the current ripple and thereby providing smaller B_{pk} and ΔB. The core losses shown in (6) is reduced, however, it is important to note that more turns comes with larger copper losses.

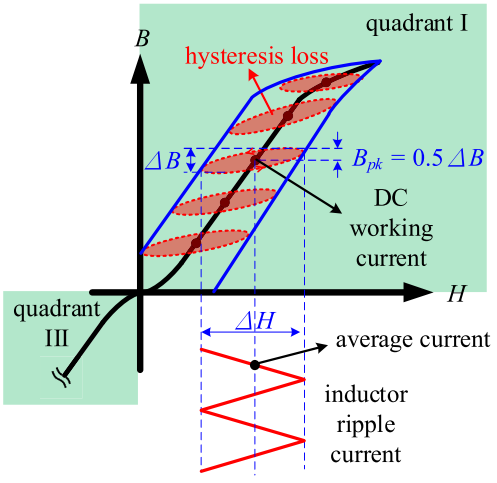


FIGURE 3. B-H curve, the relationship among B_{pk}, ΔB and inductor current.

Therefore, the optimal solution to the minimization of both core and copper losses will be investigated in this paper.

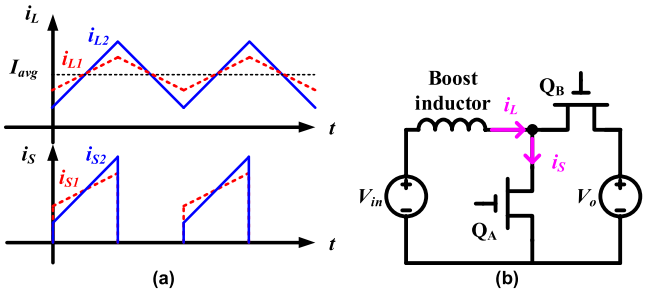


FIGURE 4. Totem-pole PFC (a) inductor current i_L and power device current i_S (b) equivalent circuit of TTP PFC at positive cycle.

C. IMPACT OF INDUCTOR ON SWITCHING LOSSES

Figure 4 shows the currents of PFC for inductor with different inductance. As shown in Fig. 4, the current ripple increases for the inductor with smaller inductance, $\Delta i_{L2} > \Delta i_{L1}$ for $L_2 < L_1$. Under the same load condition, *at the turn-on instant*, the current for larger inductance case is with larger turn-on current.

The switching losses are calculated by the following equation:

$$P_{switching} = (E_{ON} + E_{OFF}) f_{sw} \tag{7}$$

where, E_{ON} and E_{OFF}: turn-on and turn-off energy (J)

As shown in [28], the turn-on loss of power device is much greater than turn-off loss for GaN. Larger current at the turn-on instant results in bigger turn-on loss. More details about this relation will be shown by (22) in Section III. Therefore, reducing the inductance will decrease the turn-on loss and thereby reducing switching losses.

D. CALCULATION OF COPPER, CORE AND SWITCHING LOSSES

For PFC applications, the input current shape tracks its input voltage waveform to give high power factor. Therefore, the working points vary time by time, bringing the difficulty for loss calculation. In [27] and [29], only six points in the first quarter fundamental period are selected for loss calculation. Based upon this "six-step" loss calculation method, the input voltages of these six points are used for the loss calculation to give average losses as shown in (8).

$$P_{loss,avg} = \frac{\sum_{k=1}^{k=6} P_{loss}(k)}{6}\Big|_{in\frac{T_{line}}{4}} (W) \tag{8}$$

As shown in [27], the comparison results of "Six-step" loss calculation is shown, and the maximum error of different methods is 5.9%.

In short, for the inductor of GaN-based PFC with CCM control, DC copper losses, AC copper losses and hysteresis loss are considered. The impact of inductor on power devices, only the switching losses are focused, especially the turn-on loss for GaN power devices. Moreover, the sampled points of six-step method are used for the calculation of these core and switching losses.

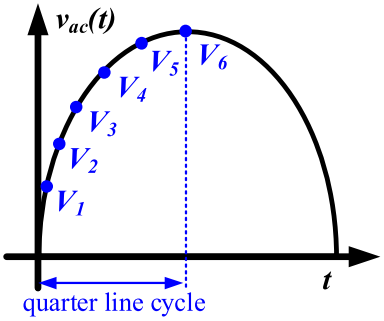


FIGURE 5. Sampled points of input voltage based-upon "Six-step" method [27], [29].

III. PROPOSED LOSS OPTIMIZATION DESIGN METHOD

A systematic design flow chart of the proposed novel efficiency optimized inductor design is shown in Fig. 6. The input parameters for the design include the winding and stack core parameters as illustrated in Table 2 using APH27P60 core as an example. The output of this design flow includes the optimal number of stack and number of turns of winding by minimization of total losses, including core and copper losses of inductor, and the switching losses of power devices.

Table 3 shows the specifications and main power device of the GaN-based PFC. The input voltage is universal, and the power is 1.5 kW. The switching frequency is operated at 65 kHz based upon EMI consideration as addressed in [18]. Transphorm GaN MOSFETs are used for power devices. The inductor design becomes one of the very essential factors to achieve such high efficiency, i.e. 97.5% and 99% under

TABLE 2. Core and winding parameters – APH27P60.

Core	APH27P60	Volume (V_e)	4.15 cm^3
Initial permeability	60	Window area (W_A)	1.56 cm^2
Outer diameter ($O.D$)	(with /without coating) 2.77/2.692 cm	Strand number (p)	10
Inner diameter ($I.D$)	(with /without coating) 1.41/1.473 cm	Wire diameter (d)	0.04 cm (AWG26)
Height ($H.T$)	(with /without coating) 1.199/1.118 cm	Cross-sectional area of wire (W_c)	0.129×10^{-2} cm^2 (AWG26)
Magnetic path length (l_e)	6.35 cm	Winding factor (K_u)	0.3-0.4
Cross-sectional area of core(A_e)	0.654 cm^2	Max. turns (N_{max})	35-49

TABLE 3. TTP PFC specifications.

Items	Specification
Power Rating	1.5 kW
Input Voltage	Universal, 90V-264 V
Output Voltage	400 Vdc
Efficiency @ 115 V	97.5% @ peak efficiency
Efficiency @ 264 V	99% @ peak efficiency
Switching Frequency	65 kHz
Main Power Device	TP65H035WS

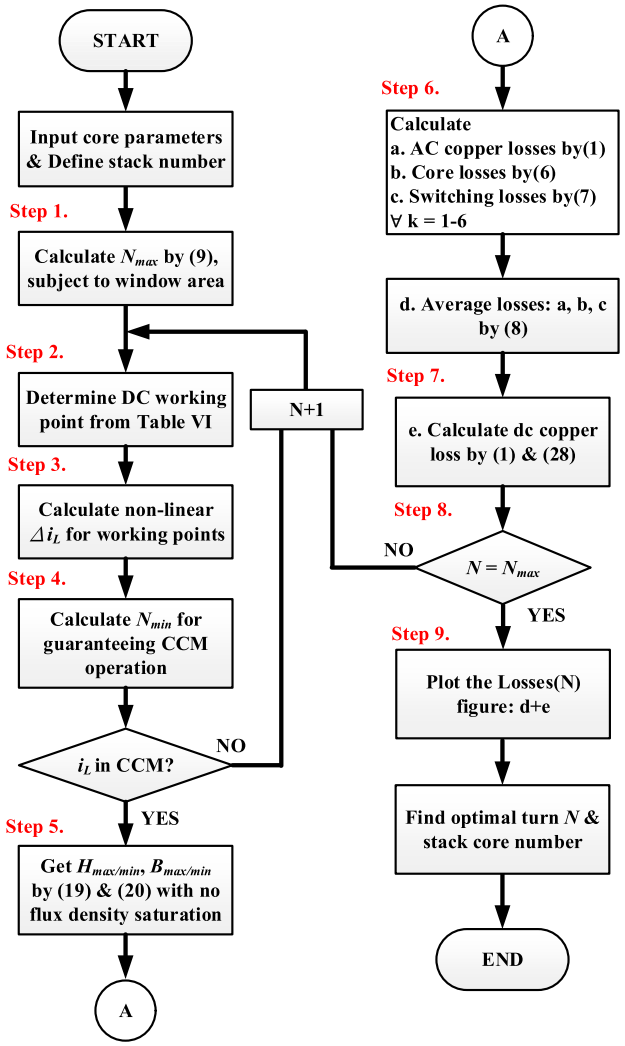


FIGURE 6. Flow chart of the proposed efficiency optimized inductor design.

115V and 264 V, respectively. Therefore, a novel efficiency optimized inductor design, which is aimed to optimize the *converter* losses, is presented.

Step 1. Calculate the maximum turn number, N_{max}

In this paper, the core size with an outer diameter of 2.7 cm (OD270) is selected for meeting the height specification of 1U rack server power [30]. Once the core for the inductor is determined, the maximum turn number, N_{max}, can be calculated using (9) which takes into account factors of the winding factor (K_u), the window area (W_A), the number of strands in parallel (p), and the cross-sectional area of the wire (W_c).

$$N_{\max} = \frac{K_u W_A}{p W_c} \tag{9}$$

Step2. Determine six DC working points

For the powder core, the DC working points of voltage and current in quarter period can be calculated by (10) and (11) to consider the variation of inductance. Under CCM condition, the six DC working points of both voltage and current in quarter period can be calculated as summarized in Table 4. The turn-on time can be calculated by the voltage boost ratio formula as shown in (12) and the results are presented in Table 4.

$$i_{Lk}(k)\Big|_{k=1}^{k=6} = I_{pk}\sin(\omega_{line}\frac{T_{line}}{4}\frac{k}{6}) \tag{10}$$

$$V_{ack}(t)\Big|_{k=1}^{k=6} = V_{acpk}\sin(\omega_{line}\frac{T_{line}}{4}\frac{k}{6}) \tag{11}$$

$$T_{ON} = \frac{V_o - |V_{ac}|}{V_o} T_{sw} \tag{12}$$

TABLE 4. Working point conditions in different interval.

Interval number	Working voltage under magnetization (V_{ack})	Working current (i_{Lk})	Turn-on time (T_{ON})
k=1	42 V	5 A	13.8 µs
k=2	81 V	9.67 A	12.3 µs
k=3	115 V	13.69 A	11 µs
k=4	140 V	16.77 A	10 µs
k=5	157 V	18.72 A	9.4 µs
k=6	162.63 V	19.4 A	9.2 µs

Step 3. Calculate current ripples for each working points as DC bias is considered

Since the inductance values are affected by the current, the current ripple is thus changed as the working points of current vary. To give more practical loss consideration, DC bias is considered. This feature is also reflected by the permeability curve as shown in Fig. 7, which is measured with single core and $N = 49$. For a specific working point of current, the permeability formula can be derived by curve-fitting using a six-order polynomial as shown in (13).

$$\mu_r = a_6H^6 + a_5H^5 + a_4H^4 + a_3H^3 + a_2H^2 + a_1H + a_0 \tag{13}$$

where a_6 = -2.3e-15, a_5 = 7.7e-11, a_4 = -7.2e-8, a_3 = 2.46e-5, a_2 = -3.12e-3, a_1 = -0.123, a_0 = 60.84

In general, constant inductance, which gives linear current as shown in Fig. 8 (a), is used for core losses calculation [13]. In reality, non-linear current ripple occurs which is contributed by the DC-bias of inductor core. Figure 8 (b) shows the non-linear inductor current ripple. A piecewise linear segment approach [22] is used to analyze non-linear inductor current. The number of piecewise linear segment depends upon the turn-on period and the "Δt" as shown in Fig. 8 (b). For example, for the turn-on period is 13.8 μs in interval 1,

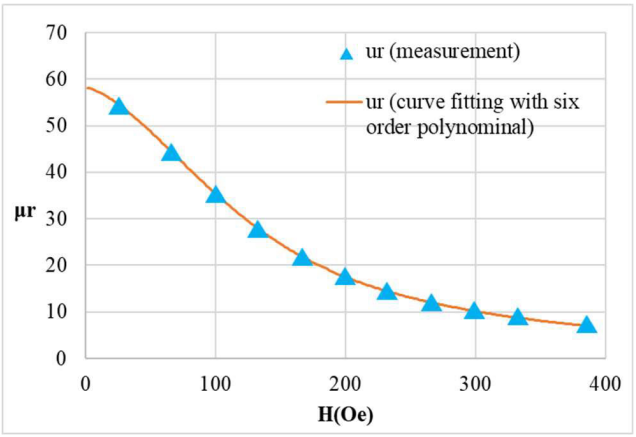


FIGURE 7. Permeability curve test with microtest impedance analyzer 6632 + DC bias system 6243.

and the "Δt" $= 0.1\ \mu$s, the number of piecewise linear segment which is used for *maximum* number of iteration for inductor current is 138.

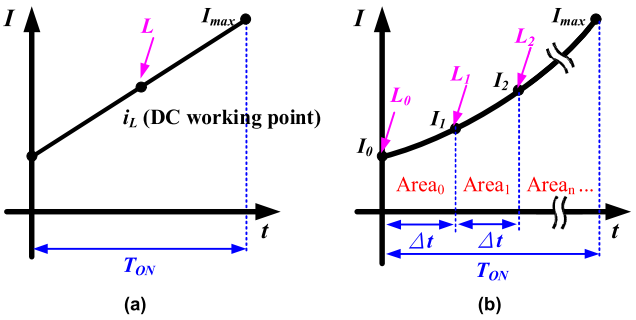


FIGURE 8. (a) Linear (b) Non-linear current ripple for a specific DC working point.

For a given stack number and the core material, the permeability is calculated by (13), the related inductance value can be derived by (14), and the linear current ripple calculation formula is showed by (15).

As the non-linearity of inductor current is considered, the current in each piecewise line segment is calculated by (16), and the non-linear current ripple is derived by (17). Notice that the DC-bias effect is reflected in the calculation of inductance, L_g. The average current in each T_{ON} can be calculated by (18).

$$L_g = \frac{\mu_o \mu_r(H_{I_g}) A_e N^2}{l_e} SN \tag{14}$$

$$\Delta i_{L,linear}(t)\Big|_{t=0}^{t=\frac{T_{line}}{2}} = \frac{V_{ac}(t) T_{ON}}{L_g} \tag{15}$$

$$I_{g+1} = I_g + \frac{V_{ac}(t)}{L_g}\Delta t \tag{16}$$

$$\Delta i_{L,non-linear}(t)\Big|_{t=0}^{t=\frac{T_{line}}{2}} = I_{\max} - I_0 \tag{17}$$

$$I_{avg} = \frac{\frac{(I_0+I_1)\Delta t}{2} + \frac{(I_1+I_2)\Delta t}{2} \ldots\ldots + \frac{(I_{\max-1}+I_{\max})\Delta t}{2}}{T_{on}} = \frac{\frac{(I_0+I_{\max})\Delta t}{2} + \sum_{g=1}^{g=\max-1} I_g \Delta t}{T_{on}} \tag{18}$$

where $g = 0, 1 \ldots \max = (T_{ON}/\Delta t)$-1

Step 4. Determine the minimum turn number N_{min} to retain CCM operation

The minimum turn number N_{min} needs to be determined to retain CCM operation in order to reduce the core losses with various stack number.

After calculating the maximum and minimum inductor currents using (17), the inductor current ripple, Δi_L, is determined. According to Table 4, the Δi_L should be less than 200% of the working current. If the calculated Δi_L exceeds this limit, it means CCM operation cannot be retained. The turn number of inductor should be increased until Δi_L is within the desired range for CCM operation. This adjusted turn number is defined as N_{min}.

For example, for interval number, $k = 6$, the working current is 19.4 A, the Δi_L, should be less than 38.8 A, accordingly. As the stack number of core = 1 and turn number of inductor winding is 34, the current ripple is 38.82 A, which is greater than twice of the working current, 38.8 A. Further increase of the turn number to give to minimum turn number of 35 turns will reduce the current ripple to meet the constraint. Similarly, the minimum turn number decreases as stack core number is increased.

Step 5. Calculate $H_{max/min}$ and Find $B_{max/min}$

The magnetic field intensity is calculated by (19) as the current is given by (17). The flux density can be derived by the B-H curve of the core as shown in (20) for APH(60μ) core which is developed based upon the B-H curve and curve-fitting results [31]. Therefore, the ΔB and B_{pk} are calculated by (21) which is used for the core losses calculation. In practice, flux saturation should be avoided and 20% of margin is retained. Once the flux density is too large, the turn number is increased to raise the inductance value and thereby reducing the current ripple and the related ΔB.

$$H_{\max/\min} = \frac{0.4\pi N I_{\max/\min}}{l_e}\ (\text{Oe}) \tag{19}$$

$$B_{\max/\min} = b_5 H^5_{\max/\min} + b_4 H^4_{\max/\min} + b_3 H^3_{\max/\min} + b_2 H^2_{\max/\min} + b_1 H_{\max/\min} + b_0 \tag{20}$$

$$\Delta B = B_{\max} - B_{\min},\ B_{pk} = 0.5\Delta B \tag{21}$$

where $b_5 = 2.2\text{e-}10$, $b_4 = -5.67\text{e-}7$, $b_3 = 5.72\text{e-}4$, $b_2 = -0.29$, $b_1 = 81.85$, $b_0 = -300.57$

Step 6. Calculate core losses, switching losses, AC copper losses and derive the average value

A. CALCULATE CORE LOSSES OF INDUCTOR

Based upon (6), the Steinmetz parameters, $C_m = 326.47$, $x = 1.29$, $y = 2.21$ for the selected core as shown in [32], and the B_{pk} which is calculated in Step 5.

B. DERIVE SWITCHING LOSSES OF GAN

Since the switching losses, E_{on} and E_{off}, depend upon the of power devices and current, for the GaN used in this paper, the switching losses under different turn on/off current are calculated by (7). E_{on} and E_{off} for the used GaN are shown in [33] which are two curves, respectively. Based upon these two curves [33], the curve-fitting results for Transphorm GaN are shown in (22) and (23), respectively. The switching losses are therefore calculated by (7) as $I_{min} = i_{S,ON}$ and $I_{max} = i_{S,OFF}$ are given.

$$E_{ON} \approx -0.0033i_{S,ON}^3 + 0.1188i_{S,ON}^2 + 2.2465i_{S,ON} + 46.147 \quad (22)$$

$$E_{OFF} \approx 0.0002i_{S,OFF}^4 - 0.0129i_{S,OFF}^3 + 0.2674i_{S,OFF}^2 - 1.8183i_{S,OFF} + 24.766 \quad (23)$$

where, $i_{S,ON}$ / $i_{S,OFF}$: switch turn-on/off current

C. CALCULATE AC COPPER LOSSES

Due to the proximity effect, R_{ac}increases as the number of winding layer increases. As shown in Fig. 9, the maximum number of turns of the N_l winding layer is derived by (4). Since Litz wires are used for winding, the equivalent diameter of winding, $dia._{eff}$, is shown in (24). For the APH27P60 core, the maximum number of turns of the first and second layer are $N_{max,1}$ =32, $N_{max,2}$ =26 by (25) and (26), the N_l can be calculated by(4). For the specified working points, the current ripple which brings high frequency current harmonics and AC losses depends upon the input voltage, duty cycle, switching frequency and inductance values. The high frequency current harmonics and AC resistance can be calculated by (2) and (3), respectively. The AC copper losses is therefore calculated by the second term of (1).

$$dia._{eff} = \left(\frac{4}{\pi}W_a p\right)^{0.5} \quad (24)$$

$$N_{max,1} = \pi\left(\frac{I.D}{dia._{eff}} - (2N_l - 1)\right) = 32, \text{ for} N_l = 1 \quad (25)$$

$$N_{max,2} = \pi\left(\frac{I.D}{dia._{eff}} - (2N_l - 1)\right) = 26, \text{ for} N_l = 2 \quad (26)$$

D. DETERMINE AVERAGE CORE LOSSES, SWITCHING LOSSES AND AC COPPER LOSSES

The average value of inductor core losses, AC copper losses and switching losses of GaN per quarter cycle is thus determined by (8) based upon the "Six-step" method [27], [29] as summarized in Section II.

Step 7. Calculate DC copper losses

As mentioned in [19], the AC copper losses is smaller as compared to the DC copper losses. Moreover, the winding length of windings, which dominate the copper resistance, are calculated by (27), respectively. The symbols, including *O.D*, *I.D*, and *H.T* with coating for the dimension are defined in Fig. 9. The equivalent DC resistance of windings is derived as shown in (28) and therefore, the DC copper losses can be calculated by the first term of (1).

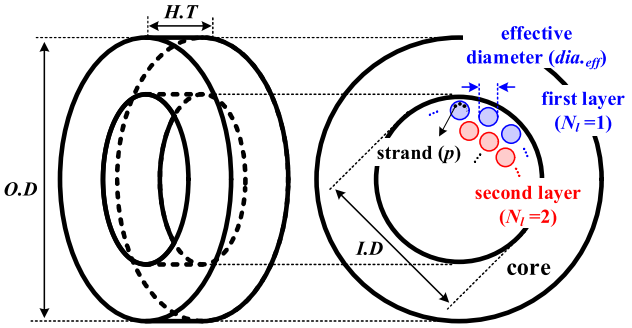


FIGURE 9. The core size definition and the copper wire distribution in core window.

$$l_T = 2\left(\frac{O.D - I.D}{2} + H.T\right)N \quad (27)$$

$$R_{dc} = \frac{\rho l_T}{W_a p} \quad (28)$$

Step 8. Check the turn number subject to N_{max}

As the turn number of inductor winding is less than the N_{max}, the turn number is increased and then go to *Step 2* for further calculation. Otherwise, the number of stack core is increased and reinitiate the proposed flow chart for the optimized inductor design.

Step 9. Determine optimal number of turn & stack core

The total losses calculated in *Step 6* and *Step 7* vs. turn number for a given stack core number can thus be derived as illustrated in Fig. 10 using stack number = 1, 2, 3 and 4 as an example. Obviously, the increase of stack core number may not provide the optimal solution regarding to the minimization of losses. As shown in Fig. 10, the minimum total losses occurs at stack core number = 3 and the turn number = 30-37. Figure 11 shows the total losses, including core losses, copper losses and switching losses for single core N = 49, stack 2

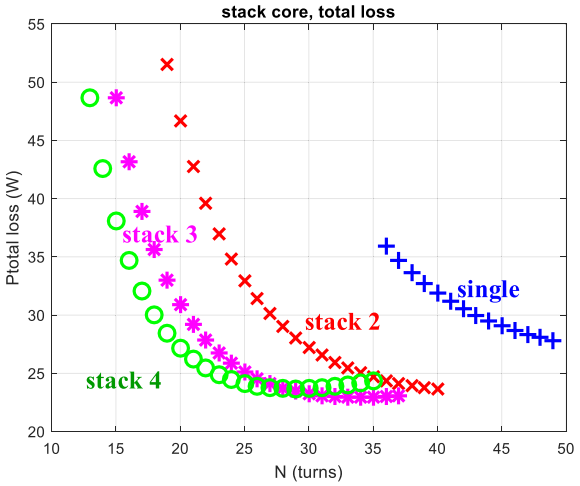


FIGURE 10. Total losses vs. turn number for a given number of core, APH27P60 cores.

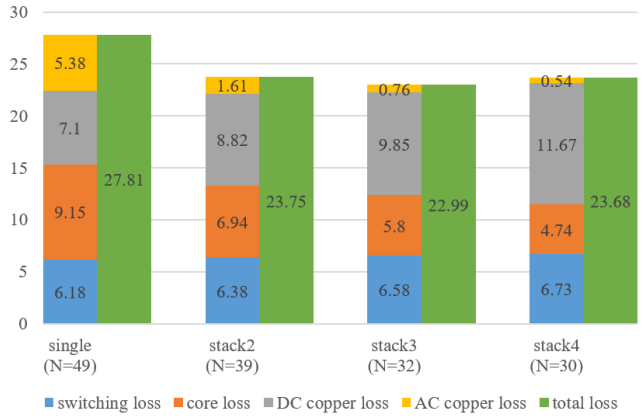


FIGURE 11. Losses breakdown, based upon analyzed current ripples, from interval 1-6.

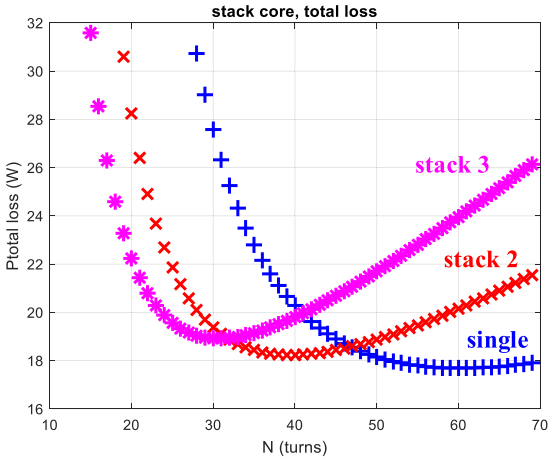


FIGURE 12. Loss of CH330060 with different stack core number and turn number.

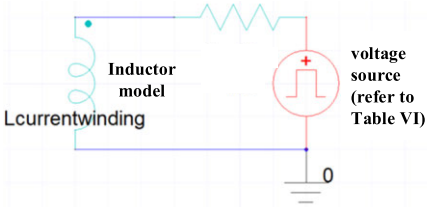


FIGURE 13. Equivalent circuit for "Six-step" method.

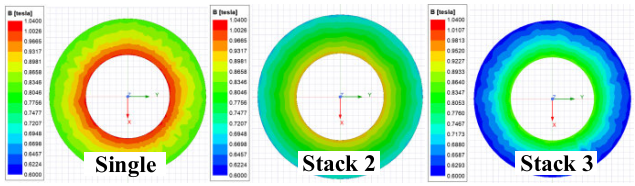


FIGURE 14. Flux density of core at interval 6, peak current condition with ANSYS® simulation.

(stack number = 2) and N = 39, stack 3 (stack number = 3) and N = 32, stack 4 (stack number = 4) and N = 30. The optimal case is for stack number = 3. The total losses are calculated based upon the average core and switching losses from interval 1-6 with analyzed current ripples as introduced in previous section. By Fig. 11, the increase of stack core number may not provide the optimal solution regarding to the minimization of total losses.

Apart from efficiency (losses), one of the most essential concerns is the volume of inductor and its core. As stack number = 2 and 3, the effective core volume can be calculated by $O.D^2H.T$ to give 162 and 243 (cm^3). Thetotal losses are 23.75 W and 22.99 W, for stack number = 2 and 3, respectively. The difference in between is 0.76 Was shown in Fig. 11, which is trivial.

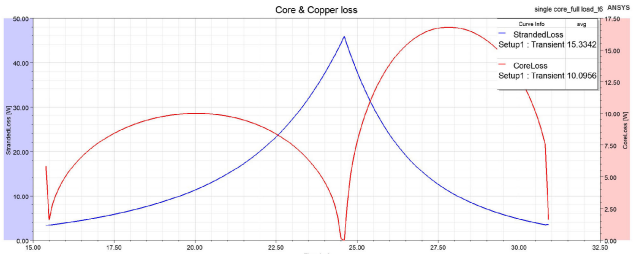
The proposed inductor design method can be applied to any other brand of core. The required change is the data based upon the core datasheet to fully reflect the special feature of the core. The details of the design flow and formula are the same as those for the illustrated example, previously. Due to the paper length limitation, only the results are shown. Fig. 12 illustrates the loss of CH330060 with different stack core number and turn number. Single core with around 60 turns of winding will give minimum total losses and thus the optimal converter efficiency.

IV. SIMULATION AND EXPERIMENTAL RESULTS

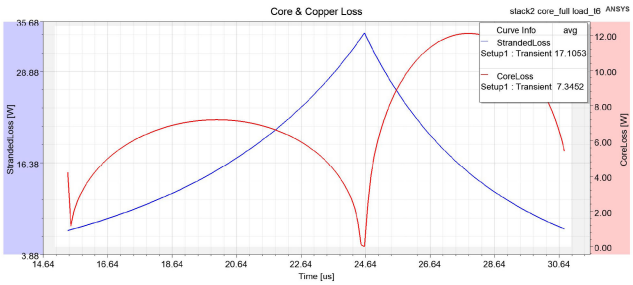
The proposed optimization design method is carried out and confirmed by simulation results using ANSYS® and test results. As the off-shelf core, APH27P60 is used, the optimal turn number of inductor is 49, 39, 32 for the stack core number = 1, 2 and 3, respectively. For other cores, the proposed optimal design procedure can be used to derive similar results with optimal efficiency.

The inductor model is created using ANSYS® PEmag. The physical core and windings are included in model. These inductor models are excited by the voltage source listed in Table 4 as shown in Fig. 13. The flux density derived from ANSYS® Transient Solver for the conditions of interval = 6 (the maximum current), $T_{ON} = 9.2\ \mu s$ is illustrated in Fig. 14. In the case of a single core, the maximum flux density reaches around 1 Tesla. However, for the cases with stacked core number 2 and 3, the flux density is reduced, as illustrated in Fig. 14. The ANSYS simulation losses are shown in Fig.15. As the stack core number increases, there is a slight increase in copper losses due to the longer winding length. However, the core losses reduction is more relevant than the increase of copper losses. Therefore, the inductor losses are reduced. Similar results can also be shown for other intervals under different current conditions. These simulation results fully support the analysis results shown in Section III.

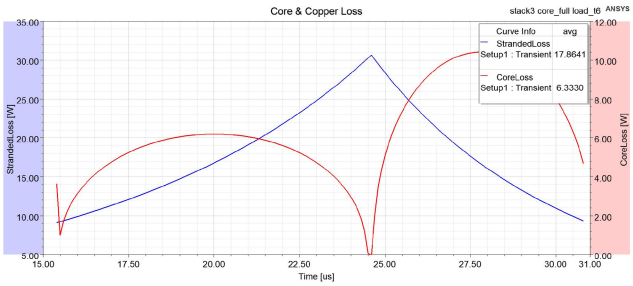
To verify the proposed optimal inductor design method, the test bench are set up as shown in Fig. 16. A MCU is used as the controller of the implemented TTP PFC. The measured temperature of inductors is shown in Fig. 17. The temperature of inductor with single core is much higher than that with two stack cores as shown in Fig. 17. High temperature is



(a) Single core with inductor loss = 25.4 W @ full load, interval = 6



(b) Stack 2 core with inductor loss = 24.45 W @ full load, interval = 6



(c) Stack 3 core with inductor loss = 24.19 W @ full load, interval = 6

FIGURE 15. Losses of inductor at interval 6 with ANSYS® simulation.

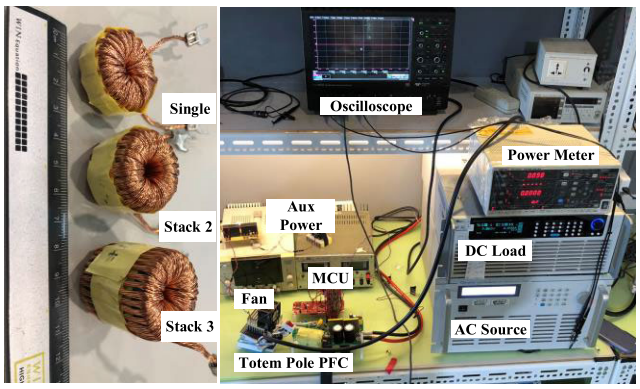


FIGURE 16. Three inductor candidate and TTP PFC test bench.

mainly contributed by larger current ripple and the related core losses.

To verify the calculated currents which are used to analyze and demonstrate the core losses in Fig. 11 (from interval 1-6), the calculated, simulation and experimental currents are illustrated using interval 6 as an example and listed in Table 5. The difference among the calculated, simulation and experimental is trivial. Fig. 18 shows the losses breakdown and total losses based upon experimental current ripples from interval 1-6. The case of stack core number = 3

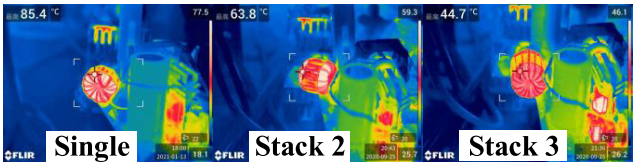


FIGURE 17. Temperature of single, stack 2 and stack 3 candidate after reaching the thermal steady state @ 115 V, full load.

TABLE 5. Inductor current ripple, calculated, ANSYS® simulation and experimental results in interval k = 6.

	Single ($N = 49$)	Stack 2 ($N = 39$)	Stack 3 ($N = 32$)
Calculation	26.13 A	15.6 A	11.82 A
Simulation	26.25 A	15.34 A	11.77 A
Experimental	28.3 A	15.79 A	11.89 A

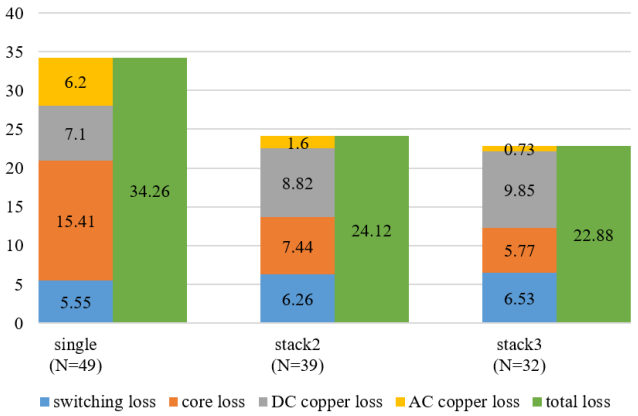


FIGURE 18. Losses breakdown, based upon experimental current ripples, from interval 1-6.

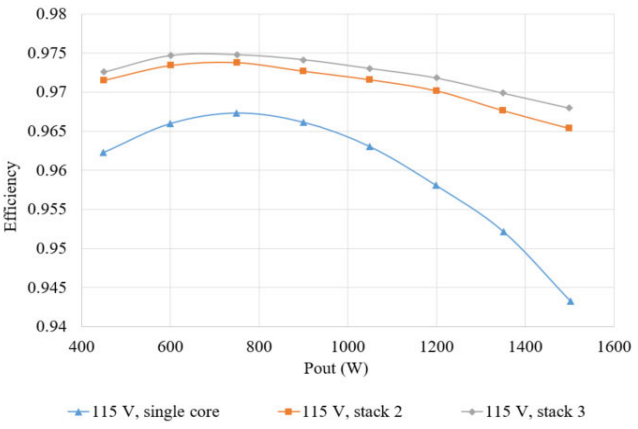


FIGURE 19. Efficiency results, 115 V, measured.

gives the optimized solution which further confirms the proposed efficiency optimized inductor design method.

Figure 19 and Fig. 20 show the measured efficiency for the TTP PFC with stack core number = 1, 2 and 3, under 115 V and 264 V, respectively. The efficiency of single core case deteriorates as compared to that of stack core number = 2 and 3. And the efficiency for the case with stack core

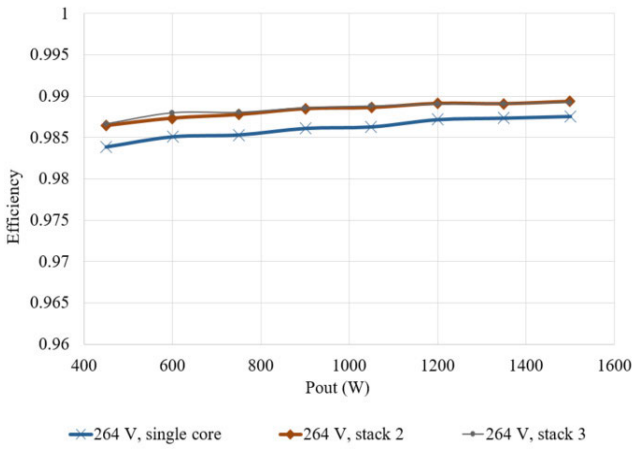


FIGURE 20. Efficiency results, 264 V, measured.

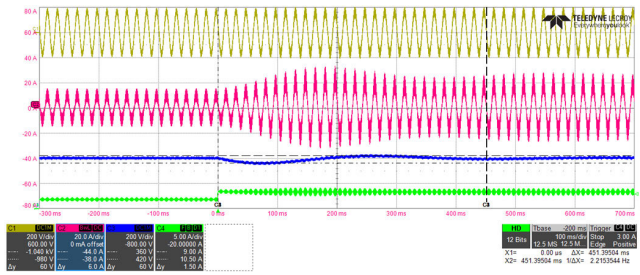


FIGURE 21. Load transient waveforms from 50% to 100% in stack 2 core condition, CH1: input voltage (200V/div), CH2: input current (20 A/div), CH3: output voltage (200V/div), CH4: output current (5A/div).

TABLE 6. Current harmonics with stack 2 core, IEC61000-3-2 Class A requirement vs. measurement.

NO.	Limits (A)	Measurement (A)	NO.	Limits (A)	Measurement (A)
2	1.08	0.0168	3	2.3	0.23
4	0.43	0.0105	5	1.14	0.157
6	0.3	0.0097	7	0.77	0.134
8	0.13	0.0034	9	0.4	0.112
10	0.18	0.037	11	0.33	0.091
12	0.15	0.0053	13	0.21	0.077
14	0.13	0.0031	15	0.15	0.069

number = 3 gives the highest efficiency. However, stack 2 is a compromised solution between the performance and actual implementation if size is considered. Of course, the cost needs to pay is 4.5 W loss (0.29% efficiency lose at full load) for using stack 2 instead of stack 3.

Figure 21 show the transient response from 50% to 100% load, and the settling time is near 450 ms. The measured input harmonics are shown in Table 6. As shown in Table 6, the harmonic meet the related requirement, IEC 61000-3-2, Class A in 115Vac, full load condition.

V. CONCLUSION

An efficiency optimized design method of inductor considering core, copper and power device losses, for PFC is proposed. Based upon the proposed method, the efficiency optimization solution to stack number and turn number of inductor considering the total losses is derived.

The contributions of this paper:

1) **Propose** a systematic PFC inductor design method to achieve efficiency optimization of *converter*
2) **Consider** the *losses* of *both* copper and core losses of inductor, *as well as* the switching losses of power device contributed by inductor
3) **Confirm** the proposed efficiency optimization method by ANSYS® simulation and experimental results.

The designed optimized inductor is applied to a GaN-based 1.5 kW Totem-pole PFC for server power and the experimental results show the peak efficiency can go up to 97.5% and 99%, under 115V and 264V of input voltage, respectively. The results fully support the effectiveness of the proposed optimization design method.

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