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RESEARCH ARTICLE

# Power-Imbalance Stimulation and Internal-Voltage Response Relationships Based Modeling Method of PE-Interfaced Devices in DC Voltage Control Timescale

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**ABSTRACT** In power systems with high penetration of renewable energy, dynamic issues associated with multi-device interaction involving DC voltage control (DVC) and AC current control (ACC) of power electronic (PE)-interfaced devices are constantly emerging. The device participates in the interaction dynamics based on the way that DVC adjusts the current reference of ACC to regulate the internal voltage amplitude/frequency under the active/reactive power imbalance. Thus, to analyze the effect mechanism of the device on system dynamics, the device should be characterized as internal voltage in response to power imbalance stimulation. However, the existing modeling works fail to recognize the process of the device participating in system dynamics, so the regulation mechanism of the internal voltage by the device under power imbalance for the system dynamics analysis remains unclear. Therefore, this paper proposes a modeling method of the PE-interfaced device based on the recognition of the regulation process of the internal voltage amplitude/frequency by the device under the active/reactive power imbalance. The model based on power-imbalance stimulation and internal-voltage response relationships is first established to characterize the regulation by detailed controls. Since the stimulation-response relationships are dominated by DVC, to directly describe the regulation by DVC, the model with ideal ACC is further proposed through the infinity gain equivalence of ACC. Based on the model, the characteristics of the device in DVC timescale and the impact mechanism of the device on system dynamics by regulating the internal voltage amplitude/frequency are revealed. Simulation results for verification are also included.

**INDEX TERMS** Characteristic, DC voltage control (DVC) timescale, modeling, participation mechanism, power electronic (PE)-interfaced devices, stimulation-response relationship, system dynamics.

## I. INTRODUCTION

With the rapid development of renewable energy generation and the weakening of power grid, more and more fast dynamic issues (around 100ms) associated with power electronic (PE)-interfaced devices are emerging in power systems [1], [2], [3], [4], [5]. For the analysis of system dynamics, it remains unclear what controls of the PE-interfaced device are involved in these dynamic issues and how the device affects system dynamics, which poses a challenge to the ambitious targets of a larger percentage of renewables. Models that illustrate the mechanism of the PE-interfaced device participating in and affecting system dynamics are urgently needed.

Under a power disturbance to the grid, the AC current control (ACC) of the PE-interfaced device regulates the internal voltage to adjust the current. In this process, the output power of the DC capacitor changes, and there may be a continuous power imbalance in the DC capacitor, which causes the DC voltage control (DVC) to participate in the system dynamics.

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References [6] and [7] observed the dynamic phenomenon caused by the action of DVC in a very weak grid case. The action of DVC affects the power imbalances of the device itself and other devices in the system [8], [9]. Thus, the system dynamics are associated with the multi-device interaction involving not only ACC but also DVC of PE-interfaced devices.

In this interaction process, the system focuses on the active and reactive powers as well as the voltage amplitude and frequency [10], [11], [12]. To maintain the power balance and a certain voltage amplitude and frequency level, PE-interfaced devices form and adjust the internal voltage amplitude/frequency according to the active/reactive power imbalance [9], [12]. Specifically, the main DVC modifies the active/reactive current reference, and the auxiliary ACC regulates the amplitude/frequency of the internal voltage according to the current reference. The grid then changes the active/reactive power corresponding to the internal voltage amplitude/frequency [8]. In the above process, the basic way of the device participating in the system dynamics is to regulate the internal voltage under power imbalance. Therefore, the model of the PE-interfaced devices should be characterized as the relationships between the active/reactive power imbalance and the internal voltage amplitude/frequency to reflect the role of the device in the system dynamics.

Concerning the power system dynamics study, models of the PE-interfaced device for simulation were first released by device manufacturers and relevant working groups [13], [14], [15], [16], [17]. These simulation models based on detailed connections of hardware and controls are good at reflecting the accurate responses of the device but do not focus on the mechanism analysis of dynamic issues. To address this, analytical models have been developed in various forms. References [18], [19], and [20] established state-space models of the PE-interfaced device to mathematically describe the device with a set of differential-algebraic equations. In [21], the model with power as stimulation and current as response was developed in the frequency domain to analyze the influence of the device on system stability. References [22], [23], [24], [25], and [26] obtained models of the PE-interfaced device by borrowing the concept of impedance in DC systems, which describes the impedance characteristics of the device. However, these models do not focus on the process of the PE-interfaced device participating in the system dynamics, so the regulation mechanism of the internal voltage by the device under power imbalance for the system dynamics analysis remains unclear.

Several modeling works [27], [28] have focused on the way of the PE-interfaced device participating in system dynamics and developed models of the device considering ACC. However, these models do not consider the involvement of DVC in system dynamics under continuous power disturbance, which makes the models unsuitable for analyzing dynamic issues associated with DVC. In summary, most device modeling works do not focus on the way in which the PE-interfaced device participates in the system dynamics, and a few

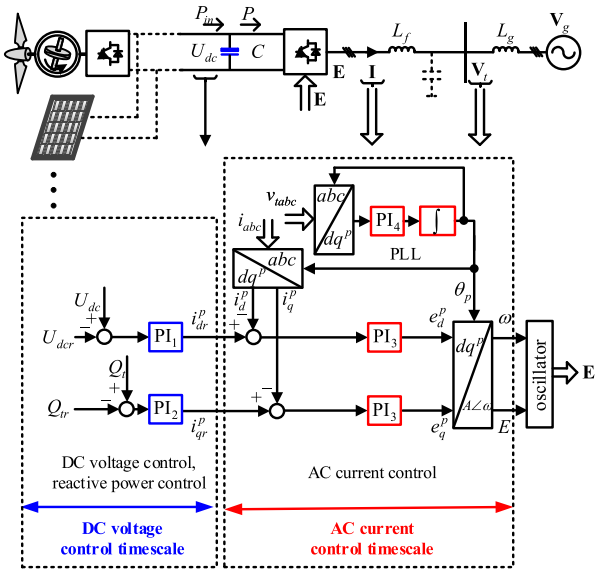


**FIGURE 1.** Diagram of a PE-interfaced device utilizing a typical vector control scheme.

modeling studies based on the way do not consider DVC. The confusion that remains unclarified in these studies is how the PE-interfaced device with DVC action regulates the internal voltage under the power imbalance and further affects the system dynamics.

Therefore, this study focuses on the process of the PE-interfaced device with DVC action participating in system dynamics to propose the modeling method of the device for the analysis of dynamic issues in DVC timescale. By establishing the model of the PE-interfaced device based on power-imbalance stimulation and internal-voltage response relationships, the regulation mechanism of the internal voltage amplitude/frequency by the device according to the active/reactive power imbalance can be depicted. Moreover, the regulation of the internal voltage is dominated by DVC. The effect of ACC dynamics makes the way DVC regulates the internal voltage unintuitive. So, it is necessary to further neglect ACC dynamics and establish the stimulation-response relationships with ideal ACC to directly describe the regulation by DVC. Subsequently, the characteristics of the PE-interfaced device in DVC timescale and its impact on the dynamics of the system can be analyzed.

The rest parts of this paper are organized as follows. Section II briefly introduces the control scheme of the PE-interfaced device. In Section III, the process of the PE-interfaced device participating in system dynamics, which determines the modeling requirements of the device, is analyzed. According to these requirements, the detailed modeling steps are presented and the characteristics of the PE-interfaced device are further revealed in Section IV. Combined with the simulation, Section V shows the feasibility of the proposed models and analyzes the role of the PE-interfaced device with DVC action in system dynamics. Finally, conclusions are drawn in Section VI.

## II. CONTROL PRINCIPLE OF PE-INTERFACED DEVICE

### A. CONTROL STRUCTURE OF PE-INTERFACED DEVICE

PE-interfaced devices such as direct-drive permanent magnet synchronous generator (PMSG)-based wind turbines (WTs) and photovoltaics (PVs) are connected to the grid through the power electronic converter as shown in Fig. 1. When analyzing dynamic issues with grid disturbance, the main consideration of PE-interfaced devices is the grid-side control due to the isolation of the DC capacitor [29]. To simplify the analysis, this study starts with the normal controls such as DVC and does not consider the switch elements such as chopper. Fig. 1 depicts a typical vector control scheme of the PE-interfaced device such as PMSG-based WT and PV [19], [30]. Based on the control parameter settings, different control loops have different bandwidths and response speeds [31]. The dual-loop vector control can be divided into the DVC and ACC timescale components according to the different response speeds of the controllers [31]. The DVC timescale component consists of the DC voltage controller and the reactive power controller. The DC voltage controller controls the voltage of the DC capacitor $U_{dc}$ by adjusting the $d$-axis current reference $i_{dr}^{p}$. The reactive power controller controls the reactive power at terminal voltage node $Q_t$ according to its reference $Q_{tr}$ by adjusting the $q$-axis current reference $i_{qr}^{p}$. The ACC timescale component contains the AC current controller and the phase-locked loop (PLL). The AC current controller detects the current $\mathbf{I}$ of the filter inductor and adjusts the $d$-axis/$q$-axis internal voltage $e_d^p/e_q^p$ to make the $d$-axis/$q$-axis current $i_d^p/i_q^p$ track the current reference. The PLL provides the phase information $\theta_p$ based on the terminal voltage. The internal voltage amplitude $E$ and frequency $\omega$ are composed of $e_d^p$, $e_q^p$, and $\theta_p$ according to the following equation:

$$E \cdot e^{j\int \omega dt} = \left(e_d^p + je_q^p\right) \cdot e^{j\theta_p} \tag{1}$$

The detailed mathematical expressions of the DVC and ACC timescale components are given in Appendix A.

As shown in Fig. 1. the DVC and ACC timescale components are interrelated. The DVC timescale component determines the current references of the ACC timescale component. Meanwhile, their inputs are constrained by the circuit structure of the PE-interfaced device. If the power loss of the switch is neglected, the output power of the DC capacitor is equal to the active power determined by the internal voltage vector $\mathbf{E}$ and current vector $\mathbf{I}$ at AC side. The imbalance between $Q_t$ and $Q_{tr}$ is equivalent to the imbalance between the reactive power at internal voltage node $Q$ and its reference $Q_r$ [32]. $Q$ is calculated from $\mathbf{E}$ and $\mathbf{I}$. Thus, $P/Q$ (input of the DVC timescale component) and $\mathbf{I}$ (input of the ACC timescale component) are mutually constrained. The relationship between them can be written as follows:

$$P + jQ = \left(E \cdot e^{j\int \omega dt}\right) \cdot \left(I \cdot e^{-j\int \omega_i dt}\right) \tag{2}$$

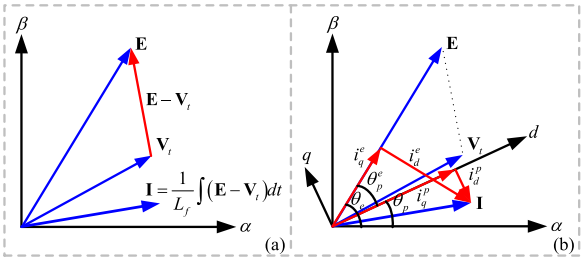


**FIGURE 2.** Relationships between different vectors and different coordinates.

### B. ORGANIZATION OF ACC TIMESCALE COMPONENT IN THE FORM OF INTERNAL VOLTAGE DEPENDING ONLY ON CURRENT ERROR

In a PE-interfaced device, the DVC timescale component aims to balance the input and output active powers as well as the reactive power and its reference. To match the DVC timescale component, the ACC timescale component makes the active/reactive current track the active/reactive current reference determined by the DVC timescale component. Although the ACC timescale component is an adjunct to the DVC timescale component, the ACC timescale component is an important bridge between the DVC timescale component and grid interactions. However, since PLL requires the acquisition of the terminal voltage phase $\theta_t$, it appears that the internal voltage formed by the ACC timescale component depends not only on the current error but also on the grid information. The indeterminate relationships of the ACC timescale component make it unclear how the DVC timescale component participates in system dynamics.

Due to the constrained relationship of filter inductance between terminal voltage vector $\mathbf{V}_t$ and $\mathbf{I}$ given in Fig 2 (a), $\theta_t$ detected by PLL depends on $\mathbf{I}$. Hence, the relationships of the ACC timescale component are the stimulation-response relationships, where the internal voltage depends only on the current and its reference. Fig 2 (b) shows the relationships between the variables of the current vector at different coordinates. The detailed mathematical expressions of the transformation in different coordinates are given in Appendix A. Based on these, both $d$-axis/$q$-axis current error $\varepsilon i_d^p/\varepsilon i_q^p$ and the phase error $\theta_p^t$ can be expressed by the active/reactive current $i_d^e/i_q^e$ and the active/reactive current reference $i_{dr}^e/i_{qr}^e$ as follows:

$$\varepsilon i_{dr}^p + \varepsilon j i_{qr}^p = \left(\varepsilon i_{dr}^e + j\varepsilon i_{qr}^e\right) \cdot e^{j(\theta_p - \theta_e)} \tag{3}$$

$$\theta_p^t = f\left(\varepsilon i_d^e, \varepsilon i_q^e, i_{dr}^e, i_{qr}^e\right) \tag{4}$$

The detailed mathematical expression of $f\left(\varepsilon i_d^e, \varepsilon i_q^e, i_{dr}^e, i_{qr}^e\right)$ is provided in Appendix B and the detailed derivation process has been given in [27]. Then, the ACC timescale component can be equivalently expressed as the relationships in the form of the internal voltage frequency/amplitude depending only on the active/reactive current error. The derivation process and mathematical expression of the ACC timescale component are given in detail in the later modeling section.

## III. REGULATION MECHANISM OF INTERNAL VOLTAGE BY PE-INTERFACED DEVICE ACCORDING TO POWER IMBALANCE IN SYSTEM DYNAMICS AND MODELING IDEAS

Based on the control structure of the PE-interfaced device, this section recognizes the mechanism of the device participation in system dynamics and modeling requirements. First, we demonstrate how the PE-interfaced device forms and controls the amplitude and frequency of the internal voltage to satisfy the system requirements with the DVC and ACC timescale components. Then, the action process of the DVC and ACC timescale components participating in system dynamics is analyzed. Based on these insights, modeling requirements are proposed.

### A. MECHANISM OF THE FORMATION OF INTERNAL VOLTAGE IN RESPONSE TO POWER IMBALANCE STIMULATION

Power systems require balancing the active and reactive power flows and maintaining the voltage magnitude and frequency [10], [11]. The PE-interfaced device is designed to transfer active and reactive powers and regulate the internal voltage magnitude and frequency for the system requirements [9], [33], [34], [35]. A PE-interfaced device can output active and reactive powers by establishing an internal voltage and can further adjust the powers by changing the internal voltage magnitude and frequency [9], [12].

Based on the control structure of the PE-interfaced device described in Section II, the formation of the internal voltage by the ACC and DVC timescale components is shown in Fig 3. Due to the power-current constraint, grid disturbance affects both the active/reactive power imbalance $\varepsilon P/\varepsilon Q$ of the DVC timescale component and the active/reactive current imbalance $\varepsilon i_d^e/\varepsilon i_q^e$ of the ACC timescale component. The DVC timescale component adjusts $i_{dr}^e/i_{qr}^e$ according to $\varepsilon P/\varepsilon Q$. The ACC timescale component regulates $E/\omega$ according to $\varepsilon i_d^e/\varepsilon i_q^e$. Eventually, the AC instantaneous value of the internal voltage $e_{abc}$ is formed by the oscillator according to $E/\omega$ and connected to the grid [36], [37].

Therefore, the internal voltage is determined by both the ACC and DVC timescale components of the PE-interfaced device. As with the ACC timescale component, the dynamics of the DVC timescale component are reflected in the amplitude and frequency of the internal voltage.

### B. MODELING IDEAS BASED ON THE REGULATION PROCESS OF INTERNAL VOLTAGE BY PE-INTERFACED DEVICE ACCORDING TO POWER IMBALANCE IN SYSTEM DYNAMICS

When the PE-interfaced device is connected to a weak grid, Fig. 4 shows the dynamic processes of electrical variables under the continuous power imbalance caused by an increase of reactive load. Before the disturbance, $i_d^e$ equals $i_{dr}^e$, and $P$ is balanced with input power $P_{in}$, as shown in Fig. 4 (a). When the power grid is disturbed, $i_d^e$ and $P$ change instantly. The fast-responding ACC timescale component detects the

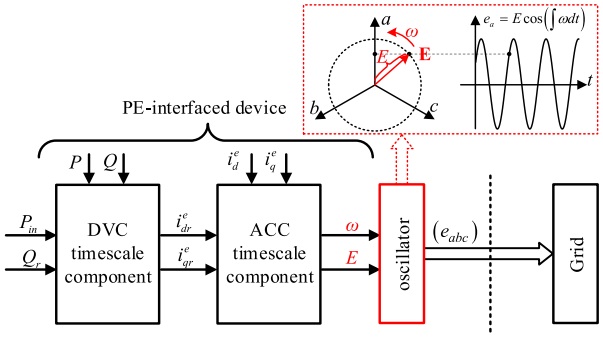


**FIGURE 3.** Formation of the internal voltage by the ACC and DVC timescale components in response to power imbalance stimulation.

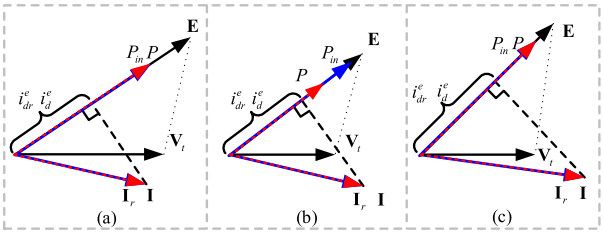


**FIGURE 4.** Dynamic processes of electrical variables under continuous power disturbance in a weak grid.

current imbalance and adjusts the internal voltage to restore the current balance. Due to the weak grid condition, the amplitude of $\mathbf{V}_t$ decreases after disturbance, and the ACC timescale component requires a reduction in the amplitude of $\mathbf{E}$ to rebalance $i_d^e$ and $i_{dr}^e$, as shown in Fig. 4 (b). $P$ is lower than $P_{in}$ because the amplitude of $\mathbf{E}$ is reduced, even though $i_d^e$ is balanced with $i_{dr}^e$. Thus, the regulation of the internal voltage by the ACC timescale component alone cannot achieve power balancing, and the continuous power imbalance causes the action of the DVC timescale component.

Based on the formation mechanism of the internal voltage shown in Fig. 3, when the DVC timescale component changes $i_{dr}^e/i_{qr}^e$, the ACC timescale component immediately regulates $E/\omega$, forcing $i_d^e/i_q^e$ to track $i_{dr}^e/i_{qr}^e$. Since the ACC timescale component regulates $E/\omega$ depending only on $\varepsilon i_d^e/\varepsilon i_q^e$, once the DVC timescale component changes $i_{dr}^e/i_{qr}^e$ according to $\varepsilon P/\varepsilon Q$, there is always a corresponding $E/\omega$. In this way, the DVC timescale component regulates $E/\omega$ until the power is rebalanced, as shown in Fig. 4 (c). Hence, the DVC timescale component of the PE-interfaced device acts to participate in system dynamics by regulating the internal voltage amplitude/frequency according to the active/reactive power imbalance.

Due to the participation of DVC timescale component, the system appears to have corresponding dynamics in DVC timescale (around 100ms). For the dynamic problems in DVC timescale, the relationships between the active/reactive power imbalance and the internal voltage amplitude/frequency involving the DVC timescale component need to be proposed to reflect the characteristic and role of the PE-interfaced device. Moreover, because the regulation of the internal voltage amplitude/frequency under active/reactive power

imbalance is dominated by the DVC timescale component, the model of the PE-interfaced device with the ideal ACC timescale component should be further established to directly reflect the characteristic in DVC timescale determined by the DVC timescale component.

## IV. MODELING OF PE-INTERFACED DEVICE BASED ON POWER-IMBALANCE STIMULATION AND INTERNAL-VOLTAGE RESPONSE RELATIONSHIPS IN DVC TIMESCALE

According to the modeling requirements, this section presents the detailed modeling steps of the PE-interfaced device. We first replace the active/reactive current with active/reactive power to establish stimulation-response relationships of the PE-interfaced device where the internal voltage depends solely on the power imbalance. Then, we neglect the influence of ACC timescale component dynamics and obtain the model of the PE-interfaced device with ideal ACC. Based on the model, the characteristics of the device in DVC timescale are revealed.

### A. REPLACEMENT OF ACTIVE/REACTIVE CURRENT BY ACTIVE/REACTIVE POWER TO ESTABLISH STIMULATION-RESPONSE RELATIONSHIPS WHERE INTERNAL VOLTAGE DEPENDS SOLELY ON POWER IMBALANCE

Based on the control structure of the PE-interfaced device, the device includes the ACC and DVC timescale components. The DVC timescale component is composed of DC capacitance, DVC, and reactive power control. The equation of the DC capacitance can be written as

$$U_{dc} = \sqrt{(2/C)\int (P_{in} - P)\,dt} \tag{5}$$

This equation constrains the relationship between $U_{dc}$ (input of DVC) and $P$. Combining (5) with the equations of DVC, reactive power control, and $T_1\left(i_{dr}^p, i_{qr}^p \rightarrow i_{dr}^e, i_{qr}^e\right)$, which are given in Appendix A, the relationships of the DVC timescale component between $\varepsilon P/\varepsilon Q$ and $i_{dr}^e/i_{qr}^e$ are obtained and shown in the blue box in Fig. 5 (a).

The ACC timescale component includes ACC and PLL. According to (3) and (4), $\varepsilon i_d^p/\varepsilon i_q^p$ and $\theta_p^t$ depend on $\varepsilon i_d^e/\varepsilon i_q^e$. Combining (3) and (4) with the equations of ACC, PLL, and $T_3\left(e_d^p, e_q^p \rightarrow E, \omega\right)$ which are given in Appendix A, the relationships of the ACC timescale component between $\varepsilon i_d^e/\varepsilon i_q^e$ and $E/\omega$ are also obtained, as shown in the green box in Fig. 5 (a). Therefore, the relationships of the PE-interfaced device shown in Fig 5 (a) can be obtained.

However, the stimulation-response relationships are not explicit because the relationships take both $P/Q$ and $i_d^e/i_q^e$ as stimulations. In fact, during the regulation of the internal voltage, the dynamics of $P/Q$ and $i_d^e/i_q^e$ are constrained by (2), which can be further expressed as:

$$P + jQ = E \cdot I \cdot e^{j\int(\omega-\omega_i)dt} = E\left(i_d^e - ji_q^e\right) \tag{6}$$

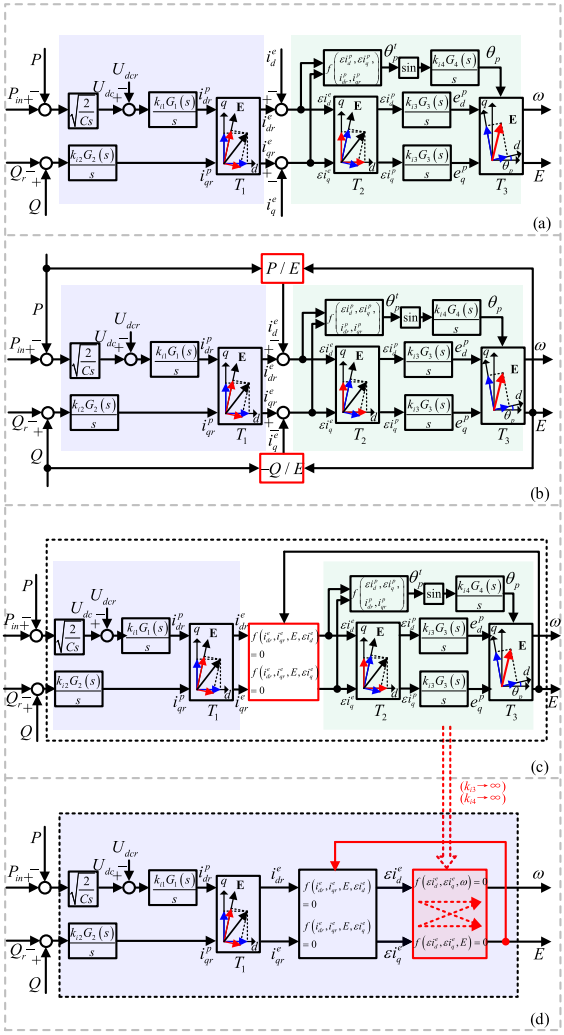


**FIGURE 5.** Septs of establishing the model of the PE-interfaced device in DVC timescale.

Under the joint constraint of this relationship and that of the ACC and DVC timescale components, there exist stimulation-response relationships where the internal voltage amplitude/frequency depends solely on the active/reactive power imbalance.

Based on (6), $i_d^e/i_q^e$ can be expressed in terms of $P/Q$ and $E$ as follows:

$$\begin{cases} i_d^e = P/E \\ i_q^e = -Q/E \end{cases} \tag{7}$$

By converting the input of the ACC timescale component into $P/Q$, the relationships shown in Fig. 5 (a) can be transformed into those shown in Fig. 5 (b).

Because $P/Q$ and $i_{dr}^e/i_{qr}^e$ are constrained by the relationships of the DVC timescale component and $P/Q$ and $i_d^e/i_q^e$ are constrained by (7), $i_{dr}^e/i_{qr}^e$ and $\varepsilon i_d^e/\varepsilon i_q^e$ are also constrained and the constraint relationships can be further collated as

$$f\left(i_{dr}^e, i_{qr}^e, E, \varepsilon i_d^e\right) = 0 \tag{8}$$

$$f\left(i_{dr}^e, i_{qr}^e, E, \varepsilon i_q^e\right) = 0 \tag{9}$$

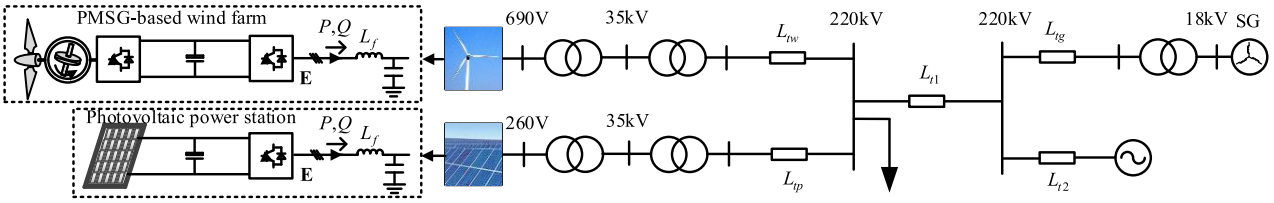


**FIGURE 6.** Simulation scenario of renewable energy generations transmitting power through long lines.

The stimulation-response relationships in Fig. 5 (b) can then be converted into those shown in Fig. 5 (c).

The relationships of the PE-interfaced device shown in Fig. 5 (c) explicitly describe how the DVC timescale component regulates the internal voltage amplitude/frequency according to the active/reactive power imbalance with the assistance of the ACC timescale component.

### B. NEGLECTION OF THE INFLUENCE OF ACC TIMESCALE COMPONENT DYNAMICS TO OBTAIN RELATIONSHIPS BETWEEN POWER IMBALANCE AND INTERNAL VOLTAGE WITH IDEAL ACC

The ACC timescale component dynamics affect the regulation of the internal voltage amplitude/frequency by the DVC timescale component. In this regulation process, the current error in DVC timescale may be large or small in different scenarios. If the current error in DVC timescale is small, the ACC timescale component enables the active and reactive currents to track their references given by the DVC timescale component in almost real time. In other words, it can be assumed that the ACC timescale component is nearly ideal. The relationships between power imbalance and internal voltage with the ideal ACC timescale component can be further established based on the relationships with the nonideal ACC timescale component, by eliminating the influence of ACC timescale component dynamics.

Specifically, the ACC integrator gain approaches infinity, which makes $\varepsilon i_d^p/\varepsilon i_q^p$ zero. Likewise, the PLL integrator gain tends to infinity, so that $\theta_t$ and $\theta_p$ are equal in real time. The equations are as follows:

$$e_d^p = (k_{i3}/p)\, G_3(s)\left(i_{dr}^p - i_d^p\right) \quad (k_{i3} \to \infty) \tag{10}$$

$$e_q^p = (k_{i3}/p)\, G_3(s)\left(i_{qr}^p - i_q^p\right) \quad (k_{i3} \to \infty) \tag{11}$$

$$\theta_p = (k_{i4}/p)\, G_4(s) \sin\left(\theta_t - \theta_p\right) \quad (k_{i4} \to \infty) \tag{12}$$

Combining these with (1), (3), and (4), we obtain:

$$f\left(\varepsilon i_d^e, \varepsilon i_q^e, \omega\right) = 0 \tag{13}$$

$$f\left(\varepsilon i_d^e, \varepsilon i_q^e, E\right) = 0 \tag{14}$$

Whenever $i_d^e/i_q^e$ deviates from $i_{dr}^e/i_{qr}^e$, the ideal ACC timescale component adjusts $E/\omega$ to the position where $i_d^e/i_q^e$ equals $i_{dr}^e/i_{qr}^e$ immediately. Thus, the relationships of the ideal ACC timescale component are obtained, as shown by the red box in Fig 5 (d). The ideal ACC timescale component can be considered as an energy storage component with an infinitesimal energy storage capacity that can act without delay, similar to [38]. Then, the relationships between the active/reactive power imbalance and the internal voltage frequency/amplitude with the ideal ACC timescale component can be established, as shown in Fig. 5 (d).

The proposed model with ideal ACC can directly illustrate the adjustment of the internal voltage amplitude/frequency by the DVC timescale component under active/reactive power imbalance. It should be noted that although the proposed model with ideal ACC ignores the influence of ACC timescale component dynamics, it retains the basic way in which the PE-interfaced device originally participates in the system dynamics. This is important for the analysis of the characteristic and role of the PE-interfaced device in the dynamics of the multi-device interaction.

### C. CHARACTERISTIC OF RELATIONSHIPS BETWEEN POWER IMBALANCE AND INTERNAL VOLTAGE IN DVC TIMESCALE

Based on the model of the PE-interfaced device with ideal ACC, the characteristic of the PE-interfaced device in regulating the internal voltage amplitude/frequency in DVC timescale can be further revealed.

As shown in Fig 5 (d), in the process of the DVC timescale component regulating $E$ and $\omega$, both $i_{dr}^e$ and $i_{qr}^e$ affect $E$ via the ACC timescale component. Subsequently, the change in $E$ influences both $\varepsilon i_d^e$ and $\varepsilon i_q^e$ through the feedback path indicated by the red arrow in Fig. 5 (d). Under these current imbalances caused by the change of $E$, both $E$ and $\omega$ vary simultaneously. Therefore, there are couplings between the $\varepsilon P$ stimulation and $\omega$ response relationship and the $\varepsilon Q$ stimulation and $E$ response relationship. Moreover, the relationships between $\varepsilon P/\varepsilon Q$ and $E/\omega$ are jointly determined by the DC capacitance and controls in DVC timescale. It makes the order of the stimulation-response relationships higher than first-order. Therefore, the PE-interfaced device exhibits coupling and high-order characteristics for the regulation of the internal voltage amplitude/frequency under the active/reactive power imbalance in DVC timescale. The coupling and high-order characteristics of the device increase the order of system dynamics, which may increase the risk of system instability.

In the following simulation section, the feasibility of the proposed models is illustrated, and how the stimulation-response characteristics of the device in DVC timescale affect the system dynamics is preliminarily explored based on the proposed model.

## V. SIMULATION ANALYSIS

### A. SIMULATION SCENARIO DESCRIPTION

The cases in [3], [4], [5], [6], and [7] with dynamic problems share a common feature: renewable energy generations transmit power through long lines and the synchronous generators (SGs) are distant from the renewable energy sources. So, the system shown in Fig. 6 is used as the simulation scenario for the analysis in this section. In the system, a PMSG-based wind farm and a PV power station are connected to the point of common coupling (PCC) bus, which is then connected to an SG and power grid through long lines. Two 30+$j$30 MVA local loads are also attached to the PCC bus. For simplicity, the wind farm with 50 PMSG-based WTs rated at 2 MW is simply represented by a single aggregated PMSG-based WT rated at 100 MW. The PV power station is represented by a PV device rated at 100 MW in the same manner. Moreover, the SG is rated at 200 MW. The parameters of PE-interfaced devices and network are listed in Appendix C.

### B. MODEL VERIFICATION AND SIMULATION OF THE REGULATION OF INTERNAL VOLTAGE UNDER POWER IMBALANCE

By organizing and deforming the original structure of the PE-interfaced device, the proposed model can directly depict the mechanism of the device participating in system dynamics and reveal the role and characteristics of the device in DVC timescale. Therefore, to illustrate the feasibility of the proposed models, the comparison of the simulation results is given to demonstrate that the proposed models are consistent with the original structure of the device in terms of DVC timescale dynamics. Then, we show that the participation mechanism determined by the original structure of the device can be represented on the proposed models.

The PMSG-based WT in Fig. 6 is taken as an observation object to illustrate the feasibility of the proposed models of the PE-interfaced device. Fig. 7 shows the comparison results with the proposed models and the device with original structure in different disturbance scenarios. The simulation results of the proposed models with the nonideal ACC and ideal ACC are high consistent with those of the device with original structure regarding DVC timescale dynamics. The high coincidence of simulation results proves that the proposed models remain consistent with the original device in terms of DVC timescale dynamics, despite the collation and deformation in modeling. In contrast, the device model considering only ACC in [27] is completely unable to capture the DVC timescale dynamics of the device, as shown by the green dashed line in Fig. 7.

Taking the case where a 30+$j$30 MVA local load cuts out at 3 s as an example, Fig 8 shows the simulation waveforms of each variable of the device with the original structure when regulating the internal voltage under power imbalance. Some of the simulation waveforms near the time of disturbance are zoomed in. When the local load is cut out, $P/Q$ gets unbalanced with $P_{in}/Q_r$, and $i_d^e/i_q^e$ gets unbalanced with $i_{dr}^e/i_{qr}^e$. As shown in Fig 8, at t1, although the ACC timescale

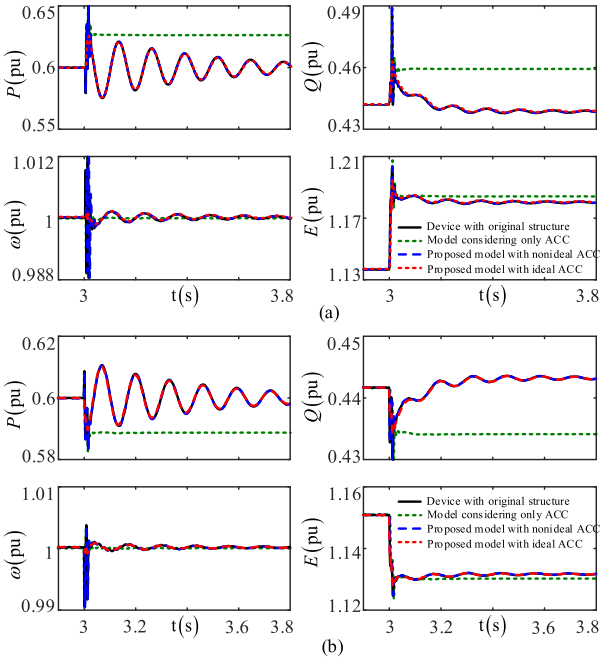


**FIGURE 7.** Comparison of simulation results with the proposed models and the device with original structure under (a) Case 1 (A 30+j30 MVA load cuts out at 3 s) and (b) Case 2 (The SG cuts out at 3 s).

component makes $i_d^e/i_q^e$ equal to $i_{dr}^e/i_{qr}^e$ by regulating $E/\omega$, $P/Q$ is still greater than $P_{in}/Q_r$ because of the increase in $E$. The continuous power imbalance causes the action of the DVC timescale component.

As shown in Fig 8, the DVC timescale component adjusts $i_{dr}^e/i_{qr}^e$ according to $\varepsilon P/\varepsilon Q$. The ACC timescale component then regulates $E/\omega$ according to $\varepsilon i_d^e/\varepsilon i_q^e$. As long as $\varepsilon i_d^e/\varepsilon i_q^e$ is not zero, the ACC timescale component regulates $E/\omega$ until $i_d^e/i_q^e$ equals $i_{dr}^e/i_{qr}^e$. With the assistance of the ACC timescale component, the dynamics of the DVC timescale component would be eventually reflected in the dynamics of $E/\omega$. As shown in the simulation results in Fig 8, the waveforms of $E/\omega$ present DVC timescale dynamics in addition to ACC timescale dynamics. The above regulation process of the internal voltage provided by the simulation of the device with original structure is consistent with that described by the proposed model. Therefore, the proposed model with the nonideal ACC can represent the actual regulation of the internal voltage amplitude/frequency by the PE-interfaced device with DVC action under active/reactive power imbalance stimulation.

In the process of regulating the internal voltage by the DVC timescale component, there are current errors due to the dynamics of the ACC timescale component. As shown in Fig. 8, the dynamics of $\varepsilon i_d^e/\varepsilon i_q^e$ in ACC timescale are relatively large, while the dynamics of $\varepsilon i_d^e/\varepsilon i_q^e$ in DVC timescale are almost zero. For the dynamics in DVC timescale focused on in this study, the ACC timescale component can effectively assist the DVC timescale component in regulating the internal voltage amplitude and frequency, and the effect of ACC timescale component dynamics is so small that it can

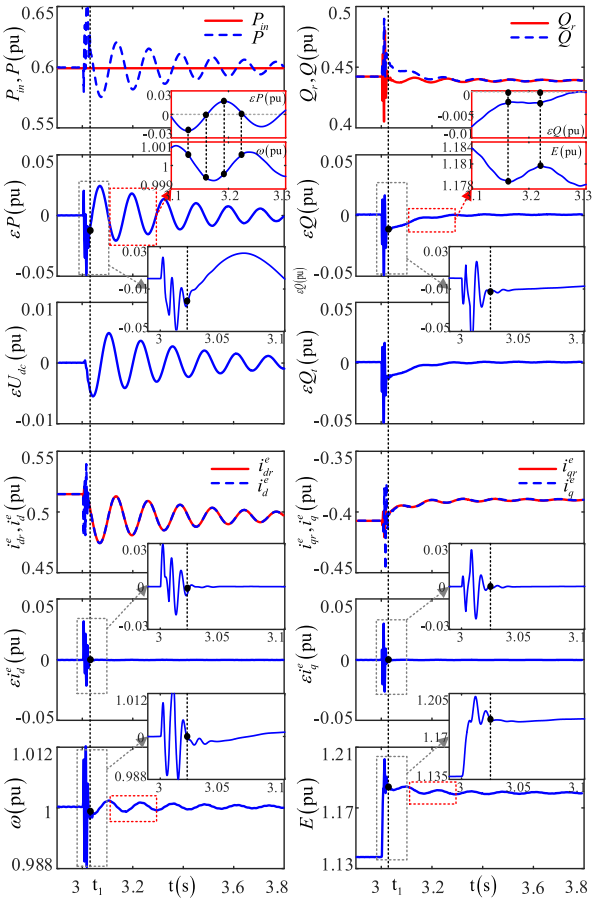

**FIGURE 8.** Time domain simulation of each variable in the regulation process of the internal voltage amplitude/frequency under the active/reactive power imbalance.

be ignored. Therefore, in this situation, the proposed model with the ideal ACC can directly represent the regulation of the internal voltage by DVC timescale controls under power imbalance and the characteristics of the device in DVC timescale.

The magnified red diagrams in Fig. 8 shows the detailed correspondence between the power imbalance and the internal voltage in DVC timescale. Due to the coupling and high-order characteristics of the PE-interfaced device in DVC timescale, the correspondence between the waveforms of the active/reactive power imbalance and the internal voltage magnitude/frequency is not simply a 90-degree phase shift of first-order integration, but a more complex correspondence.

### C. PRELIMINARY UNDERSTANDINGS OF THE ROLE OF PE-INTERFACED DEVICE WITH DVC IN SYSTEM DYNAMICS

In an actual system, different control parameters of the PE-interfaced device result in different system dynamics. Furthermore, the diversity of control schemes adopted by different device manufacturers makes the dynamic issue more complex. It is difficult to analyze how the DVC timescale controls of the PE-interfaced device affect the system dynamics based directly on the detailed connections of hardware

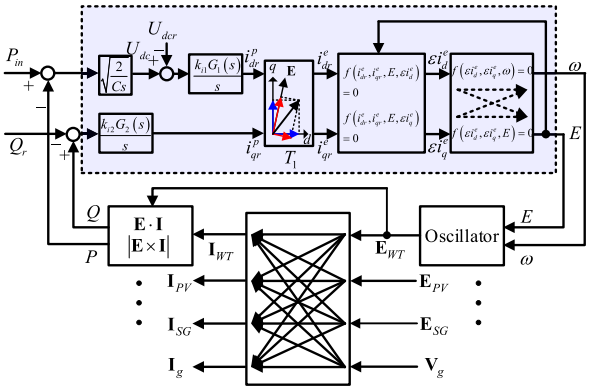

**FIGURE 9.** Block diagram of the closed loop for the multi-device system.

and controls of the device, without a mechanism description of the device. Because the proposed model directly illustrates the mechanism of the PE-interfaced device with DVC action participating in system dynamics, how the device with coupling and high-order characteristics in DVC timescale affects system dynamics can be further analyzed based on the proposed model.

According to the proposed model in DVC timescale, the block diagram of the closed loop for the multi-device system can be obtained, as shown in Fig 9. When the system is disturbed and deviates from the steady-state operating point, active/reactive power imbalance acts on the PE-interfaced device. The DVC timescale component of the device regulates the magnitude/frequency of the internal voltage according to the active/reactive power imbalance. The variation of the internal voltage magnitude/frequency further alters the AC instantaneous value of the internal voltage through the oscillator. The AC instantaneous values of the internal voltages of the device and other devices act on the network to change the AC instantaneous values of the currents. The AC instantaneous values of the internal voltages and currents determine the output powers of the devices, which in turn affect the power imbalances of the devices. The cycle continues until the system reaches a steady-state operating point. Therefore, in this multi-device interaction process, the basic way in which DVC timescale controls of the PE-interfaced device affect the active/reactive power and voltage amplitude/frequency in the system is by regulating the internal voltage amplitude/frequency.

Fig 10 shows the waveforms of the internal voltage amplitude/frequency of the studied device and the waveforms of the active/reactive powers of PE-interfaced devices for different DVC parameters under the same disturbance. It can be seen that the changes of the DVC parameters are directly reflected in the internal voltage amplitude/frequency. Regardless of which control parameters are selected, the DVC timescale controls always regulate the internal voltage amplitude/frequency to affect the system dynamics.

The proposed model reveals a unified mechanism for the PE-interfaced device such as PMSG-based WT and PV with different DVC parameters influencing system dynamics.

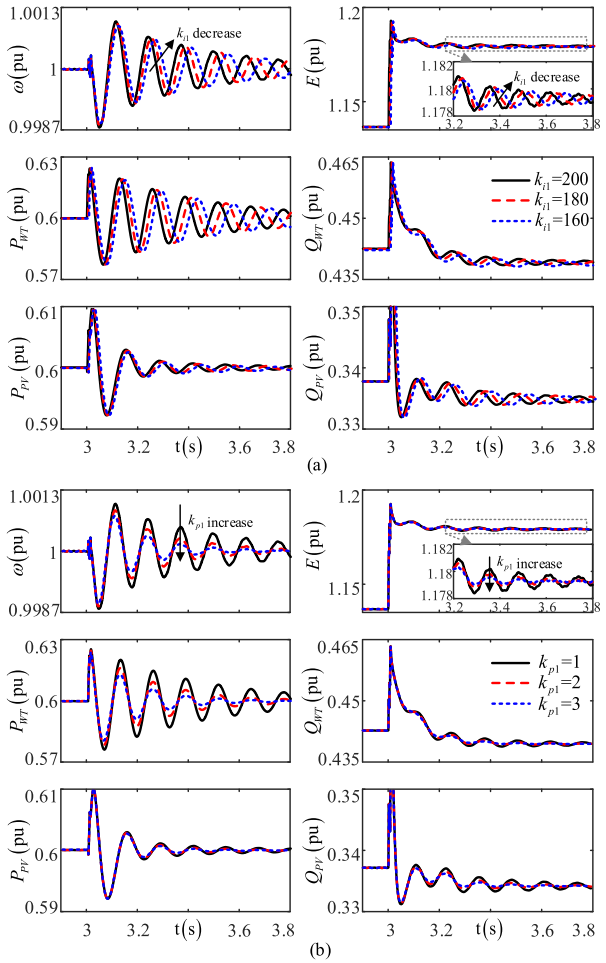


**FIGURE 10.** Time domain simulation of the internal voltage amplitude/frequency and active/reactive powers for different control parameters.

The different characteristics of the PE-interfaced device in DVC timescale illustrated by the stimulation-response relationships of the proposed model can lead to different system dynamics. This implies that we can further tune and optimize the characteristics of the PE-interfaced device in DVC timescale for the dynamic stability of the multi-device system based on our model. These studies will be conducted in the near future.

## VI. CONCLUSION

For dynamic issues in DVC timescale associated with multi-device interaction involving DVC and ACC of PE-interfaced devices, this paper proposes a modeling method of the PE-interfaced device to analyze the characteristic and role of the device in the dynamics of the multi-device interaction. The main conclusions are listed as follows:

(1) The mechanism of the PE-interfaced device to participate in system dynamics is recognized. Both the ACC and DVC timescale components act on the grid by regulating the internal voltage amplitude/frequency. The characteristics of the PE-interfaced device are manifested as the regulation of the internal voltage magnitude/frequency according to the active/reactive power imbalance.

(2) The model of the PE-interfaced device based on the relationships between power-imbalance stimulation and internal-voltage response, which depicts the regulation of the internal voltage amplitude/frequency by the detailed controls under the active/reactive power imbalance, is established. To directly depict the regulation by the main DVC timescale component, the model of the PE-interfaced device with ideal ACC is further proposed through the infinity gain equivalence of ACC.

(3) The coupling and high-order characteristics the PE-interfaced device in DVC timescale are revealed based on the proposed model. The characteristics of the device affected by the control parameters are reflected in the internal voltage amplitude/frequency. No matter what control parameters are chosen, the PE-interfaced device affects system dynamics by regulating the internal voltage amplitude/frequency.

The regulation of the internal voltage amplitude/frequency according to the active/reactive power imbalance, which illustrates the characteristics of the PE-interfaced device, can be optimized based on the proposed model. The optimization of the characteristics of the PE-interfaced device for the dynamic stability of the multi-device system in DVC timescale will be studied in the near future.

## APPENDIX A
## DETAILED MATHEMATICAL EXPRESSIONS OF THE DVC AND ACC TIMESCALE COMPONENTS

### A. DVC TIMESCALE COMPONENT

$$C_{dc}:\ U_{dc}=\sqrt{(2/C)\int (P_{in}-P)\,dt}$$

$$\begin{aligned}\text{DC voltage control}:\ i_{dr}^{p}&=\left(k_{p1}+k_{i1}/s\right)\left(U_{dc}-U_{dcr}\right)\\&=\left(k_{i1}/s\right)\left(T_1 s+1\right)\left(U_{dc}-U_{dcr}\right)\\&=\left(k_{i1}/s\right)G_1\left(s\right)\left(U_{dc}-U_{dcr}\right)\end{aligned}$$

$$\begin{aligned}\text{Reactive power control}:\ i_{qr}^{p}&=\left(k_{p2}+k_{i2}/s\right)\left(Q_t-Q_{tr}\right)\\&=\left(k_{p2}+k_{i2}/s\right)\left(Q-Q_r\right)\\&=\left(k_{i2}/s\right)\left(T_2 s+1\right)\left(Q-Q_r\right)\\&=\left(k_{i2}/s\right)G_2\left(s\right)\left(Q-Q_r\right)\end{aligned}$$

### B. ACC TIMESCALE COMPONENT

$$\begin{aligned}d\text{-axis current control}:\ e_d^p&=\left(k_{p3}+k_{i3}/s\right)\left(i_{dr}^p-i_d^p\right)\\&=\left(k_{i3}/s\right)\left(T_3 s+1\right)\left(i_{dr}^p-i_d^p\right)\\&=\left(k_{i3}/s\right)\left(T_3 s+1\right)\varepsilon i_d^p\\&=\left(k_{i3}/s\right)G_3\left(s\right)\varepsilon i_d^p\end{aligned}$$

$$\begin{aligned}q\text{-axis current control}:\ e_q^p&=\left(k_{p3}+k_{i3}/s\right)\left(i_{qr}^p-i_q^p\right)\\&=\left(k_{i3}/s\right)\left(T_3 s+1\right)\left(i_{qr}^p-i_q^p\right)\\&=\left(k_{i3}/s\right)\left(T_3 s+1\right)\varepsilon i_q^p\end{aligned}$$

$$
\begin{aligned}
&= (k_{i3}/s)\, G_3\,(s)\, \varepsilon i_q^p \\
\text{PLL control}:\ \theta_p &= 1/s \cdot \left(k_{p4} + k_{i4}/s\right) \cdot \\
&\quad \times \sin\left(\theta_t - \theta_p\right) \\
&= (k_{i4}/s)\left[\left(T_4 s + 1\right)/s\right] \\
&\quad \times \sin\left(\theta_t - \theta_p\right) \\
&= (k_{i4}/s)\left[\left(T_4 s + 1\right)/s\right] \sin\left(\theta_p^t\right) \\
&= (k_{i4}/s)\, G_4\,(s) \sin\left(\theta_p^t\right)
\end{aligned}
$$

$$
\begin{aligned}
L_f:\ V_t \cdot e^{j\theta_t} &= E \cdot e^{j\int \omega dt} \\
&\quad - L_f d\left(I \cdot e^{j\int \omega_i dt}\right)/dt
\end{aligned}
$$

### C. TRANSFORMATION

$$
T_1\left(i_{dr}^p, i_{qr}^p \to i_{dr}^e, i_{qr}^e\right):\ i_{dr}^e + j i_{qr}^e = \left(i_{dr}^p + j i_{qr}^p\right) \cdot e^{j(\theta_p - \theta_e)}
$$

$$
T_2\left(\varepsilon i_d^e, \varepsilon i_q^e \to \varepsilon i_d^p, \varepsilon i_q^p\right):\ \varepsilon i_d^p + j\varepsilon i_q^p = \left(\varepsilon i_d^e + j\varepsilon i_q^e\right) \cdot e^{j(\theta_e - \theta_p)}
$$

$$
T_3\left(e_d^p, e_q^p \to E, \omega\right):\ E \cdot e^{j\int \omega dt} = \left(e_d^p + j e_q^p\right) \cdot e^{j\theta_p}
$$

$$
T_4\left(i_d^e, i_q^e \to I, \omega_i\right):\ I \cdot e^{j\int \omega_i dt} = \left(i_d^e + j i_q^e\right) \cdot e^{j\int \omega dt}
$$

## APPENDIX B
## RELATIONSHIP BETWEEN ACTIVE/REACTIVE CURRENT ERROR AND PHASE ERROR

Combining equations of $L_f$ and $T_4$, the equation of $f_1\left(L_f\right)$can be obtained as

$$
\begin{aligned}
\theta_t^e = \theta_e - \theta_t = \arctan\Big[&\left(sL_f i_q^e + \omega L_f i_d^e\right)/ \\
&\times \left(E - sL_f i_d^e + \omega L_f i_q^e\right)\Big]
\end{aligned}
$$

where $\theta_e = \int \omega dt$. The relationship in the red dashed box is $\theta_p^t = f\left(\varepsilon i_d^e, \varepsilon i_q^e, i_{dr}^e, i_{qr}^e\right)$.

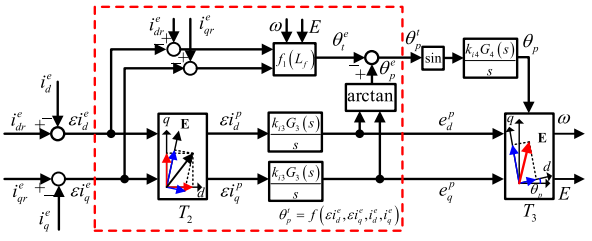


**FIGURE 11.** Relationship between active/reactive current error and phase error in the ACC timescale component.

## APPENDIX C
## PARAMETERS OF THE STUDY SYSTEM

### A. PARAMETERS VALUES OF THE TRANSMISSION LINES

**TABLE 1.** Parameters values of the transmission lines.

| Line name | Value (km) | Line name | Value (km) |
|---|---|---|---|
| $L_{tw}$ | 10 | $L_{tg}$ | 10 |
| $L_{tp}$ | 10 | $L_{t1}$ | 210 |
| $L_{t2}$ | 30 | | |

### B. PARAMETERS VALUES OF THE PMSG-BASED WT

Rated values: $S_{base\_WT} = 2$ MW, $V_{base\_WT} = 690$ V, $f_{base} = 50$ Hz, $U_{dcbase\_WT} = 1200$ V.

**TABLE 2.** Controller parameters values of the PMSG-based WT.

| Parameter | Value (pu) | Parameter | Value (pu) |
|---|---|---|---|
| DC voltage control ($k_{p1}$, $k_{i1}$) | (1, 200) | AC current control ($k_{p3}$, $k_{i3}$) | (1, 500) |
| Reactive power control ($k_{p2}$, $k_{i2}$) | (0.1, 10) | PLL control ($k_{p4}$, $k_{i4}$) | (100, 4800) |

### C. PARAMETERS VALUES OF THE PV

Rated values: $S_{base\_PV} = 400$ kW, $V_{base\_PV} = 260$ V, $f_{base} = 50$ Hz, $U_{dcbase\_PV} = 500$ V

**TABLE 3.** Controller parameters values of the PV.

| Parameter | Value (pu) | Parameter | Value (pu) |
|---|---|---|---|
| DC voltage control ($k_{p1}$, $k_{i1}$) | (5, 200) | AC current control ($k_{p3}$, $k_{i3}$) | (1, 200) |
| Reactive power control ($k_{p2}$, $k_{i2}$) | (1, 50) | PLL control ($k_{p4}$, $k_{i4}$) | (50, 1200) |

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