## RESEARCH ARTICLE

# Normally-Off AlGaN/GaN HEMTs With a Low Reverse Conduction Turn-On Voltage

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**ABSTRACT** Third quadrant operation is vital for power applications such as synchronous DC-DC converters and inverters, which require a low drain-source voltage drop to reduce conduction losses. However, typical gallium nitride (GaN) transistors have a higher voltage drop when the gate is off. To address this issue, we propose a dual-gate high-electron-mobility transistor (HEMT) to enhance reverse conduction. The device is modulated by the main gate electrode adjacent to the source, while a fixed bias is applied on the auxiliary gate electrode near the drain contact. We achieve a reverse conduction voltage as low as $-0.16$ V and 89.03 % lower reverse conduction power loss with the proposed device structure. The results can be explained by a freewheeling path between the drain electrode and the auxiliary gate, which enables effective dissipation of the stored charges.

**INDEX TERMS** Dual-gate (DG) structure, GaN, HEMT, reverse conduction.

## I. INTRODUCTION

Low-loss switches with a strong reverse blocking capability are desired in power electronic systems. GaN-based high-electron-mobility transistors (HEMTs) possess a high off-state breakdown voltage ($V_{BR}$), low on-state resistance, and high-switching speed, making them one of the favored candidates for compact and high-efficiency power applications [1], [2], [3]. Generally, the reverse conduction path is required in the low-side transistor for typical power conversion to avoid a large voltage drop in power-switching circuits, such as AC-DC inverters and DC-DC converters at the off-state. For silicon (Si) and silicon carbide (SiC) power transistors, the body diode inherently exists to ensure the release of the stored charges at the off-state. However, there is no body diode in a planar structure AlGaN/GaN HEMTs. As a result, when GaN HEMT is adopted for DC-DC converters, the transistor is usually paired with an external diode to allow reverse conduction current flow at the off-state to help dissipate the stored charges. For example, the GaN transistors

were connected with the intrinsic body diode of Si metal-oxide-semiconductor field-effect transistor (MOSFET) heterogeneously [4], [5], [6] or with the Si Schottky barrier diodes (SBDs) in the backside of Si substrate [7]. There were methods to avoid the parasitic effects [8] of the heterogeneous wire connection by monolithically fabricating GaN HEMTs and reverse current conduction components. The GaN transistors can be integrated with a lateral rectifier [9] or a GaN-based built-in diode in the source contact [10], [11], [12]. In addition, an RC-HEMT (reverse-conduction HEMT) with integrated tri-anode SBDs was demonstrated [13] to provide a sufficient freewheeling capability for reverse conduction. There was also a device simulation on establishing a freewheeling path of the reverse current between the second gate deposited on a regrown p-GaN and the drain [14]. The above approaches exhibited good reverse conduction characteristics with the reverse turn-on voltage between $-0.46$ and $-1$ V under a reverse drain current of 1 mA/mm from the 3rd quadrant current-voltage curves. However, some of the above approaches include extra diodes or additional steps of material regrowth, making the fabrication of low-reverse conduction transistors complicated.

The associate editor coordinating the review of this manuscript and approving it for publication was Marcelo Antonio Pavanello [ID].
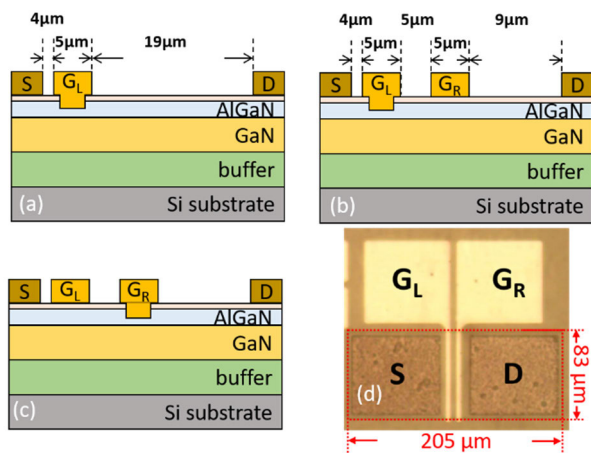
**FIGURE 1.** The schematic cross-sectional structure of an SG-HEMT (a) and DG-HEMT with a recessed gate on the left (b) and right (c). (d) OM image of the DG-HEMT. The red frame indicates the mesa region.

Previously, we demonstrated that the DG GaN HEMTs could effectively suppress the current collapse phenomenon [15]. The fixed voltage at the additional gate electrode attracts extra electrons to compensate depleted carriers due to current collapse. Since the introduction of DG affects the carrier re-distribution in the channel, the induced carrier may provide a freewheeling path of current flow at off-state. That is, additional carriers may accumulate in the channel, resulting in the earlier turn-on of the device from the off-state. In this work, we designed DG-HEMTs and characterized their reverse conduction behaviors. Unlike employing the 2nd gate as the source field plate [10], [11], gate bias voltages can be separately applied on these two gate electrodes, allowing the flexibility of adjusting the reverse current flow across gate electrodes. Our results demonstrate a lower reverse conduction turn-on voltage for power-switching applications.

## II. DEVICE FABRICATION
Fig. 1(a) - (c) shows the schematic illustrations of a single-gate (SG) and a DG AlGaN/GaN HEMT. The SG-HEMT in Fig. 1(a) is a trench gate structure for baseline reference. The gate length, $L_G$, and width, $W_G$, are 5 and 80 $\mu$m, respectively. For a DG-HEMT, the distance between the left gate ($G_L$) and the source electrode, $L_{GL-S}$, is 4 $\mu$m; the right gate ($G_R$) and the drain electrode, $L_{GR-D}$, is 9 $\mu$m; and $G_L$ and $G_R$ is 5 $\mu$m. As shown in Fig. 1(b) and (c), the recessed $G_L$ and $G_R$ having a footprint of 3 $\mu$m is denoted as "main gate" and is used to modulate (drive) the device.

The epitaxy layer structure grown on the Si substrate consists of a nucleation layer, 4 $\mu$m-thick Carbon-doped (C-doped) GaN buffer layer, 0.3 $\mu$m un-doped GaN channel, 20 nm AlGaN layer with a 25% Al content, and 3 nm GaN cap layer. The device fabrication started with mesa isolation by inductively coupled plasma reactive-ion etching (ICP-RIE) using a gas mixture of BCl$_3$ and Cl$_2$ with an etching depth of around 200 nm. The gate recessed region was defined by ICP-RIE with a depth of around 13 nm. Next, source and

drain ohmic contacts, Ti/Al/Ni/Au (25/125/50/125 nm), were evaporated, followed by rapid thermal annealing (RTA) at 900 °C for 30 s in N$_2$ ambient. The Ni/Au (20/300 nm) Schottky gate was then deposited. All the samples were fabricated simultaneously on the same wafer.

## III. RESULTS AND DISCUSSION
The $I_{DS}$-$V_{GS}$ (drain current – gate voltage) transfer curves of the SG-HEMT and DG-HEMT with the drain voltage ($V_{DS}$) fixed to 5 V are shown in Fig. 2(a). For the DG-HEMT, "$G_L$-drive/$G_R$-bias" means a gate bias is applied on the electrode of $G_L$ to modulate (drive) the device, while $G_R$ is applied by a fixed bias to replenish carriers depleted by the recessed gate ($G_L$) in the channel. In such a case, $G_L$ is the "main gate", while $G_R$ is considered the "auxiliary gate". The SG-HEMT exhibits a normally-off operation with a threshold voltage ($V_{TH}$) of 1.07 V. For the DG-HEMT, when the auxiliary gate voltage, $V_{GR\_Aux}$, is biased at 0 and +1 V, the $V_{TH}$ is 1.02 and 1.12 V, respectively (under the $G_L$-drive). Ideally, the threshold voltage of the SG-HEMT and the DG-HEMT w/$V_{GR\_Aux}$ = 0 V should be the same, but there are small variations in the gate recess depth among devices. In forward conduction, the output characteristics of the SG-HEMT and the DG-HEMT with $V_{GR\_Aux}$ biased at 0 and +1 V are shown in Fig. 2(b), (c) and (d), respectively. For a DG-HEMT, the saturation current level at a high main gate bias is lowered than that of an SG-HEMT. It is mainly because the $V_{GR\_Aux}$ limits the 2DEG carriers underneath the auxiliary gate. For switching power operations, one of the critical parameters, channel on-resistance ($R_{ON(fwd)}$), is less affected. $R_{ON(fwd)}$ of the SG-HEMT and DG-HEMT with $V_{GR\_Aux}$ of 0 and +1 V is 22.34, 27.73, and 24.83 $\Omega \cdot$ mm, respectively, at $V_{GS}$ = 3V. The increase of $R_{ON(fwd)}$ of the DG-HEMT can be explained by the decrease of channel carriers underneath the auxiliary Schottky gate electrode [16].
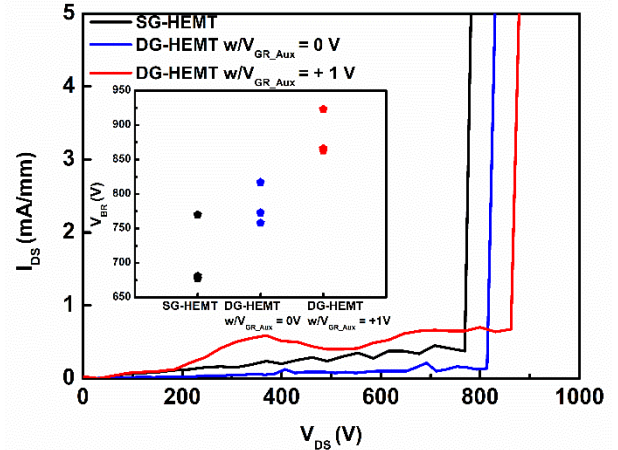
The breakdown voltage ($V_{BR}$) of the devices is next examined. By applying $V_{GS}$ at −2V (off-state) and auxiliary gate at 0 and +1 V, the $I_{DS}$-$V_{DS}$ curves of the SG-HEMT and the DG-HEMT with "$G_L$-drive/$G_R$-bias" are shown in Fig. 3. At the defined breakdown current level of 1 mA/mm, $V_{BR}$ of SG-HEMT is measured to be 770 V. In contrast, for DG-HEMT with $V_{GR\_Aux}$ = 0 and + 1 V on $G_R$, the $V_{BR}$ are 817 and 863 V, respectively. The inset illustrates the distribution of measured breakdown voltage for 3 devices of each type. The $V_{BR}$ of SG-HEMTs is within the range of 650 to 800 V, while for DG-HEMTs w/ $V_{GR\_Aux}$ = 0 and + 1 V, the ranges are 750 to 850 V and 850 to 950 V, respectively. Compared to the SG-HEMT, the slightly larger $V_{BR}$ of the DG-HEMT is attributed to the metal ring effect to suppress the electric field intensity underneath $G_R$ (the gate electrode near the drain side) [16], [17], [18], [19]. Moreover, as we compare the breakdown voltage of the DG-HEMT with $V_{GR\_aux}$ = 0 or 1 V, the major difference lies in the amount of 2DEG carriers underneath the auxiliary gate. For the device with the 2DEG carriers attracted under a positive auxiliary gate voltage, the increase of drain voltage first
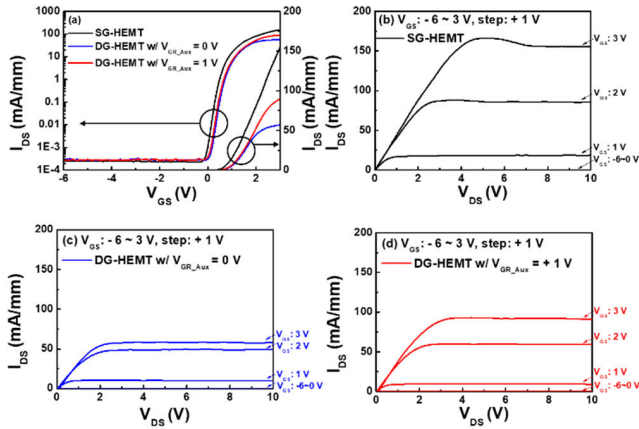
**FIGURE 2.** (a) Transfer curves of an SG-HEMT and a DG-HEMT with the $G_L$-drive/$G_R$-bias ($V_{GR\_Aux}$ = 0 and +1 V) configuration. The $I_D$-$V_D$ modulation curves of (b) an SG-HEMT, (c) a DG-HEMT with $G_L$-drive/$G_R$-bias ($V_{GR\_Aux}$ = 0 V), and (d) a DG-HEMT with $G_L$-drive/$G_R$-bias ($V_{GR\_Aux}$ = +1 V) in forward-conduction mode.



**FIGURE 3.** (a) Breakdown voltage measurement of the SG-HEMT and DG-HEMT with $G_L$-drive/$G_R$-bias. The inset shows the distribution of measured breakdown voltage of three types of device.



**FIGURE 4.** Reverse $I_{DS}$-$V_{DS}$ curves of an SG-HEMT (a), a $G_L$-drive/$G_R$-bias DG-HEMT with $V_{GR\_Aux}$ of 0 V (b) and $V_{GR\_Aux}$ of +1 V (c). (d) A $G_R$-drive/$G_L$-bias DG-HEMT with $V_{GL\_Aux}$ of 0 V.

depletes channel carriers before building up an electric field in the auxiliary electrode. Thus, the breakdown phenomenon occurs at a higher drain voltage in the case of 1V auxiliary gate voltage. Moreover, the surface leakage current increases with a higher auxiliary gate voltage because of larger 2DEG carriers and the induced surface states. It explains a higher leakage current when $V_{GR\_aux}$ increases from 0 to 1V.

The reverse conduction turn-on voltage, $V_{SD}$(where $V_{SD}$ is equivalent to $-V_{DS}$), is a parameter for evaluating the device performance in the third quadrant. Due to the inherent reverse conduction capability, the current also conducts when the device is switched off. The device acts like a diode in the third quadrant, in which $V_{SD}$ is determined from the drain voltage at a given constant drain current value of $-1$ mA/mm [20], [21]. In order to understand how the DG device structure affects the reverse conduction properties, we next measured the third-quadrant current-voltage ($I_{DS}$-$V_{DS}$) curves. Fig. 4. shows the plot of the output characteristics of the SG-HEMT and the DG-HEMT with "$G_L$-drive/$G_R$-bias" and "$G_R$-drive/$G_L$-bias" in the third quadrant. At the reverse on-state, the SG-HEMT exhibits a relatively higher $V_{SD}$ of 6.58 V (at $I_{DS}$ of $-1$ mA/mm and $V_{GS}$ of $-6$ V), shown in Fig. 4(a). For the "$G_L$-drive/$G_R$-bias" case, it can be observed that the $V_{SD}$ shifts from 2.22 to 0.16 V when the auxiliary gate bias increases from 0 to +1 V, shown in Fig. 4(b) and (c). SG-HEMT shows typical third quadrant electrical properties of GaN-based HEMTs in which I-V curves are distinctively dependent on the applied gate voltage. A lower drain current is obtained when the gate bias is more negative. On the other hand, for a "$G_R$-drive/$G_L$-bias" DG-HEMT, the channel is conducting at a low absolute value of drain voltage, even at a more negative gate voltage. The I-V curves are more closely overlapped when $V_{GR\_Aux}$ is applied with +1 V, as compared with a case with $V_{GR\_Aux}$ of 0 V. It suggests that higher current conduction can be obtained when the auxiliary gate is more positively biased.
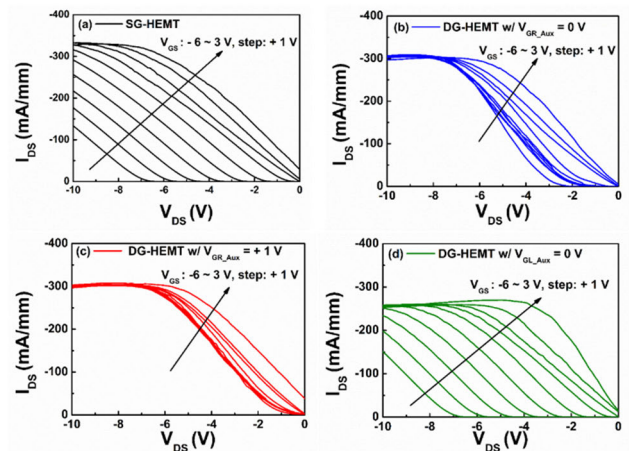
For comparison, when the DG-HEMT is in a "$G_R$-drive/$G_L$-bias" configuration, shown in Fig. 4(d), the reverse output characteristic is similar to that of SG-HEMT, suggesting the reverse current conduction is limited. In Fig. 4(d), $V_{SD}$ is 6.67 V, close to the value of the SG-HEMT. It indicates that the DG-HEMT with a "$G_R$-drive/$G_L$-bias" configuration does not possess a freewheeling path to dissipate the stored energy appropriately in the reverse direction.

The main gate and auxiliary gate currents were next extracted to understand the current flow paths. Fig. 5(a) shows the measurement setups of DG-HEMTs with "$G_L$-drive/$G_R$-bias" (upper graph) and "$G_R$-drive/$G_L$-bias" (lower graph). The auxiliary gate currents are demonstrated in Fig. 5(b), (c), and (d) for DG-HEMTs with $V_{GR\_Aux}$ of 0 V, $V_{GR\_Aux}$ of 1 V, and $V_{GL\_Aux}$ of 0 V, respectively. For the "$G_L$-drive/$G_R$-bias" case, $I_{GR\_Aux}$ decreases from a higher current level when $V_{GS}$ increases from $-6$ V, while the $I_{GL\_Aux}$ in "$G_R$-drive/$G_L$-bias" is kept at a relatively lower value. As we compare Fig. 5(b)$\sim$(d) with Fig. 4(b)$\sim$(d), the reverse conduction drain current of "$G_L$-drive/$G_R$-bias" case
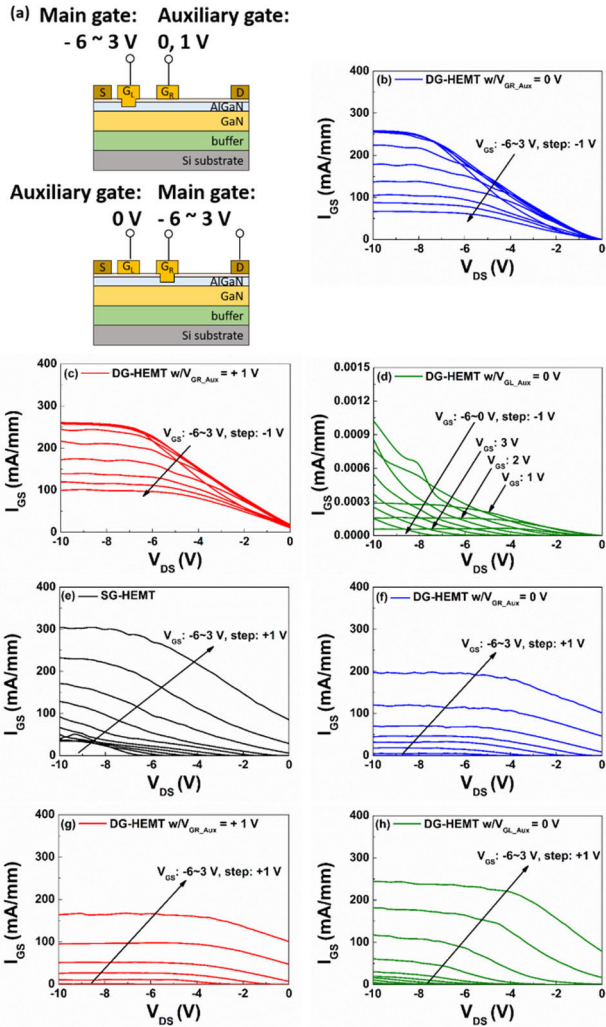
**FIGURE 5.** (a) Schematic diagram of the DG-HEMT with "$G_L$-drive/$G_R$-bias" (upper graph) and "$G_R$-drive/$G_L$-bias" (lower graph) for gate current measurements. The auxiliary gate current profiles ($I_{GS}$-$V_{DS}$) of a DG-HEMT with the (b) $G_L$-drive/$G_R$-bias ($V_{GR\_Aux} = 0$ V) (c) $G_L$-drive/$G_R$-bias ($V_{GR\_Aux} = +1$ V) and (d) $G_R$-drive/$G_L$-bias ($V_{GL\_Aux} = 0$ V) configurations. The main gate current profiles ($I_{GS}$-$V_{DS}$) of (e) an SG-HEMT, a DG-HEMT with the (f) $G_L$-drive/$G_R$-bias ($V_{GR\_Aux} = 0$ V), (g) $G_L$-drive/$G_R$-bias ($V_{GR\_Aux} = +1$ V) and (h) $G_R$-drive/$G_L$-bias ($V_{GL\_Aux} = 0$ V) configurations.

at lower main gate bias is contributed to the freewheeling current flow across the auxiliary gate electrode. The reverse drain current is significantly lower for the "$G_R$-drive/$G_L$-bias" case because the main gate negative voltage depletes 2DEG carriers and suppresses the current in the right auxiliary gate.

The main gate current distribution profiles of the SG- and DG-HEMTs are shown in Fig. 5(e)-(h). For the SG-HEMT, Fig. 4(a) and Fig. 5(e) suggest that the reverse conduction drain current mainly flows across the gate, which increases only when the Schottky gate-2DEG diode becomes conducting. As for the DG-HEMT with "$G_L$-drive/$G_R$-bias", the main gate current behaves differently from the auxiliary gate when $V_G$ increases. With the increase of main gate bias, $V_{GS}$, from around $-3$V, the auxiliary gate current decreases while the main gate current increases. The main and
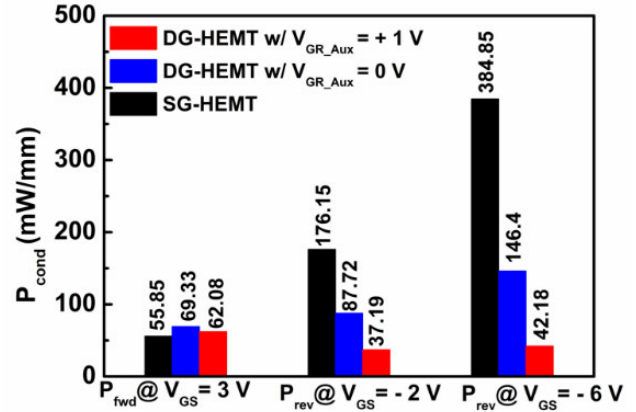


**FIGURE 6.** Comparison of estimated forward and reverse conduction loss of an SG-HEMT and a DG-HEMT at $V_{GR\_Aux} = 0$ and 1 V.

auxiliary gate current flows ensure drain current conduction for DG-HEMTs in Fig. 4(b) and (c). As for a DG-HEMT with "$G_R$-drive/$G_L$-bias", the main gate flow is similar to an SG-HEMT.

Generally, the total switching power loss compromises the switching and conduction loss ($P_{cond}$). The latter can be further categorized as the forward conduction loss ($P_{fwd}$) and reverse conduction loss ($P_{rev}$), in which $P_{fwd}$ is represented by [22]

$$P_{fwd} = I_{DS}^2 \times R_{ON(fwd)} \tag{1}$$

and $P_{rev}$ by [23]

$$P_{rev} = I_{SD}^2 \times R_{ON(rev)} + I_{SD} \times V_{SD} \tag{2}$$

where $I_{SD} = -I_{DS}$ and $R_{ON(rev)}$ is the channel resistance at the reverse conduction mode.

The $R_{ON(rev)}$ of the SG-HEMT, the DG-HEMT at $V_{GR\_Aux}$ of 0 V and 1V, is 20.03, 14.16 and 13.67 $\Omega\cdot$ mm, respectively, as extracted from the Fig. 4 at $V_{GS} = -6$ V. Assuming the operating drain current of 50 mA/mm, the forward conduction loss is calculated to be 55.85, 69.33 and 62.08 mW/mm, respectively, of an SG-HEMT, a DG-HEMT at $V_{GR\_Aux}$ of 0 and 1 V.

Fig. 6 summarizes the conduction loss of the devices in the forward and reverse modes. Although the DG-HEMT possesses ~11-24% higher on-resistance and thus a higher forward conduction loss, the reverse-conduction loss is significantly reduced by 89.03 % for a DG-HEMT with $V_{GR\_Aux}$ of 1V, and the corresponding $P_{cond}$ is decreased by 76.34 %. The reverse conduction loss is less severe when the off-state gate bias is higher. As shown in Fig. 6, at $V_{GS} = -2$ V, the reverse conduction loss of an SG-HEMT becomes 176.15 mW/mm, which, however, is still 4.74 times higher than that of the DG-HEMT at $V_{GR\_Aux}$ of 1 V.

We next explain the physical mechanism of reverse conduction based on carrier transport. The operation principle of the DG-HEMT can be understood from the carrier distribution schematically drawn in Fig. 7. When the device with "$G_L$-drive/$G_R$-bias" is at the off-state and $V_D$ is under a
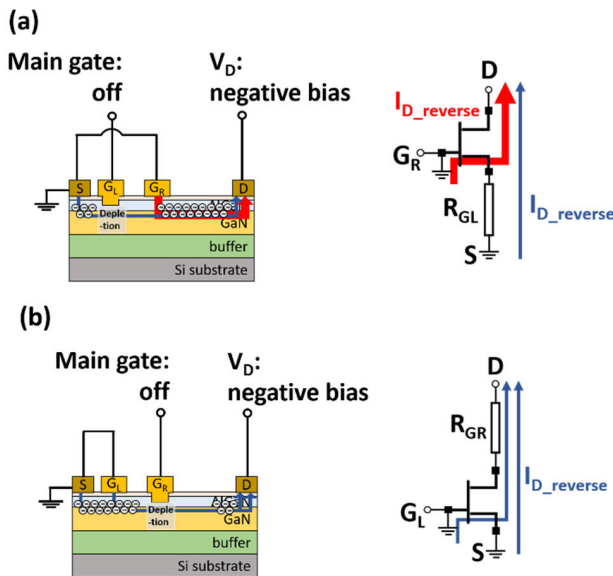
**FIGURE 7.** Carrier distribution of a DG-HEMT with (a) $G_L$-drive/$G_R$-bias and (b) $G_R$-drive/$G_L$-bias in reverse conduction. $R_{GL}$ and $R_{GR}$ are the channel resistance underneath the driving gate $G_L$ and $G_R$, respectively. The red arrow of $I_{D\_reverse}$ indicates the reverse conduction current without passing through the depleted resistive region, while the blue one is the current through the resistor.

**TABLE 1.** Comparisons of GaN HEMT electrical properties and the third quadrant performance.

| | $V_{TH}$ (V) | $V_{SD}$ (V) @ $I_{DS}$ = -1mA/mm | $R_{ON(fwd)}$ (Ω·mm) | $I_{D\_MAX}$ (mA/mm) | $P_{rev}$ (mW/mm) | Approaches |
|---|---|---|---|---|---|---|
| This work | 1.12 | 0.16 @ $V_{GS}$= -6V | 24.8 | 91 @$V_{GS}$=3V, $V_{DS}$=10V | 42.18 @$V_{GS}$= -6V | Dual-gate structure |
| [7] | ~ 1.8 | *0.85 | ~ 2.6 | ~900 @$V_{GS}$=5V, $V_{DS}$=10V | ** | Si-based SBD |
| [9] | 0.9 | *0.1 | ~11.11 | 350 @$V_{GS}$=3V, $V_{DS}$=10V | ** | Lateral Field-Effect Rectifier |
| [10] | 2 | 0.8 @ $V_{GS}$=0V | ~ 26.7 | 97 @$V_{GS}$=12V, $V_{DS}$=20V | 89.6 @$V_{GS}$=0V | Embedded SBD |
| [11] | ~ 3 | 1.0 @ $V_{GS}$=0V | ~14 | 252 @$V_{GS}$=16V, $V_{DS}$=12V | 74.2 @$V_{GS}$=0V | Embedded SBD |
| [12] | ~ - 2 | 1.4 @ $V_{GS}$=-9V | 11.1 | 619 @$V_{GS}$=1V, $V_{DS}$=10V | 115 @$V_{GS}$= -6V | Separated SBD |
| [13] | ~ - 3.5 | 0.55 @ $V_{GS}$=-7V | 8.83 | 240 @$V_{GS}$=3V, $V_{DS}$=5V | 53.83 @$V_{GS}$= -7V | Tri-anonde diodes |
| [20] | ~ 2 | 0.455 @ $V_{GS}$=-1V | 20 | 140 @$V_{GS}$=8V, $V_{DS}$=3V | 72.75 @$V_{GS}$= -1V | Lateral Schottky Barrier Controlled Schottky Rectifier |
| [21] | 1.8 | 0.6 @ $V_{GS}$=-4V | 12.1 | 300 @$V_{GS}$=8V, $V_{DS}$=10V | 70 @$V_{GS}$= -4V | Built-in SBD |

* Estimated from the SBD
** Third quadrant current-voltage curves not provided

negative bias, electrons under $G_L$ are depleted. A conduction path is formed between the negative voltage drain electrode and $G_R$ (0 or +1 V in our case) (see Fig, 7(a)). In addition, the

depleted region under $G_L$ can be considered a resistive path. In such a case, the DG-HEMT can be modeled as a transistor in series with a resistor at the off-state (see the right side of Fig. 7(a)). On the other hand, when the device is driven by $G_R$ and an additional bias is applied on $G_L$, i.e., "$G_R$-drive/$G_L$-bias" (with the results in Fig. 4(d)), the depleted region underneath $G_R$ is highly resistive (see Fig. 7(b)). The reverse conduction current is thus limited by the resistivity of the depleted region under $G_R$. The reverse conduction occurs when the drain bias is more negative than the gate bias, which explains a higher $V_{SD}$ in Fig. 4 (a) and (d).

A summary of research works on enhancing the reverse conduction of GaN HEMTs is listed in Table 1. Our DG-HEMT with "$G_L$-drive/$G_R$-bias" demonstrates a superior $V_{SD}$ performance than other HEMTs with a built-in diode. Although gate recess needs optimization to reduce channel on-resistance, $R_{ON}$, our DG-HEMT can be applied to future power electronics such as an AC-DC inverter which requires a low $V_{SD}$ to reduce power loss, improve conversion efficiency and achieve faster switching speed.

## IV. CONCLUSION

A DG HEMT structure with a separate auxiliary gate bias is proposed to enhance reverse conduction. The improvement of $V_{SD}$ is mainly attributed to the formation of the conduction path across the additional Schottky gate contact between gate-drain electrodes. For the "$G_L$-drive/$G_R$-bias" case, when a main gate bias is applied on $G_L$ and a positive bias on $G_R$, a freewheeling path is formed between the drain electrode and the $G_R$ to dissipate the stored charges effectively. A $V_{SD}$ as low as $-0.16$ V was obtained at $V_G$ of $-6$ V and $G_R$ bias of $+1$ V, which resulted in the significant reduction of $P_{rev}$ by 89.03 %. Finally, a circuit model that illustrates the conduction path of the DG-HEMT was utilized to explain the reverse conduction of the proposed devices.

## REFERENCES

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[2] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[3] A. S. A. Fletcher and D. Nirmal, "A survey of gallium nitride HEMT for RF and high power applications," *Superlatt. Microstruct.*, vol. 109, pp. 519–537, Sep. 2017, doi: 10.1016/j.spmi.2017.05.042.

[4] X. Huang, Z. Liu, Q. Li, and Fred. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 1279–1286, doi: 10.1109/APEC.2013.6520464.

[5] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014, doi: 10.1109/TPEL.2013.2264941.

[6] X. Huang, W. Du, F. C. Lee, Q. Li, and Z. Liu, "Avoiding Si MOSFET avalanche and achieving zero-voltage switching for cascode GaN devices," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 593–600, Jan. 2016, doi: 10.1109/TPEL.2015.2398856.

[7] T. Morita, S. Ujita, H. Umeda, Y. Kinoshita, S. Tamura, Y. Anda, T. Ueda, and T. Tanaka, "GaN gate injection transistor with integrated Si Schottky barrier diode for highly efficient DC–DC converters," in *IEDM Tech. Dig.*, Dec. 2012, p. 7, doi: 10.1109/IEDM.2012.6478996.

[8] S. Jiang, K. B. Lee, I. Guiney, P. F. Miaja, Z. H. Zaidi, H. Qian, D. J. Wallis, A. J. Forsyth, C. J. Humphreys, and P. A. Houston, "All-GaN-Integrated cascode heterojunction field effect transistors," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8743–8750, Nov. 2017, doi: 10.1109/TPEL.2016.2643499.

[9] W. Chen, K.-Y. Wong, and K. J. Chen, "Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796635.

[10] B.-R. Park, J.-G. Lee, and H.-Y. Cha, "Normally-off AlGaN/GaN-on-Si power switching device with embedded Schottky barrier diode," *Appl. Phys. Exp.*, vol. 6, no. 3, Mar. 2013, Art. no. 031001, doi: 10.7567/APEX.6.031001.

[11] B.-R. Park, J.-Y. Lee, J.-G. Lee, D.-M. Lee, M.-K. Kim, and H.-Y. Cha, "Schottky barrier diode embedded AlGaN/GaN switching transistor," *Semicond. Sci. Technol.*, vol. 28, no. 12, Oct. 2013, Art. no. 125003, doi: 10.1088/0268-1242/28/12/125003.

[12] R. Reiner, P. Waltereit, B. Weiss, M. Wespel, R. Quay, M. Schlechtweg, M. Mikulla, and O. Ambacher, "Integrated reverse-diodes for GaN-HEMT structures," in *Proc. IEEE 27th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 45–48, doi: 10.1109/ISPSD.2015.7123385.

[13] T. Wang, J. Ma, and E. Matioli, "1100 V AlGaN/GaN MOSHEMTs with integrated tri-anode freewheeling diodes," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1038–1041, Jul. 2018, doi: 10.1109/LED.2018.2842031.

[14] K. S. Sriramadasu and Y.-M. Hsin, "Normally-off p-GaN gate AlGaN/GaN transistor with a new Schottky second gate," *ECS J. Solid State Sci. Technol.*, vol. 11, no. 10, Oct. 2022, Art. no. 105004, doi: 10.1149/2162-8777/ac9602.

[15] D.-J. Lin, J.-Y. Yang, C.-K. Chang, and J.-J. Huang, "Study of current collapse behaviors of dual-gate AlGaN/GaN HEMTs on Si," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 59–64, 2022, doi: 10.1109/JEDS.2021.3132429.

[16] W. Li, Z. Zhang, K. Fu, G. Yu, X. Zhang, S. Sun, L. Song, R. Hao, Y. Fan, Y. Cai, and B. Zhang, "Design and simulation of a novel E-mode GaN MIS-HEMT based on a cascode connection for suppression of electric field under gate and improvement of reliability," *J. Semicond.*, vol. 38, no. 7, Jul. 2017, Art. no. 074001, doi: 10.1088/1674-4926/38/7/074001.

[17] M.-W. Ha, S.-C. Lee, J.-C. Her, K.-S. Seo, and M.-K. Han, "AlGaN/GaN high-electron-mobility transistor employing an additional gate for high-voltage switching applications," *Jpn. J. Appl. Phys.*, vol. 44, p. 6385, Sep. 2005, doi: 10.1143/JJAP.44.6385.

[18] S. C. Lee, M. W. Ha, J. C. Her, S. S. Kim, J. Y. Lim, K. S. Seo, and M. K. Han, "High breakdown voltage GaN Schottky barrier diode employing floating metal rings on AlGaN/GaN hetero-junction," in *Proc. IEEE 17th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Aug. 2005, pp. 247–250, doi: 10.1109/ISPSD.2005.1487997.

[19] S.-C. Lee, J.-C. Her, S.-S. Kim, M.-W. Ha, K.-S. Seo, Y.-I. Choi, and M.-K. Han, "A new vertical GaN Schottky barrier diode with floating metal ring for high breakdown voltage," in *Proc. 16th Int. Symp. Power Semiconductor Devices IC's*, 2004, pp. 319–322, doi: 10.1109/WCT.2004.240037.

[20] L. Bi, X. Kang, X. Wang, H. Yin, J. Fan, K. Wei, Y. Zheng, S. Huang, and X. Liu, "Monolithic integrated normally OFF GaN power device with antiparallel lateral Schottky barrier controlled Schottky rectifier," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1778–1783, Apr. 2021, doi: 10.1109/TED.2021.3058114.

[21] J. Lei, J. Wei, G. Tang, Q. Qian, Z. Zhang, M. Hua, Z. Zheng, and K. J. Chen, "Reverse-conducting normally-OFF double-channel AlGaN/GaN power transistor with interdigital built-in Schottky barrier diode," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2106–2112, May 2019, doi: 10.1109/TED.2019.2904038.

[22] J. Klein. (Nov. 21, 2024). *Synchronous Buck MOSFET Loss Calculations With Excel Model*. [Online]. Available: https://www.fairchildsemi.com/design/design-tools/switching-loss-calculation-tool/

[23] B. Sun, "Does GaN have a body diode?—Understanding the third quadrant operation of GaN," Texas Instrum., Dallas, TX, USA, Appl. Rep. SNOAA36, Feb. 2019.

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