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RESEARCH ARTICLE

Investigation Into the Degradation of DDR4 DRAM Owing to Total Ionizing Dose Effects

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ABSTRACT Total ionizing dose (TID) effects of gamma rays were investigated on DDR4 dynamic random access memory (DRAM) and analyzed using TCAD simulations. In this study, we considered the operating states, dose rates, temperatures, and annealing to analyze the impact of TID under different conditions. The worst degradation was observed in the operated state and at a low-dose rate because of the absence of an electrostatic barrier that reduced the possibility of interface trap formation under unbiased and high-dose rate conditions. At lower temperatures, the effects of radiation were mitigated by the reduced production of protons (H^+). In addition, the unbiased DRAM and high-temperature conditions are the fastest to recover during post-irradiation annealing. In TCAD simulations, the retention time decreased with increasing temperature because the band-to-band tunneling (BTBT) generation increased. Furthermore, the retention time and row activation latency (t_{RCD}) degraded as the concentration of the interface traps increased. This is because the interface traps caused leakage currents and hindered the flow of electrons.

INDEX TERMS Annealing, DDR4, dose rate, DRAM, gamma ray, interface trap, operation, retention time, temperature.

I. INTRODUCTION

Dynamic random access memory (DRAM) is widely used not only in electronic devices such as smartphones and computers but also in harsh environments such as electric vehicles, spacecraft, and satellites [1]. Owing to its multifaceted applications, DRAM is critical for the stability and functionality of various systems. Failures within DRAM may precipitate catastrophic effects, including data loss from the blue screen in personal computing systems, mission failures in aerospace operations, or even fatalities during failures of autonomous vehicles. Therefore, an advance in research to enhance the reliability of DRAM is of utmost importance.

DRAM organized in one transistor-one capacitor (1T-1C) architecture stores binary information ('1' or '0'), depending on the state of charge of the capacitor [2], [3]. Although effective, this data storage strategy is susceptible to leakage currents. The charge stored in the capacitor leaks over time, thus leading to data loss. To prevent data loss, the JEDEC standard mandates a periodic refresh of DRAM every 64 ms [4]. Nevertheless, when a DRAM is exposed to a radiation environment, it may encounter a single-event upset (SEU) phenomenon, which leads to transient bit flips [5], [6], or exhibit total ionizing dose (TID) effects, which reduce the retention time to less than 64 ms [7], [8], [9], [10], [11], [12].

Ionizing radiation can induce charge accumulation in oxides and insulators, potentially leading to device degradation and failure. The mechanism of the TID effect has been extensively researched [13], [14], [15], [16], [17], [18]. When semiconductors are subjected to gamma radiation, traps are generated at the interface between SiO_2 and Si. In semiconductors with an N-channel MOS structure, traps are

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generated; oxide traps carry a positive charge and interface traps carry a negative charge [19]. These traps can induce severe performance degradation in semiconductor devices, such as increased leakage current, decreased on-current, and changed threshold voltage [20]. In the case of DRAM, the same degradation can be caused by TID, and this degradation can reduce the retention time of DRAM. A principal factor contributing to the reduction in retention time was the gate-induced drain leakage current (GIDL) at the storage node (SN) in DRAM. This effect is primarily facilitated by the trap-assisted tunneling (TAT) mechanism in interface traps [21], [22], [23].

A previous study evaluated the retention times to observe the TID effects in DRAM using ^{60}Co gamma sources [8]. This paper compared the variable retention time (VRT) related to the capacity of DRAM and verified that radiation-induced VRT can induce intermittently stuck bits (ISBs) and cause bit errors [8]. The row hammer effects of the TID on the timing parameters were analyzed, and the activation energy of the interface trap was extracted [7]. Although these studies are valuable because they provide an insightful analysis of the impact of TID on DRAM, they are limited because they study only unbiased states. It is essential to investigate the effect of TID by comparing the operated and unbiased states, considering that the concentration of interface trap generation can fluctuate with changes in the electric field [24]. A study exists that undertakes real-time evaluations [9]. However, its scope is limited owing to its exclusive focus on DDR3 DRAM. In addition, there has been no comparison of dose rate effects in TID studies on DRAM. Considering the impact of dose rate effects, known as enhanced low-dose rate sensitivity (ELDRS) in bipolar devices, it is difficult to evaluate the impact of radiation on DRAMs at a single dose rate [25], [26], [27], [28]. Moreover, it is essential to note that the assurance of data retention time in DRAM is subject to potential variations influenced by external factors such as temperature. Most memory manufacturers require an evaluation of ambient temperatures, however, no previous study has evaluated the temperature dependence and TID effects of DRAM simultaneously with real-time measurements.

In this study, we evaluated the effects of radiation on the DDR4 DRAM by considering conditions such as operations, dose rates and temperatures. Because DRAM cell transistors are classified as confidential, device-level measurements are difficult; therefore, TCAD simulations were utilized to analyze the DRAM devices under different conditions.

II. TEST EQUIPMENT SETUP

To study the effect of TID on DDR4 DRAM, this experiment was conducted at the low-level gamma-ray irradiation facility operated by the Advanced Radiation Research Institute of the Korea Atomic Energy Research Institute (KAERI). The manufacturer of the device is NORDION, Canada. Three dose rate conditions (25 Gy/h, 55 Gy/h, and 200 Gy/h) were used in this study, and the gamma rays were irradiated to reach a total dose of 800 Gy. For DRAM measurements, we used a field programmable gate array (FPGA) board from Xilinx, and the memory interface and control software were customized for real-time operated measurements. The sample used 8GB DDR4 DRAM, all with the same part number DRAM from the same manufacturer. The DRAM had a maximum speed of 2666 MT/s. It was organized into 16 banks, each containing 65536 rows and 1024 column addresses.

In evaluating the operated DRAM, error bits were printed in real-time by repeatedly performing write/read operations during gamma irradiation. The unbiased DRAM was measured the same as the operated DRAM immediately after gamma irradiation, with all the pins grounded. If the data is different from the pattern, an error vector is generated and transmitted to the PC via a high-speed USB connection. In the gamma-ray irradiation, a 'Write All 0' operation was conducted on the DRAM. This operation yielded no observable alterations in the data patterns. Consequently, the scope of this paper is limited to the exploration of the 'Write All 1' operation. To mitigate any potential confusion between DRAM errors and those originating from degradation owing to the TID on the FPGA board, we engineered a custom lead shielding box.

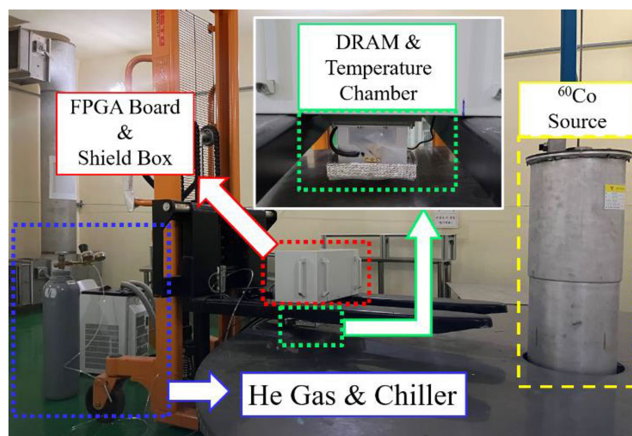

FIGURE 1. Test equipment setup of the DRAM memory samples in the irradiator, a ^{60}Co source at the Korea Atomic Energy Research Institute (KAERI).

Fig. 1 depicts a variable temperature chamber, which is designed as a container for simultaneous experimentation under specified operational and thermal conditions. The chamber is strategically equipped with a window to enable the irradiation process. The DRAM module is connected to the FPGA board via an extender PCB inside this temperature-controlled environment. The temperature chamber consists of a Peltier device, a chiller, and PT sensors; it was designed for remote control via a dedicated temperature controller. An alanine dosimeter was attached to all DRAM samples and measured using a Magnettech ESR5000 instrument from BRUKER after gamma irradiation [29]. The observed total measured dose exhibited an error margin of less than 7% compared to the pre-set target dose of 800 Gy.

Fig. 2 presents an overview of the DRAM test bed using an FPGA board. The temperature of the chamber was controlled

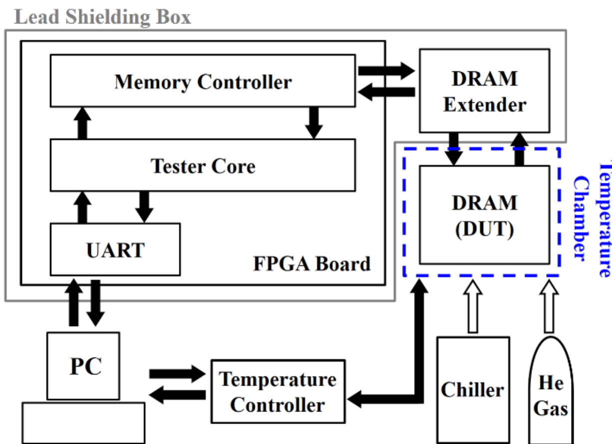

FIGURE 2. Simplified illustration of a test bed for DRAM. The FPGA board was shielded by a lead shielding box; only the DRAM was exposed to radiation.

using the temperature controller connected to a Peltier device via a PC, and a chiller-assisted low-temperature operation. Helium gas was continuously injected to prevent condensation inside the chamber. This FPGA board contains a custom test design programmed to write an 'All 1' pattern to the DRAM. If the read data differs from the original data pattern, the error vectors are sent to a host PC. Because the PC was located outside the radiation facility using the long cable, universal asynchronous receiver/transmitter (UART) and repeater were used to reduce noise when connected to the FPGA board. The memory controller is composed of user logic combined with a physical layer (PHY) and is designed to interface with the DRAM.

III. RESULT AND DISCUSSION

A. RADIATION EFFECTS

Fig. 3 illustrates the relationship between the error density and total dose, where the error density is defined as the ratio of the number of error bits to the total number of bits. For this experiment, the measurement was conducted in real-time with the total dosage set at 800 Gy at a dose rate of 55 Gy/h. The dose threshold at which the errors began was identified as 337 Gy, and an exponential increase in the error density was observed from approximately 600 Gy. These results support the conclusion that degradation worsens exponentially as the total dose increases.

The increase in the error density corresponding to the increasing dose can be explained by the creation of traps owing to gamma rays. When oxide is exposed to ionizing radiation, ionization induces the generation of a substantial number of electron-hole pairs. Among the generated carriers, most electrons move toward the gate, whereas the holes within the oxide move through a hopping motion toward the silicon/oxide interface [18]. As these holes approached the interface, a subset was trapped, culminating in the formation of a positive oxide trap. Some of the holes release hydrogen ions (H^+, protons), and the released protons interact with the silicon dangling bonds at the interface, triggering depassivation [17], [19]. This interaction results in the formation of a P_b center at the interface. Consequently, the electrons on Si are effortlessly trapped in the P_b center by the positive electric field, thereby becoming negative traps. This positive field effectively traps the electrons and inhibits their emission [16]. Therefore, as gamma rays accumulate, the occurrence of electron-hole pairs within the oxide intensifies, thus leading to a significant release of H^+. With an increase in H^+, there is a higher propensity for interaction with the dangling bonds, thereby resulting in a higher concentration of interface traps.

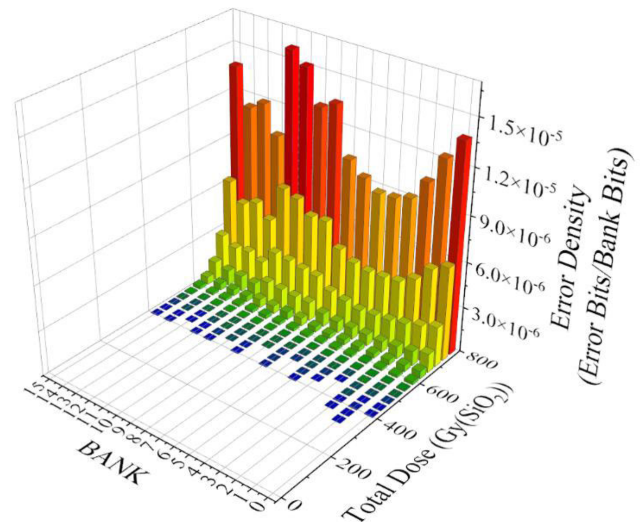

FIGURE 3. Error density per bank of operated DRAM during real-time measurements. The total dose is 800 Gy and dose rate is 55 Gy/h.

As depicted in Fig. 3, the exponential increase in the error density was correlated with the retention time of the DRAM cell transistor and the initial absence of errors during the onset of gamma-ray irradiation. Failure of the DRAM due to the TID occurs when the charge stored in the capacitor cannot be maintained for a 64 ms refresh time (t_{REF}) and leaks out. Because of process variations, the retention time distribution of a DRAM cell is not uniform across cells and is typically determined by the retention time of the tail cell [21], [22]. As a result of the TID, the Gaussian distribution of the retention time of DRAM undergoes a shift in the negative direction [30]. This shift initially causes the tail cell portion to be less than 64 ms, yielding fewer error bits. However, as TID accumulation induces a further negative shift in the retention time, the mean (μ) value of the Gaussian distribution approaches 64 ms. Consequently, a large number of cells fail, thus culminating in an exponential increase in error density. Furthermore, during the examination of the error density across banks, it was observed that the distribution was uniform. This suggests that no specific bank noticeably influences the overall error density.

Fig. 4 compares the error density between the operated and unbiased DRAM tests conducted under identical conditions

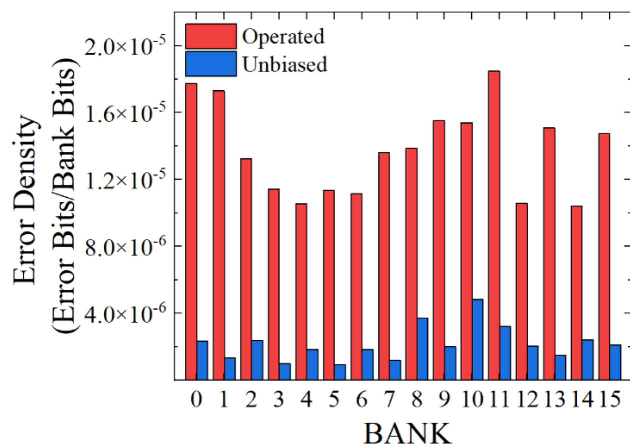

FIGURE 4. Comparison of error density with and without operation. The total dose is 800 Gy and dose rate is 55 Gy/h.

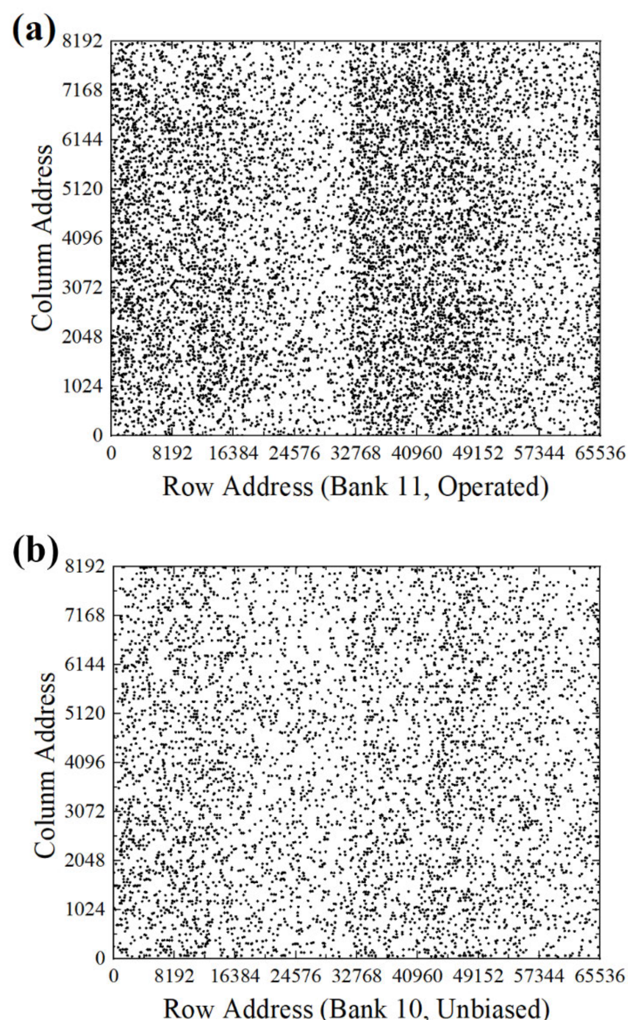

FIGURE 5. Bit-maps for (a) bank 11 of operated DRAM and (b) bank 10 of unbiased DRAM with the highest error density.

(dose rate = 55 Gy/h, total dose = 800 Gy). An analysis of the error density of different banks is presented to discern whether the error distribution is uneven or whether certain banks are predisposed to larger error magnitudes. As depicted in Fig. 4, bank 10 exhibits the most significant error density of unbiased DRAM, whereas bank 11 has the highest error density of operated DRAM. Nevertheless, owing to the randomness of the error density across all banks without any discernible pattern, it is not possible to assert that bank 11 is always prone to significant error bit occurrences.

To examine the impact of this random distribution within banks, bit-maps representation is depicted in Fig. 5. Fig. 5(a) and (b) depict bank 11 of operated DRAM and bank 10 of unbiased DRAM (both exhibiting the highest error density), respectively. A comparison of Fig. 5(a) and (b) shows that the failed cells occur evenly and randomly. The randomness of the error density among the cell transistors can be attributed to the variation of retention times in the DRAM process and the unpredictability of the gamma-ray interactions. Because no specific pattern is detected in the bit map, DRAM cell transistors are more sensitive to TID than active pages or sense amplifiers.

Furthermore, as depicted in Fig. 4, despite having the same total dose and dose rate, the operated DRAM exhibited larger overall errors. This resulted in an error density difference of at least 4.8 times greater for the operated DRAM than for the unbiased DRAM. A comparison of Fig. 5(a) and (b) indicates that the operated DRAM has more failed cells. This reflects the operated DRAM, which is consistent with the observations depicted in Fig. 4. Therefore, the difference in error density is related to the field caused by the bias of the interface trap in the DRAM cell transistor.

Studies have reported this phenomenon on both operated and unbiased MOS structures [31], [32]. This occurs because an electric field is applied to the oxide during operated test. In the unbiased state, the probability of H^+ approaching the interface is reduced because there is no electric field. Furthermore, when the production of oxide traps exceeds a certain threshold, these traps accumulate near the interface, further resulting in a local field reversal [24]. The holes generated by the gamma rays are trapped in the oxide near the interface, and the charge of the holes creates positively charged oxide traps. As the total dose increases, the generation of oxide traps increases concomitantly. This locally reversed field acts as an electrostatic barrier that prevents positively charged H^+ from hopping toward the interface. Consequently, this hinders the generation of interface traps.

By contrast, in the operated case, a positive field is generated on the oxide by the applied bias, as depicted in Fig. 6. In the operated state, there is a heightened concentration of interface trap generation compared to the unbiased state. Despite oxide trap accumulation, the local field reversal near the interface is inhibited, thus facilitating the unhindered movement of H^+ to the interface. Consequently, this amplified concentration of interface traps leads to an increase in the current produced through trap-assisted tunneling (TAT), i.e., the leakage current.

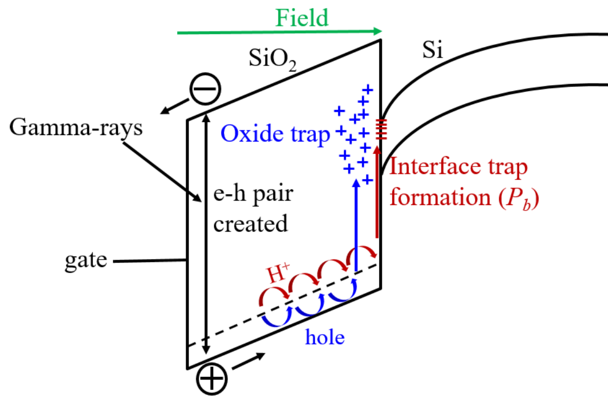

FIGURE 6. Illustration of electron-hole pair generation, charge transport, and trapping in irradiated SiO_2 when in the operated state [15].

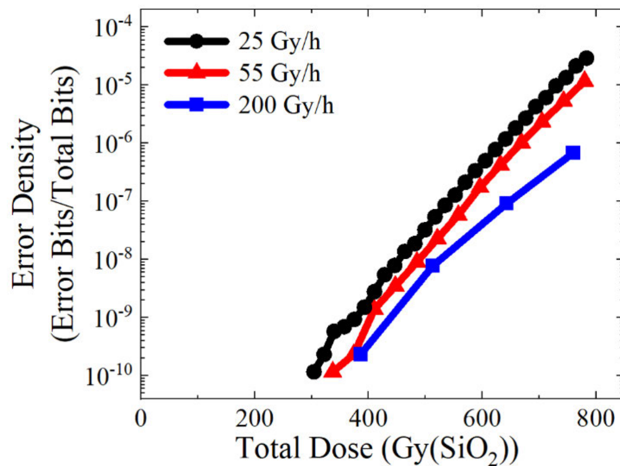

FIGURE 7. Error density according to dose rate for operated DRAM in real-time measurement.

B. DOSE-RATE EFFECTS

In Fig. 7, we analyzed the effect of the dose rate by evaluating three different rates: 25 Gy/h, 55 Gy/h, and 200 Gy/h. The tests were performed to reach the same total dose (800 Gy) for operated DRAM in real-time measurement. The data in Fig. 7 reveal that smaller dose rates are associated with larger error densities for the same total dose. At a total dose of 800 Gy, the error density for the low-dose-rate was approximately 30 times larger than that for the high-dose-rate, with an error density of approximately 2×10^{-5} for a dose rate of 25 Gy/h and 6.8×10^{-7} for 200 Gy/h, despite having a dose rate eight times smaller. These results provide unequivocal evidence of the dose-rate effect on the degradation rate of DRAM.

This is due to the difference in the interface trap generation with the dose rate, as illustrated in Fig. 8. Under a high-dose rate, more electron-hole pairs are generated than under a low-dose rate for the same amount of time. Because the mobility of holes is greater than that of protons, the holes move quickly to the interface and are trapped near the interface [24]. These positively charged trapped holes form an electrostatic barrier that hinders protons from interacting with the interface.

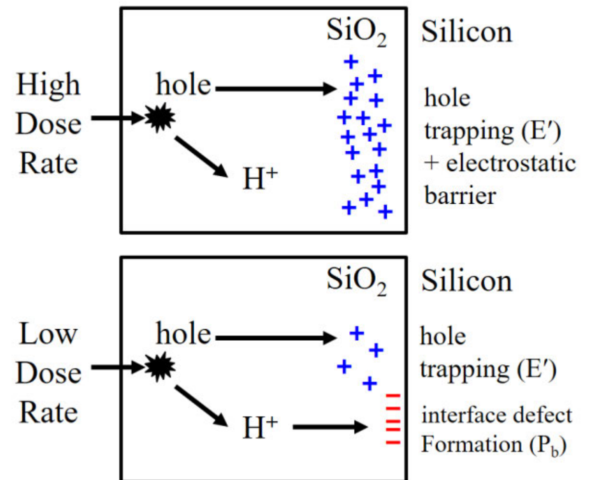

FIGURE 8. Interface trap buildup for high and low dose rates. For high-dose rates, an electrostatic barrier appears near the interface due to trapped holes [24].

Consequently, relatively fewer interface traps are generated at a high-dose rate because the access of protons to the interface is obstructed by these trapped charges or their interaction is inhibited. This leads to the formation of a larger number of interface traps under a low-dose rate than under high-dose rates, resulting in a more significant degradation under low-dose conditions.

C. EFFECT OF TEMPERATURES

Fig. 9 depicts the results obtained under different temperature conditions during real-time measurements of gamma-ray irradiation using the temperature chamber. These temperature conditions were set at three different values (243 K, 300 K, and 353 K), to evaluate the radiation effects at low, normal, and high temperatures, respectively. The dose rate and total dose were fixed at 25 Gy/h and 800 Gy, respectively. At a total dose of 800 Gy, the error density was 1.8×10^{-4} at high temperatures and 3.4×10^{-8} at low temperatures, thereby resulting in an error density of approximately 5000 times greater at high temperatures than at low temperatures. This result clearly indicates the temperature dependence of DRAM. This increase in the error density suggests that interface traps may form differently depending on the temperatures. To investigate the effect of temperature on the interface trap formation, we evaluated the error density at room temperature (300 K) immediately post-irradiation.

In the post-irradiation measurements depicted in Fig. 9, all samples were evaluated at room temperature (300 K). The error densities observed at low temperature, room temperature, and high-temperature conditions were 1.3×10^{-6}, 4.2×10^{-5}, and 2.4×10^{-5} respectively. By considering the room temperature condition, which exhibited the highest error density, as a reference, it was found that the error density at the high temperature was approximately 1.75 times smaller. This can be attributed to the high-temperature annealing recovery effect. The lowest error density observed under the

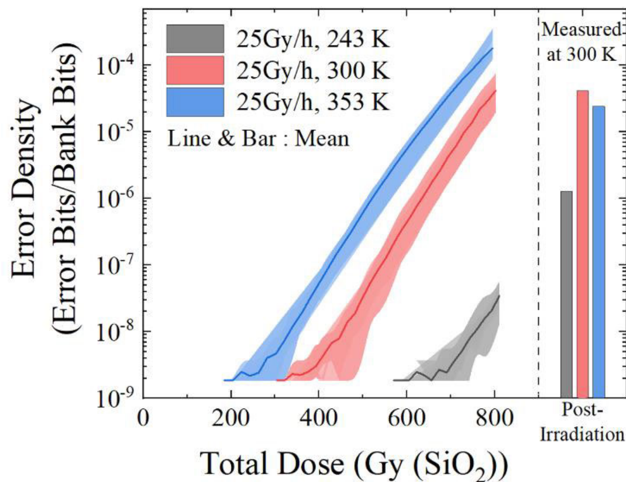

FIGURE 9. Temperature-dependent error density during real-time operation measurement and measurements at room temperature (300 K) post-irradiation.

low-temperature condition is approximately 32 times smaller than the highest error density recorded at room temperature. This implies that the radiation effect is less severe at low temperatures than at room temperature. This can be attributed to the variability in the concentration of interface traps generated under different temperature conditions.

Fig. 10(a)–(c) illustrate the proton transport phenomena at low, room, and high temperatures, respectively, while also demonstrating the formation of interface traps resulting from subsequent interactions near the interface. The symbols H^+, VH (hydrogenated oxygen vacancies), blue circles, and red bars represent protons, hydrogenated oxygen vacancies, Si-H bonds, and interface traps, respectively. The relative magnitude of the reaction or transport rate is indicated by the size of the arrows. During irradiation, the competing proton generation and recombination processes determine the number of protons that can reach the interface and contribute to the creation of interface traps. Therefore, the number of protons generated is the most dominant factor in the creation of interface traps. These protons can react either with the Si-H dangling bond to create an interface trap or with VH to create H_2 [19].

Fig. 10(b) illustrates the process by which protons are released by holes and transported to the interface. Because of the moderate concentration of protons at room temperature, the rate of the dimerization reaction, in which protons react with VH to produce H_2, is lower despite the presence of VH defects. However, the temperature-induced excess proton concentration near the interface causes additional H_2 generation and interferes with the formation of interface traps, thus resulting in a reduced number of interface traps (Fig. 10(c)). As a result, the rapidly generated protons at high temperature reacting with VH in the oxide can inhibit the supply of protons to the interface, thus inhibiting the formation of interface traps.

This process may also include an annealing effect in which the traps created are naturally recovered during high

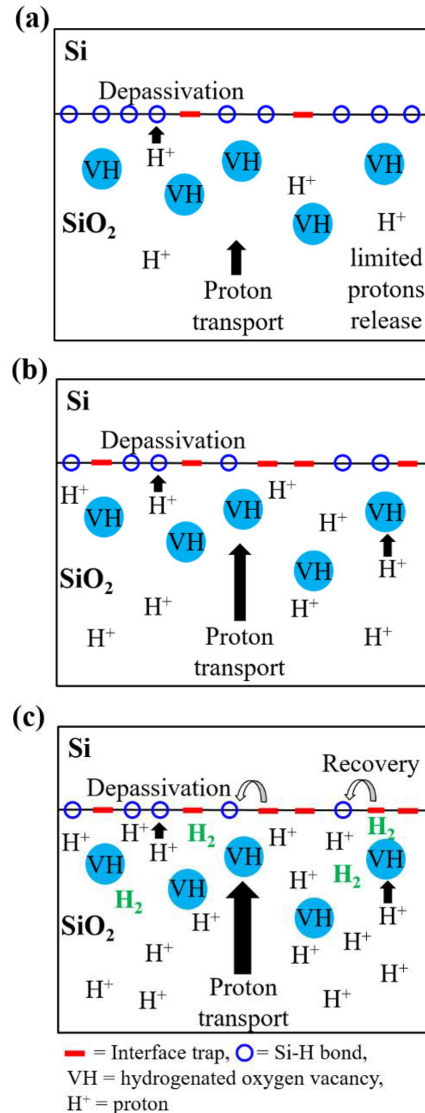

FIGURE 10. Illustration of proton transport and interactions at or adjacent to SiO_2/Si interfaces. The dimensions of the arrows provide an approximate indication of the reaction or transport rate magnitudes under different conditions: (a) Low-Temperature (b) Room-Temperature, and (c) High-Temperature.

temperature irradiation [28]. This recovery can be attributed to the recovery of Si-H bonds, facilitated by protons and H_2 interacting with the interface. Additionally, the trapping of electrons in oxide traps and their subsequent recombination can lead to a charge-neutral state. In contrast, under the low-temperature conditions depicted in Fig. 10(a), the reduced reaction rate and mobility of the holes reduce the probability of the holes reacting with VH, i.e., emitting protons. As a result, a reduction in the number of interface traps decreases the error density.

D. ANNEALING EFFECTS

After gamma irradiation, annealing was conducted to assess the recovery, as depicted in Fig. 11. The conditions described in the previous section, which indicated varying degradation rates during gamma irradiation, did not significantly affect

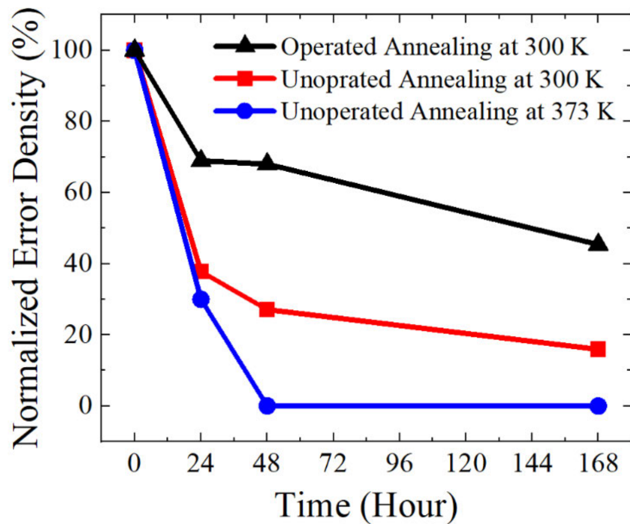

FIGURE 11. Normalized error density for 168 h was evaluated under three conditions: operated at 300 K, unbiased at 300 K, and unbiased at 373 K.

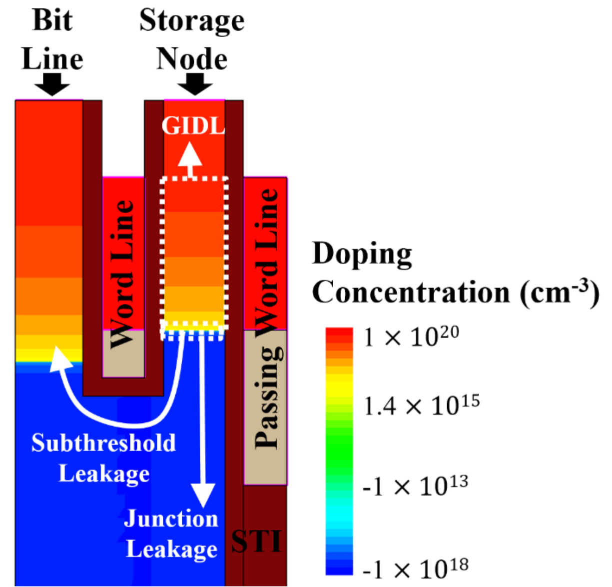

FIGURE 12. Structure of a saddle fin based DRAM with three leakage current paths using TCAD simulation.

the recovery during annealing. A 168 h annealing process was conducted under operational states (operated, unbiased) and temperature conditions (300 K, 373 K). To compare the recovery rates during annealing, the error densities were normalized. The operated DRAM was measured for 168 h post-irradiation, while the unbiased DRAM was measured only at 24, 48, and 168 h. High-temperature annealing was initially performed at room temperature for 24 h post-irradiation, followed by annealing at 373 K in the temperature chamber.

Under the 300 K annealing condition, the unbiased DRAM demonstrated approximately 30% greater recovery compared to the operated DRAM. The operated DRAM recovered only 54.6% after 168 h, whereas the unbiased DRAM showed a recovery of 84.1%. This difference is attributed to the inability of electrons to be released from the interface by the gate voltage of the operated DRAM, as depicted in Fig. 6. Annealing effect is a phenomenon in which the interface traps react with protons and H_2, thereby causing the Si-H bond to recover [33]. This annealing effect tends to be more active at elevated temperatures, owing to the increased reaction rate. In addition, electrons are quickly released from the trap energy level. This is because the electrons gain sufficient energy to be released from the trap at a high temperature. Therefore, the created traps recover more quickly at high temperatures, further resulting in a lower error density than at room temperature.

E. TCAD SIMULATION

A cross-sectional schematic of the saddle fin based DRAM is depicted in Fig. 12. TCAD simulations are used to analyze the results of the experiments at the cell transistor level. The simulations were performed using the Sentaurus simulator (Synopsys^{TM}). The DRAM consists of a word line (WL), passing word line (PWL), bit line (BL), and storage node (SN). The gate channel length and gate depth of the DRAM were 14 nm and 100 nm with the 6 nm thick SiO_2 layer. The fin height and width used in the simulation were 32 nm and 10 nm, respectively. High-field saturation and Scockley-Read-Hall (doping and temperature dependent) recombination models were used in this simulation with the Inversion-accumulation layer mobility model. A hydrodynamic model was utilized for temperatures, and the Hurkx band-to-band tunneling model was adopted for GIDL. The impact of TID was emulated by assigning the concentration of interface traps (N_{it}) to the interface region of Si/SiO_2. Acceptor-like trap was used as the type of interface traps in the simulation.

Fig. 13(a)-(c) depict the band-to-band tunneling (BTBT) generation using TCAD simulation to evaluate the leakage current as a function of temperature depicted in Fig. 9. The contour images of BTBT illustrate the sensitivity of BTBT to temperature changes. An increase in BTBT is observed as the temperature rises, from the low temperature of 243 K depicted in Fig. 13(a), to room temperature of 300 K depicted in Fig. 13(b), and finally to the high-temperature condition of 353 K depicted in Fig. 13(c). This increase in BTBT is attributable to a rise in the number of electrons tunneling as the temperature elevates. The electrons that are trapped within the significant quantity of interface traps gain sufficient energy due to the increased temperature. As the number of tunneling electrons increases, both the leakage current elevates and the potential at the SN decreases. This can reduce the retention time to 64 ms or less. Consequently, the SN may fail to retain the stored data, further leading to errors. Thus, the amplified degradation observed at high temperatures can be attributed to the temperature-dependent increase in the leakage current, which affects the retention time of DRAM devices.

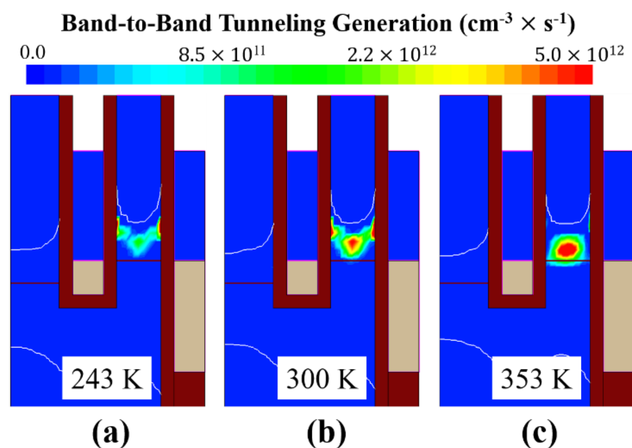

FIGURE 13. Band-to-band tunneling generation contour plot of DRAM structure for varying temperatures: (a) 243 K, (b) 300 K and (c) 353 K.

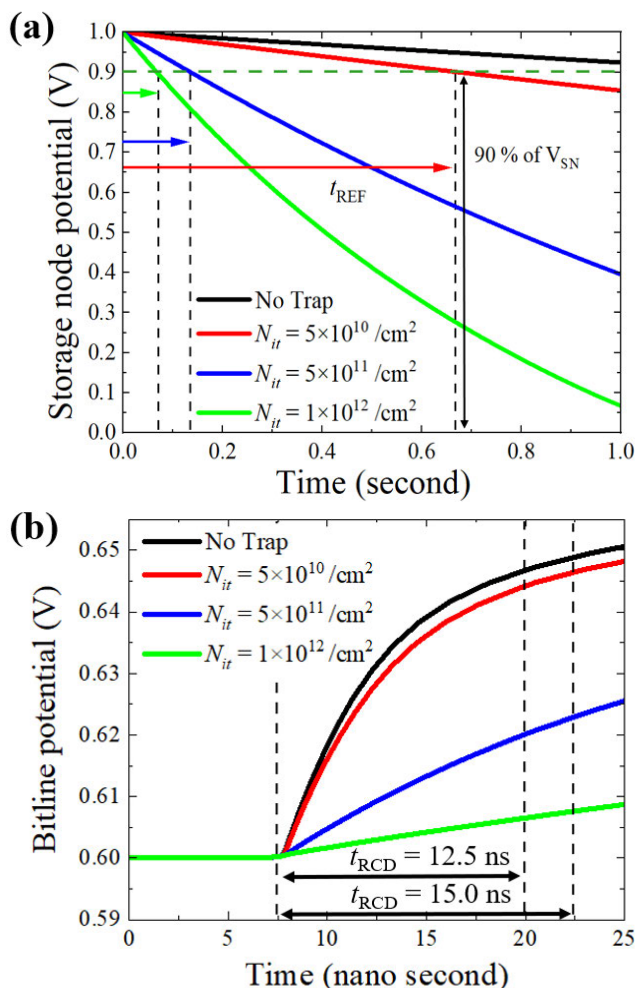

FIGURE 14. (a) Retention time during hold operation and (b) storage node (SN) potential variation during row activation as the concentration of interface trap for saddle fin DRAM in TCAD simulation.

Fig. 14(a) depicts the simulation results for the retention time as a function of the concentration of the interface trap. In Fig. 14(a), when the concentration of the interface trap is $N_{it} = 5\times10^{10}$ /cm^2, $N_{it} = 5\times10^{11}$ /cm^2, $N_{it} = 1\times10^{12}$ /cm^2, it shows a decrease in SN potential of 7.6%, 57.3%, and 92.2% respectively, compared to no trap at time = 1 s. Assume 90% of the SN potential as the minimum voltage that the sense amplifier can sense after charge sharing [34]. In this case, if the concentration of the interface traps increases by 20 times, the retention time decreases by 90%.

Fig. 14(b) depicts the charge sharing during row activation. When the word line is asserted, each cell capacitor in the activated row is connected to the corresponding BL and charge sharing occurs. The sense amplifier senses and amplifies the BL voltage to a certain level. However, if the potential does not increase to a certain level owing to an interface trap, data may not be accessible during the row activation latency (t_{RCD}). An increase in the concentration of interface traps prevents the channel of the access transistor from being inverted, i.e., V_{th} increases. In addition, scattering occurs at the interface in the channel region, which hinders the flow of electrons. Therefore, a longer time is required for the SN capacitor and BL to share the charge.

IV. CONCLUSION

In this study, the total ionizing dose (TID) effects of gamma rays on the DRAM were investigated under various conditions (operations, dose rates, temperatures). For gamma irradiation in both the operated and unbiased DRAMs, the error density of the operated DRAM was approximately 4.8 times greater than that of the unbiased DRAM. This result indicates that DRAMs exhibit greater radiation sensitivity of operated DRAM than unbiased DRAM. There was a dose rate effect, in which the performance degradation was more pronounced at a low dose rate because the oxide trap acted as an electrostatic barrier at a high dose rate. Furthermore, at lower temperatures, the impact of radiation diminished owing to the decreased production of protons. Annealing experiments showed a fast recovery rate at a high temperature in the unbiased state.

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(Gyeongyeop Lee and Minki Suh are co-first authors.)

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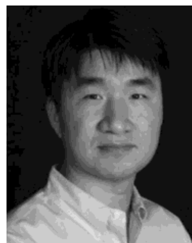

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