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RESEARCH ARTICLE

A Subthreshold Operation Series-Parallel Charge Pump Incorporating Dynamic Source-Fed Oscillator for Wide-Input-Voltage Energy Harvesting Application

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ABSTRACT This work proposes a CMOS reconfigurable charge pump (CP) for a low-voltage energy harvesting system. It utilizes the low effective resistance from the parallel CP to enhance its power conversion efficiency (PCE). The CP exhibits an adaptive configuration with different stages depending on the input voltage, changing its voltage conversion ratio (VCR) to limit the output voltage under 1.8-V. Additionally, this work develops a novel dynamic source-fed oscillator that modulates the oscillating frequency by utilizing a dynamic source for the ring-voltage controlled oscillator (RVCO). The independent source from the RVCO and the clock-generating units from the proposed technique permit the implementation of frequency modulation without affecting the clock amplitude. Fabricated in 65-nm CMOS, the proposed prototype measures 62% peak PCE with an input voltage range of 0.26-V to 0.64-V.

INDEX TERMS Reconfigurable charge pump (CP), ring-voltage controlled oscillator (RVCO), dc-to-dc converter, low power energy harvesting, CMOS, power conversion efficiency (PCE).

I. INTRODUCTION

Acapacitive-based CMOS DC-DC boost converter, also called a charge pump (CP) plays an important role in energy harvesting (EH) applications to step up the input voltage to a higher voltage level suitable for load applications. The conventional CP block shown in Fig. 1 consists of an oscillator that generates clock signals to govern the pumping operation, a non-overlap clock (NOC) generator that converts the sinusoidal clock signals into two non-overlapping square waves [1], and the CP itself, which boosts the scavenged DC voltage to a usable level for the load [2].

Cross-coupled charge pump (CCCP) [3], [4], [5], [6], [7], [8] and Dickson CP [9] are the two conventional CP topologies in vogue for EH applications. In low input voltage applications, switch-based CCCP is preferred over diode-based

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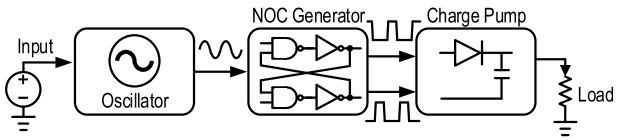


FIGURE 1. The basic block diagram of a conventional charge pump.

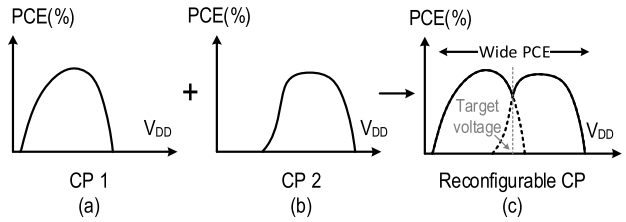


FIGURE 2. The PCE vs input voltage curve of (a) individual CP1 (b) individual CP2 (c) reconfigurable CP by combining CP1 and CP2.

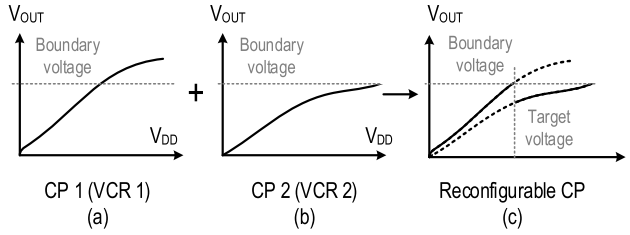


FIGURE 3. The output voltage of (a) individual CP1 (b) individual CP2 (c) reconfigurable CP by combining CP1 and CP2.

Dickson CP as the diode-based Dickson topology suffers from high V_{TH} conduction loss. On the other hand, Dickson CP has an advantage in high input voltage applications due to its minimal reversion loss. To reduce the conduction loss, some studies have incorporated low voltage threshold (LVT) devices to enhance the performance of charge pumps in subthreshold operation [4], [8], [10]. Nevertheless, the attempt to minimize conduction loss entails a compromise of increased reversion loss, which negatively impacts the charge pump's overall performance. Over the past few decades, a wide range of techniques for improving CP performance has been documented in the literature [2], [11], [12], [13], [14], [15], [16], aimed at addressing the aforementioned challenges. Despite significant research focused on optimizing CP topologies, there remains potential for further innovation in architectural improvements.

In energy harvesting applications, the input voltage of the CP varies due to the fluctuation in the harvested power, which is an external influence on the system. For instance, weather conditions can have an impact on the harvesting of solar energy, while the harvesting of kinetic energy can be affected by factors such as humans. There are several problems accommodated with a wide input voltage range CP. Firstly, their power conversion efficiency (PCE) cannot remain high over a wide input voltage range, as it depends on the CP topology. Additionally, the frequency generated by the oscillator is influenced by the input voltage. Therefore, a wide

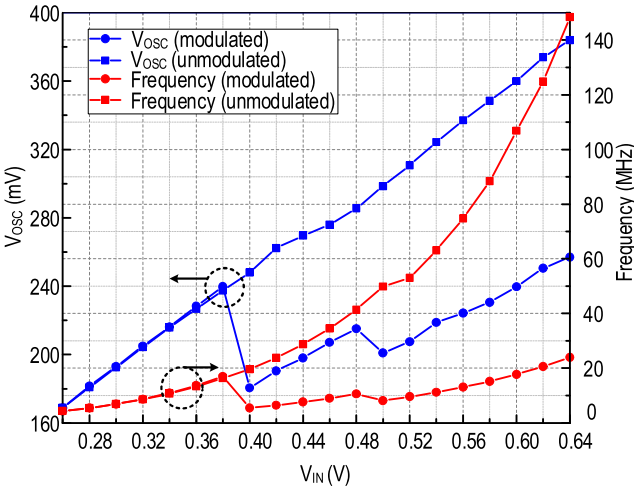


FIGURE 4. Plots of the relationship between input voltage, oscillator source voltage and the modulated and unmodulated oscillating frequencies.

input voltage range would cause the oscillator to produce a broad frequency range, which would further degrade the CP's performance. Furthermore, a high input voltage would result in a highly boosted output voltage, which can cause voltage overstress on the operating transistors, as well as cause output load breakdown. This effect is more pronounced in circuits designed for low voltage performance, where devices with low voltage overstress thresholds such as LVT devices or short gate length transistors are used [17], [18].

Some of the recent EH CP works [3], [4], [5], [19] proposed charge pumps that lack consideration in the oscillator circuit; instead, two non-overlapping clocks with a stable frequency are supplied by a function generator to model the generated clock signals from the oscillator for pumping. This is important to evaluate the CP's performance, especially for EH applications [6], [7] that have a fluctuating input voltage. Furthermore, the unstable frequency generated from the fluctuating input voltage will affect the CP's performance. The work in [7] provides constant 10 MHz clock signals to its reconfigurable CP despite having an input voltage ranging from 0.45 V to 0.75 V. Another work in [6] reveals the high power loss caused by the high frequency from increasing input voltage. Yet, the work used external trimming to suppress the increasing oscillation frequency. Some works incorporated a proper frequency modulation technique in the reconfigurable CP, such as the variable delay stages configuration from [20] and the dynamic delay block's sources from [21] and [22]. However, these frequency modulation techniques lead to some performance hindrances, which will be discussed later in this paper.

The previously mentioned issues highlight the need for a reconfigurable CP. Hence, this work proposed a reconfigurable CP that exploits the low effective resistance in the parallel CP to reduce the forward conduction loss and the high voltage conversion ratio (VCR) of the series CP for subthreshold operation wide input voltage energy harvester.

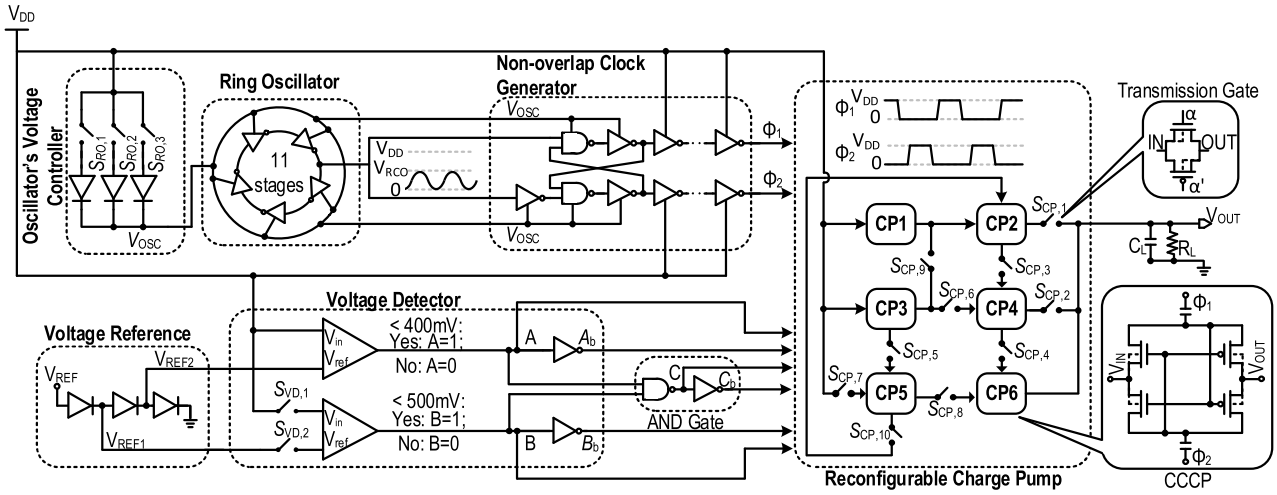


FIGURE 5. Top architecture of the proposed series-parallel reconfigurable CP.

TABLE 1. Control logic high signal for stage reconfigurable CP.

V_{DD} State	$S_{CP,1}$	$S_{CP,2}$	$S_{CP,3}$	$S_{CP,4}$	$S_{CP,5}$	$S_{CP,6}$	$S_{CP,7}$	$S_{CP,8}$	$S_{CP,9}$	$S_{CP,10}$	$S_{VD,1}$	$S_{VD,2}$	$S_{RO,1}$	$S_{RO,2}$	$S_{RO,3}$
$V_{DD} < 0.4V$	1	1	0	0	0	1	1	1	0	0	1	1	0	0	1
$0.4V \leq V_{DD} < 0.5V$	0	1	1	0	1	0	0	1	0	0	1	1	0	1	0
$V_{DD} \geq 0.5V$	0	0	1	1	0	0	1	0	1	1	0	0	1	0	0
Control HIGH Signal	C	Ab	Cb	A	B	C	Bb	Ab	A	A	Ab	Ab	A	B	C

By configuring the six-stage parallel CP into 4 stages, 3 stages, and 2 stages, the proposed reconfigurable CP limits the output voltage under 1.8 V while attaining high efficiency in a low input voltage range.

In this study, we address the issue of unstable frequency resulting from fluctuating input and present an innovative frequency modulation approach by employing a dynamic source-fed oscillator. This technique can suppress the high generated clock frequency during high input voltage to reduce the switching loss effect in the CP. Moreover, the proposed technique incorporates an independent source for the oscillator and the clock-generating unit, allowing for the provision of a high-amplitude clock signal from the input voltage to the CP while limiting the source voltage of the oscillator.

The rest of this paper is organized as follows. Section II reviews the conventional reconfigurable CPs. Section III discusses the design methodology of reconfigurable CP. Section IV describes the operation of the proposed reconfigurable CP. Section V details the operation principle of a clock generation unit in the CP, and the proposed dynamic source-fed oscillator. Section VI presents the measurement results and the performance comparison. Section VII concludes the work.

II. CONVENTIONAL RECONFIGURABLE CP

The main objective of a reconfigurable CP is to enhance the efficiency and control the VCR to limit the output voltage. Reference [23] introduces a power-efficient reconfigurable CP that configures between linear CP and Fibonacci CP in high voltage and low voltage ranges respectively. However, the work only concentrates on achieving maximum efficiency, without taking into account the need to limit V_{OUT} to prevent transistor overstress and load breakdown.

An adaptive VCR reconfigurable CP was implemented in [24], capable of switching between 1, 2, and 3 stages to achieve maximum efficiency, but the diode-based design restricts its use in low voltage energy harvesting applications. Reference [25] introduces a circuit with a reconfigurable soft transition VCR, but it is for step-down CP. Reference [22] proposed a hybrid Dickson and Cockcroft-Walton CP capable of configuring between 4 and 6 stages. Despite having multiple VCRs, the work only tested at a narrow input voltage range of 0.9, 1, and 1.1 V. Similarly [26] proposed a reconfigurable CP with VCRs of 2 and 3 while [27] proposed a stage selection CP that can configure between 1 to 3 stages. However, these CPs were only tested on the high input voltage ranges. Besides limiting the output voltage with adaptive VCR, [27] also included transistor electrical overstress and gate-oxide unreliability consideration in the design for the 1.8V/3.3V CMOS process. Reference [19] presents an intriguing output voltage regulation by utilizing the trans-conductive loop implemented through the bulk terminal of the PMOS transistor in CCCP. The work, however, ignored the impact of variable frequency in a wide input

TABLE 2. Truth table for reconfigurable CP's control signals.

Scenario	V_{DD} State	No. stage	A	Ab	B	Bb	C	Cb
III	$V_{DD} \geq 0.5\ V$	2 stages	0	1	0	1	1	0
II	$0.4\ V \leq V_{DD} < 0.5\ V$	3 stages	0	1	1	0	0	1
I	$V_{DD} < 0.4\ V$	4 stages	1	0	0	1	0	1
-	-	-	1	0	1	0	x	x

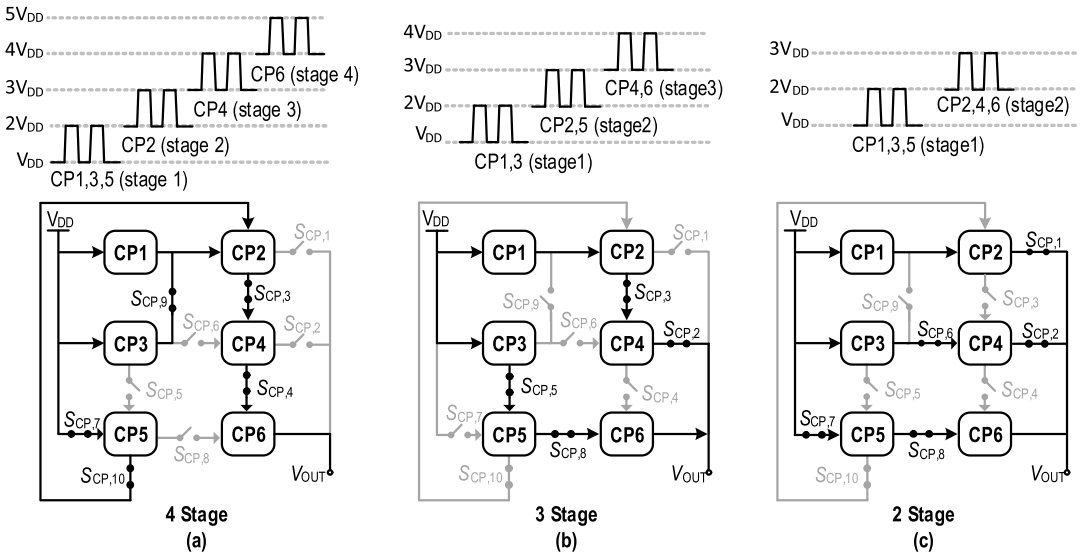


FIGURE 6. Proposed reconfigurable CP (a) scenario I, 4 stages (b) scenario II, 3 stages (c) scenario III, 2 stages.

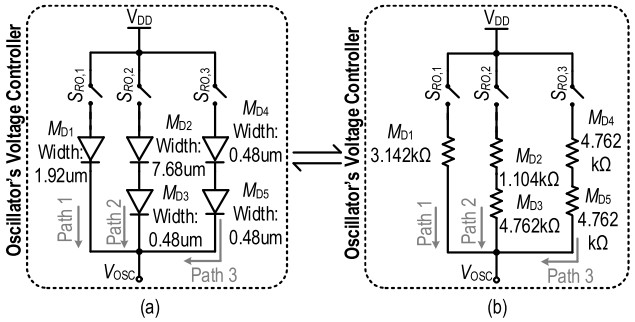


FIGURE 7. Proposed oscillator's voltage controller unit's (a) schematic diagram and (b) equivalent resistant model.

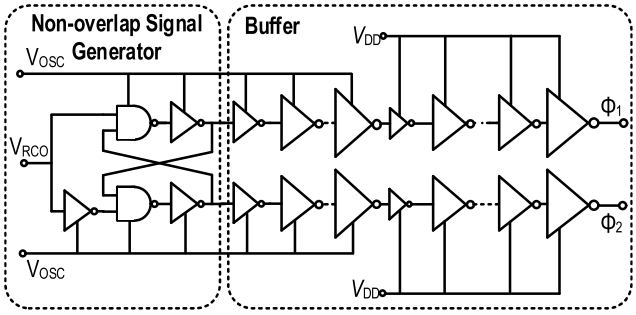


FIGURE 8. Block diagram of a non-overlap clock generator. The size of inverters in the buffer represents the transistors' width.

voltage range as it only provides a constant 1MHz clocking frequency in the design throughout the input voltage range.

Another method of changing the VCR is by controlling the clock amplitude of the CP. Reference [7] implemented a clock amplitude reducer to reduce the VCR by half in addition to a reconfigurable CCCP capable of switching between 2 and 4 stages. Reference [21] introduces a novel self-oscillating CP where a different level of source voltages is supplied to the CP to achieve an adaptive VCR. Although the self-oscillating CP does not necessitate the use of an oscillator, this frequency of the self-oscillating charge pump cannot be independently adjusted, so an external frequency modulation block is needed.

Frequency modulation is important in wide input reconfigurable CP as the high switching loss caused by high oscillating frequency will deteriorate the CP performance. However, it is often overlooked in the past reconfigurable CP works. Reference [28] proposed a subtraction-mode CP that can tolerate high switching frequency loss with frequency in the range of 60 MHz and 100 MHz, but the frequency range is too small in wide input energy harvesting applications. This can be seen in Fig. 4, where the frequency of an oscillator can rise by 100 MHz from a 0.4 V input increment. Reference [20] implemented frequency modulation to his 9 stages CP at which each stage can be deactivated using a stage control block. The frequency modulation is achieved using variable delay cell configuration which will induce

high power consumption. The details of power consumption in the frequency modulation technique will be discussed in Section V.

III. RECONFIGURABLE CP DESIGN METHODOLOGY

The first step of designing a reconfigurable CP is to individually design the CP for each voltage range. The performance of each CP topology is identified and optimized individually in a way that each CP has a peak performance at a separate input voltage range as depicted in Fig. 2. The determination of the target voltage, at which the CP reconfigures, is based on the intersection of the CPs' PCE curve as illustrated in Fig. 2(c) [29], [30], and [31]. Similarly, to design a reconfigurable CP with an adaptive VCR that limits a bounded output voltage [25], each CP is first individually designed to identify the correlation between VCR and output voltage (V_{OUT}). The target voltage for the reconfiguration to occur is determined when the V_{OUT} of the CP with higher VCR exceeds the boundary voltage as depicted in Fig. 3. The boundary voltage is selected based on the application, depending on the load breakdown voltage and the transistor's operating point. Next is to develop the control algorithm for the reconfigurable CP. A comparison of the structure of each CP is carried out to determine the number of switches needed for the reconfiguration process. Subsequently, the state of each switch in the various configurations is identified. The third step of the reconfigurable CP design process involves developing a control circuit to implement the algorithm designed in the previous step. The control circuit is composed of a series of logic gates that generate the necessary control signals to activate the switches for the CP reconfiguration process.

The voltage detector is implemented to detect the target voltage where the reconfiguration occurs. There are a few approaches to implementing the voltage detector. A closed-loop system detects the output voltage level to achieve CP reconfiguration [24], [32] whereas an open-loop system detects the input voltage [26]. The closed-loop system offers the benefit of high stability and precise control, whereas the open-loop circuit is simpler to design and has lower power consumption due to its less complex circuitry. The selection of a closed-loop or open-loop system for reconfigurable charge pump design is dependent on the specific application requirements.

Finally, the performance of the reconfigurable CP is tested and compared with the individual CP. Further optimization will be carried out to improve the reconfigurable CP performance.

IV. PROPOSED RECONFIGURABLE CP

A. PROPOSED SERIES-PARALLEL RECONFIGURABLE CP

The proposed CP scheme is shown in Fig. 5. The CCCP's VCR changes by reconfiguring the number of stages in series or parallel, respective to the input voltage (V_{DD}). Three main circuit blocks define the scheme. First, the clock generation unit is used to provide two non-overlap clock signals with modulated frequency. The logic control unit provides the control signals for the CP. Finally, the reconfigurable CP is responsible for output voltage boosting.

The reconfigurable CP consists of 6 individual CCCP which are capable of configuring into 4 stages, 3 stages, or 2 stages based on the detected input voltage. The CP configuration is achieved by controlling the transmission gates, SCP,1-10 which act as the control switches for the reconfigurable CP. The main advantage of using series-parallel reconfigurable CP is that each CP cell is fully in operation under all different input voltage scenarios. Moreover, parallel CP has a lower conduction loss due to its lower equivalent circuit resistance, contributing to a much lower power loss during the charge-transferring phase [33].

As shown in Fig. 6, the proposed CP has three operation modes. When the input voltage V_{DD} from the EH source is below 0.4 V (VDD $<$ 0.4 V), SCP,3,4,7,9,10 are turned ON while the remaining gates are turned OFF. Thus, the CP reconfigures to a 4-stage CP with a VCR of 5. In this configuration, CP1, CP3, and CP5 are connected in parallel in the first stage, boosting the voltage from V_{DD} to $2V_{DD}$; followed by CP2 in the second stage, boosting voltage to $3V_{DD}$, CP4 in the third stage, and CP6 in the fourth stage as shown in Fig. 6(a). For V_{DD} between 0.4V and 0.5V, SCP,2,3,5,8 are turned ON while the rest are turned OFF. The CP is then reconfigured into 3 stages with 2 parallel paths where CP1, CP2, and CP4 form the first CP path, and CP3, CP5, and CP6 form the second pumping path. Where CP1,3 boosts voltage from V_{DD} to $2V_{DD}$; CP2,5 boosts $2V_{DD}$ to $3V_{DD}$ and CP4,6 boosts $3V_{DD}$ to $4V_{DD}$. When V_{DD} is scenario above 0.5V ($V_{DD} > 0.5$ V), SCP,1,2,6,7,8 are turned ON while the rest is OFF. The CP is reconfigured into 2 stages with 3 parallel paths. The first path is made of CP1 and CP2, the second is made of CP3 and CP4 and the last is made of CP5 and CP6. In this configuration, CP1,3,5 is the first CP stage; boosting V_{DD} to $2V_{DD}$ whereas CP2,4,6 is the second stage responsible for boosting $2V_{DD}$ to $3V_{DD}$.

B. LOGIC CONTROL UNIT

The logic control unit is responsible for providing the control signals for controlling the CP configuration. Table 1 shows the breakdown of the control signal for each transmission gate where logic 1 represents the transmission gate being turned ON and logic 0 represents the switch turned OFF. From the table, it is evident that the circuit requires three distinct control signals (A, B, C) and their respective complementary signals (Ab, Bb, Cb) for the topology reconfiguration. For example, SCP,4,9,10 share the same logic signal of 0, 0, and 1 when CP is configured into 2, 3, and 4 stages, respectively. On the other hand, SCP,2,8 share the logic of 1, 1, and 0, which is the direct complement of the control signal A.

To provide the necessary control signals, a voltage detection unit of two Op-amp-based comparators is implemented to detect three voltage levels, below 0.4 V, between 0.4 V and 0.5 V, and beyond 0.5 V. This work adopted the comparator from [34] for voltage detection. Two reference voltages (V_{REF1}, V_{REF2}) are extracted from an external source

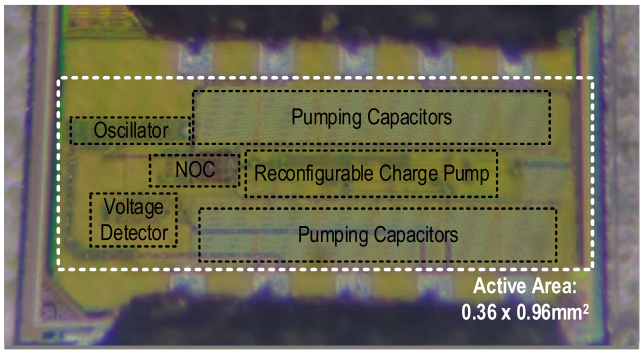


FIGURE 9. Photomicrograph of the proposed reconfigurable CP.

(V_{REF}) using diode-connected transistors which act as a voltage divider. The V_{REF} can be provided by a battery in a battery-assisted energy harvesting system. These reference voltages are then fed into the comparator in the voltage detection unit for voltage comparison.

The first comparator will compare V_{DD} with V_{REF2} of 0.4 V and return A = 1 if V_{DD} is smaller than the VREF2 and return A = 0 otherwise. As long as signal A is high, $S_{VD,1}$ and $S_{VD,2}$ will turn OFF to deactivate the second comparator to prevent unnecessary power consumption, this will also force signal B to remain low. When V_{DD} is larger than 0.4 V, signal A will be LOW, and the second comparator will be activated. It will compare V_{DD} with V_{REF1} of 0.5 V and return B = 1 if V_{DD} is less than V_{REF1} and return B = 0 if V_{DD} is larger than V_{REF1}.

The circuit can identify the three different input voltage ranges (below 0.4V, between 0.4 and 0.5V, and beyond 0.5V) by only using the two control signals generated from the comparators (signals A and B). However, signal A and signal B alone are not sufficient to control the CP configuration, as shown in Table 1. Therefore, an extra signal (C and Cb) is generated from signal A and signal B using an AND logic gate. The truth table of AND logic for signal C and Cb generation is described in Table 2. Using two comparators and an AND logic gate, six control signals covering all possible logic combinations can be generated.

This opens the possibility for future reconfigurable CP work which configure into a different number of stages.

V. CLOCK GENERATION

A. VOLTAGE-CONTROLLED RING OSCILLATOR

A ring voltage-controlled oscillator (RVCO) is a key block in the clock generation unit in the CP scheme to generate an oscillating clock signal [35], [36], [37], [38]. The generated oscillating frequency is dependent on the number of inverter cells and the delay time, as shown in the equation below [39] and [40]:

$$fosc = \frac{1}{2 \cdot N \cdot t_d} \quad (1)$$

where N represents the number of delay cell stages and t_d represents the delay time for each stage. The delay time depends on the input voltage of the oscillator and the transistor size [6]. Since the input voltage of an oscillator varies according to

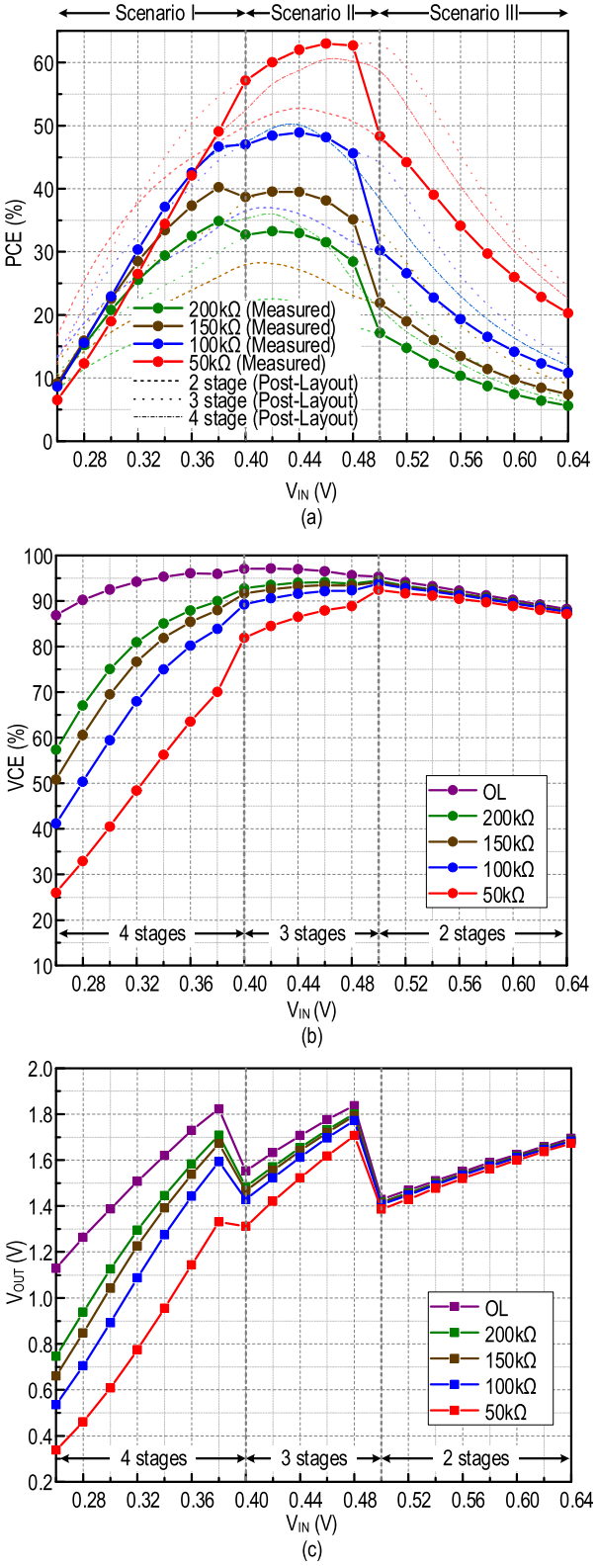
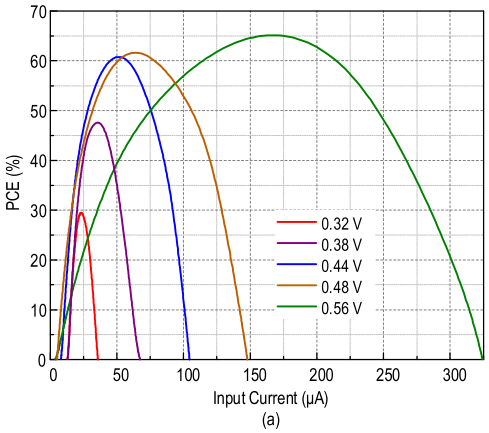


FIGURE 10. Measured performance of (a) PCE versus VIN (b) VCE versus V_{IN} (c) V_{OUT} versus V_{IN} at various output load condition.



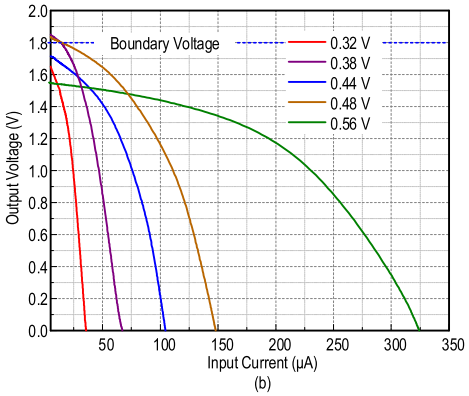


FIGURE 11. (a) Graph of PCE versus input current and (b) Graph of output voltage versus input current at various input voltage under 100k Ω condition.

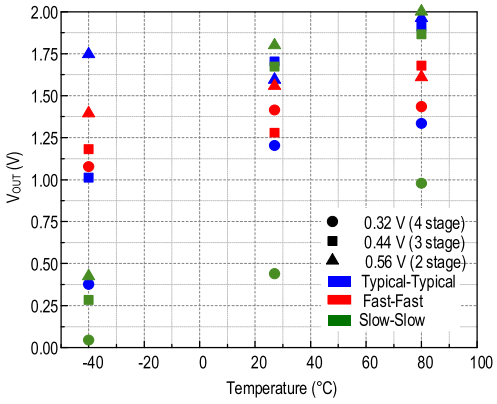


FIGURE 12. Post-layout PVT simulation of V_{OUT} at different input voltage at 100 kΩ.

the circuit's input voltage (V_{DD}), the output clock frequency range of the RVCO varies with V_{DD}. This effect is severe in EH applications where a wide input voltage range is common. In addition, high frequency increases switching losses in the charge pump. As the switching loss is inversely proportional to the conduction loss [41], it is important to regulate an optimal frequency for a balance point between the switching loss and the conduction loss for optimal CP performance.

The oscillating frequency can be reduced by increasing the number of delay cell stages or by reducing the oscillator's input voltage (V_{OSC}). However, increasing the number of delay cell stages is not a suitable method for frequency regulation as it will increase the oscillator's power consumption, which can be discernible from the equation below [39]:

$$P_C = N \cdot f_{OSC} \cdot C_L \cdot V_{OSC}^2 \tag{2}$$

Although reducing V_{OSC} seems like a good approach to satisfy the reduction in the oscillating frequency and the power consumption at the same time, reducing V_{OSC} will also reduce the oscillating signal's output amplitude swing, which reduces the conduction of the CP. Generally, the amplitude of the CP's clock signals is the same as the oscillating signal's amplitude. Having a lower amplitude will greatly reduce the CP performance and its CR, due to the increase in the on-resistance (R_{on}) of the charge transfer transistors as described in the equation below [41], [42]:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{3}$$

where μ is the mobility of the electron/holes; C_{ox} is the oxide capacitance; W/L is the ratio of width to length of the transistor, and V_{GS} is the gate-to-source voltage of the transistor which is equivalent to the clock amplitude.

As a countermeasure, a dynamic source-fed oscillator as a clock generation unit is proposed where a dynamic input voltage independent from the source voltage of the non-overlap clock is supplied for the oscillator. This is to achieve frequency regulation by changing V_{OSC} without affecting the output clock amplitude, V_Φ which is discussed next.

B. OSCILLATOR'S VOLTAGE CONTROLLER

The proposed clock generation unit consists of an oscillator's voltage controller (OVC), an RVCO, and a non-overlap clock (NOC) generator. The OVC is used to extract a lower voltage from V_{DD}, providing a dynamic input voltage for the RVCO. As depicted in Fig. 7, the OVC has three voltage divider paths with different effective resistances which can be activated using transmission gates SRO,1, SRO,2, and SRO,3 that are controlled through signals A, B, and C, respectively. In this work, the gate voltage for all transmission gates is derived from the V_{REF} with an amplitude of 1.5 V.

Path 1 consists of a single large-size diode-connected NMOS with an effective resistance of 3.142 kΩ. Path 2 consists of two diode-connected transistors with a width of 7.68 μm and 0.48 μm, yielding a total effective resistance of 5.806 kΩ. Path 3 has the highest total effective resistance of 9.524 kΩ from the two small-sized transistors with a width of 0.48 μm each.

The working principle is explained through 3 operational scenarios similar to Section II-B. In scenario I, as V_{DD} is low ($V_{DD} < 0.4$ V), SRO,1 will be turned on to activate the first voltage divider path, which has a relatively lower effective resistance. The resistance in path 1 will reduce the V_{DD} from 0.26 V ∼ 0.4 V to 269 mV ∼ 240 mV, providing a lower VOSC for the oscillator. In scenario II, the second path will be activated with SRO,2 turned on. The 5.806 kΩ

TABLE 3. Performance summary and the state-of-art comparison of the proposed circuit.

Parameters	This work	[20]	[51]	[22]	[21]	[52]	[7]
CMOS	65nm	180nm	130nm	180nm	180nm	180nm	65nm*
No. of Stage	2,3,4	1~9	4	4~6	4	4	2 ~ 4
Output Voltage Regulation Technique	Series-Parallel CP	Variable stage selection	Resistive voltage divider	Variable stage selection	Variable cascaded stage	Fast-transient dynamic reconfigure	Variable stage selection + clock amplitude reduction
Frequency Modulation Technique	Dynamic source-fed oscillator	Variable delay cell stage	Test register	Dynamic voltage for delay blocks	Dynamic voltage for delay blocks	TFM	-
Input Voltage (V)	0.26~ 0.64	0.25~ 1.1	0.27~ 1.4	1	1.2	2	0.45 ~ 0.7
Regulated Voltage (V)	1.8	1.8	1.4	3~6	2.2	6~10	1.2 ~ 3
Frequency (MHz)	4.3~ 24	0.75~7.5	0.6~1	0.01~20	70×10^{-6} ~ 19	-	10
Peak PCE (%)	62	57	58	58	75	69.8	73*
Area (mm^2)	0.346	-	0.42	0.5	0.069	0.66	0.023**

*simulation result
** oscillator not included

resistance from path 2 will decrease the VOSC to 180.5 mV ∼ 201 mV from V_{DD} of 0.4 V ∼ 0.5 mV as depicted in Fig. 5. In scenario III, SRO,3 will turn on to activate the highest resistance path 3 (e.g., 9.524 kΩ) to produce a V_{OSC} of 207 mV ∼ 257 mV. By using the three voltage dividing paths, a stable V_{OSC} can be regulated for the RVCO to generate a modulated frequency.

This work adopted an RVCO from [43] for clock frequency generation which has a better performance compared to the conventional oscillator in subthreshold operation. However, instead of utilizing the supply at node V_{DD}, this work uses V_{OSC} generated from OVC earlier as the voltage supply node. V_{OSC} is bounded from 169 mV to 257 mV using the control signals, A, B, and C. Thus, the frequency generated from the oscillator will also be maintained in the range of 4.3 MHz to 24 MHz, as depicted in Fig. 5. It is worth heeding that the unbounded V_{OSC} would rise from 168 mV to 384 mV, causing the unmodulated frequency to surge from 4 MHz to 148 MHz as delineated in the same figure.

C. NON-OVERLAP CLOCK GENERATOR

The non-overlap clock generator is an integration of two parts as shown in Fig. 8. The early part consists of two cross-connected NAND gates which are responsible for creating two non-overlapping signals for the CP pumping operation. The later part consists of a series of cascading inverters, forming a series of buffer that shapes the sinusoidal wave from RVCO into a square wave. The last few stages of inverters in the series of buffer takes V_{DD} as the supply voltage instead of V_{OSC}. This ensures the final output clock amplitude remains as V_{DD}, independent from the lower amplitude V_{OSC} of the RVCO.

VI. MEASUREMENT RESULT

We implemented the proposed CP in 65-nm CMOS, adopting on-wafer probing for the chip with an active area of 0.36×0.96 mm^2, shown in the photomicrograph in Fig. 9. To optimize the performance in subthreshold operation [44], this work adopted low-voltage threshold (LVT) devices in all charge transfer transistors to elevate the forward conduction loss. Other circuit blocks, such as OVC and the comparator, utilize standard threshold (SVT) transistors. Each CP stage in the circuit utilizes two 20 pF metal-insulator-metal (MIM) capacitors for the charge pumping operation. Additionally, a 120 pF MIM capacitor is employed as the load capacitor to reduce the output voltage ripple and provide a smoother output voltage.

To evaluate the proposed system's performance, we measure the PCE and the system's voltage conversion efficiency (VCE) at different load conditions as portrayed in Fig. 10 (a) and (b). PCE is a metric used to measure the effectiveness of a power conversion system in converting input power to usable output power while VCE is a measure of how effectively a voltage conversion system converts input voltage to output voltage. The formula for PCE and VCE is given below:

$$PCE = \frac{P_{OUT}}{P_{IN}} \times 100\% \tag{4}$$

$$VCE = \frac{V_{OUT(measured)}}{V_{OUT(ideal)}} \times 100\% \tag{5}$$

In scenario I where $V_{DD} < 0.4$ V, the LVT device and the switch-connection parallel CP configuration allow the reconfigurable CP to achieve a high PCE in subthreshold operation. In scenario II, the CP is configured into 3 stages with 2 parallel paths which lowers its effective resistance to

allow a high PCE. The performance of the CP in scenario II is observed to be superior compared to scenario I as the transistors are not operating in the subthreshold region owing to the higher input voltage. The peak PCE is recorded in scenario II with 62 % at 0.48 V when driving 50 kΩ loads. In scenario III, the CP performance drops despite having three parallel pumping paths. This is because the CP is optimized for low input voltage operation. The CP suffers high reverse current leakage across the LVT transistors in high-voltage operations. Moreover, the utilization of a 2-stage CP leads to a circuit mismatch that results in an ineffective transfer of power to the output load. To limit the output voltage under 1.8 V for safeguarding the system, the CP performance is sacrificed in scenario III.

Fig. 10 (b) depicts the VCE of the proposed reconfigurable CP. It exhibits over 80% VCE at all voltage ranges, with a peak VCE of 97% recorded at open load conditions with 0.4 V input voltage. The proposed circuit successfully limits the output voltage under 1.8 V in all load conditions for an input voltage of 0.26 V to 0.64 V as shown in Fig.10(c). As the input voltage rises from 0.26 V to 0.4 V, the circuit is reconfigured into 3 stages, lowers its CR to 4, and decreases the V_{OUT} under 1.8 V. The same phenomenon repeats itself at 0.5 V with the circuit configured into 2 stages, as illustrated in Fig. 10(c). This can prevent voltage overstress on the LVT devices used in the reconfigurable CCCP. The measured performance of the CP is provided in Fig. 11(a) as a function of the input current. From the figure, it can be observed that the peak PCE is shifted towards the right at a higher input voltage. In other words, lower stage configuration performs better with higher input current. The proposed CP is tested with various input currents up to a range of 325 μA. Fig. 11(b) illustrates the relationship between the input current and output voltage of the proposed circuit. The figure demonstrates that the proposed circuit effectively maintains the output voltage within the boundary level for most input current levels, except when the input voltage is near the configuration switching points (0.48V and 0.38V). Nevertheless, the circuit is capable of maintaining the boundary voltage at the input current level as low as 15 μA.

As depicted in Figure 12, the proposed circuit shows process variations of 17.66% (FF) and 63.4% (SS) for the 4-stage configuration at an input voltage of 0.32V. For the 3-stage and 2-stage configurations, the process variations are 24.88% (FF), 1.739% (SS), and 2.31% (FF), 12.86% (SS) respectively. Additionally, the circuit exhibits temperature variations of 68.7% (-40 °C) and 11% (80 °C) for the 4-stage configuration. The 3-stage configuration has temperature variations of 40.56% (−40 °C) and 12.3% (80 °C), while the 2-stage configuration has variations of 36.5% (−40 °C) and 19.9% (80 °C).

While the proposed circuit is effective in limiting the output voltage under 1.8V, it cannot regulate and maintain the output voltage level across the wide input voltage range. However, an auxiliary closed-loop regulation mechanism [19], [45], [46], [47], [48], [49], [50] can be implemented in conjunction with the proposed circuit to maintain a consistent output voltage. In this configuration, the proposed circuit caps the output voltage, while the auxiliary closed-loop circuit fine-tunes and maintains the desired output voltage level.

Table 3 summarizes and compares the proposed system with the state-of-the-art reconfigurable CP. Reference [51] limits the output voltage under 1.4 V using an output feedback mechanism with a resistive voltage divider. This technique compares the output voltage with a bandgap reference voltage to adapt the division ratio of the resistive voltage divider for voltage regulation. As a consequence, the output will suffer in power losses for the voltage absorbed by the resistive voltage divider. The works in [20], [21], and [22] regulated the output voltage by varying the number of CP stages in operation in a way similar to the proposed work. However, the work deactivates the CP to reduce its pumping stage instead of connecting them in parallel. This technique fails to utilize the advantage of the low equivalent circuit resistance that is obtained by connecting multiple CPs in parallel, resulting in a potential loss of harvesting efficiency.

Concerning using the approach of frequency regulation, [20] used a variable delay cell configuration for frequency modulation. Such configuration comprises different stages of delay cells to generate the desired frequency. However, as described in equation (2), the high number of delay stages will increase the power consumption in the clock generation circuit. The works in [21] and [22] perform frequency modulation by varying the voltage source of the delay cell, similar to the proposed work. The difference is, that the work utilizes the output from the CP as the dynamic source for the delay stages. Nevertheless, the high boosted voltage from the CP output will result in a high-power loss in the delay cells.

Table 3 demonstrates that the proposed reconfigurable CP exhibits the highest PCE among other state-of-the-art reconfigurable CPs for low-voltage energy harvesting applications [20], [22], [51] which achieved a peak PCE of approximately 58%. Although [21] and [52] achieved a slightly higher PCE, it was at a higher input voltage. Additionally, [7] achieved a 73% PCE, but it was based on simulation results and did not consider the power consumption of the oscillator. Furthermore, the proposed work recorded the lowest circuit complexity, occupying a silicon area of only 0.346 mm2.

VII. CONCLUSION

This work proposed a series-parallel CP architecture, consisting of a novel dynamic source-fed oscillator, a logic control unit, and a reconfigurable CCCP for low voltage energy harvesting application. By arranging the CCCP into 4, 3, or 2 stages in series and parallel, the proposed CP modified its VCR to maintain the output voltage under 1.8 V. It leveraged the advantage of low effective resistance in a parallel CP topology to enhance the CP performance. Additionally, this work devised a novel dynamic source-fed oscillator for frequency regulation using a dynamic input voltage for the RVCO that enabled frequency modulation without affecting the clock's amplitude. Validated on 65-nm CMOS, the

proposed architecture attained a 62% peak PCE and a 97% VCE performance with the lowest circuit complexity when compared with state-of-the-art reported designs.

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