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RESEARCH ARTICLE

Reference Temperature Sensor for TMOS-Based Thermal Detectors

ELISABETTA MOISELLO[1], (Member, IEEE), MARIA ELOISA CASTAGNA[2], ANTONELLA LA MALFA[2], GIUSEPPE BRUNO[2], PIERO MALCOVATI[1], (Senior Member, IEEE), AND EDOARDO BONIZZONI[1], (Senior Member, IEEE)

[1]Department of Electrical, Computer and Biomedical Engineering, The University of Pavia, 27100 Pavia, Italy
[2]STMicroelectronics, 95121 Catania, Italy

Corresponding author: Elisabetta Moisello (elisabetta.moisello@unipv.it)

ABSTRACT This paper presents a temperature sensor system providing the reference temperature of TMOS-based thermal detectors, in order to enable contactless absolute temperature measurements. The proposed system directly employs a few pixels of the TMOS detector as sensing element, thus detecting the local TMOS temperature, while the readout circuit is integrated on a separate chip. The readout circuit features a two-phase time-domain architecture, which provides biasing to the sensing element by alternatively switching between two different bias current values in subsequent phases. The temperature reading is converted to the digital domain thanks to a switched-capacitor 1-bit second-order sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC). The proposed readout system was fabricated in a 130-nm CMOS process and extensively characterized through measurements, together with the TMOS detector, realized in a 130-nm CMOS SOI technology and bonded on the same package. The proposed reference temperature sensor system, burning 10.8-μW power, features 97-mK resolution when considering a 4096-ms conversion time and 0.13°C peak-to-peak inaccuracy after three point calibration in the 15–40°C range, thus satisfying the characteristics for contactless human body temperature measurements.

INDEX TERMS Sensor, temperature, TMOS, thermal detector, interface circuit, resolution, inaccuracy, temperature-to-digital converter, switched capacitor, sigma delta, ADC.

I. INTRODUCTION

Thermal detectors, including bolometers, pyrometers, thermopiles and the recently developed TMOS, are employed in a wide range of applications: contactless absolute temperature measurements, presence and movement detection, gas analysis, climate control systems, space and military applications, security systems, medical devices, temperature monitoring in manufacturing processes, appliances and consumer products (microwave ovens, clothes driers, laser printers) [1]. Thermopiles [2], [3], [4], [5], [6], [7], [8] and the TMOS sensor [9], [10], [11], [12], [13], [15], in particular, have proven to be the most apt thermal detectors as they are compatible with standard CMOS processes and, therefore, enable large volume low cost production. Thermopiles operation relies on the Seebeck effect [1], [2], [7], while the TMOS sensor, consisting of a thermally isolated equivalent transistor able to absorb thermal radiation, exploits how the transistor I-V characteristics change depending on the temperature variation caused by the absorbed thermal radiation [1], [10], [11], [12]. The TMOS sensor, as it is an active device, features an intrinsic gain which results in enhanced responsivity with respect to thermopiles, while still enabling low power operation, as the TMOS is biased in subthreshold region. For these reasons, the TMOS appears to be particularly promising and the case of a TMOS-based thermal detector is considered in this paper.

The TMOS actually consists of a pair of devices, one active (i.e. exposed to the target thermal radiation) and one blind (i.e. covered by an aluminum mirror and thus shielded from the radiation) [11], [12] and the supplied signal depends on the temperature difference between the active and the blind device. Hence, in order to perform a contactless absolute temperature measurement, the blind device temperature, which

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acts as reference, must be known. Current commercial TMOS based solutions [14], however, designed for presence and motion detection, are not suited for absolute temperature measurements as the reference temperature sensor, implemented with a conventional solution, is not sufficiently accurate (±0.3°C in the -10°C to 60°C range). Furthermore, the reference sensor does not measure the blind TMOS temperature as it is not located on the TMOS chip, but on its readout circuit chip. Indeed the TMOS sensor is sealed under vacuum employing wafer level packaging while its bias and readout circuit are integrated on a separate chip, which is subsequently bonded on the same package as the TMOS sensor [15].

This paper proposes a solution to measure the reference temperature accurately and directly, with the aim of enabling the use of TMOS sensors, now limited on the market to presence and motion detection solutions, to absolute temperature measurements applications, and in particular human body temperature measurements. Indeed, the proposed solution allows directly measuring the blind TMOS temperature by exploiting as sensing elements a few of the pixels constituting the mosaic structure of TMOS detector, while still maintaining the bias and readout circuit on a separate chip. As different pixels, connected together in parallel and acting as an equivalent transistor, are employed, the average temperature across the pixels is measured. However, it can be supposed that no significant temperature difference among the pixels is present: this is reasonably the case, as the pixels are located on the same chip and are placed under vacuum. Hence it can be assumed that the measured temperature corresponds to the temperature of the overall blind TMOS device.

The changes required to the TMOS sensor are minimal and do not impact significantly its sensitivity.

The proposed bias and readout circuit for the reference pixels employs a two-phase time-domain architecture [16], which provides biasing to the sensing element by alternatively switching between two different bias current values in subsequent phases. The subtraction operation between the voltage signal found at two subsequent phases, resulting in a proportional-to-absolute-temperature (PTAT) dependency, and the temperature-to-digital conversion are performed by means of switched-capacitor 1-bit second-order $\Sigma\Delta$ ADC. The proposed reference readout system, fabricated in a 130-nm CMOS process, and the modified TMOS detector, realized in a 130-nm CMOS SOI technology, were bonded on the same package and extensively characterized through measurements. The proposed reference temperature sensor system features 10.8-μW power consumption, 97-mK resolution when considering 4096 digital samples and 0.13°C peak-to-peak inaccuracy after three point calibration in the 15–40°C range, thus satisfying the characteristics for contactless human body temperature measurements.

The paper is organized as follows. Section II illustrates the sensing element bias and readout circuit design, showing the required changes to the standard TMOS structure; Section III reports the measurement results characterizing the proposed

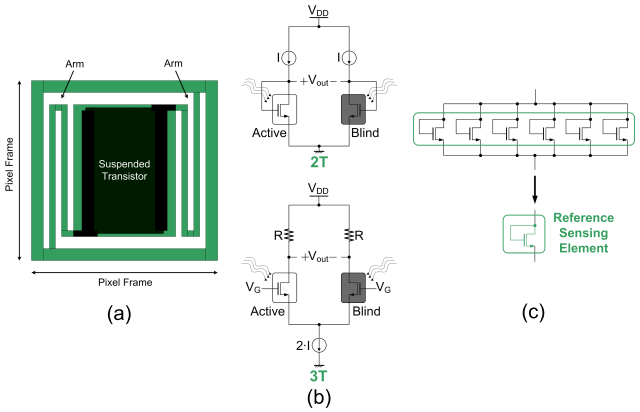

FIGURE 1. (a) schematic illustration of the TMOS pixel, (b) 2T and 3T TMOS configurations, (c) proposed reference sensing element.

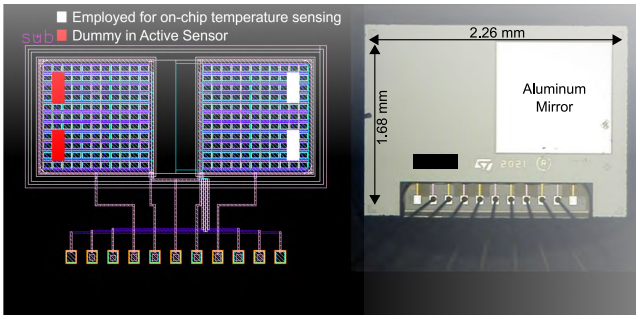

FIGURE 2. Modified TMOS (a) layout and (b) chip photograph.

reference temperature sensor system as well as the modified TMOS sensor; Section IV concludes the paper.

II. PROPOSED TEMPERATURE REFERENCE SENSOR SYSTEM

The TMOS sensor comprises two 8 × 8 pixels matrices, one active and one blind. Each pixel consists of a thermally isolated NMOS transistor on a suspended micromachined membrane, able to absorb thermal radiation, as shown in Fig. 1(a). All the pixels belonging to the same matrix are connected in parallel, thus implementing two equivalent transistors. A mosaic structure is employed as it enhances the sensor signal-to-noise ratio (SNR) [10]. The two equivalent transistors are operated in a 2-terminals (2T) or 3-terminals (3T) fashion and, considering a voltage mode approach where a bias current is applied, the differential voltage found at the drains is the signal providing the temperature difference between active and blind device, i.e. between the target and the reference, as illustrated in Fig. 1(b) [11]. Alternatively, also a current mode approach where a bias voltage is applied and a signal current is generated, can be considered [17].

In order to directly measure the blind device temperature, acting as reference, the matrix connections are modified: indeed six pixels from the blind device matrix are not placed in parallel to the others, but are connected together implementing an equivalent diode-connected NMOS device, which

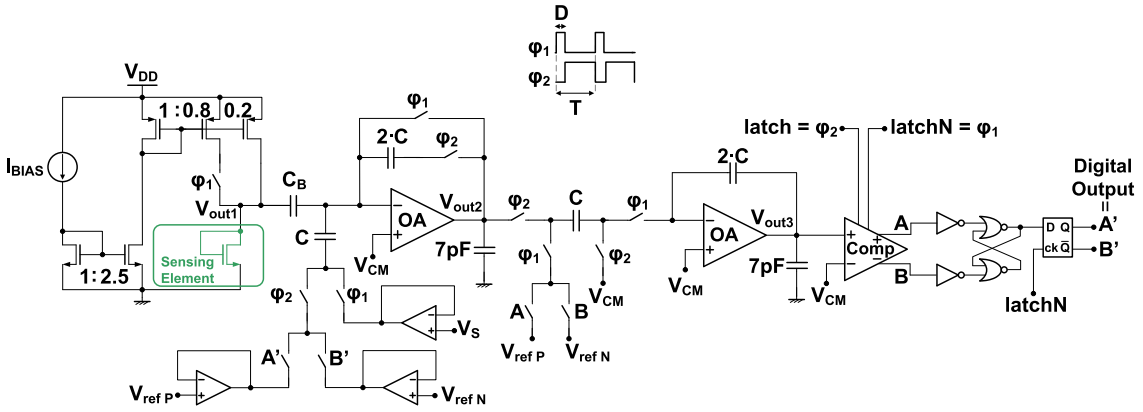

FIGURE 3. Proposed reference temperature sensor system.

is employed as sensing element, as illustrated in Fig. 1(c). The pixels location was selected in order to provide minimal disruption of the original TMOS pixels connections and easiness of layout. For matching purposes six pixels from the active device are not placed in parallel to the others as well: hence the active and blind devices actually consist of 58 pixels each, instead of 64. The TMOS package, which enables maintaining the sensor under vacuum, remains unchanged, apart from the extra pads required for bonding the reference sensing element source and drain terminals to the readout circuit on the separate chip. The modified TMOS layout and photograph are shown in Fig. 2(a) and (b), respectively.

The reference sensor system, employing the six diode-connected pixels from the blind device as reference sensing element, is illustrated in Fig. 3. During *Phase* 1, when ϕ_1 is high, the sensing element bias current is $2.5{\cdot}I_{BIAS}$, while during *Phase* 2, when ϕ_2 is high instead, the bias current is $2.5{\cdot}0.2{\cdot}I_{BIAS}$. The sensing element equivalent transistor is operated in subthreshold region, hence, provided that the drain-to-source voltage, V_{DS}, is larger than a few kT/q (i.e. the thermal voltage), V_{out1} during *Phase* 1 and *Phase* 1 is given, respectively by

$$V_{out1,\,1} = V_{TH} + \frac{n \cdot k \cdot T}{q} ln \frac{2.5 \cdot I_{BIAS}}{I_{D0}} \tag{1}$$

and

$$V_{out1,\,2} = V_{TH} + \frac{n \cdot k \cdot T}{q} ln \frac{2.5 \cdot 0.2 \cdot I_{BIAS}}{I_{D0}} \tag{2}$$

where V_{TH} is the equivalent transistor threshold voltage, k the Boltzmann constant, T the temperature expressed in Kelvins, q the magnitude of the electron charge, n a process dependent parameter, I_{D0} the drain-to-substrate leakage current of the equivalent transistor acting as sensing element times its aspect ratio, and $V_{out1,\,i}$ stands for the voltage at node V_{out1} during *Phase* i.

The voltage difference between $V_{out1,\,1}$ and $V_{out1,\,2}$, therefore, is

$$V_{out1,\,1} - V_{out1,\,2} = \frac{n \cdot k \cdot T}{q} ln \frac{2.5 \cdot I_{BIAS}}{2.5 \cdot 0.2 \cdot I_{BIAS}} \tag{3}$$

The readout circuit, consisting of a switched capacitor second-order 1-bit $\Sigma\Delta$ ADC, performs the difference between $V_{out1,\,1}$ and $V_{out1,\,2}$, while applying a gain and a voltage shift: indeed the voltage converted to the digital domain is

$$\frac{C_B}{C}(V_{out1,\,1} - V_{out1,\,2}) + V_S \tag{4}$$

which yields a PTAT behaviour as its first derivative with respect to temperature is

$$\frac{C_B}{C}\frac{d(V_{out1,\,1} - V_{out1,\,2})}{dT} = \frac{C_B}{C}\frac{n \cdot k}{q} ln \frac{1}{0.2} \tag{5}$$

With respect to [16], both the amplification and the analog-to-digital conversion are performed by the ADC block, without employing an additional amplifier to provide gain before the ADC.

Reference voltages, $V_{ref,P}$ and $V_{ref,N}$, as well as V_S, are provided through analog buffers. The integrators, whose feedback networks implement 0.5 coefficients, are realized by amplifiers featuring a standard mirrored architecture [16]. A latched comparator, whose architecture is reported in [16], implements the single-bit quantizer. The autozero technique is applied to the first amplifier. Compensation capacitances equal to 7 pF are added to ensure the amplifiers stability. Capacitances C are set equal to 200 fF and C_B is set equal to C as well: indeed, choosing a gain equal to 1 allows minimizing C_B and thus the area. For the same reason an additional analog gain stage, as the one in [16], is not employed.

The switching period T and duty cycle D must be chosen taking into account that $D \cdot T$ has to be long enough to allow settling, T should be minimum for minimizing the conversion time and D, together with the value of I_{BIAS}, should be selected in order to avoid self-heating effects in the sensing element. The value of I_{BIAS} is chosen equal to 78 nA, resulting in a sensing element bias current switching between I_1, equal to 195 nA, and I_2, equal to 39 nA. The root-mean-square (RMS) bias current, I_{RMS}, hence is

$$I_{RMS} = \sqrt{D \cdot I_1^2 + (1 - D) \cdot I_2^2} \tag{6}$$

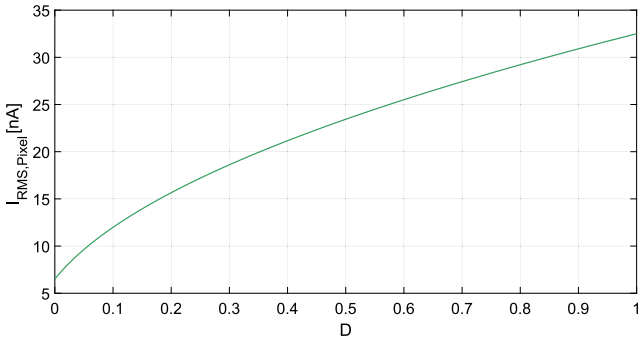

FIGURE 4. Single pixel RMS bias current as a function of the duty cycle.

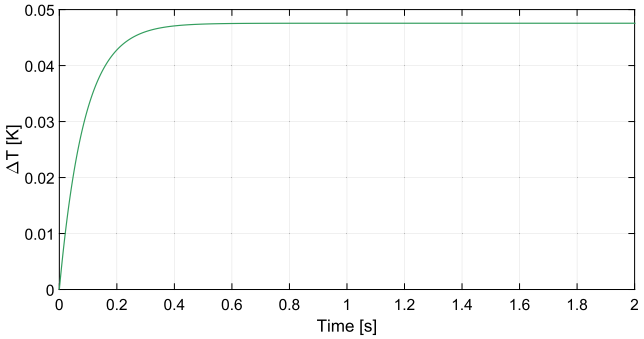

FIGURE 5. Self-heating temperature increase as a function of time.

Since the TMOS pixels are thermally isolated, and the thermal time constant of the whole matrix is equal to the one of the single pixel [10], the self heating effect can be studied considering a single pixel in the proposed reference sensing element: the single pixel RMS bias current, $I_{RMS,Pixel}$, equal to $I_{RMS}/6$, is reported in Fig. 4 as a function of D. The TMOS thermal detector employs a constant 15.625 nA bias current per pixel, hence, in order not to exceed this value for the sensing element pixel bias current as well, a duty cycle equal to 0.15 was selected, corresponding to $I_{RMS,Pixel}$=13.94 nA.

The TMOS pixel self heating can be modeled as temperature increase ΔT [18]

$$\Delta T = \frac{P_{Jh}}{G_{th}} e^{-\frac{t}{\tau}} \tag{7}$$

where P_{Jh}=$I_{RMS,Pixel}$ · V_{DS} is the Joule heating, G_{th}=8.5·10^{-8} W/K the thermal conductance [12], τ=87 ms the thermal time constant [12] and t the time. The sensing element drain-to-source voltage V_{DS} is considered equal to 0.29 V (i.e. the largest expected value of V_{DS}). The temperature increase as a function of time is reported in Fig. 5, considering the chosen I_{BIAS} and D values. As the required settling time at node V_{out1} is 150 μs, T is chosen equal to 1 ms. By looking at Fig. 5 it is evident that the self-heating temperature increase is limited to 47.6 mK, which is deemed acceptable for the application. Furthermore, this could be reduced by periodically turning off the system in order to allow the cool down [18].

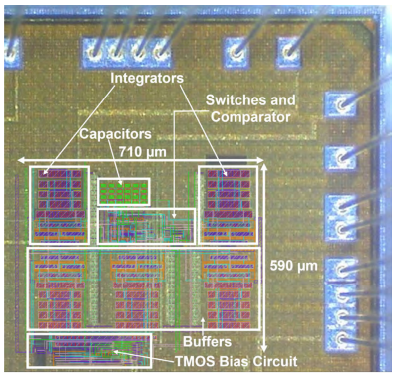

FIGURE 6. Proposed bias and readout circuit chip micrograph.

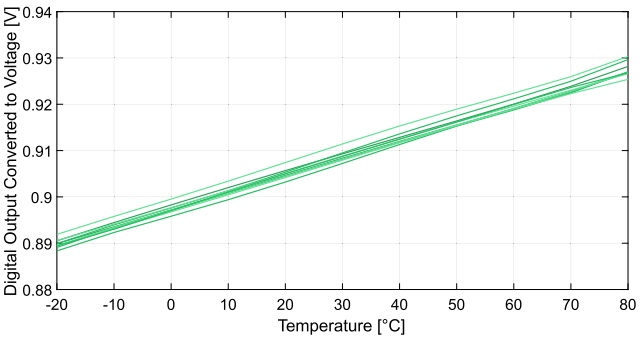

FIGURE 7. Measured digital output converted back to voltage as a function of temperature for the considered 10-samples batch.

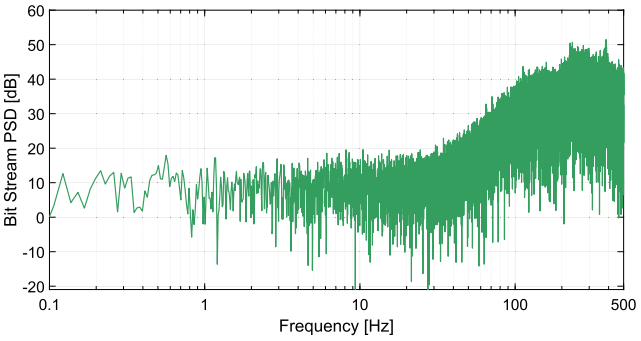

FIGURE 8. Measured bit-stream power spectral density as a function of frequency.

III. MEASUREMENT RESULTS

The proposed temperature reference sensor bias and readout circuit was fabricated in a standard 130-nm CMOS process by STMicroelectronics. The chip photograph, with the layout superimposed, is shown in Fig. 6. The total core area is 0.4 mm^2, including the reference buffers. The readout test chip was bonded on the same package with the modified TMOS sensor, sealed under vacuum through wafer level packaging. A batch of 10 samples, belonging to the same wafer lot, was considered for experimentally characterizing the proposed system. The measurement setup, controlled by means of a LabVIEW program, comprised two Agilent

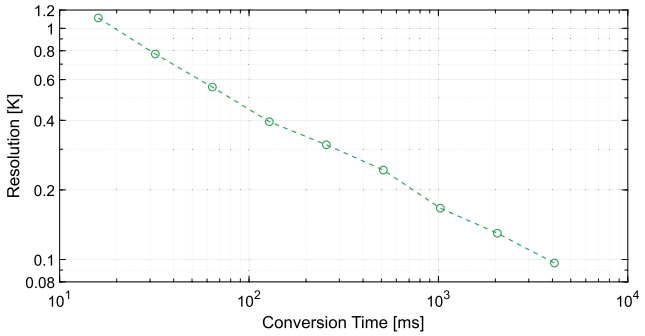

FIGURE 9. Measured system resolution as a function of the conversion time.

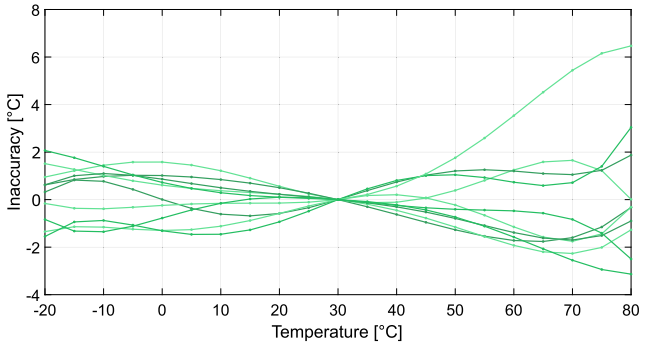

FIGURE 10. Measured inaccuracy across 10 samples after 1-point calibration at 30°C.

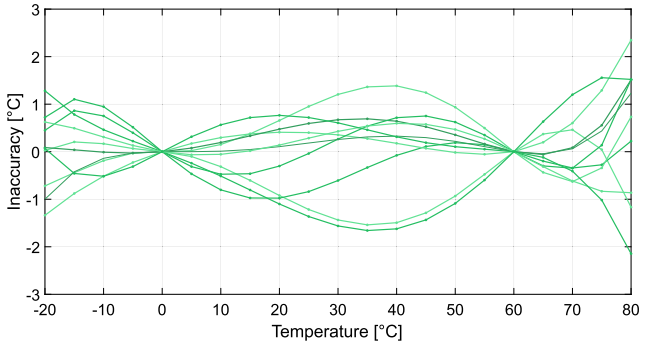

FIGURE 11. Measured inaccuracy across 10 samples after 2-points calibration at 0 and 60°C.

E3631A power supplies, employed for providing the reference and supply voltages, a Tektronix AFG3252 function generator, which supplied the 1-kHz 0.15-duty cycle clock signal, and a Digilent Digital Discovery working as a logic analyzer to gather the digital output data, which were then processed through MATLAB. The fabricated circuits were tested in a climatic chamber, with a controlled ambient temperature ranging between -20 and 80°C. The supply voltage, V_{DD}, was set to 1.8 V, V_{CM} to 0.9 V, V_{refP} to 0.94 V, V_{refN} to 0.86 V and V_S to 0.84 V. Current I_{BIAS} was regulated to 78 nA by means of on-board trimming resistors. The total power consumption is 10.8 μW.

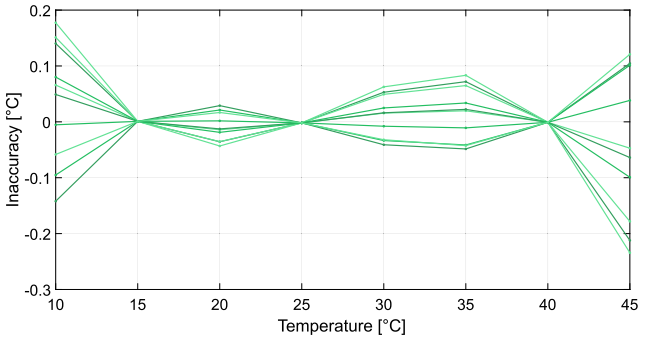

FIGURE 12. Measured inaccuracy across 10 samples after 3-points calibration at 15, 25 and 40°C.

The measured digital output, converted back to voltage, for the considered ten chip samples is illustrated in Fig. 7. The measurements were performed averaging 65536 digital output samples for each considered temperature.

In order to verify the $\Sigma\Delta$ ADC noise shaping effect, the measured bit-stream power spectral density (PSD) is plotted in Fig. 8 as a function of the frequency: the +40dB/dec noise shaping effect of the second-order $\Sigma\Delta$ ADC is clearly visible. The PSD was derived considering 65536 samples measured at room temperature, processed with a Hann window.

The system resolution was evaluated as a function of the conversion time, after performing a decimation with an 8^{th}-order Chebyshev filter in MATLAB, and plotted in Fig. 9. Resolution lower than 97 mK can be obtained with a conversion time larger than 4096 ms.

Different digital calibrations, including 1, 2 or 3 temperature trimming points, were performed in MATLAB. The measured output voltage characteristics as a function of temperature for each sample of the proposed sensor were considered and inverted, thus obtaining the temperature characteristics as a function of the sensor output voltage for each sample. The obtained curves were then averaged, deriving a reference temperature characteristics as a function of the sensor output voltage.

When considering a single temperature calibration point, the difference between the specific sample output voltage and the reference characteristic output voltage at the calibration temperature is derived and then subtracted from each specific sample output voltage characteristic, thus deriving the one-point calibrated characteristics.

When considering a 2-point temperature calibration, the sensitivity is calculated as the ratio of the difference between the output voltages at the two calibration temperatures and the difference between the two temperatures; the sensitivity derivation is performed for the specific samples characteristics as well as for the reference characteristic: the gain used to correct each sample characteristic is then obtained as the ratio between the specific and the reference sensitivity.

In the case of the 3-point calibration, the output voltages of the reference characteristics corresponding to the three temperatures chosen for the calibration were considered as

reference output voltages. A specific second-order polynomial function for each sample characteristics was derived by fitting the sample output voltages with respect to the reference output voltages. The output voltage of each sample was then processed through the corresponding derived correction polynomial, thus obtaining the calibrated voltages.

The resulting inaccuracy values as a function of temperature resulting after 1, 2 or 3-point calibration are reported in Fig. 10, Fig. 11 and Fig. 12, respectively. One temperature trimming point allows achieving 9.61% relative inaccuracy (Rel IA) in the -20–80° temperature range, which is reduced to 4.49% when two trimming points are employed. For very low inaccuracy applications, such as human body contactless temperature measurements, three temperature trimming points should be employed, resulting in a peak-to-peak inaccuracy (PP IA) of 0.41 and 0.13 considering the 10–45° and 15–40° temperature range, respectively. The large inaccuracy values when considering one or two trimming points is due to the fact that relatively low matching can be achieved from one TMOS detector (and hence reference temperature sensing element) to the other without calibration: indeed the TMOS pixels are obtained through MEMS micromachining, which is less controlled than regular CMOS processes. Considering that calibration is required for the TMOS detector itself, provided that the same trimming temperature points are used for the detector and the reference, the additional calibration cost is not significant. For example the TMOS detector calibration could be performed employing a black body at 37°C as target object, while varying the ambient, and thus reference, temperature.

The proposed reference temperature sensor system performance is summarized and compared to other on-chip temperature sensors, all comprising an ADC, in Tab. 1. Different sensor types and technology nodes are considered in order to provide a complete overview of the state-of-the-art. The proposed sensor system achieves a peak-to-peak inaccuracy value comparable with the state-of-the-art, when considering 2-points temperature calibration, and excellent inaccuracy when reducing the temperature range and performing 3-points trimming, targetting contactless human body temperature measurement applications. The 10.8-μW power consumption well matches the other reported sensors and is compatible with low power operation, as required by wearable and portable devices. The drawback of the proposed sensor system is the long conversion time, which is more than an order of magnitude larger than the second-longest reported in Tab. 1. However, it must me taken into account that the proposed system necessitates a very low clock frequency (1 kHz), in order to allow settling, while most of the other reported temperature sensors feature an ADC clock frequency in the MHz range: hence the number of digital samples and clock cycles required for obtaining the reported resolution is not so large, compared with the-state-of-the-art.

In order to verify that sacrificing six pixels of the TMOS detector does not impact on the thermal sensor performance, the modified TMOS (featuring 58 pixels each for the active and blind detector device) and the standard TMOS detector (featuring 64 pixels instead of 58) were studied by means of simulations and measurements considering a 2T configuration, as illustrated in Fig. 1(b). The difference between blind and active device drain voltage was considered as output voltage (V_{out}) in order to obtain a positive sensitivity value; indeed if the difference between active and blind voltage was considered instead, the sensitivity would be negative [12].

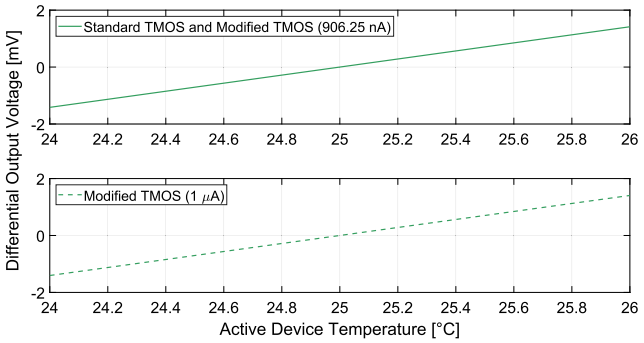

FIGURE 13. Simulated TMOS detector output voltage as a function of the active device temperature. The blind device temperature was set to 25°C.

Simulations were performed in Cadence Virtuoso changing the active TMOS block temperature with respect to the overall simulation temperature: in this way a temperature difference between active and blind device was modeled. The overall simulation temperature, acting as ambient temperature, was set equal to 25°C, while the active TMOS block temperature was varied from 24 to 26°. The simulation was performed setting the bias current I, equal for both the active and the blind device, to 1 μA for the standard TMOS case; for the modified TMOS case the simulations were performed considering a 1-μA, as well as a 906.25-nA, bias current: in this way the modified TMOS was studied maintaining the same overall bias current of the standard TMOS in one case and the same current per pixel in the other. When maintaining the same bias current per pixel, the same simulation results of the standard TMOS were obtained for the modified TMOS: this was expected as the same current per pixel ensures that the same operating point is maintained for the same local temperature variations. The simulation results, illustrating the differential output voltage as a function of the active device temperature for all considered cases, are reported in Fig. 1. Considering the slopes of the simulated curves, the sensitivity to the TMOS temperature values are derived and reported in Tab. 2.

The modified and standard TMOS detectors, fabricated in 130-nm CMOS-SOI technology, were also studied experimentally: they were measured employing a 4 inches × 4 inches SR-800R 4D/A [19] black body source and the same 2T configuration. The bias current I was provided by a sourcemeter. Four samples for each type of TMOS detector were considered. The black body temperature was varied from 0 to 120°C in 20°C increments and the drain differential output voltage, V_{out}, of each sample was acquired

TABLE 1. Sensor System Performance Summary and Comparison With Other State-of-the-Art On-Chip Temperature Sensors.

	This Work	JSSC '17 [20]	ASSCC '17 [21]	TCAS-II '20 [22]	TCAS-II '21 [23]	ISSCC '22 [24]	TVLSI '22 [25]	ESSCIRC '22 [26]	TIM '23 [16]
Technology [nm]	130	180	10	180	65	5	16	180	130
Sensor Type	Micromachined MOS	MEMS	BJT	BJT & MOS	Resistor	Resistor	MOS	BJT	MOS
Area [mm^2]	0.4	0.54	0.01	0.12	0.47	0.0064	0.0007	0.08	0.63
Number of Samples	10	NA	20	15	14	20	16	20	16
Trimming Points	1 [a], 2 [b], 3 [c,d]	NA	1	1	2	2	2	2	1
Temperature Range [°C]	-20 to 80 [a,b], 10 to 45 [c], 15 to 40 [d]	-40 to 85	30 to 85	-10 to 100	-5 to 95	-40 to 150	-20 to 100	-20 to 80	-40 to 90
PP IA [°C]	9.61 [a], 4.49 [b], 0.41 [c], 0.13 [d]	NA	5.6	4.7	3.4	3.6	4	1.39	1.7
Rel IA [%]	9.61 [a], 4.49 [b], 1.17 [c], 0.52 [d]	NA	10.18	4.3	3.4	1.89	3.3	1.39	1.3
Power Consumption [μW]	10.8	19000	125	0.0005	0.3	15	41.8	39.6	23.6
Conversion Time [ms]	4096 [e], 32 [f]	5	1	200	10	0.012	0.0069	0.064	6.4
Resolution [mK]	97 [e], 774 [f]	0.2	173	300	9.8	114	320	158	40

[a] considering 1-point trimming and -20–80°C range

[b] considering 2-point trimming and -20–80°C range

[c] considering 3-point trimming and 10–45°C range

[d] considering 3-point trimming and 15–40°C range

[e] considering 4096-ms conversion time

[f] considering 32-ms conversion time

TABLE 2. Standard and Modified TMOS Sensitivity Values.

	Standard TMOS	Modified TMOS	Modified TMOS
Number of pixels	64	58	58
Bias Current [μA]	1	1	0.90625
Simulated Sensitivity to Active TMOS Temperature [μV/°C]	1416	1406	1416
Measured Sensitivity to Black Body Temperature [μV/°C]	69.42	67.29	73.07

through a digital multimeter. The bias current I was set to 1 μA for the standard TMOS, while the modified TMOS samples were measured twice, for both 1-μA and 906.25-nA bias currents. The measured TMOS thermal detector output voltage, considering a 3-cm distance between the black body and the detector, is reported in Fig. 14 for the standard TMOS case, while the measurement results for the modified TMOS sensor case, considering both a 1-μA and a 906.25-nA bias current, are shown in Fig. 15.

The TMOS thermal sensor output signal depends on $(T^4_{BlackBody} - T^4_{Ambient})$ [2], however its behaviour can be well approximated through a linearization considering a limited temperature range. Hence, considering the linear fit of the measured results in the 0–60°C temperature range, it was possible to calculate the thermal detector sensitivity, with respect to the black body temperature, as the linear fit slope for each sample taken into consideration. The derived sensitivity values for the same type of TMOS detector (with the same bias current) were then averaged in order to obtain a reference sensitivity for the standard and for the modified TMOS detectors. The derived sensitivity values with respect to the black body temperature are reported in Tab. 2. The difference between the sensitivity with respect to the local TMOS temperature and the one with respect to the black body temperature is determined by the transfer factor coefficient (TF) [9], which in turns depends on the thermal detector geometry (e.g. its fill factor): hence, the TF varies depending on the number of active pixels and is different for the standard and modified TMOS case. The black body thermal radiation, therefore, does not result in the same local temperature variation in the standard and in the modified TMOS case: for this reason,

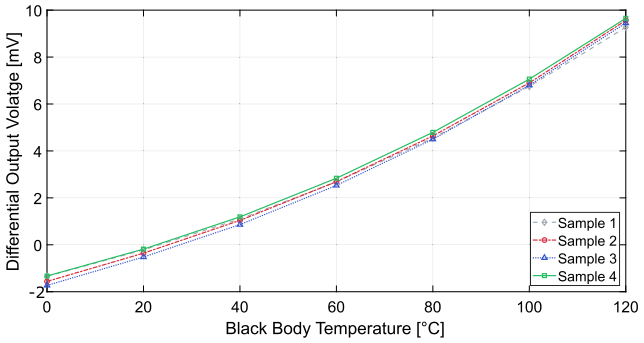

FIGURE 14. Measured standard TMOS detector output voltage as a function of the black body temperature.

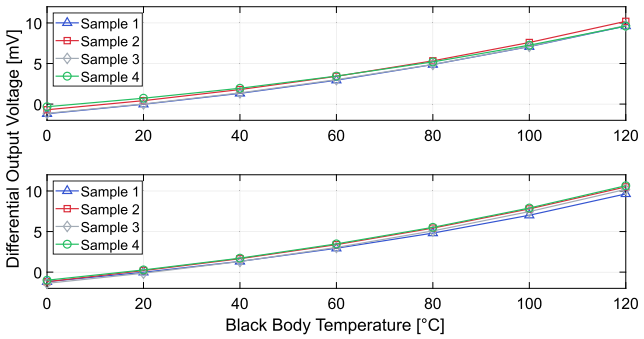

FIGURE 15. Measured modified TMOS detector output voltage as a function of the black body temperature for a 1-μA (top) and a 906.25-nA (bottom) bias current.

the decrease in the sensitivity to the target object temperature and the one in the sensitivity to the local TMOS temperature, observed in the modified TMOS case with respect to the standard TMOS case (for the same overall biasing current), are not proportionally the same. Furthermore, although the same sensitivity is expected for both the standard and the modified TMOS case, provided that the bias current is scaled accordingly, the modified TMOS features a higher sensitivity value: this is due to the fact that the manufactured TMOS samples in the two cases belong to different wafer lots and thus inherently feature slightly different performances.

By looking at Tab. 2 it is evident that sacrificing six pixels for implementing the reference temperature sensor does not compromise the thermal detector performance.

IV. CONCLUSION

This paper has presented a temperature sensor system in order to provide the reference temperature of TMOS-based thermal detectors. Six pixels of the standard TMOS detector are employed as sensing element, thus detecting the local TMOS temperature, while the bias and readout circuit, comprising a switched-capacitor 1-bit second-order $\Sigma\Delta$ ADC, is integrated on a separate chip. The regular TMOS detector hence is slightly modified while still maintaining good sensitivity and the same package to ensure vacuum. The proposed reference temperature sensor system, featuring 10.8-μW power consumption, was experimentally characterized: 97-mK resolution was achieved when considering 4096 digital samples and 0.13°C peak-to-peak inaccuracy was obtained after three point calibration in the 15–40°C range. As typically the environment temperature range when considering human body temperature measurement is -15 to 40°C and the desired overall inaccuracy is $\pm$0.3°C, spending one third of the ''inaccuracy budget'' for the proposed reference sensor enables the design of a thermal detector with feasible inaccuracy requirements that satisfy the characteristics for contactless human body temperature measurements. The proposed reference temperature sensor, therefore, can be employed in applications performing absolute as well as relative temperature measurements. Furthermore, the proposed strategy, i.e. sacrificing a few of the pixels for implementing the reference sensor, is not necessarily limited to the case of TMOS detectors, but can be extended to other types of thermal detectors, e.g. thermopiles, consisting of multiple pixels. Future developments will include the employment of additional techniques, such as dynamic element matching (DEM) on the current mirrors biasing the sensing element, in order to furtherly improve the sensor accuracy.

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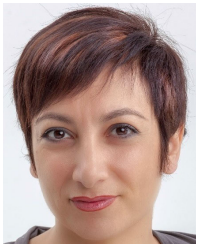
ELISABETTA MOISELLO (Member, IEEE) was born in Pavia, Italy, in 1993. She received the master's degree (summa cum laude) in electronic engineering and the Ph.D. degree in microelectronics from The University of Pavia, in 2017 and 2020, respectively. She is currently a Postdoctoral Research Fellow and a Contract Professor with the University of Pavia. Her research topics include interface circuits for integrated temperature sensors, switching dc–dc converters, and wireless power transfer.



MARIA ELOISA CASTAGNA received the bachelor's degree in physics from the University of Catania, with a research thesis in the optoelectronic field. In 2001, she joined the STMicroelectronics Research and Development Group, focusing on the design and characterization of optoelectronic components and related integration in several technological platforms. Her research interest includes the evaluation and start-up of optical architectures for signals transduction in bio-technological platforms for applications on healthcare and diagnostic field.

ANTONELLA LA MALFA received the master's degree (summa cum laude) in computer engineering from the University of Catania, Italy, in 2017. In 2017, she joined STMicroelectronics, as a Characterization Engineer, working with ASIC interface for MEMs environmental sensors and infrared TMOS sensors.

GIUSEPPE BRUNO received the degree in electronic engineering from the University of Palermo, Italy, in 1994. In 1995, he joined STMicroelectronics, where he was involved in the design of power bipolar transistors. From 1998 to 2007, he was appointed as the Cellular Front End Module Design Manager. In this period he has focused on the development of fully integrated power amplifier modules for mobile handset GSM/WCDMA. Since 2010, he has been the Innovation Product Design Manager with ST Analog MEMS and Sensor (AMS) Research and Development Organization, with main focus on environmental and optical MEMS sensors and bio-potential acquisition systems.

PIERO MALCOVATI (Senior Member, IEEE) graduated in electronic engineering from The University of Pavia, Italy, in 1991. He received the Ph.D. degree in electrical engineering from ETH Zurich, in 1996. He was an Assistant Professor (1996–2001) and an Associate Professor (2002–2017) with the Department of Electrical, Computer, and Biomedical Engineering at the University of Pavia, where he has been a Full Professor since 2017. His research activities are focused on micro sensor interface circuits, power electronics circuits, and high-performance data converters. He was/is a member of the Technical Program Committees for several international conferences, including ISSCC, ESSCIRC, SENSORS, ICECS, and PRIME. He is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

EDOARDO BONIZZONI (Senior Member, IEEE) received the Laurea degree (summa cum laude) in electronic engineering and the Ph.D. degree in electronic, computer, and electrical engineering from the University of Pavia, Italy, in 2002 and 2006, respectively. He is currently an Associate Professor with the Department of Electrical, Computer, and Biomedical Engineering at the University of Pavia. His current research interests are focused on the design and testing of A/D converters, dc–dc converters, high-precision amplifiers, and sensors interfaces. He is a TPC Member of IEEE CICC. From 2016 to 2019, he was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS. He is currently the incoming Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS for the 2024-2025 term.

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