IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 27 June 2023, accepted 27 August 2023, date of publication 6 September 2023, date of current version 15 September 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3312600

RESEARCH ARTICLE

An Ultra-Small Area and High-Sensitivity Wireless Receiver for ISM and MICS Band Application

WENYA CHEN, HAOHAN YANG, AND SHUSHAN QIAO, (Member, IEEE)
Institute of Microelectronics of the Chinese Academy of Sciences, Chaoyang, Beijing 100029, China
University of Chinese Academy of Sciences, Shijingshan, Beijing 100049, China

Corresponding author: Shushan Qiao (qiaoshushan@ime.ac.cn)

This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFB2204601.

ABSTRACT In this work, a 0.43mm^2 high-sensitivity low-intermediate-frequency (low-IF) receiver under 0.18 μm technology is reported for Industrial Scientific Medical (ISM) and Medical Implant Communications Service (MICS) band applications, which supports the 2ASK/GFSK demodulation mode. To reduce the area, a low noise amplifier (LNA) with an active inductor, a compact Gm-C filter, an AC current bleeding technique for controlling the receiver gain and, a ring-VCO LO PLL were used, without any passive inductors. The main methods for improving sensitivity are reducing the receiver noise figure (NF) and improving the signal-to-noise ratio for demodulation. Thus, the LNA adopts a two-stage 40 dB gain to suppress the NF of the subsequent stage. An automatic gain control (AGC) loop is used to control the receiver gain to overcome the large signal nonlinearity from the large LNA gains. Additionally, a Gm-C complex filter rejects image and blocks interference, improving the sensitivity to harsh environments. Under the CSMC 0.18 μm process, the die of the receiver is only 0.43 mm^2 and covers 300-500 MHz, MICS and some ISM bands. The measurement results show that when the internal 2ASK demodulator is adopted, it has a -115 dBm sensitivity at 2 Kbps; and when the external GFSK digital baseband is adopted, it has a -121 dBm sensitivity at 2 Kbps. At 300 Kbps, only 6.5 mW of power is consumed. It is suitable for low-power wide-area network (LPWAN) applications.

INDEX TERMS Active inductor load LNA, AGC loop, Gm-C filter, ISM/MICS band, low-IF receiver, LPWAN, radio frequency, 2ASK/GFSK modulation.

I. INTRODUCTION

Low-power wide-area network (LPWAN) has become the mainstream technique for Internet of Things (IoT) access in recent years. It has the characteristics of low power, long distance and low cost. Regarding its applications, it is often used in parking management systems, smart homes, and industrial automation. With the development of medical monitoring technology, LPWAN plays an important role in biological sign monitoring, bringing convenience to patients and doctors [1], [2]. Consequently, Industrial Scientific Medical (ISM) and Medical Implant Communications Service (MICS) band-related academic research have been updating iteratively.

ISM belongs to the nonauthorized free frequency band, which is widely used by NB-IoT. [e.g., China & Europe (433.05-434.79 MHz)]. Especially, owing to the low frequency, the 433 MHz frequency band is suitable for low-power and high-sensitivity designs. As reported in [3], the sensitivity of the ISM band receiver was -130 dBm. However, the RF front-end area of the receiver reached 5.91 mm^2 (180 nm), which does not satisfy the low-cost characteristics of the LPWAN. References [4] and [5] reported two receivers of the ISM band, whose areas were 0.79 mm^2 (180nm) and 0.45 mm^2 (40nm) respectively; however, the sensitivity was only -82 dBm at 50 Kbps and -101.5 dBm at 31.25 Kbps, respectively. In addition, they have poor anti-interference performance and are not suitable for harsh industrial environments.

In 1999, the FCC classified 402-405 MHz as the MICS band and expanded it to 413-457 MHz to form a medical micro power network (MMN). The rates of different medical devices are shown in Table 1 [2]. References [6] and [7]

The associate editor coordinating the review of this manuscript and approving it for publication was Tae Wook Kim.

reported two ultralow power MICS band receivers, which eliminate low noise amplifiers (LNA) and have small areas of 0.3 mm^2 and 0.137 mm^2, respectively. However, its noise figure (NF) and sensitivity are insufficient, and [8] also reported an OOK receiver without the conventional RF part, consuming only 1.79 μW and occupying an area of 0.92 mm^2. However, its sensitivity is only −40 dBm, and it has no anti-interference ability, easy to be interfered with by traditional ISM applications.

TABLE 1. Data rates for different traffics.

Sensing parameter	Data rate
Heart rate	1 sample/s or 600 bps
Blood pressure	1.2 kbps
Body temperature	1 sample/s to 16 kbps
Respiratory rate	240–800 bps
EEG	4.2–32 kbps
ECG	1.2–250 kbps

The main problem of the MICS/ISM band receiver described above is that its sensitivity, area and anti-interference ability are mutually restricted under low-power conditions. On this basis, a small-area, high-sensitivity and low-power MICS/ISM receiver is proposed in this study. Active inductors replace passive inductors in LNAs, and a compact Gm-C filter with PLL tuning is used to improve the anti-interference capability. The variable gain mixer and variable gain amplifier (VGA) are designed by AC current bleeding (ACCB), which reduces the overall area. Through link analysis, the receiver NF is reduced, the decision noise margin is increased, and GFSK demodulation is supported by the external baseband, effectively improving the sensitivity. In addition, the receiver integrates a ring-VCO PLL, bandgap, and other necessary modules to work independently.

The remainder of this paper is organized as follows. In the second section, the architecture of the proposed low-intermediate-frequency (low-IF) receiver and methods for improving its sensitivity and reducing its area from the receiver chain perspective are introduced. In the third section, the design principles and optimization details of each module are discussed. Finally, in the fourth and fifth sections, the receiver performance test results and conclusions of this study are presented.

II. THE PROPOSED LOW-IF RECEIVER

A. IMPLEMENTATION OF SMALL AREA

Passive inductors are commonly used in RF receivers and are primarily used for LC oscillators or LNA loads. It has the advantage of a low noise figure, but occupies a large area. Therefore, the inductor-less design technique, small-area module design technique, and module reuse are the main bases for reducing the chip areas.

The receiver structure is shown in Fig. 1. The first stage is an LNA loaded with an active inductor. A single-ended design is adopted to reduce power consumption, and the area is significantly reduced. After the quadrature Gilbert mixer, the signal is converted to a differential output. To enlarge the dynamic range of the receiver, both the mixer and VGA adopt ACCB to adjust their gain, avoiding the use of large-area switches and variable resistors. The IF filter uses a self-biased transconductance unit to form a compact Gm-C complex bandpass filter to enhance the anti-interference capability, and its center frequency and bandwidth are calibrated through PLL tuning technology, suppressing the impact of PVT variations.

The IF part integrates a charge-pump AGC loop, which has a simple structure that is beneficial for reducing the area. Additionally, the peak detector (PKD) in the AGC loop is reused to integrate a 2ASK demodulation with a dynamic threshold to directly output baseband signals to the MCU. It is used in ultralow-power, low-cost environments that only have easy logic processing capabilities, such as wireless remote controllers and wireless doorbells. It also supports the VGA signal output to an external GFSK digital demodulation baseband, which is used in high-speed data transmission environments such as ECGs and walkie-talkies.

The receiver also integrates the LO PLL based on ring-VCOs to reduce the LO area, crystal oscillator (XOSC) and bandgap, which has complete receiver functions.

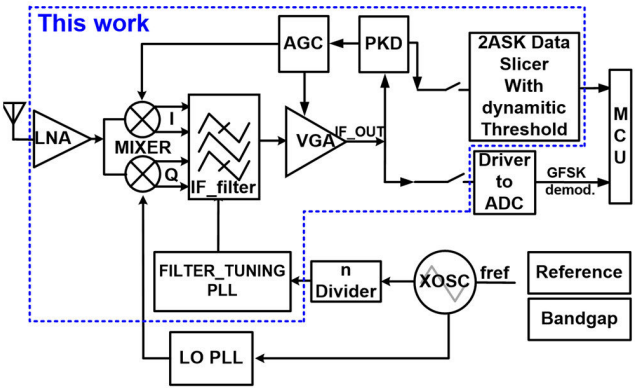

FIGURE 1. Block diagram of the proposed receiver.

B. THE PERFORMANCE ANALYSIS OF THE RECEIVER

The low-IF receiver has a lower frequency IF signal with only one down conversion, which is easy to integrate. This IF signal is slightly higher than the DC and is not easily affected by 1/f noise and DC offset, thus improving the NF. However, a low-IF receiver is vulnerable to image signal interference, as shown in Fig. 2. The complex filter can effectively suppress the image interference of the negative frequencies.

To improve the anti-blocking ability, a fourth-order real filter with a tunable center frequency is placed after complex filtering to attenuate the blocking signal outside the band and prevent interference from blocking the RF input signal by saturating the AGC loop.

The receiver sensitivity is given by (1). To improve the receiver sensitivity, the NF, signal-to-noise ratio (SNR) and bandwidth (BW) can be optimized. The NF is shown in (2);

therefore, increasing the LNA gain is an effective method to reduce the contribution of the subsequent noise figure of the stage. Here, the LNA adopts a two-stage gain, up to 40 dB. To avoid increasing the power consumption, the feedback stage of the active inductor is reused to optimize the receiver NF and the power consumption.

$$Sensitivity = 10\log(KT) + 10\log(BW) + NF + SNR \tag{1}$$

$$NF = NF_{LNA} + \frac{NF_{MIXER} - 1}{G_{LNA}} + \frac{NF_{IF\_filter} - 1}{G_{LNA}G_{MIXER}} + \frac{NF_{VGA} - 1}{G_{LNA}G_{MIXER}G_{IF\_filter}} \tag{2}$$

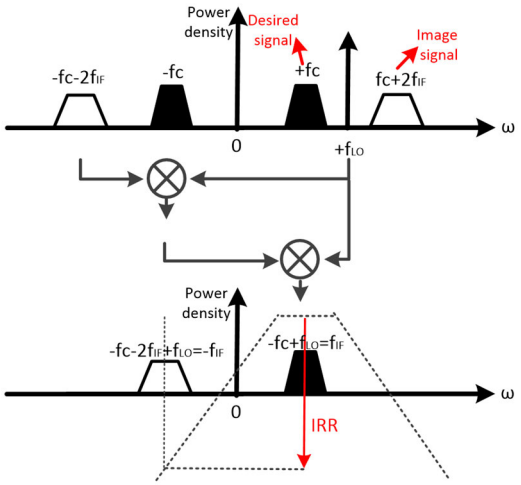

FIGURE 2. IRR principle of the proposed receiver.

However, a large LNA gain seriously deteriorates the IIP3 of the receiver, as shown in (3). Therefore, the current output mode MIXER is adopted to improve system linearity, and its gain can vary according to the amplitude of the input signal.

$$\frac{1}{IIP3_{Total}} = \frac{1}{IIP3_{LNA}} + \frac{G_{LNA}}{IIP3_{MIXER}} + \frac{G_{LNA}G_{MIXER}}{IIP3_{IF\_filter}} + \frac{G_{LNA}G_{MIXER}G_{IF\_filter}}{IIP3_{VGA}} \tag{3}$$

With the charge pump AGC loop control, under a large signal, the mixer reduces the gain and improves the system linearity. Under a small signal, it increases the gain and improves the sensitivity. The nonlinear problem of a strong signal receiver caused by large LNA gains is solved, and the dynamic input range of the system is expanded.

Second, the sensitivity can be optimized by reducing the SNR. In the 2ASK mode, the digital baseband signal modulated in amplitude is obtained mainly by determining the IF envelope from the PKD; therefore, the noise margin of the data slicer limits the required SNR. Fig. 3 shows that when the decision threshold is in the middle of the IF envelope, the decisions of 0 and 1 have the maximum noise margin. For example, when the threshold value is high, the decision noise margin of 0 is increased, but the decision noise margin of 1 is reduced so that the overall noise margin is reduced, resulting in a bit error at Point A; otherwise, it will cause a bit error at Point B.

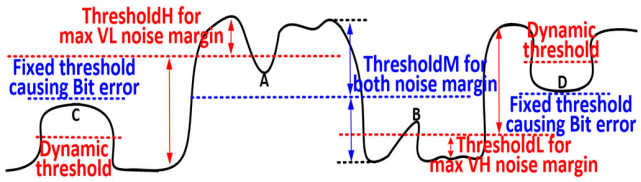

FIGURE 3. Noise margin of data slicer in different thresholds.

Consequently, the receiver integrates a 2ASK demodulator with a dynamic threshold to track the intermediate level of the envelope signal, improve the noise margin, reduce the SNR, and optimize the sensitivity. It also prevents the bit errors caused by the low amplitude of the IF (C and D in Fig. 3), which fail to reach a fixed decision threshold owing to insufficient VGA amplification when a weak signal is input. Combining these two points, the demodulator can improve the sensitivity of the receiver.

Third, it can be observed in [9] that the SNR requirement of 2ASK is higher than that of GFSK. Therefore, using an external digital baseband to achieve GFSK demodulation is also a way to improve the sensitivity. At the same time, the external digital baseband can be integrated with a digital bandpass filter to obtain a bandwidth smaller than the analog IF filter, reaching higher sensitivity in the low-speed communication mode. The bandwidth of the analog IF filter is about 600 kHz, which is compatible with multiple modulation methods. However, the minimum bandwidth of the external digital baseband filter is only 20 kHz.

III. BUILDING BLOCKS OF THE LOW-IF RECEIVER

A. LNA WITH AN ACTIVE INDUCTOR

Fig. 4 shows an inductive source-degenerated LNA loaded with an active inductor. M1 forms an inductive common source amplifier stage, which adopts a constant-gm offset and DC isolated input. L2 is a bonding wire inductor that provides a real part of the input impedance and facilitates input matching, L1 is also an inductor of the input bonding wire, and C1 is the DC isolation capacitor. M2 is a cascode transistor that enhances the output and input isolations, reduces the Miller effect of the Cgd of M1, and improves the stability and gain. Because the proposed LNA uses an active inductor load, an M3 current source is required as a high-resistance load to improve the quality factor of the active inductor. The OPA detects the M2 drain voltage and adjusts the M3 gate to form a common mode feedback loop (CMFB) to prevent common mode voltage drift and improve the linearity of the LNA.

Here, M4, M5, I1, I2, and C3 form a gyrator and convert Cgs4, Cgd4, Cgd5, and C3 into small signal grounding inductors. It is connected to the LNA Zout point to greatly reduce

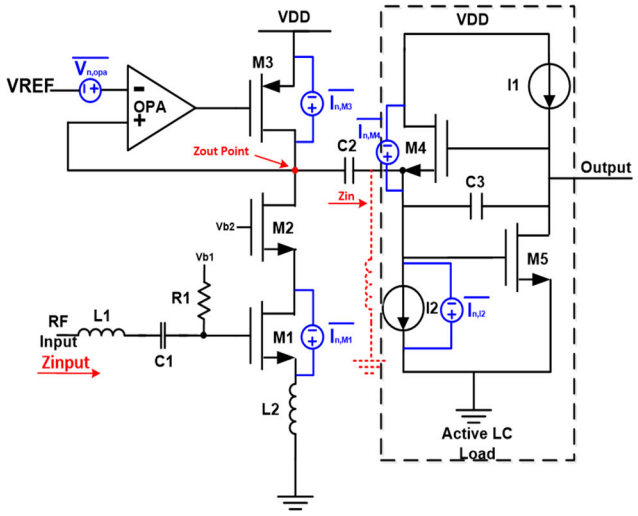

FIGURE 4. Schematic of the LNA with an active inductive load.

the area occupied by the passive inductor. It reuses the gain of the M5 in the active inductor to increase the gain of the LNA to reduce the NF contribution of the subsequent stage. The impedance seen from Zin is (4),

$$\begin{aligned} Zin &= \frac{gds5 + s(Cgs4 + Cgd5 + Cgd4 + C3)}{(gds5 + gm5 + sCgd4)(gm4 + s(Cgs4 + Cgd5))} \\ &\approx \frac{gds5 + s(Cgs4 + C3)}{(gm5 + sCgd4)(gm4 + sCgs4)}, \\ \omega p1 &= \frac{gm5}{Cgd4}, \quad \omega p2 = \frac{gm4}{Cgs4} \end{aligned} \tag{4}$$

The impedance has two poles: $\omega_{p1} > f_{t5}$, $\omega_{p2} = f_{t4}$; therefore, the inductance and resistance are connected in series at low frequencies. Parasitic conductance gds5 can adjust the inductance quality factor and control the load bandwidth. This inductor forms an LC load resonance with the parasitic capacitor at the drain point Zout. The post-simulation results of the LNA are shown in Fig. 5. Compared with a 5.8 nH passive inductor (area 286 μm×287 μm), the proposed active inductor is up to 42 nH, which is only an area of 15 μm×72 μm, and the area of the LNA is reduced to 147 μm×66.58 μm, which is smaller than the area of the LNA reported in [4] and [9].

However, the OPA, M3 and the active inductor introduce additional noise and deteriorate the noise figure of the LNA. Fortunately, the LNA operates at a narrowband frequency, which is much higher than the noise corner frequency of this process; therefore, flicker noise can be ignored. The main noise sources are the channel thermal noise and the gate-induced noise of M1 [10].

The total noise is divided into three parts. Reference [10] provides the noise current of the common source transistor M1 $\overline{indg}$:

$$\overline{indg^2} = kT\gamma gm1(1 - 2|c|\sqrt{\frac{\delta}{5\gamma}} + (4Q^2 + 1)\frac{\delta}{5\gamma}) \tag{5}$$

where k is the Boltzmann constant, T is the thermodynamic temperature, γ is a bias-dependent factor, δ is the coefficient of gate noise, Q is the quality factor of the amplifier input circuit, c is the correlation coefficient with drain noise and gmi is the transconductance of Mi (i = 1-5).

The CMFB loop introduces noise current $\overline{indc}$:

$$\overline{indc^2} = \overline{V_{n,opa}^2}\left(\frac{gm3}{gm3 \cdot Zout_{LNA} \cdot A_0 - 1}\right)^2 + 4kT\gamma gm3 \tag{6}$$

where $\overline{V_{n,OPA}}$ is the noise of the OPA, A_0 is the magnification of the OPA, and $ZOUT_{LNA}$ is the impedance from Zout in Fig.4.

The active inductor introduces noise current $\overline{inda}$:

$$\overline{inda} = 4kT\gamma gm4 + 4kT\gamma gm_{I2} \tag{7}$$

where $\overline{gm_{I2}}$ represents the transconductance of I2.

The second stage has a large gain, ignoring the output noise generated by M5 and I1. In fact, from the simulation results, their noise contribution is less than 5%, so the main voltage output noise power is given by (8):

$$\begin{aligned} &\overline{V_{n,total}^2} \\ &= (\overline{indg^2} + \overline{indc^2} + \overline{inda^2})(Zout_{LNA} \cdot gm5 \cdot rds5)^2 \\ &\approx [kT\gamma gm1(4Q^2 + 1)\frac{\delta}{5\gamma} + \overline{V_{n,opa}^2}gm3^2 \\ &\quad + 4kT\gamma(gm3 + gm4 + gm_{I2})] \cdot (Zout_{LNA} \cdot gm5 \cdot rds5)^2, \\ &\quad when\ \mathrm{Q} \gg 1,\ \omega < \omega p1, \omega p2\ and\ \mathrm{A}_0 > 1 \end{aligned} \tag{8}$$

When the input port matches the antenna impedance RS, the noise generated by the input source at the output is (9):

$$\begin{aligned} \overline{V_{n,RSO}}^2 &= (gm1Q)^2\overline{V_{n,RS}}^2 \cdot (Zout_{LNA} \cdot gm5 \cdot rds5)^2 \\ &= (gm1Q)^2 4kT\gamma RS \cdot (Zout_{LNA} \cdot gm5 \cdot rds5)^2 \end{aligned} \tag{9}$$

$$\begin{aligned} NF_{LNA} &= 1 + \frac{\overline{V_{n,total}^2}}{\overline{V_{n,RSO}^2}} \\ &= 1 + \frac{kT\gamma gm1(4Q^2 + 1)\frac{\delta}{5\gamma} + \overline{V_{n,opa}^2}gm3^2 + 4kT\gamma(gm3 + gm4 + gm_{I2})}{(gm1Q)^2 4kT\gamma RS} \\ &= 1 + (\frac{\omega_0}{\omega T_1})\gamma\frac{1}{2Q}(4Q^2 + 1)\frac{\delta}{5\gamma} + \frac{\overline{V_{n,opa}^2}gm3^2}{(gm1Q)^2 4kT\gamma RS} + \frac{(gm3 + gm4 + gm_{I2})}{(gm1Q)^2 RS} \end{aligned} \tag{10}$$

Therefore, the LNA noise figure is as in (10), shown at the bottom of the previous page.

From (10), increasing gm1 and ω_{T1} can reduce the deterioration of the noise figure introduced by the CMMB and active inductor, optimizing the receiver NF. Here, M1 adopts a large current of 0.82 mA, gm1 is 10.8 mS, and f_{T1} is 6.03 GHz. When Vgs3-Vth3 is doubled, gm3 is reduced to half of the original value, and the noise of the common-mode feedback loop is reduced by 3/4. Thus, a value of 550 mV provides a good balance between linearity and noise. When the M1 noise is dominant, Q =2.5 can reduce the M1 noise contribution and increase the gain to reduce the NF deterioration introduced by the mixer.

The LNA simulation results are shown in Fig. 5. The noise is 2.874 dB@315 MHz and 2.892 dB@433.92 MHz, and the gain is greater than 40 dB. Compared with the typical two-stage source degenerate passive inductive LNA [10], the NF deterioration is controlled within 0.8 dB.

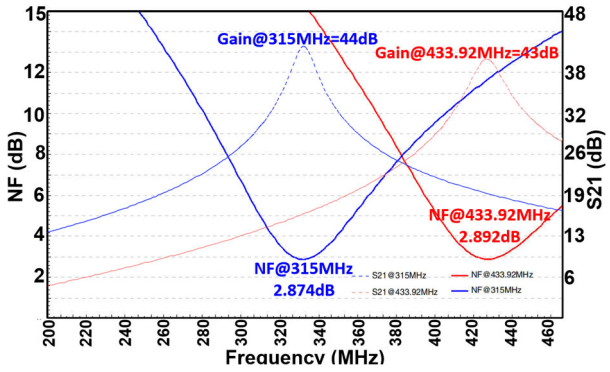

FIGURE 5. S21 and NF simulation results of proposed LNA.

B. VARIABLE GAIN GILBERT MIXER

The schematic in Fig. 6 shows a current-output Gilbert mixer. Compared to the voltage mode circuit, the current mode mixer has better linearity owing to its small internal node impedance, which reduces distortion [11]. Therefore, the diode load formed by M7 and M8 is used in the output stage of the Gilbert mixer, with the M9 and M10 current mirrors drawing out the IF current signal to avoid distortion. To increase the dynamic input range of the system, the ACCB is used to control the gain of the mixer to prevent the nonlinearity of the large-gain LNA. The ACCB is composed of M12-M17. The M13/M15 drain current and the M14/M16 drain current use cross connections to cancel each other's AC signal current or, in other words, AC current bleeding occurs. Therefore, the M13-M16 gate is controlled by the AGC output voltage VAGC, but the M12 and M17 gates adopt a fixed bias voltage Vbias3, which controls the proportion of AC current finally output to the load. As shown in Eqs. (11)-(15),

$$\begin{aligned} IOUTN &= Vgs14gm14 + Vgs16gm16 + Vgs17gm17 \\ &= gm_{14,16}(Vgs14 + Vgs16) + Vgs17gm17 \\ &= Inn \cdot Rin \cdot gm17, whenRout \gg Rin \end{aligned} \tag{11}$$

where Vgsi represents the voltage difference between the gate and source of Mi in Fig 6.

$$\begin{aligned} Rin &= \frac{1}{gm15 + gm16 + gm17} \\ &= \frac{1}{2\beta(V_{AGC} - VA - Vth) + \beta(Vbias3 - VA - Vth)} \end{aligned} \tag{12}$$

Assume that the M11 bias current is 2IC:

$$\frac{\beta}{2}(Vbias3 - VA - Vth)^2 + 2\frac{\beta}{2}(V_{AGC} - VA - Vth)^2 = IC \tag{13}$$

From Eqs. (12)-(14):

$$\frac{IOUTN}{Inn} = \frac{1}{3} + \frac{4}{3}\left(\frac{V_{AGC} - Vbias3}{\sqrt{4V_{AGC}^2 + 12\frac{IC}{2\beta}}}\right), \quad when\ V_{AGC} \approx Vbias3 \tag{14}$$

$$\frac{\partial \frac{IOUTN}{Inn}}{\partial V_{AGC}} \approx \frac{1}{\sqrt{4V_{AGC}^2 + 12\frac{IC}{2\beta}}} > 0, \quad when\ V_{AGC} \approx Vbias3 \tag{15}$$

Therefore, if the VAGC voltage is greater than Vbias3, most IF AC currents flow to the load through M12 and M17; in contrast, most of the AC current will be canceled by M13-M16, reducing the frequency conversion gain of the mixer.

The ACCB does not change the common-mode currents flowing through M9, M10, M18 and M19; therefore, the common-mode voltage of each node is relatively stable, reducing device distortion. In addition, the ACCB is realized in the current mode, which reduces the V-I conversion, improving the linearity of the mixer.

The output impedance exhibits low pass characteristics, as shown in (16). IOUTN and IOUTP are filtered and converted into voltages, which suppress the harmonics after mixing and further suppress the interference out of the band.

$$Zout_{mixer} = \frac{R1}{1 + R1(C3 + 2C2)s} \tag{16}$$

The simulation results show that the 3dB bandwidth is 3.5 MHz. When the conversion gain range is −7-21 dB, the corresponding IIP3 of the mixer reaches 0.7 dBm to 0.37 dBm, and the corresponding NF range is 37.8 dB to 28.5 dB. Here, M18 and M19 mainly generate an input bias voltage for the IF filter and use C3-C6 to stabilize the output common mode, increasing the common mode rejection ratio and power supply rejection ratio.

The simulation results show that the 3dB bandwidth is 3.5 MHz. When the conversion gain range is −7 to 21 dB, the corresponding IIP3 of the mixer reaches 0.7 dBm to 0.37 dBm, and the corresponding NF range is 37.8 dB to 28.5 dB. Here, M18 and M19 mainly generate an input bias voltage for the IF filter and use C3-C6 to stabilize the output common mode, increasing the common mode rejection ratio and power supply rejection ratio.

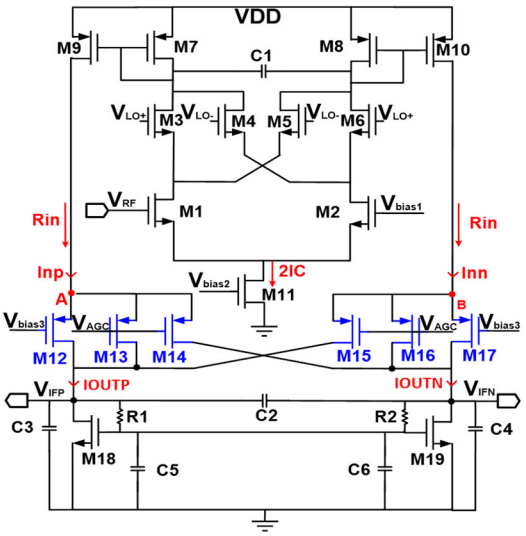

FIGURE 6. Schematic of the mixer and the ACCB techniques.

C. GM-C COMPLEX FILTER WITH PLL TUNING

To avoid the interference of primary ISM applications on MICS band receivers, it is necessary to improve the image rejection and anti-interference ability of the receiver. Compared to the active-RC or poly-phase filters, at a low frequency band, the Gm-C filter has a smaller area and flexibility of the center frequency because of the lack of a large resistor or capacitor. In this study, a 3-order complex filter is used, and a 4-order real filter is cascaded in the I-path channel to enhance the adjacent channel rejection (ACR).

As shown in Fig. 7(a), the complex filter part is a 3-order low-pass filter consisting of a first-order RC low-pass filter cascaded with a Biquad low-pass filter; and the cross-couple transconductance is used to move the center of this low-pass filter to the positive IF frequency, suppressing the mirror signal at the negative frequency.

Its transfer function is (17):

$$\mathrm{H_C(s)} = \frac{gm1}{gm + (s - j\frac{gm_{IF}}{C1})C1} \cdot \frac{gm^2}{(s - \frac{gm_{IF}}{C1})^2 C1^2 + (s - j\frac{gm_{IF}}{C1})C1gm + gm^2} \tag{17}$$

$\omega_{IFC} = \frac{gm_{IF}}{C1}$ is the center frequency of the complex filter.

The 4-order real filter part is formed by cascading two 2-order Biquad bandpass filters. The first stage places center 1 slightly lower than the IF, and the second stage places center 2 slightly higher than the IF. Therefore, the two are cascaded to form a bandpass filter centered on the IF, which enhances the flatness in the band and makes it easy to adjust the bandwidth.

The real filter transfer function is (18),

$$H_R(s) = \frac{sC_3gm3}{(s^2C_2C_3 + sC_3gm + gm_{IF}^2)} \cdot \frac{sC_5gm}{(s^2C_4C_5 + sC_5gm + gm_{IF}^2)} \tag{18}$$

$\omega_{IF1} = \frac{gm_{IF}}{\sqrt{C2C3}}$ is the center frequency of the first bandpass filter. $\omega_{IF2} = \frac{gm_{IF}}{\sqrt{C4C5}}$ is the center frequency of the second bandpass filter.

Therefore, the center frequency of the 4-order real bandpass filter ω_{IFR} is (19),

$$\omega_{IFR} = \frac{\omega_{IF1} + \omega_{IF2}}{2} = \frac{gm_{IF}}{2}(\frac{1}{\sqrt{C4C5}} + \frac{1}{\sqrt{C2C3}}) \tag{19}$$

To reduce the area, a compact transconductance with a self-biased output is adopted, as shown in Fig. 7(b). M1 and M2 form a fully differential pair; the Vgs of M3 and M4 clamping the Vds of M5 and M6 make them work in the linear area; thus, M5 and M6 sense the output common-mode voltage to form a CMFB loop to maintain the stability of the output common-mode voltage. The tuning PLL adjusts the $\mathrm{gm_{IF}}$ by adjusting the current of M7 to control the center frequency. This unit takes up only seven transistor areas and is suitable for large-scale integration.

However, the PVT makes $\mathrm{gm_{IF}}$ and the capacitor change easily, causing the IF filter center frequency to drift. Therefore, the PLL tuning technology was used to calibrate ω_{IFC}, ω_{IFR} to n divisions of the crystal oscillation frequency f_{ref} to counteract the PVT impact and adjust the filter center to work at different IF frequencies, as shown in Fig. (2).

As shown in Fig. 8, the traditional VCO of the tuning PLL uses an active inductor and capacitor resonance to produce an LC oscillator without the blue unit $\frac{1}{2}gm_{IF}$ [12]. Therefore, points A and B are high-impedance nodes and Gm1 and Gm2 are seriously distorted, resulting in $\mathrm{gm_{IF}}$ inconsistency between the VCO and the filter, causing the filter center to shift. On this basis, the amplitudes of A and B are controlled in this work to optimize the nonlinearity of Gm1 and Gm2 by adding a $\frac{1}{2}gm_{IF}$ load behind Gm1, limiting the magnification. The characteristic equation of this VCO is shown in (20),

$$gm_{IF}^2 + (\frac{gm_{IF}}{2} + sC_1 - GmL)(\frac{gm_{IF}}{2} + sC_1) = 0 \tag{20}$$

where GmL is the transconductance of Gm_Limit.

According to the (20), the characteristic root is:

$$s_{1,2} = \frac{3GmL - 3gm_{IF} \pm j\sqrt{36gm_{IF}^2 - 9GmL^2}}{6C_1} \tag{21}$$

Therefore, $\omega_0 = \frac{\sqrt{36gm_{IF}^2 - 9GmL^2}}{6C_1}$ is the VCO frequency.

When VCO starts to vibrate, $\mathrm{S_{1,2}}$ is located in the right half plane, that is, $3GmL - 3gm_{IF} > 0$, but owing to the nonlinear effect of Gm_Limit, the vibration is eventually stable, so $3GmL - 3gm_{IF} = 0$. When the VCO is locked by the tuning PLL, ω_{IFC} is accurately located on the n division of the reference frequency f_{ref}. (22) presents the relationship:

$$\omega_0 = \frac{\sqrt{27gm_{IF}^2}}{6C_1} = \frac{3\sqrt{3}}{6}\frac{gm_{IF}}{C_1} = \frac{\sqrt{3}}{2}\omega_{IFC} = \frac{f_{ref}}{n} \tag{22}$$

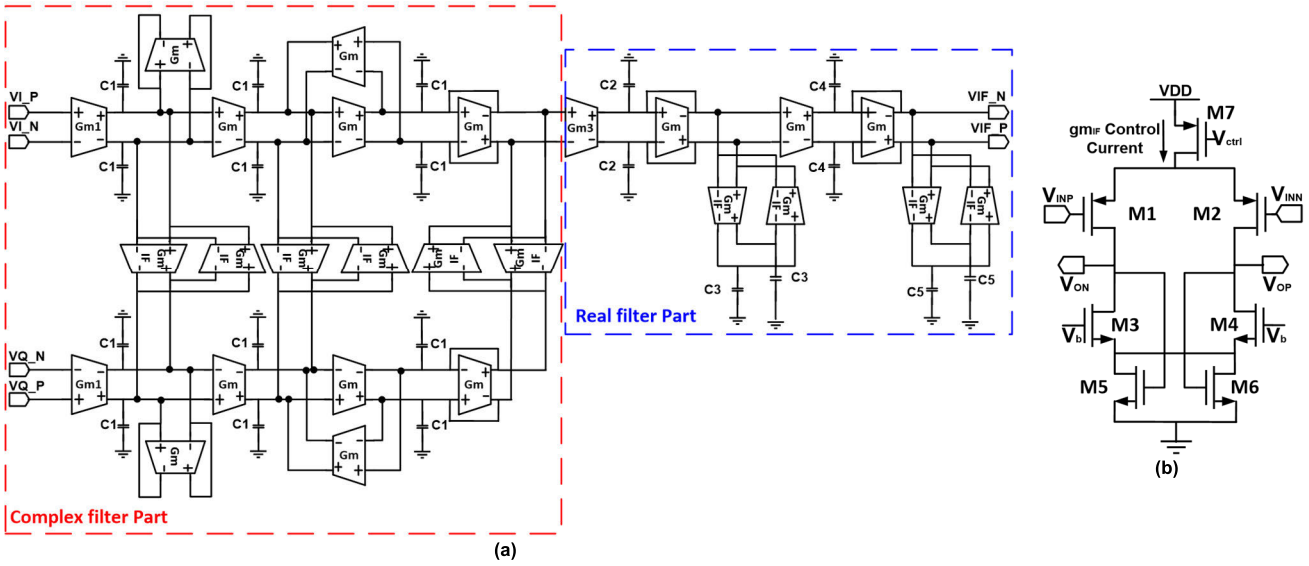

FIGURE 7. Top structure of the Gm-C filter (a) and the transconductance unit (b).

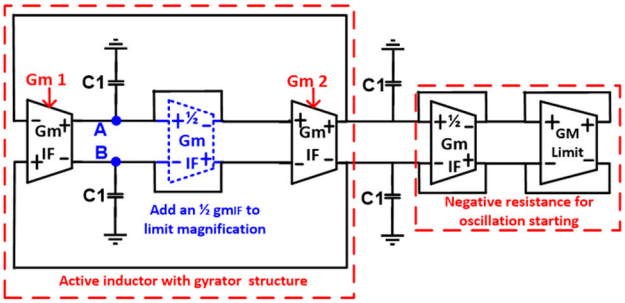

FIGURE 8. Conventional VCO and the proposed VCO.

Because ω_{IF1} is slightly smaller than ω_{IFC}, ω_{IF2} is slightly greater than ω_{IFC} and $\frac{1}{C1} \approx (\frac{1}{\sqrt{C4C5}} + \frac{1}{\sqrt{C2C3}})$, so $\omega_{IFR} \approx \omega_{IFC}$. Thus, ω_{IFR} is also locked to the n division of f_{ref}.

Through simulation, when the two VCOs work in 1 MHz sinusoidal signals, the total harmonic distortion (THD) of the proposed VCO is only 10.3%, while the VCO in [12] is 16%. When the RF input is 433.92 MHz, the IF is 1.239 MHz after tuning, and the bandwidth is 570 kHz. When the RF input is 315 MHz, the IF is 0.899 MHz after tuning, and the bandwidth is 420 kHz, with deviations in every corner smaller than 3.9%.

D. THE CHARGE PUMP AGC LOOP

The AGC can increase the receiver gain under a small signal to improve the sensitivity and decrease the receiver gain to improve the linearity under a large signal. Thus, it optimizes the dynamic range, compatible with more modulation types.

As shown in Fig. 9, the AGC loop uses a charge pump (CP) structure. The PKD samples the IF amplitude and compares it with a fixed voltage Vref. When its amplitude is higher than Vref, the CP discharges C, reducing VAGC and the gain of the mixer and VGA. In contrast, it charges C and increases the gain of both. Here, capacitor C integrates the CP current, filters out the interference of the baseband and carrier signal, extracts the DC amplitude information, controls the gain of the mixer and VGA, and maintains a stable output amplitude of the VGA. It is convenient for subsequent ADC or 2ASK demodulators to sample.

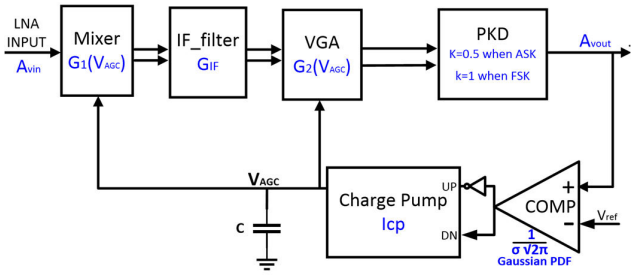

FIGURE 9. Charge pump AGC loop.

In Fig. 9, the blue font represents the AC model parameter, G1 is the response of the mixer gain to VAGC, G2 is the response of the VGA gain to VAGC, and Avin and Avout are the input and output amplitudes, respectively. K represents the response of the PKD to different signals. The comparator uses bang-bang detection in the AGC loop. Therefore, [13] considers that the amplitude fluctuation is mainly Gaussian noise and gives its gain: $\frac{1}{\sigma\sqrt{2\pi}}$. Then, its transfer function is

$$\frac{Avout}{Avin} = \frac{G_{IF}G_1(V_{AGC})G_2(V_{AGC})I_{cp}\frac{k}{\delta\sqrt{2\pi}}}{sC + G_{IF}G_1(V_{AGC})G_2(V_{AGC})I_{cp}\frac{k}{\delta\sqrt{2\pi}}} \quad (23)$$

Fig. 10 (a) is the VGA top-level circuit, and (b) is the single-stage VGA circuit. The VGA uses a five-stage variable gain amplifier to achieve a change of -25 dB-53 dB. AC

coupling is used between stages to suppress flicker noise and DC offset to simplify the circuit design and reduce the area. Each level of the VGA also uses the ACCB to control the gain, preventing large-area switches and variable resistors for a minimal area. From (14), the gain of the mixer and VGA is controlled by the VAGC, as shown in Eqs. (24)-(26),

$$G_1(V_{AGC}) = \alpha_1 \frac{\partial \frac{IOUTN}{Inn}}{\partial V_{AGC}} \approx \frac{\alpha_1}{\sqrt{4V_{AGC}^2 + 12\frac{IC}{2\beta}}} > 0, \quad when\ V_{AGC} \approx Vref \tag{24}$$

where $\alpha 1$ represents the input Gilbert stage transconductance conversion gain and the output impedance, which is a constant.

$$G_2(V_{AGC}) = \approx \frac{\alpha_2}{\sqrt{4V_{AGC}^2 + 12\frac{IC}{2\beta}}} > 0, \quad when\ V_{AGC} \approx Vref \tag{25}$$

where $\alpha 2$ represents the first stage gain and the output cascode amplifier gain, which is a constant.

When the loop is stable, the VAGC changes little, regarding it as a constant. Therefore, this is a single-pole system with strong stability, and its bandwidth and setup time can be adjusted using the CP current and C to adapt to different conditions. The time constant is given by (26),

$$\tau = \frac{C}{G_{IF} G_1(V_{AGC}) G_2(V_{AGC}) I_{cp} \frac{k}{\delta\sqrt{2\pi}}} \tag{26}$$

The simulation results show that under the control of the AGC loop, the gain range of the receiver can be from 33 to 122 dB. When the input signal changes from -115dBm to 0dBm, it takes 8ms to establish a stable VAGC.

E. DYNAMIC THRESHOLD 2ASK DATA SLICER

In some low-power medical implantation scenarios, the 2ASK modulation is mostly used. Thus, a dynamic threshold data slicer (DTDS) is integrated in this work, which can directly demodulate and output the digital baseband signal contained in the PKD output, as shown in Fig. 11 (a).

It mainly includes an analog dynamic threshold extractor, as shown in Fig. 11(b), which can follow the intermediate level of the envelope signal and improve the noise margin and decision accuracy for weak amplitude signals, thus reducing the bit error rate and improving the receiver sensitivity.

As shown in Fig. 11(b), A1 and M1 constitute the minimum-voltage detector. When VIN is lower than VA, M1 is opened to discharge C3 until VA is equal to the lowest voltage of VIN. Similarly, A2 and M2 constitute the highest voltage detector, and the highest voltage of VIN is extracted at Point B. Next, the VA and VB voltages are divided by R1 and R2 (R1= R2) after being driven by two buffers. Therefore, VOUT is in the middle of the highest and lowest VIN voltages.

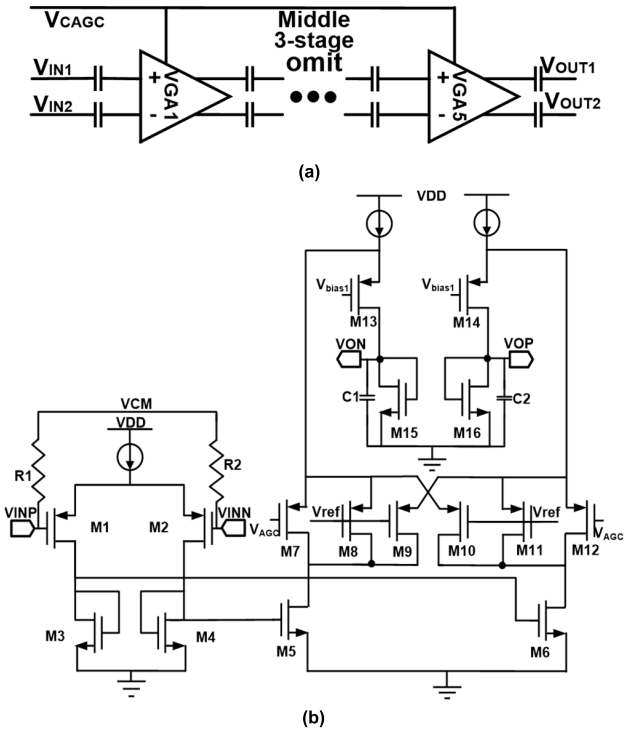

FIGURE 10. VGA top schematic (a) and a single-stage amplifier (b).

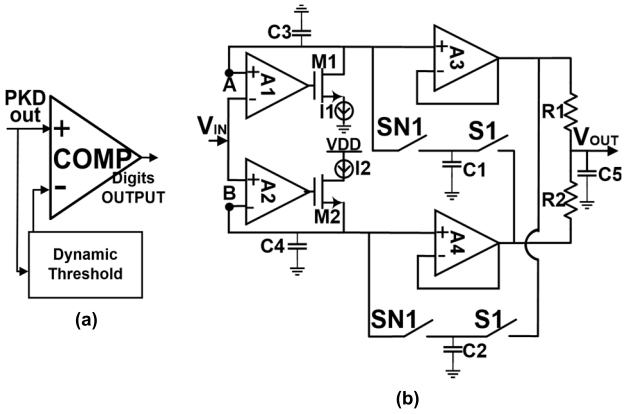

FIGURE 11. Data slicer (a) and dynamic threshold extractor (b).

The work process is shown in Fig. 12(a), where one end of two sets of S1 and SN1 are connected at the peak and valley storage points, and the other is connected at C1 or C2. When the switch is turned on alternately, C1 and C2 are charged and discharged to periodically 0, refresh the stored peak and valley voltage at Points A and B, and find the new peak and valley again. S1 and SN1 are connected in such a way that the peak and valley act as limitations of each other, avoiding VA > VB and demodulation errors.

Zooming in on Fig. 12(a) gray windows, Fig. 12(b) shows that during refreshing the valley, the peak is driven by the high level of VIN and remains; during refreshing the peak, the valley is driven by the low level of VIN and remains.

Therefore, those switched capacitors continuously refresh the wave peaks and valleys alternately with the ΔV amplitude determined by C1 and C2. However, the refreshing amplitude ΔV needs to be designed according to the speed of the PKD to maintain the change in the PKD output amplitude to prevent bit errors. Thus, it is not suitable for a high-speed rate because of an excessively large ΔV worsening the noise margin. The simulation results show that, compared with the fixed threshold, the dynamic threshold data slicer can effectively improve the 2ASK demodulation sensitivity by 3 dB.

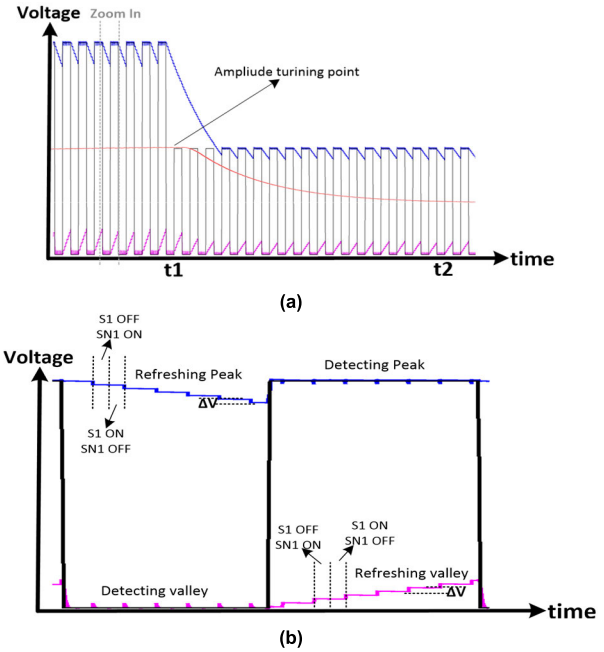

FIGURE 12. Work process of the dynamic threshold extractor (a) and the valley and peak refreshing phase (b).

IV. MEASUREMENT RESULTS

The proposed receiver was fabricated using CSMC 0.18μm CMOS technology. The chip micrograph and layout are shown in Fig. 13. The receiver occupies an active area of 0.7 mm $\times$ 0.62 mm, including ESD I/Os. For the minimum area, all MIM capacitors are placed on top of the circuit, which are the square objects in Fig. 13(a). The circuit layout is also shown in Fig. 13(b).

The measurement setup is shown in Fig. 14. When the receiver operates in the 2ASK mode at 433.92 MHz, the 1.8-V supply consumes a 2.91mA current; 3.61mA current is consumed in the GFSK mode (0.7 mA for the external DDB). When working in the 2ASK mode at 315 MHz, the 1.8-V supply consumes a 2.68mA current, and a 3.38mA current is consumed in the GFSK mode. In the 433.92 MHz GFSK mode (300Kbps), the receiver only consumes 6.5 mW, equivalent to 21.7 nJ/bit.

As shown in Fig 15, S11 at 315MHz and 433.92MHz are less than -10dB.

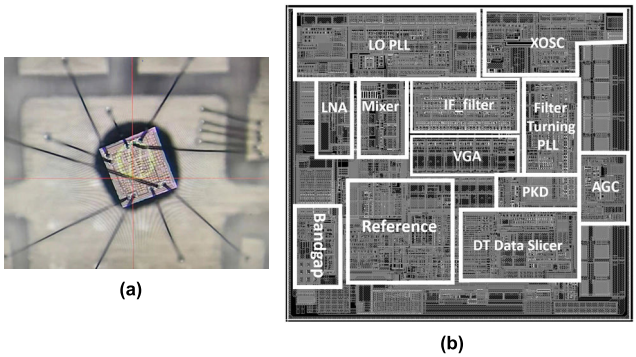

FIGURE 13. Chip micrograph (a) and layout (b).

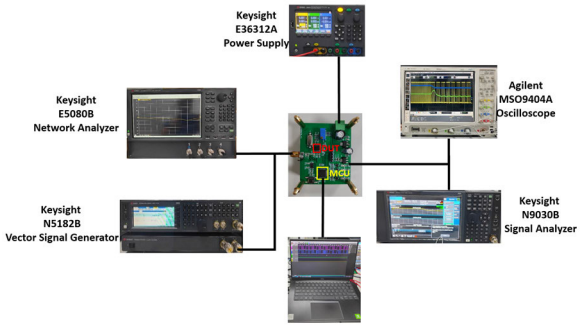

FIGURE 14. Measurement setup of the proposed receiver.

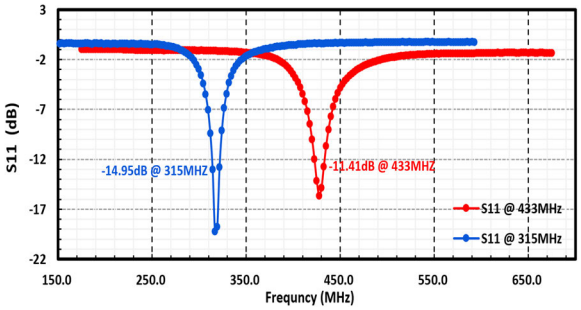

FIGURE 15. Measurement of S11 at 433.92/315 MHz.

The sensitivities in the 2ASK mode at different bit rates are shown in Fig. 16(a). The blue line indicates a fixed threshold data slicer and the red line indicates the DTDS. In the low-rate mode (less than 10 Kbps), the sensitivity difference between them is only 2-3 dBm; in the high-speed mode, the fixed mode can barely demodulate the signal correctly. The main reason for this is that as the bit rate is increased, the baseband signal amplitude is also reduced, and thus, the fixed mode cannot work. For the DTDS, its threshold can always be in the middle of the wave peak and valley with the highest noise margin. Therefore, there is a sensitivity optimization of 2-3 dBm in the low-speed mode, and it can operate at a higher speed rate. Meanwhile, due to the external digital baseband (DBB), the GFSK sensitivity is better than -121 dBm at 2 Kbps and can work at a higher data rate, up to 300 Kbps, as shown in

Fig. 16(b). This is mainly owing to the variable bandwidth of the digital baseband filter.

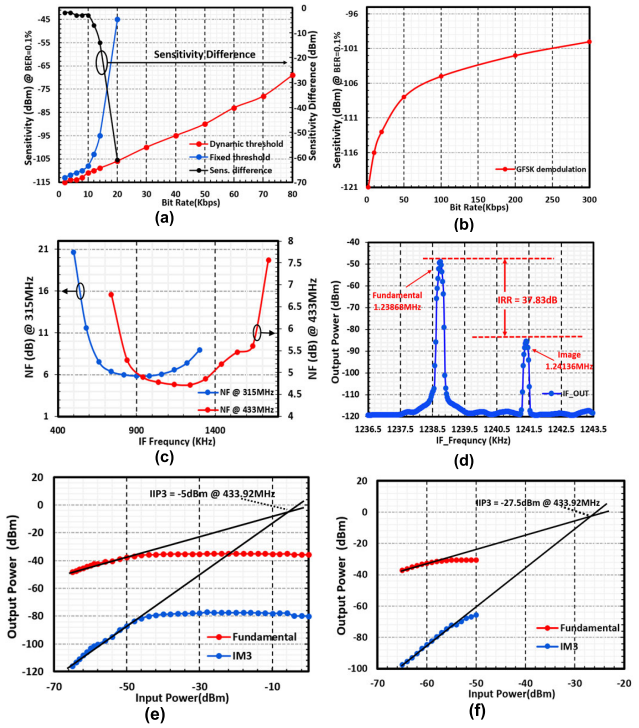

FIGURE 16. RF performance measurement: (a) 2ASK mode sensitivity, (b) GFSK mode sensitivity, (c) NF, (d) IRR, (e) In-band IIP3 at low gain, and (f) In-band IIP3 at high gain.

Fig. 16(c) shows the SSB NF measured at the IF filter output with maximum gain. The NF of 315 M is 5.84 dB, and the NF of 433.92 M is 4.72 dB. Here, the latter is 1.12 dB higher than the former, mainly because the resonant point of the active inductor is shifted to a higher frequency (460 MHz) than the simulation result of 400 MHz. From (4), adjusting gm4 and gm5 can calibrate the resonant frequency to obtain a better NF at the frequency of interest.

Inject 433.92 MHz and 431.44 M dual tone signals from the input. The IF frequency of the desired RF signal is 1.23936 MHz, while the IF frequency of the image signal is 1.24064 MHz. As shown in Fig. 16(d), the IRR is 37.83 dB. The IF center frequency measured at 433.92 MHz is 1.239 MHz, and the bandwidth is 600 kHz. At 315 MHz, the IF center frequency is 0.894 MHz, and the bandwidth is 425 kHz, consistent with the simulation results in Section III-C.

Fig. 16(e) and (f) show the measured in-band IIP3 of the receiver. When the receiver gain is minimum, IIP3 is −5 dBm; and when the gain is maximum, IIP3 is -27.5 dBm.

Fig. 17(a) shows the RF input and demodulation output of the 2ASK mode when the input power is -100 dBm at 20 Kbps. Fig. 17(b) shows the VGA output and baseband signal from the UART of the MCU in the GFSK mode when the input power is -100 dBm at 20 Kbps.

Fig. 18 shows the AGC response when the RF signal increased from −115 dBm to 0 dBm. At t =3 ms, the RF signal was switched to 0 dBm, and the PKD output amplitude instantaneously increased to a large amplitude. As the loop operated, the amplitude started to decrease. Until t =13 ms, the PKD amplitude returned to that before the jump. The stability time of the AGC is approximately 10 ms, which can be adjusted by C or Icp in Fig. 9.

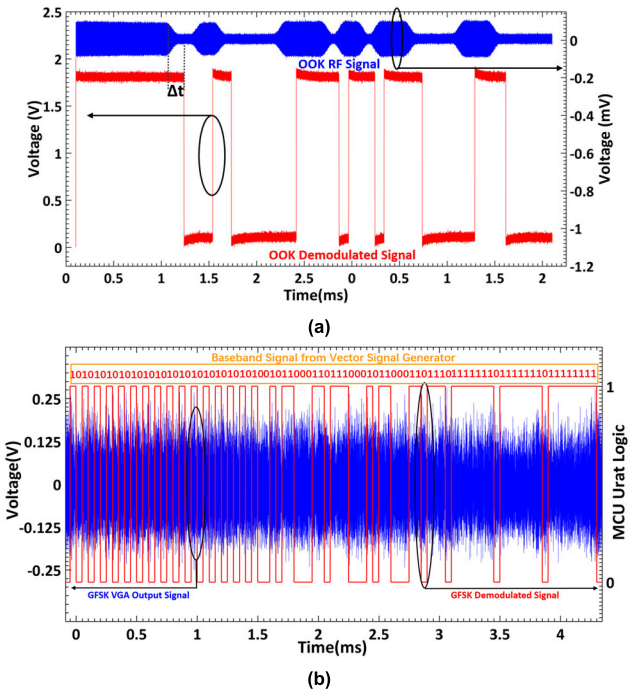

FIGURE 17. ASK mode wave (a) and GFSK mode wave (b).

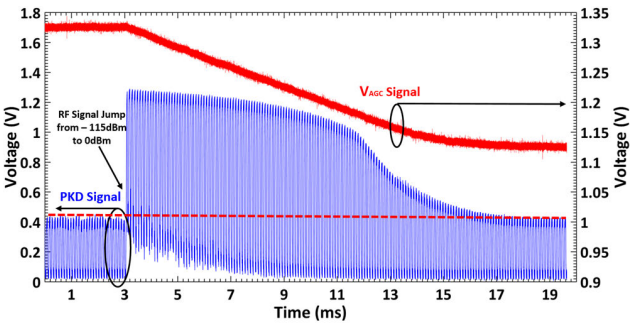

FIGURE 18. AGC loop adjustment process when the RF input amplitude jumps from −115 dBm to 0 dBm.

Table 2 summarizes the performance of this work and the comparison with the state-of-the-art MICS/ISM band receivers. Excluding the area of the digital baseband and ADC, the receiver area is smaller than that reported in [9], [14], [15], and [16], which has a lower cost. In addition, this receiver has better sensitivity at low speeds than [14] in the 2ASK mode, which reaches −115 dBm at 2 Kbps/-90 dBm

TABLE 2. Comparison with previously reported works.

	This work	JBHI 15[9]	TCAS-I 16[14]	ISSCC 16[15]	JSSC 21[16]
Technology (nm)	180	40	180	180	55
Area (mm^2)*	0.42	1.53	3.3	2.36	2.72
Modulation type	2ASK/GFSK	GMSK/DBPSK	OOK/BFSK	GFSK	SC-BFSK
Frequency band (MHz)	300-500	402-405/420-450	402-405	160-960	900
Sensitivity (dBm) 0.1% BER	-115 (2ASK@2Kbps) -121 (GFSK@2Kbps) -100(GFSK@300Kbps)	-110 (GMSK@187.5Kbps) -112 (DBPSK@11Kbps)	-55 (OOK@50Kbps) -53.5(BFSK@120Kbps)	-123 (GFSK@169MHz) -122 (GFSK@915MHz) (All on 2.4Kbps data rate)	-123(BFSK@0.39Kkbps) -106(BFSK@50Kkbps)
Data Rate (Kbps)	0.5-300	11-4500	50-120	0.1-400	0.39-50
NF (dB)	4.72	5	—	5-6	6
IRR (dB)	37.8	—	—	55	22
In-band IIP3 (dBm)	-5dBm at low gain -27.5dBm at high gain	—	-15.9dBm at low gain	-8.5dBm at high gain	—
Supply (V)	1.8	1	0.45	2.2	0.9-1
Power (mW)+	5.24(2ASK)/6.5(GFSK)	2.2	0.352	57.2	19.88

*Excluding ADC and DBB areas.
+Including DBB, excluding XOSC, Bandgap and Bias circuits.

at 50 Kbps. Under the GFSK mode at a 2 Kbps rate, the sensitivity reaches −121 dBm, which is close to [15] and [16] and superior to [9] and [14].

V. CONCLUSION

An ultrasmall low-IF receiver with high sensitivity was designed for MICS/ISM applications. After RF link optimization, the receiver also integrated a low-power 2ASK demodulator and used DTDS to improve the sensitivity. Meanwhile, the GFSK demodulation was achieved by an external baseband, improving low-speed sensitivity and supporting high-speed applications. It used a source degenerated LNA with an active inductor load. To improve linearity, a variable gain Gilbert mixer and VGA were designed with the ACCB, which was controlled by a charge pump AGC loop. A Gm-C filter with a compact area was used to avoid image and out-of-band interference, with the PLL tuning technique calibrating the center frequency. An LO based on ring-VCOs was also adopted for the lower area. The receiver adopts an inductor-less and small-area circuit design method to achieve low cost and high sensitivity.

The receiver is fabricated on a CSMC 0.18 μm process with an area of only 0.42 mm^2, which is smaller than that in recent years. The results show that the receiver can cover the 300 -500 MHz band, fully covering the MICS bands and supporting some of the ISM bands. In the 2ASK mode, the sensitivity reaches -115 dBm at 2 kbps. In the GFSK mode, the sensitivity reached -121 dBm at 2 Kbps. With the 300 Kbps high-speed mode, the maximum power consumption is only 6.5 mW, which is equivalent to 2.7 nJ/bit. Compared with previous works, it has the advantages of low cost, low power and high sensitivity and is suitable for LPWANs.

REFERENCES

[1] M. Iqbal, A. Y. M. Abdullah, and F. Shabnam, "An application based comparative study of LPWAN technologies for IoT environment," in *Proc. IEEE Region 10 Symp. (TENSYMP)*, Jun. 2020, pp. 1857–1860. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9230597

[2] M. N. Islam and M. R. Yuce, "Review of medical implant communication system (MICS) band and network," *ICT Exp.*, vol. 2, no. 4, pp. 188–194, Dec. 2016, doi: 10.1016/j.icte.2016.08.010.

[3] Z. Song, X. Liu, X. Zhao, Q. Liu, Z. Jin, and B. Chi, "A low-power NB-IoT transceiver with digital-polar transmitter in 180-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2569–2581, Sep. 2017, doi: 10.1109/TCSI.2017.2707412.

[4] S. Hong, S. Lee, J. Lee, and M. Je, "A multi-mode ULP receiver based on an injection-locked oscillator for IoT applications," *IEEE Access*, vol. 8, pp. 76966–76979, 2020, doi: 10.1109/ACCESS.2020.2989192.

[5] H. Guo, T. F. Chan, Y. T. Lai, K. C. Wan, L. Chen, and W. P. Wong, "30.3 a SAW-less NB-IoT RF transceiver with hybrid polar and on-chip switching PA supporting power class 3 multi-tone transmission," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 1–7. [Online]. Available: https://ieeexplore.ieee.org/document/9063093

[6] S. Lee, I. Choi, H. Kim, and B. Kim, "A sub-mW fully integrated wide-band receiver for wireless sensor network," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 5, pp. 319–321, May 2015, doi: 10.1109/LMWC.2015.2409808.

[7] Z. Liu, F. Yang, H. Jiang, X. Hao, J. Liu, and H. Liao, "An 89 μW MICS/ISM band receiver for ultra-low-power applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/8050667

[8] Z.-C. Zhang, C.-Y. Chiu, H.-C. Yuan, and T.-H. Lin, "A 0.5-V, 1.79-μW, 250-kbps wake-up receiver for IoT application in 90-nm CMOS," in *Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT)*, Aug. 2020, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/9196261

[9] A. Ba, M. Vidojkovic, K. Kanda, N. F. Kiyani, M. Lont, X. Huang, X. Wang, C. Zhou, Y.-H. Liu, M. Ding, B. Büsze, S. Masui, M. Hamaminato, H. Sato, K. Philips, and H. de Groot, "A 0.33 nJ/bit IEEE802.15.6/proprietary MICS/ISM wireless transceiver with scalable data rate for medical implantable applications," *IEEE J. Biomed. Health Informat.*, vol. 19, no. 3, pp. 920–929, May 2015, doi: 10.1109/JBHI.2015.2414298.

[10] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997, doi: 10.1109/4.568846.

[11] W.-C. Cheng, C.-F. Chan, C.-S. Choy, and K.-P. Pun, "A 900 MHz 1.2 V CMOS mixer with high linearity," in *Proc. Asia–Pacific Conf. Circuits Syst. (APCCAS)*, Oct. 2002, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/1114896

[12] J. Galan, R. G. Carvajal, A. Torralba, F. Munoz, and J. Ramirez-Angulo, "A low-power low-voltage OTA-C sinusoidal oscillator with a large tuning range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 2, pp. 283–291, Feb. 2005, doi: 10.1109/TCSI.2004.841599.

[13] J. Lee, K. S. Kundert, and B. Razavi, "Analysis and modeling of bang-bang clock and data recovery circuits," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1571–1580, Sep. 2004, doi: 10.1109/JSSC.2004.831600.

[14] J.-Y. Hsieh, Y.-C. Huang, P.-H. Kuo, T. Wang, and S.-S. Lu, "A 0.45-V low-power OOK/FSK RF receiver in 0.18 μm CMOS technology for implantable medical applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 8, pp. 1123–1130, Aug. 2016, doi: 10.1109/TCSI.2016.2589338.

[15] N. Kearney, C. Billon, M. Deeney, E. Evans, K. Khan, H. Li, S. Liang, K. Mulvaney, K. A. O'Donoghue, S. O'Mahony, P. Quinlan, S. Selvanayagam, S. Onkar, and C. Agrawal, "26.4 A 160-to-960 MHz ETSI class-1-compliant IoE transceiver with 100 dB blocker rejection, 70 dB ACR and 800pA standby current," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 1–9.

[16] K.-M. Kim, H.-G. Seok, O.-Y. Jung, K.-S. Choi, B. Yun, S. Kim, W. Oh, E.-R. Jeong, J. Ko, and S.-G. Lee, "A–123-dBm sensitivity split-channel BFSK reconfigurable data/wake-up receiver for low-power wide-area networks," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2656–2667, Sep. 2021, doi: 10.1109/JSSC.2021.3063134.

WENYA CHEN was born in Shangqiu, Henan, China, in 1995. He received the B.S. degree from the School of Physics and Electronics, Henan University, Kaifeng, China, in 2018. He is currently pursuing the Ph.D. degree with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. His current research interests include analog and RF circuits, such as wireless transceivers, PLLs, and SerDes.

HAOHAN YANG received the B.S. degree from the Institute of Electronic Engineering, Harbin Institute of Technology, Harbin, China, in 2017. He is currently pursuing the Ph.D. degree with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. His current research interests include analog and RF circuits, such as power detectors and power amplifiers.

SHUSHAN QIAO (Member, IEEE) received the Ph.D. degree from the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, in 2008. From 2008 to 2010, he was a Research Associate with the Institute of Microelectronics, Chinese Academy of Sciences, where he was an Associate Professor, from 2011 to 2017, and has been a Professor, since 2018. He has also been a Professor with the University of Chinese Academy of Sciences, Beijing, since 2018. His current research interests include artificial intelligence, ultra-low-power processors, intelligent microsystems, and communication chips.