IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 14 August 2023, accepted 23 August 2023, date of publication 4 September 2023, date of current version 8 September 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3311177

RESEARCH ARTICLE

Fully Integrated Efficient and Wideband Distributed Amplifier Employing Dual-Feed Output Stage With Active Input Split-Stage in 0.13μm CMOS

MOHSIN M. TARAR[1], SAAD QAYYUM[2], AND RENATO NEGRA[3]
[1]Department of Electronics Engineering, University of Chakwal, Chakwal 48800, Pakistan
[2]Department of Electrical and Computer Engineering, Pak-Austria Fachhochschule: Institute of Applied Sciences and Technology, Haripur 22620, Pakistan
[3]Chair of High Frequency Electronics, RWTH Aachen University, 52074 Aachen, Germany

Corresponding author: Mohsin M. Tarar (mohsin.tarar@uoc.edu.pk)

ABSTRACT This work presents the analysis, design, and implementation of an efficient and wideband active-split dual-feed distributed amplifier (AS-DFDA) in 0.13μm CMOS technology. It consists of a dual-feed (DF) output stage with a passive combiner and an active-split (AS) input stage. The dual-feed stage is used to enhance the gain and output power of the proposed AS-DFDA by utilising both the forward and reverse gains of a conventional distributed topology. The DF stage requires an in-phase equi-amplitude signals feeding the DF gate lines from both sides which is accomplished by an active-split stage based on the split drain-line topology providing a wideband input match along with the extra leaverage in gain. An external capacitance in series with the DF stage devices is deployed to increase the cut-off frequency of the dual-feed gate lines. Further, the interstage lines are terminated with idle-line terminations on both ends to target flat gain. The amplified signal from DF stage is combined through an output impedance matched direct passive combiner. The measured results show a 13-10 dB gain from 4-22 GHz and output return loss of 6dB over the entire bandwidth. The measured output saturated power, P_{SAT}, of 10.6 dBm with peak power added efficiency (PAE) of 15.1% is acheived at 5 GHz while a minimum peak PAE of 9% is obtained over the entire bandwidth. The AS-DFDA has a noise figure of 4-6 dB and occupies an active area of only 0.45 mm^2, respectively.

INDEX TERMS Distributed amplifier, dual-feed, active-split, capacitive compensation, split-drain line.

I. INTRODUCTION

Rapid growth of high-speed internet e.g. digital subscriber line (DSL) and Fibre-to-home drives the demand for high data-rate, high-capacity transmission systems. Wavelength division multiplexing (WDM) provides a very attractive solution by placing multiple data channels on a single piece of optical fibre for increasing transmission capacity [1]. Additionally, optical links benefit from distance insensitivity due to the inherently low-loss fibres [2]. However, cost and power dissipation are still a bottleneck for such high capacity systems where data-rates of 40 Gbps or higher have already been reported [1], [3]. Extremely broadband amplifiers are required to meet the high data-rate requirements for ultra-massive-capacity transmission systems. Apart from broadband operation, the design of power-efficient amplifiers in a low-cost technology becomes critical to meet the stringent requirements of cost and power dissipation.

Distributed amplifiers (DAs) are well known for broadband operation but generally exhibit poor efficiency, low gain, and occupy large area [4] [5]. Although, distributed amplifiers in III-V technologies show superior performance but are costly [3], [6]. On the other hand, CMOS DAs provide cost-effective solution but fall short in terms of performance. This creates demand for novel circuit-level implementations to enhance the performance and compete for ever-growing

The associate editor coordinating the review of this manuscript and approving it for publication was Fabian Khateb.

data-rate requirements. Low gain in conventional distributed amplifiers (CDAs) is due to its additive gain mechanism which is further worsened with the idle terminations absorbing half of the generaterd output current from the gain cells. DAs implemented in cascaded configurations obtain high gain and output power [8], [9], [10], however, all of them are bulky and deploy a large footprint. For instance, [8], [9] managed to achieve high gain with low noise but the DAs dissipate 250 mW and 238 mW power, respectively and occupy an area of 2.24 mm^2 and 0.83 mm^2, respectively. Distributed amplifiers with compact area can be found in the literature as well. In [15], a compact, power efficient, low noise distributed amplifier is demonstrated. It dissipates only 12.5 mW but the output power is quite low. Bhagavatula et al. [16], demonstrates a compact DA with an active area of only 0.15 mm^2 with only 5 dB gain. DAs with nonuniform techniques like tapered lines, weighted unit cells, gate-drain transformer feedback [11], [12], [13], [14] signify some of the performance metrics but fall short in terms of an optimum solution that should target all aspects. Dual-Feed (DF) distributed amplifier topology also improves the gain, output power, and efficiency of a conventional distributed amplifier (CDA) [7].

In a dual-feed distributed amplifier (DFDA), the input signal is fed from both sides of the gate-line and the amplified output signal is collected from both ends of the drain line. Since both the forward and reverse gains are utilised, the gain obtained is twice the gain of a CDA for the same number of gain sections. Subsequently, the output power 1 dB compression point and efficiency of the amplifier are also improved. However, these performance enhancements come at the cost of high input and output return loss as the idle gate- and drain-line terminations are removed. An active-split stage can be utilised as input stage to drive the DF stage which not only assures a good input match but also provides additional gain as well. Further, the DF amplified output signal can be combined through a direct passive combiner without utilizing the idle terminations. Thus, high gain along with large bandwidth, reasonable output power at low DC power dissipation and a compact size could all be accomplished, simultaneously.

This paper presents an active-split stage dual-feed distributed amplifier (AS-DFDA). Section II describes the basic idea along with the detailed theoretical analysis of both stages, followed by the frequency response of the proposed design. AS-DFDA implementation details are discussed in section III with measurement results demonstrated in section IV. Finally, the paper is concluded in section V.

II. PROPOSED ACTIVE-SPLIT DUAL-FEED DISTRIBUTED AMPLIFIER

The block diagram of the proposed AS-DFDA is shown in Fig. 1. It consists of an input active-split stage (AS), a dual-feed stage (DF) and an output combiner. The RF input is fed to the active-split stage which generates two in-phase outputs on the split-drain lines of the AS stage. Both outputs of the AS stage drive a dual-feed output stage and are amplified by the forward and reverse gains of the DF stage and further combined through a passive combiner. In order to analyse the circuit functionality, it is assumed that the signal travelling down the gate-line from left to right creates a forward gain equivalent to an n-stage conventional distributed amplifier (CDA) while the input signal traveling from the right to left creates a reverse gain of the same order of magnitude. By combining both amplified signals, an equivalent gain of a $2n$-stage CDA can be achieved which is shown in the following sections. It also provides the analysis for the active-split and dual-feed stages. Each stage is individually analysed and later combined to extract the overall gain of the AS-DFDA. Also, the frequency response of the AS-DFDA is analysed along with the implementation details followed by the measurement results validating the analysis and the design approach.

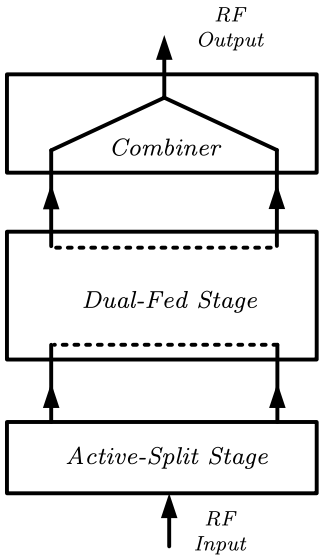

FIGURE 1. Block diagram of the proposed active-split stage dual-feed distributed amplifier (AS-DFDA).

A. ACTIVE-SPLIT STAGE

The schematic of an n-stage active spliter is shown in Fig. 2. Based on the split drain-line topology [17], it consists of an artificial gate-line exciting all the gates of the devices and two artificial drain-lines receiving the amplified signal at the drain nodes. The artificial gate-lines are synthesized with lumped inductors, L_g, and the gate capacitances, C_g, of the devices M_{1-n} where as the artificial drain-lines are formed between the inductors, L_{int}, and the drain-to-source capacitance, C_{ds}, of the devices. Z_g and Z_d are the gate-line and the drain-line terminations. Since the drain-line of the AS-stage is an interstage line of the AS-DFDA, the idle terminations at the interstage can be removed to see the effect on gain-bandwidth performance. Thus, the AS stage is analysed with two possible scenarios:

1) without idle drain-line terminations
2) With idle drain-line terminations

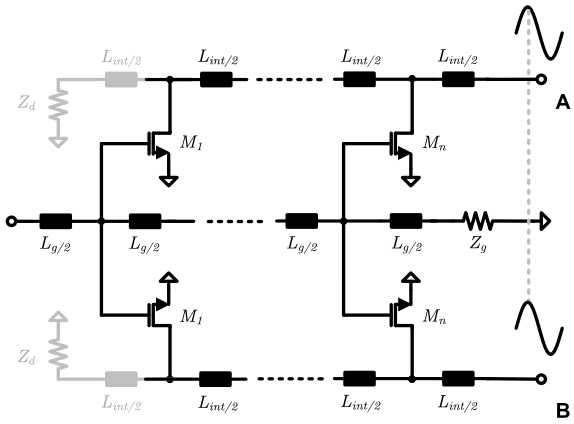

FIGURE 2. Input active-split stage with split-drain-line topology with and without idle drain-line termination.

1) WITHOUT IDLE DRAIN-LINE TERMINATIONS

The gain characteristics of the active-split stage (AS) is derived in this section. The following analysis is an extension of the analysis presented in [18] and [23] with gate- and drain-line attenuation parameters incorporated into the gain formulae of the active-split stage with-and-without idle terminations, later in the section. According to the reference equivalent circuit shown in Fig. 3(a), the current delivered to the n-active-split-stage load is given by

$$I_{D,AS} = e^{-\frac{\gamma_d}{2}}\left[I_{Dk,dk} + I_{Dk,rev}\right]. \tag{1}$$

$I_{Dk,dk}$ and $I_{Dk,rev}$ are the direct and reverse currents that flow through the load. $\gamma_d = \alpha_d + \beta_d$, is the drain-line propagation constant and consists of attenuation (α) and phase (β) constants. Using $I_d = g_m V_g$, the forward and reverse currents can be expressed as

$$I_{Dk,dk} = \frac{1}{2} g_m \sum_{k=1}^{n} V_{gk} e^{-(n-k)\gamma_d} \tag{2}$$

$$I_{Dk,rev} = \left(\frac{1+\Gamma}{2}\right) g_m \sum_{k=1}^{n} V_{gk} e^{-(n+k-2)\gamma_d} \tag{3}$$

Γ is the reflection coefficient for the reverse current at the open node where the idle drain-line termination is removed. g_m is the transconductance of the unit-gain cell. Since the drain-line is assumed to be uniform, it follows that there are no reflections between the two adjacent drain-line section of the active-split stage (this assumption also holds for the dual-feed stage, shown later in this section). V_{gk} is the voltage at the gate terminal of the k^{th} FET and can be written as [18]

$$V_{gk} = \frac{V_{in} e^{-(2k-1)\frac{\gamma_g}{2}} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{\sqrt{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}}. \tag{4}$$

In (4), the exponential term, $e^{-jtan^{-1}\frac{\omega}{\omega_g}}$, represents the frequency dependent voltage division between the gate resistance and the capacitance. $\omega_g = (1/R_g C_{gs})$ is the radian gate cut-off frequency and $\omega_c = (2/\sqrt{L_g C_{gs}}) = (2/\sqrt{L_d C_{ds}})$ is the radian cut-off frequency of the gate and drain-lines, respectively. ω is the operating radian frequency while the $\gamma_g = \alpha_g + \beta_g$ is the gate-line propagation constant. V_{in} is the input voltage. The direct and reverse currents could be further elaborated as

$$I_{Dk,dk} = \frac{g_m V_{in} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{2\sqrt{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}} \sum_{k=1}^{n} e^{-(n-k)\gamma_d} e^{-(2k-1)\gamma_g/2} \tag{2a}$$

$$I_{Dk,rev} = \frac{g_m V_{in} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{2\sqrt{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}} \sum_{k=1}^{n} e^{-(n-k+2)\gamma_d} e^{-(2k-1)\gamma_g/2} \tag{3a}$$

Using 2a, 3a in (1) would result in the total current delivered to the load as

$$I_{D,AS,wot} = \frac{g_m V_{in} e^{-n\frac{(\gamma_d+\gamma_g)}{2}} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{2\sqrt{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}} \times \left[\frac{\sinh((\gamma_d-\gamma_g)\frac{n}{2})}{\sinh((\gamma_d-\gamma_g)\frac{1}{2})} + \frac{\sinh((\gamma_d+\gamma_g)\frac{n}{2})}{\sinh((\gamma_d+\gamma_g)\frac{1}{2})} e^{-(n-1)\gamma_d}\right]. \tag{5}$$

The first term in the bracket corresponds to the direct current while the second term relates to the reverse current. The available power at the gate-line of the AS stage and the output power delivered to the load can be written, respectively, as

$$P_g = (|V_g|^2/2Z_{Ig}).Re[Z_{Ig}] \simeq (|V_g|^2/2)\sqrt{\frac{L_g}{C_g}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]} \tag{5a}$$

and

$$P_{d,AS} = \frac{|I_{D,AS,wot}|^2}{2} Re[Z_{Id,int}] \simeq \frac{|I_{D,AS}|^2}{2}\sqrt{\frac{L_{d,int}}{C_{ds}}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}. \tag{5b}$$

Using (4) and (5) in the above equations (5a) and (5b) respectively, the total power gain of the AS stage for n

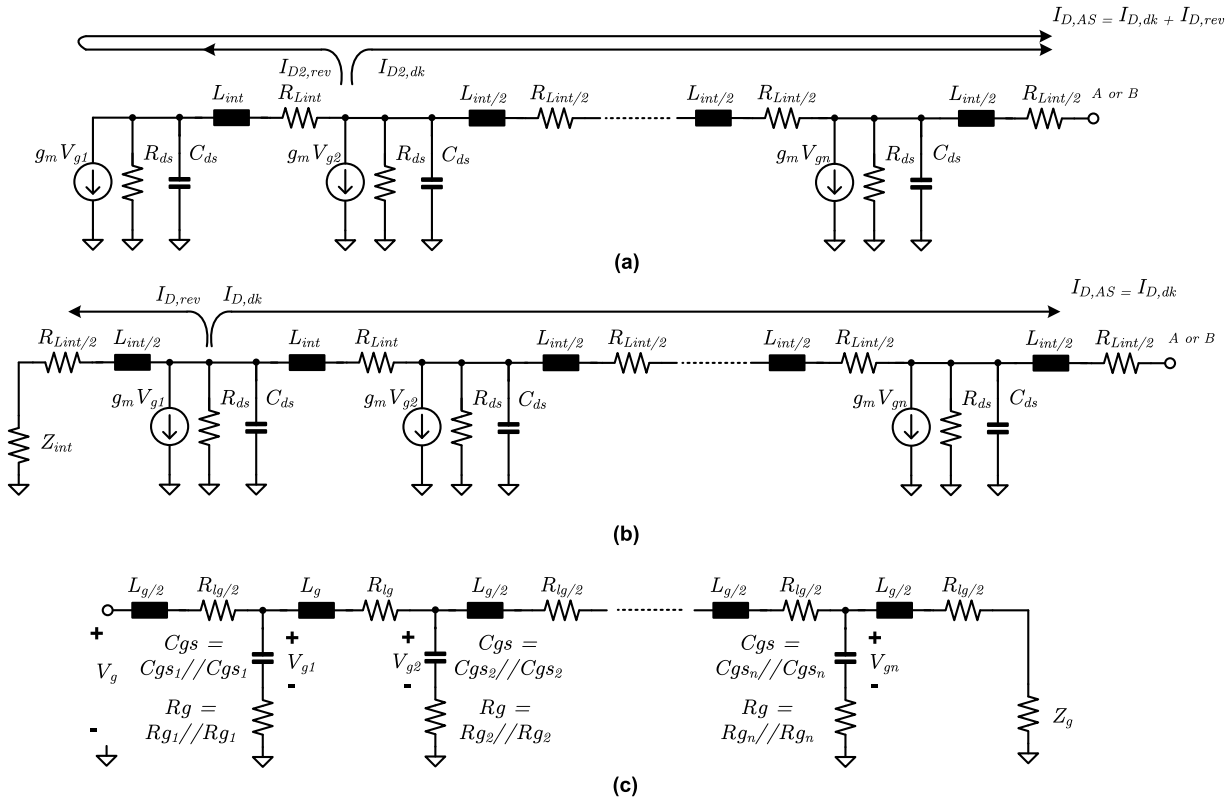

FIGURE 3. Equivalent circuit with lumped element line models (a) Active-split stage drain-line without termination (b) Active-split stage drain-line with termination (c) Active-split stage gate-line.

stages becomes

$$G_{AS,wot} = \frac{g_m^2 Z_{int} Z_g e^{-n(\gamma_d+\gamma_g)}}{4\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]} \times \left[\frac{\sinh((\gamma_d-\gamma_g)\frac{n}{2})}{\sinh((\gamma_d-\gamma_g)\frac{1}{2})} + \frac{\sinh((\gamma_d+\gamma_g)\frac{n}{2})}{\sinh((\gamma_d+\gamma_g)\frac{1}{2})} e^{-(n-1)\gamma_d}\right]^2. \quad (6)$$

The gain for the active-split stage without idle drain-line terminations, $G_{AS,wot}$, looks similar to the gain of a conventional distributed amplifier apart from the second term in the squared bracket which originates from the reverse current that is reflected back to the load.

2) WITH IDLE DRAIN-LINE TERMINATIONS

The small-signal model for the active-split stage with the idle drain-line terminations is shown in Fig. 3(b). The reverse currents from each generator terminate in the idle drain termination while the direct currents sum up in the load. Following the same procedure as described in the previous section, the current delivered to the load can be written as

$$I_{D,AS,wt} = \frac{g_m V_{in} e^{-n\frac{(\gamma_d+\gamma_g)}{2}} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{2\sqrt{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}} \times \left[\frac{\sinh((\gamma_d-\gamma_g)\frac{n}{2})}{\sinh((\gamma_d-\gamma_g)\frac{1}{2})}\right]. \quad (7)$$

Using (4) and (7), the gain for the active-split stage with idle drain-line terminations, $G_{AS,wt}$, becomes

$$G_{AS,wt} = \frac{g_m^2 Z_{int} Z_g e^{-n(\gamma_d+\gamma_g)}}{4\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]} \times \left[\frac{\sinh((\gamma_d-\gamma_g)\frac{n}{2})}{\sinh((\gamma_d-\gamma_g)\frac{1}{2})}\right]^2. \quad (8)$$

$G_{AS,wt}$ is similar to the gain of a CDA since the idle drain-line termination is employed. Note that the active-split stage gains ($G_{AS,wot}$, $G_{AS,wt}$) in (6) and (8) represent the one-sided gains of the AS stage.

B. DUAL-FEED STAGE

Output stage with dual-feed topology is depicted in Fig. 4, and its analysis is an extension of the work on dual-feed distributed amplifier in [7] and [19]. The analysis is modified to firstly, include the reverse current that accounts for the reverse gain of the dual-feed stage. Secondly, the attenuation parameters are included in the gain formulae to see the impact at high frequencies. For the gain analysis of the dual-feed stage, the equivalent circuit models of the drain- and gate-lines are shown in Fig. 5(a) and Fig. 5(b), respectively. Since, the DF stage is fed from both sides, there will be direct and reverse currents both contributing to the overall gain of the DF stage. The direct current, $I_{D,df}$ results from the input signal traveling from left to right over the gate-line while the reverse current, $I_{R,df}$ originates from the input signal moving

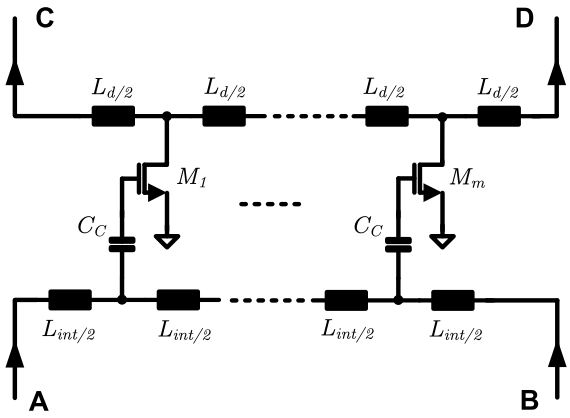

FIGURE 4. Output stage with dual-feed topology.

from right to left over the gate-line. The direct and reverse currents can be written as

$$I_{D,df} = \frac{g_m V_{in} e^{-n\frac{(\gamma_d+\gamma_g)}{2}} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{2\sqrt{\left[1+\left(\frac{\omega}{\omega_{g,df}}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}} \times \left[\frac{\sinh((\gamma_d-\gamma_g)\frac{n}{2})}{\sinh((\gamma_d-\gamma_g)\frac{1}{2})}\right] \tag{9}$$

and

$$I_{R,df} = \frac{g_m V_{in} e^{-(n-1)\frac{(\gamma_d+\gamma_g)}{2}} e^{-\gamma_g} e^{-jtan^{-1}\frac{\omega}{\omega_g}}}{2\sqrt{\left[1+\left(\frac{\omega}{\omega_{g,df}}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]}} \times \left[\frac{\sinh((\gamma_d+\gamma_g)\frac{n}{2})}{\sinh((\gamma_d+\gamma_g)\frac{1}{2})}\right]. \tag{10}$$

The total current delivered to the load becomes

$$I_{load,DF} = \sum_{i=1}^{m} \left(I_{D,df,i} + I_{R,df,i}\right). \tag{11}$$

Following the guidelines used for the active split stage to determine the power gain of the dual-feed stage and using (9), (10) and (11), the power gain for the dual-feed stage can be written as

$$G_{df} = \frac{g_m^2 Z_d Z_{int} e^{-n(\gamma_d+\gamma_g)}}{4\left[1+\left(\frac{\omega}{\omega_{g,df}}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]} \times \left[\frac{\sinh((\gamma_d-\gamma_g)\frac{n}{2})}{\sinh((\gamma_d-\gamma_g)\frac{1}{2})} + \frac{\sinh((\gamma_d+\gamma_g)\frac{n}{2})}{\sinh((\gamma_d+\gamma_g)\frac{1}{2})} e^{(\gamma_d-\gamma_g)}\right]^2. \tag{12}$$

Since both AS and DF stages are in cascaded configuration, the combined gain can be written as

$$G_C = G_{AS,wot/wt}.G_{df} \tag{13}$$

The above equation represents the one-sided gain from the active-split stage (with or without termination) cascaded with the dual-feed stage. The other side of the active-split stage along with the dual-feed stage contributes the same amount of gain. Thus, the total gain of the proposed AS-DFDA is the sum of both gains and is given by

$$G_T^{AS-DFDA} = 2G_C = 2.\left(G_{,AS,wot/wt}\, G_{,df}\right). \tag{14}$$

To get a quantitative analysis of the total gain $G_T^{AS-DFDA}$, derived in (14), $G_T^{AS-DFDA}$ is calculated for lossless condition and normalised to the CDA gain for lossless condition with the following three scenarios: 1) AS stage with the idle drain-line terminations ($AS-DFDA_{wt}$); 2) AS stage without the idle drain-line terminations ($AS-DFDA_{wot}$); 3) AS stage with the termination on one-side and omitted from the other side. The normalised AS-DFDA gains with the above stated scenarios are shown in Fig. 6. To make a fair comparison, the total number of sections (n) in the CDA are equal to the combined sections ($n+m$) of the AS-DFDA. For instance, a 4-section CDA corresponds to the 2-section (n) active-split stage and 2-section (m) dual-feed stage of the AS-DFDA. The (2-2) AS-DFDA with the idle drain-line termination, $G_{AS,wt}$, offers 6 dB more gain than a 4-section CDA whereas (2-2) AS-DFDA without idle drain-line termination, $G_{AS,wot}$, provides around 18 dB more gain than a 4-section CDA. Note that the $G_{AS,wot}$ offers 12 dB more gain than the $G_{AS,wt}$ which stems from the fact that the reverse current of the AS stage is reflected back to the load due to the omission of the idle drain-line terminations. Similarly, the AS-DFDA with the termination on one side and omitted on the other side offers 6 dB more gain than the $G_{AS,wt}$. The difference in gain increases with increasing the number of sections in the AS and in the DF stages of the AS-DFDA.

C. FREQUENCY RESPONSE OF THE AS-DFDA

Gain of the AS-DFDA depends upon gate- and drain-line attenuation and phase components of the propagation constant. Considering equal phase velocities for both lines, gain is influenced by the attenuation component originated from the active devices loss and the series resistance of the line. As per [23],

$$\alpha_g = \frac{c + aX_K^2}{\sqrt{1-(1-a^2)X_K^2}} \tag{15}$$

$$\alpha_d = \frac{b+d}{\sqrt{1-X_K^2}}. \tag{16}$$

The variables $a = (\omega_c/\omega_{Rg})$, $b = (\omega_{Rds}/\omega_c)$, $c = (\omega_{Lg}/\omega_c)$ and $d = (\omega_{Ld}/\omega_c)$. Where $\omega_{R_g} = (1/R_{gs}C_{gs})$, $\omega_{R_{ds}} = (1/R_{ds}C_{ds})$, $\omega_{L_g} = (R_{Lg}/L_g)$, $\omega_{L_d} = (R_{Ld}/L_d)$, and $X_K = \frac{\omega}{\omega_c}$. At low frequencies $X_K \approx 0$. Using (15) and (16), the gains in (6) and (8) can be rewritten as

$$G_{AS,wot,dc} \approx \frac{g_m^2 Z_{int} Z_g e^{-n(b+c+d)}}{4} \left[\frac{\sinh(\frac{n}{2}(b+d-c))}{\sinh(\frac{1}{2}(b+d-c))}\right.$$

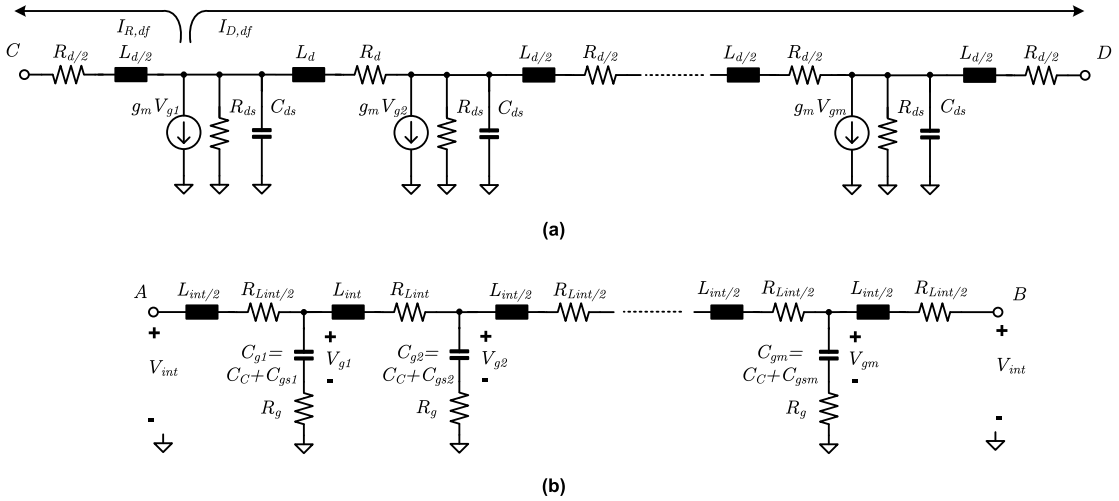

FIGURE 5. Equivalent circuit with lumped element line models (a) Dual-feed stage drain-line (b) Dual-feed stage gate-line.

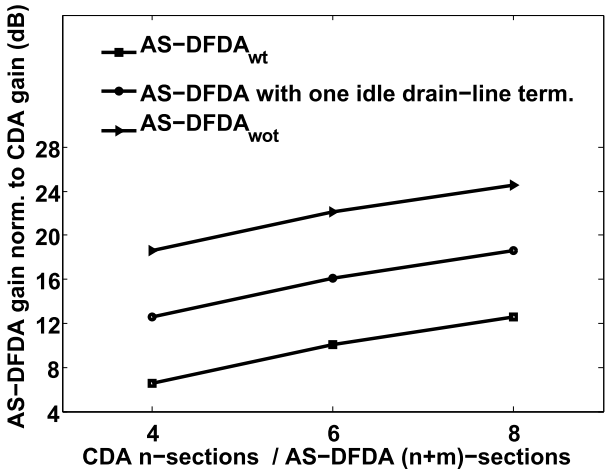

FIGURE 6. $(n+m)$-section AS-DFDA lossless gain normalized to the n-section CDA lossless gain.

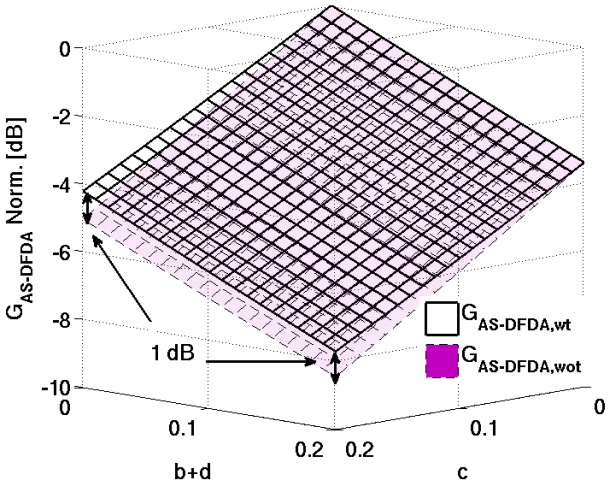

FIGURE 7. Low frequency $AS-DFDA_{wot/wt}$ gain normalised to respective lossless gains versus gate-line (c) and drain-line ($b+d$) attenuations.

$$+\left.\frac{\sinh(\frac{n}{2}(b+d+c))}{\sinh(\frac{1}{2}(b+d+c))}e^{-(n-1)(b+d)}\right]^2 \quad (17)$$

$$G_{AS,wt,dc} \approx \frac{g_m^2 Z_g Z_{int} e^{-n(b+c+d)}}{4}\left[\frac{\sinh(\frac{n}{2}(b+d-c))}{\sinh(\frac{1}{2}(b+d-c))}\right]^2. \quad (18)$$

Similarly, the dual-feed stage gain in (12) can be modified using (15) and (16) as

$$G_{df,dc} \approx \frac{g_m^2 Z_d Z_{int} e^{-n(b+c+d)}}{4} \times \left[\frac{\sinh(\frac{n}{2}(b+d-c))}{\sinh(\frac{1}{2}(b+d-c))} + \frac{\sinh(\frac{n}{2}(b+d+c))}{\sinh(\frac{1}{2}(b+d+c))} \times e^{(b+d-c)}\right]^2. \quad (19)$$

To see the effects of the gate- and drain-line attenuations on the gain of the proposed AS-DFDA, the total gain $G_T^{AS-DFDA}$ in (14), is calculated based on the AS stage gains in (17), (18), and the DF stage gain in (19). Subsequently, the total calculated gain is normalised to the gain at lossless conditions and plotted as surface plots against the attenuation parameters (b, d, and c) in Fig. 7. The normalised gains decrease monotonically with the increase in attenuation for both cases, *i.e*, AS stage with and without termination. However, the gain reduction in case of 2-section active-split stage dual-feed distributed amplifier without termination ($AS-DFDA_{wot}$) is around 1dB more than the 2-section active-split stage dual-feed distributed amplifier with termination ($AS-DFDA_{wt}$) because of the reverse current component suffering from the drain-line attenuation at low frequency (the second term in (17) multiplied by a decaying exponent). By increasing the number of the sections, the gain reduction increases further and gets even worst in case of $AS-DFDA_{wot}$.

At high frequency, the gate-line attenuation, α_g, increases with the square of the frequency (15) and becomes the

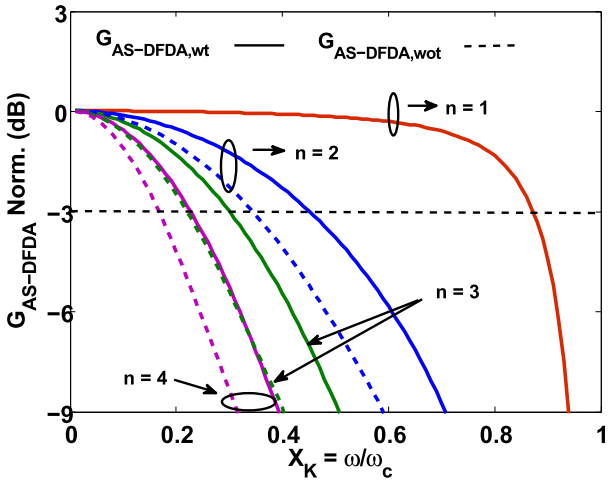

FIGURE 8. Low frequency $AS-DFDA_{wot/wt}$ gain normalised to respective lossless gains versus gate-line (c) and drain-line ($b+d$) attenuations.

critical factor in defining the optimum number of sections in a distributed topology. For both AS-DFDA topologies, $G_T^{AS-DFDA}$ is calculated with a different set of parameters a, b, c, and d with multiple sections, n, and normalised to the low-frequency gain and plotted against the normalised frequency, X_K, in Fig. 8. $G_T^{AS-DFDA}$ is normalised with its dc-to-low-frequency version and not the lossless version due to the presence of drain-line attenuation at very low frequency which makes it the maximum available gain of the AS-DFDA topology. Note that the frequency dependent gate- and drain-line attenuations are discussed in detail in [18]. From Fig. 8, it can be seen that with increasing n, the obtainable bandwidth is reduced in both AS-DFDA topologies. This reduction is more severe in case of the termination-less AS-DFDA which is due to the reflections from the open end of the artificial transmission line, also reported in [23]. For instance, with $n = 2$ and for the same set of parameters $gm = 35\ mS, a = 0.3, b = 0.14, c = d = 0.05$, the 3-dB bandwidth for the AS-DFDA,wt is 0.45 while in the case of the AS-DFDA,wot the obtained bandwidth is reduced to 0.34. With more sections $n = 3, 4$, the bandwidth reduces further for both topologies. The AS-DFDA,wot provides less bandwidth than the AS-DFDA,wt though it provides higher gain, especially at low frequencies. Nevertheless, a trade-off exists between the device peripheries (related parasitics that define the artificial lines series inductance and their resistive losses) and the optimal number of sections which in turn affect the gain, output power, and bandwidth requirements.

III. TOPOLOGY SELECTION AND CIRCUIT IMPLEMENTATION

The design and implementation of the AS-DFDA prototype is performed on guidelines that are based on the analysis described in the previous sections along with some critical observations made during the design procedure. These details are listed in the following subsections.

A. ACTIVE-SPLIT AND DUAL-FEED STAGES

The first and foremost criteria in the AS-DFDA design is the topology selection for the AS stage, *i.e.* with or without drain-line terminations. Based on previously described analysis, the AS-DFDA,wt provides more bandwidth than the AS-DFDA,wot for the same number of sections. However, the AS-DFDA,wot provides higher gain at low frequencies which tends to drop drastically with the increase in frequency yielding a low gain-bandwidth product.

The very high gain at low frequency could potentially lead to instability. Therefore, the AS stage with drain-line termination is adopted in this design. Critical observations related to the device sizing, number of sections for both stages, and the artificial gate- and drain-line impedances are as follows: 1) the common-source (CS) devices for both the AS and the DF stages are sized considering the cut-off frequency of the synthetic artificial gate-lines and the gain obtained per section. In case of the AS stage, increasing the width of the CS transistors would result in higher gain only at low frequencies plus the power dissipation also increases significantly. The high gain of the AS stage could lead to an early saturation of the CS devices in the DF stage. Similarly, the CS widths for the dual-feed stage critically impact the output power and efficiency performance obtained over the entire bandwidth. Thus, a choice has to be made between the maximum gain, power, and achievable bandwidth of the design; 2) the phase velocity equalization of the gate- and drain-lines for both stages are not critical simply because of the fact that both AS and the DF stages are in cascade configuration.

In a cascade configuration, the total current is independent of the individual currents generated by each device in a way that eventually they add up in the load. This also provides a degree of freedom in designing the AS stage drain-lines with relatively high impedance to enhance the gain of the AS stage. The increased impedance (argubly from the increased inductance) could limit the cut-off frequency of the dual-feed artificial gate-line because the AS stage drain-line serves as the gate-line for the DF stage. Therefore, bandwidth compensation capacitors, C_C, in series with the gate capacitance of the DF stage devices can be employed to enhance the cut-off frequency. Additionally, the CS devices in the DF stage can be optimised for high output power and efficiency in the presence of these compensation capacitors since they decrease the gate capacitance of the device.

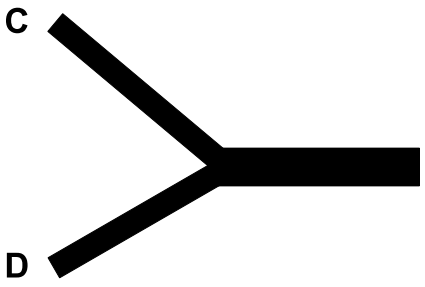

FIGURE 9. Y-shaped power combiner.

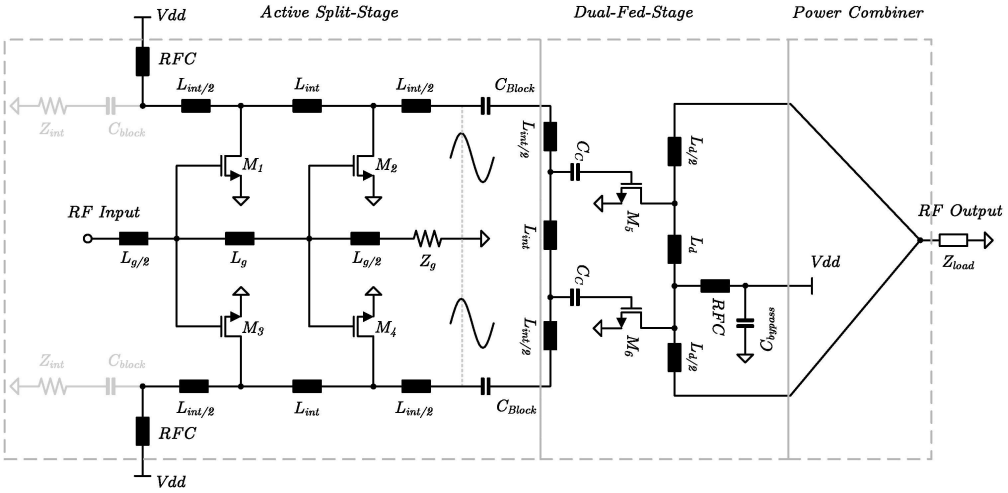

FIGURE 10. Complete schematic of the proposed AS-DFDA with and without drain-line termination.

TABLE 1. Design parameters of the AS-DFDA with termination.

Active-split stage	Dual-feed stage
$M_1 - M_4$	M_5, M_6
Length: 0.12 µm Unit width: 1.25 µm Fingers: 10 Multipliers: 3	Length: 0.12 µm Unit width: 1.25 µm Fingers: 14 Multipliers: 3
$L_{choke,AS}$, L_g, L_{int}	$L_{choke,DF}$, L_d, C_C
3.5 nH, 0.4 nH, 0.23 nH	3.5 nH, 0.12 nH, 0.5 pF

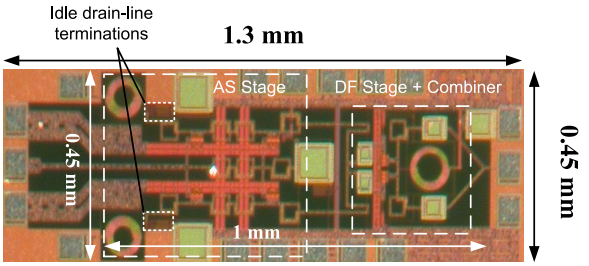

FIGURE 11. Chip microphotograph of the fabricated AS-DFDA with idle drain-line termination.

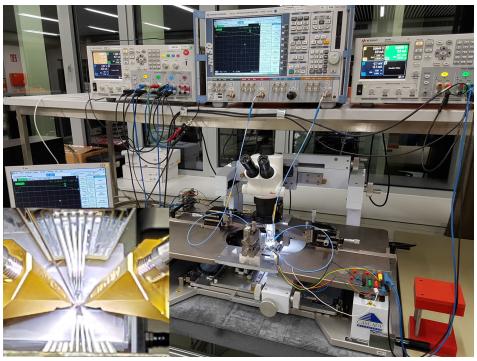

FIGURE 12. Measurement setup of the AS-DFDA. A magnified picture of probing the chip is shown in inset.

B. POWER COMBINER

There are two possible ways to combine the output powers from both sides of the DF stage. One way is to utilise an active topology; for instance, a similar topology like the AS stage could be employed as an active combiner. Such an arrangement would have split gate-lines connected to the drain-lines of the DF stage. A single drain-line of the active combiner shall collect the drain currents and delivers it to the 50-Ω load. However, there are a couple of drawbacks associated with this approach; 1) the DF stage amplifies the signals with high gain such that the devices in the next stage would be early saturated which leads to nonlinearities. 2) A two-stage topology is required to maintain the gain and bandwidth of the amplifier. This requires additional four active devices which not only increase the power dissipation but also increases the size significantly. For instance, at least twelve inductors are required to implement the active combiner stage with four active devices which increase the area. The second possibility is to use conventional passive combiners, *e.g.* a Wilkinson combiner or transformer-based combiners. In order to cover a wide bandwidth, multi section combiners (in case of a Wilkinson) are needed at the cost of higher insertion loss, large size, and increased complexity. The port-to-port isolation of the Wilkinson combiner enhances the complexity which needs to be maintained over wide bandwidth. By assuming that all the inputs are in-phase, port-to-port isolation is no longer a major constraint.

Under such an assumption, precise quarter-wavelength segments in a Wilkinson combiner are no longer required and can be replaced by lines with arbitrary lengths subject only to impedance transformation and layout constraints [20]. A Y-shaped combiner provides the feasibility to combine

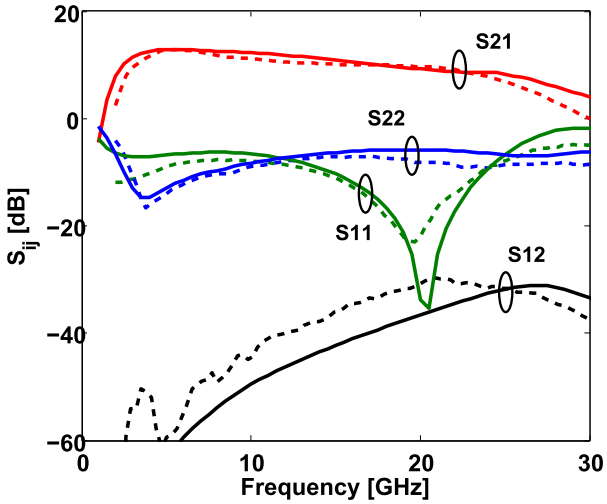

FIGURE 13. Measured (dashed lines) and simulated (solid lines) small-signal S-parameters of the AS-DFDA.

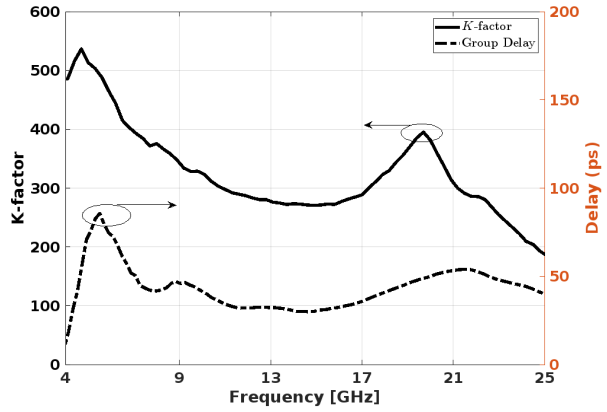

FIGURE 14. Measured group delay and the stability of the AS-DFDA.

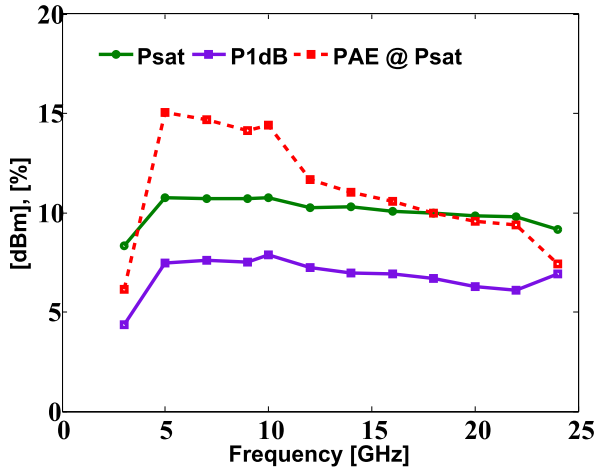

FIGURE 15. Measured P_{SAT}, P_{1dB} and PAE of the AS-DFDA with idle drain-line termination.

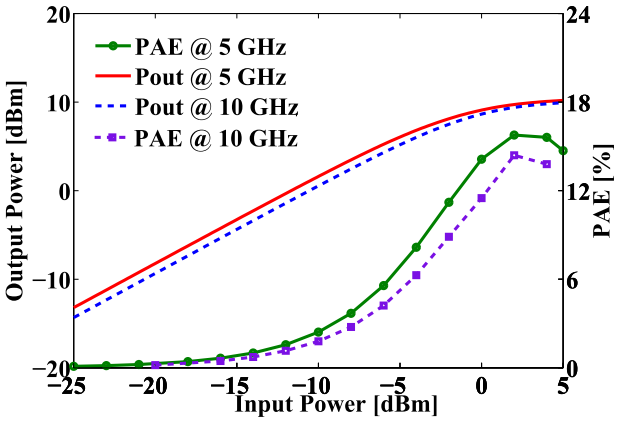

FIGURE 16. Measured PAE, output power of the AS-DFDA @ 5 GHz, 10 GHz.

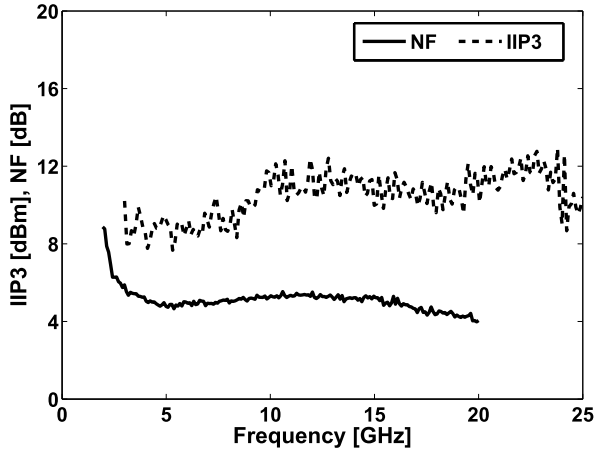

FIGURE 17. Measured noise figure and IIP3 of AS-DFDA.

two inputs with relatively low insertion loss and significantly less area as compared to that of a Wilkinson combiner [21]. In mm-wave power amplifier design, this is an effective technique as high output powers are obtained by combining multiple PAs where the size of the combiners and insertion loss play an important role. In context of the proposed AS-DFDA, the Y-shaped combiner is an attractive solution since only two in-phase inputs (terminal c and d as shown in Fig. 9) are combined and transformed to 50-Ω.

Based on the above observations, the AS-DFDA prototype is designed and shown in Fig. 10. A two section AS and a two section DF stage are designed with respect to the gain, power, bandwidth, and area for the AS-DFDA prototype. Transistors M_{1-4} and M_{5-6} form the gain cells for AS and DF stages, respectively. The gate-line of the AS stage is designed to be 50 Ω. The drain-line is designed to have relatively high impedance while the DF stage has both high impedance gate- and drain-lines. The forward and reverse gains of the DF stage are combined using a Y-shaped passive combiner. The inputs of the combiner are matched to the drain-line impedance of the DF stage and the output of the combiner is matched to 50 Ω. The drain-lines are fed through an RF choke of 3.5 nH for both the DF and the AS stage. Note, that a total of three RF chokes are implemented. The symmetry between the two drain-lines of the AS stage is critical because it affects the gain combination at the output of the dual-feed stage. Finally, the AS-DFDA is tweaked for optimum performance. The final parameters are tabulated in Table 1.

TABLE 2. Performance comparison of broadband amplifiers.

Ref.	Tech. (CMOS)	Topology	BW (GHz)	Gain (dB)	GBW (GHz)	P_{DC} (mW)	P_{1dB} (dBm)	NF (dB)	Size (mm^2)	FOM X 1000
[8]	0.18 μm	Cascaded/ Distributed	39.4	20	394	250	6.5 @ 20 GHz	8-9.4 < 18 GHz	2.24	19
[9]	0.18 μm	Cascaded Distributed	33	24	523	238	7.5 @ 5 GHz	6.5-7.5 < 18 GHz	0.83	48
[11]	0.13 μm	Weighted Distributed	12	15	67.5	26	-4 @ 1.8 GHz	2.3-4.5 < 10.6 GHz	0.435	6
[12]	90 nm	Distributed	70	13	312.7	85.4	1 @ 25 GHz	N/A	0.78	NF N/A
[16]	40 nm	Compact Distributed	30	5	53.4	34	2 @ 30 GHz	< 6.2	0.15	FT N/A
[15]	90 nm	Efficient Distributed	21	15	118	12.5	N/A	4.4-6	0.41	P1dB N/A
[24]	65 nm	I/O match Transf. VGA	20-43	14.5	122	30.8	**-3.5 @ 24G	5.5-8.2	0.34	2
[25]	90 nm	Variable gain Distributed	3.7-43.7	21	448	33	1.9 @ 35G	4.5-9.2	0.72	38
AS-DFDA	0.13 μm	Dual-feed Distributed	3-22	13-10	60	45	7.87-6.11	4-6 < 22 GHz	0.45	34

** From the Figure

IV. MEASUREMENT RESULTS

The proposed AS-DFDA is fabricated in a standard 0.13μm bulk CMOS technology. The fully integrated AS-DFDA prototype has a total area of 0.59 mm^2 while the active area is only 0.45 mm^2. The chip micro-photograph is shown in Fig. 11.

To demonstrate the performance of the AS-DFDA, on wafer measurements are done with 100 um-pitch GSG RF probes. DC biasing is applied through a 5-pin 100 um-pitch DC probe. Out of the twelve DC pads, six are used for the feeding the DC while the rest are used for probe landing and grounding. The complete setup is shown in Fig. 12.

S-parameter measurements are performed using a Rohde & Schwarz ZVA50 and are plotted along with the simulation results in Fig. 13. It should be noted that simulations are carried out with device RF models available from the foundry while the complete layout along with the artificial lines have been EM-simulated. The input artificial Tlines are interfaced with 50 Ω impedance of the equipment that leads to a fix characteristic impedance of the lines. Increasing the size would result in increased capacitance. The lumped inductance needs to be increased as well to keep the ratio same i.e. 50 Ω. Increased value of the inductor would not only increase the series attenuation on the line but the cut-off frequency of the lines would also scale down drastically. Therefore, an optimum size should be chosen that should best fit required parameters.

The fabricated AS-DFDA demonstrates peak small-signal gain of 13 dB at 5 GHz. A minimum of 10 dB gain is measured from 3 to 22 GHz, yielding a gain-bandwidth product (GBW) of 60 GHz. The AS-DFDA was designed for flat gain over the bandwidth. Although, a gain higher than 13 dB could have been extracted from the topology, it would have confined the total obtainable bandwidth and, hence, resulting in a reduced GBW. Input and output return loss are better than 10 dB and 6 dB over the entire bandwidth, respectively. The input-output isolation is better than 30 dB. The ON-chip drain-biasing chokes along with the RC of the drain-line blocking capacitors and terminations define the low frequency cut-off of the amplifier. Same is reflected in the stability and group delay plots of the amplifier, shown in Fig. 14.

Fig. 15 shows the measured power added efficiency (PAE), saturated output power P_{SAT}, and 1-dB output power compression P_{1dB}, of the AS-DFDA over the operating frequency range. When biased from a 1.2 V drain supply, the AS-DFDA shows measured P_{SAT} from 10.7 dBm to 8.3 dBm over the entire operating bandwidth. The P_{1dB} varies from 7.87 dBm to 6.11 dBm. There is a variation of 0.9 dB in the P_{SAT} and 1.3 dB in P_{1dB} of the AS-DFDA from 5 to 22 GHz. The output power capability originates mainly from the DF output stage that acts as the power stage of the proposed amplifier. The total power dissipation of the AS-DFDA is only 45 mW and delivers peak efficiency of 15% at 5GHz. A minimum of 10% PAE is obtained over 15GHz of bandwidth. Peak efficiencies at 5G and 10G against the input power are plotted in Fig. 16.

To characterize the linearity of the proposed AS-DFDA, a two-tone linearity test is performed with 10 MHz spacing at an RF input power level per tone of -10 dBm. The measured IIP_3 is plotted in Fig. 17. The input third-order intercept point, IIP_3 is greater than 8 dBm throughout the bandwidth, highlighting the linearity of the amplifier.

The noise figure (NF) measurements are performed with a PNA-X 70 GHz Microwave Network Analyser along with an Electronic Calibration Module (ECAL). A commercial low-noise amplifier was also utilised to enhance the gain and NF of the total system. This is the normal setup adopted to accurately extract the noise figure of the DUT (AS-DFDA). The PNA-X de-embeds the NF and gain of the LNA from the total gain and NF measurements. The measured NF of the AS-DFDA is also shown in Fig. 17. It can be observed that the NF lies between 4-6 dB from 3-22 GHz and is a reasonable value compared to other published works. Table 2 summarizes the performance and provides a comparison to previously reported works.

V. CONCLUSION

An efficient, wideband, fully integrated, active-split stage dual-feed distributed amplifier in 0.13μm CMOS for various high data rate applications is presented. The fabricated prototype demonstrates a measured wideband operation from 3-22 GHz with more than 10 dB of gain, yielding a gain-bandwidth product of 60 GHz. It delivers a saturated peak output power of 10.7 dBm with 0.9 dB variation from 5-22 GHz. The sustained output power over the wide bandwidth shows the effective and homogeneous driving capability of the proposed AS-DFDA. DC power consumption is 45 mW which highlights the power efficiency of the amplifier. The proposed topology also features good noise and linearity performance. The active area is 0.45 mm^2. The achieved area can be further reduced by removing the second drain bias-line along with the DC decoupling capacitors. The biasing can be applied through a single drain bias-line feeding both drain-lines of the active-split stage. With further layout modifications, there is a possibility of reducing the area by another 10-15 %. From the above performance parameters, it can be concluded that the AS-DFDA provides a suitable solution for ultrawideband communication systems.

ACKNOWLEDGMENT

The authors would like to thank Ahmed Hamid and Muh-Dei Wei for the fruitful discussions.

REFERENCES

[1] H. Shigematsu, M. Sato, I. Hirose, F. Brewer, and M. Rodwell, "40 Gb/s CMOS distributed amplifier for fiber-optic communication systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 476–477.

[2] K. T. Settaluri, S. Lin, S. Moazeni, E. Timurdogan, C. Sun, M. Moresco, Z. Su, Y.-H. Chen, G. Leake, D. LaTulipe, C. McDonough, J. Hebding, D. Coolbaugh, M. Watts, and V. Stojanović, "Demonstration of an optical chip-to-chip link in a 3D integrated electronic-photonic platform," in *Proc. 41st Eur. Soild-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 156–159.

[3] H. Shigematsu, M. Sato, T. Hirose, and Y. Watanabe, "A 54-GHz distributed amplifier with 6-V_{PP} output for a 40-Gb/s $LiNbO_3$ modulator driver," *IEEE J. Solid-State Circuits*, vol. 37, no. 9, pp. 1100–1105, Sep. 2002.

[4] R.-C. Liu, C.-S. Lin, K.-L. Deng, and H. Wang, "Design and analysis of DC-to-14-GHz and 22-GHz CMOS cascode," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1370–1374, Aug. 2004.

[5] B. Sewiolo and R. Weigel, "A novel 2–12 GHz 14 dBm high efficiency power distributed amplifier for ultra-Wideband-applications using a low-cost SiGe BiCMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2008, pp. 1123–1126.

[6] K. W. Kobayashi, "Linearized Darlington cascode amplifier employing GaAs PHEMT and GaN HEMT technologies," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2116–2122, Oct. 2007.

[7] C. S. Aitchison, N. Bukhari, C. Law, and N. Nazoa-Ruiz, "The dual-fed distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1988, pp. 911–914.

[8] J.-C. Chien and L.-H. Lu, "40 Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18-μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 538–620.

[9] J.-C. Kao, P. Chen, P.-C. Huang, and H. Wang, "A novel distributed amplifier with high gain, low noise, and high output power in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1533–1542, Apr. 2013.

[10] T.-Y. Huang, Y.-H. Lin, J.-H. Cheng, J.-C. Kao, T.-W. Huang, and H. Wang, "A high-gain low-noise distributed amplifier with low DC power in 0.18-μm CMOS for vital sign detection radar," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–3.

[11] Y.-J. Wang and A. Hajimiri, "A compact low-noise weighted distributed amplifier in CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 220–221.

[12] S.-H. Chen, S.-H. Weng, Y.-C. Liu, H.-Y. Chang, J.-H. Tsai, M.-H. Li, and S.-Y. Huang, "A monolithic DC-70-GHz broadband distributed amplifier using 90-nm CMOS process," in *Proc. IEEE Eur. Microw. Integr. Circuit Conf.*, Oct. 2013, pp. 540–543.

[13] C.-Y. Hsiao, T.-Y. Su, and S. S. H. Hsu, "CMOS distributed amplifiers using gate-drain transformer feedback technique," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2901–2910, Aug. 2013.

[14] K. Entesari, A. R. Tavakoli, and A. Helmy, "CMOS distributed amplifiers with extended flat bandwidth and improved input matching using gate line with coupled inductors," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 2862–2871, Dec. 2009.

[15] B. Machiels, P. Reynaert, and M. Steyaert, "Power efficient distributed low-noise amplifier in 90 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2010, pp. 131–134.

[16] V. Bhagavatula, M. Taghivand, and J. C. Rudell, "A compact 24–54 GHz CMOS band-pass distributed amplifier for high fractional bandwidth signal amplification," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, vol. 57, no. 12, pp. 71–74.

[17] W. Ciccognani, G. Giolo, E. Limiti, and P. E. Longhi, "Split gate line distributed power amplifier using tapered drain line approach and active broadband input power divider," in *Proc. Eur. Microw. Conf. (EuMC)*, Sep. 2009, pp. 1425–1428.
[18] J. B. Beyer, S. N. Prasad, R. C. Becker, J. E. Nordman, and G. K. Hohenwarter, "MESFET distributed amplifier design guidelines," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-32, no. 3, pp. 268–275, Mar. 1984.
[19] I. A. Botterill and C. S. Aitchison, "Effect of hybrids on gain performance of dual-fed distributed amplifiers," *Electron. Lett.*, vol. 30, no. 13, pp. 1067–1068, Jun. 1994.
[20] W. Tai, L. R. Carley, and D. S. Ricketts, "A 0.7 W fully integrated 42 GHz power amplifier with 10% PAE in 0.13 μm SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, vol. 30, no. 13, pp. 142–143.
[21] Y.-S. Lin and V. K. Nguyen, "94-GHz CMOS power amplifiers using miniature dual Y-shaped combiner with RL load," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1285–1298, Jun. 2017.
[22] J. B. Beyer, S. N. Prasad, J. E. Nordman, R. C. Becker, G. K. Hohenwarter, and Y. Chen, "Wideband monolithic microwave amplifier study," ONR, Arlington, VA, USA, Tech. Rep. NR243-033, Sep. 1983.
[23] A. Worapishet, I. Roopkom, and W. Surakampontorn, "Theory and bandwidth enhancement of cascaded double-stage distributed amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp. 759–772, Apr. 2010.
[24] T. Wu, C. Zhao, H. Liu, Y. Wu, Y. Yu, and K. Kang, "A 20 $\sim$ 43 GHz VGA with 21.5 dB gain tuning range and low phase variation for 5G communications in 65-nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 71–74.
[25] T.-Y. Chiu, Y. Wang, and H. Wang, "A 3.7–43.7-GHz low-power consumption variable gain distributed amplifier in 90-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 2, pp. 169–172, Feb. 2021.

MOHSIN M. TARAR received the B.Sc. degree in electronics from IIU Islamabad, the master's degree in electrical engineering with specialization in communication and electronics from Linköping University, Sweden, and the Ph.D. degree from RWTH Aachen University, Germany, where his dissertation was in wideband power amplification for various high data rate applications using CMOS technology. In 2018, he joined the Innovation for High Performance Microelectronics (IHP), as a Team Lead, where he designed high data rate TIAs and driver circuits for high-speed optical transceivers in SiGe:BiCMOS and electronics-photonic integrated circuits (EPIC) technologies. In 2019, he moved to Ulm University, where he designed a state-of-the-art 200 Gbaud trans-impedance amplifier and driver designs which will be incorporated with high-speed Mach-Zehnder modulators and photodiodes to realize the high-speed electro-optical transceivers. Recently, he joined the University of Chakwal, as an Assistant Professor, where he is currently heading the Electronics Engineering Department.

SAAD QAYYUM received the B.Sc. degree (Hons.) in computer engineering from CIIT, Abbottabad, Pakistan, in 2006, the M.Sc. degree in microelectronics systems design from the University of Southampton, Southampton, U.K., in 2007, and the Dr.-Ing. degree in electrical engineering from the Chair of High Frequency Electronics, RWTH Aachen University, Aachen, Germany, in 2019. From 2006 to 2019, he was a Lecturer with CIIT. Since 2020, he has been an Assistant Professor with the Department of Electrical and Computer Engineering, Pak-Austria Fachhochschule: Institute of Applied Sciences and Technology, Pakistan. His current research interests include microwave and millimeter-wave circuit design and the application of machine learning for modern wireless communication systems. He was a recipient of the fully funded scholarships for master's and doctoral studies offered by CIIT and HEC, Pakistan/DAAD, Germany, respectively.

RENATO NEGRA received the M.Sc. degree in telematics from the Graz University of Technology, Graz, Austria, in 1999, and the Ph.D. degree in electrical engineering from ETH Zürich, Zürich, Switzerland, in 2006. His doctoral research was focused on power-efficient linear amplification of wireless communication signals. During the M.Sc. studies, he spent one year as an Exchange Student with the Norwegian University of Science and Technology (NTNU), Trondheim, Norway. From 1998 to 2000, he was with Alcatel Space Norway AS (now NorSpace AS), Horten, Norway, where he was involved in the design and characterization of space-qualified RF equipment. In April 2000, he joined the Laboratory for Electromagnetic Fields and Microwave Electronics, ETH Zürich. From 2006 to May 2008, he was a Postdoctoral Fellow with the iRadio Laboratory, University of Calgary, Calgary, AB, Canada, where he was involved with switching-mode PAs and advanced wireless transmitter architectures. Since June 2008, he has been an Assistant Professor with RWTH Aachen University, Aachen, Germany, where he heads the Mixed-Signal CMOS Circuits Group, Ultra High-Speed Mobile Information and Communication (UMIC) Research Centre. His research interests include highly efficient PAs, advanced transmitter architectures, software-defined and reconfigurable radios, linearization, and mixed-signal, as well as millimeter-wave circuits.