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RESEARCH ARTICLE

Enhancing Power Module Lifespan Through Power Distribution Approaches in a Three-Phase Interleaved DC/DC Converter

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ABSTRACT This paper comprehensively analyzes various power distribution approaches to balance the stress on power modules (PM) in a three-phase interleaved DC/DC converter and increase its lifespan. Two implementations of power distribution are investigated: a symmetrical approach, where the PM utilizations are balanced by controlling the duration of their active intervals, and an asymmetrical approach, achieved by adjusting their reference currents. Regardless of the power distribution method, the estimation of accumulated PM stress is evaluated using two utilization metrics: energy-related and current-related. Different utilization and distribution control algorithms are validated using a hardware-in-the-loop (HiL) simulation setup, considering varying load profiles. The additional control modules require only minor modifications to the conventional two-loop controller structure, exhibit consistent responses, and steadily reduce the balance mismatch for all control combinations. The results demonstrate that asymmetrical control combined with energy utilization estimation yields the most favorable balance mismatch rate. Moreover, this methodology demonstrates superior energy efficiency in intervals characterized by balance mismatch, though it necessitates a significant initial labor investment for constructing the thermal mode.

INDEX TERMS Interleaved converter, SiC MOSFET, power distribution, switch utilization, thermal model, load balancing, control algorithm, enhanced lifespan, hardware-in-the-loop.

I. INTRODUCTION

As with any other electrical device, power converters are prone to fail during their expected lifespan due to the individual component fault. Among all components, the study [1] shows that complex multi-layer structure [2] is the main reason for the highest failure rate of modern power switches. The most frequent fatigues are thermally related and include bond wire lift-off [3], bond wire heel-cracking, solder fatigue [2], [4], and cracks in joints between the direct-bonded-copper (DBC) substrate and base plate, and power chip [3]. These cracks increase thermal impedance and intensify temperature divergence during thermal cycling, i.e., accelerating material fatigue growth.

In order to reduce thermally induced failures, passive solutions are widely used during manufacturing, including vacuum soldering, cleaning processes, sintered connections, heavy copper wire bonding, and buffered layers between materials [3], [4]. Further improvements are achieved by improving cooling systems, e.g., integrating the heat pipes or Peltier Devices into the DBC substrate [5]. Top and double-side cooled packages offer another promising advance [6], [7].

However, due to the preferred small design margins usually challenged in high-temperature applications and the missing thermal considerations [8], [9], [10], [11], the failure rate

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is expected to increase without adequate active countermeasures [4]. The active solutions are gaining increased attention, particularly in multi-level and multi-phase converters, due to their inherent capability to dynamically redistribute the power flow, i.e., the thermal stress among subunits. The same applies to multi-phase DC/DC converters with interleaved structures, which are generally required [12] to attain high efficiency and high device utilization [13] in broad power applications, e.g., automotive chargers and photovoltaic boost converters.

Various control strategies are implemented in multi-phase interleaved converters, including the average current-sharing control strategy. This strategy typically involves a conventional nested control structure with outer and inner loops—one for voltage control and the other for current tracking [14], [15], [16]. Achieving balanced operation is essential, as even symmetrically designed interleaved converters can experience slight deviations due to differences in leg impedances and driver mismatches. Balancing techniques aim to achieve several objectives, such as reducing the number of current transducers used, preventing circulating currents, and maintaining equal current loading of components [17], [18], [19]. Additionally, converter dynamics must not be compromised, including reference tracking capability, power quality, harmonic distortion, efficiency, and electromagnetic interference (EMI). However, it is essential to note that individual research efforts often focus on one indicator at a time.

The primary focus of balancing techniques, emphasizing aging, revolves around active thermal control (ATC) strategies. These strategies can be implemented at various control levels, such as the component, modulation, power, and system levels, considering the preferred control bandwidth and complexity preferences [20], [21]. ATC at Power Module Layer involves active gate control or pulse placement using intelligent gate drivers [4], adjusting the driver's current, voltage, and gate resistance to directly influence switching losses and, thus, the power module's temperature. The advantage of active gate control is its ability to affect losses without compromising the converter's basic functionality [21]. However, these intelligent drivers may be costlier compared to discrete drivers. Another approach is to tailor switching and conduction losses through modulation frequency or strategy adjustments at the modulation layer. This approach has limitations concerning the range of possible switching frequencies, considering factors like increased ripple current and switching losses at higher frequencies [20], [22].

Significant advantages in thermal control are observed at the power controller layer as the thermal stress can be effectively managed by distributing power on a larger scale among the converter's legs, as demonstrated in [22] and [23]. The ATC is integrated into the current mode controller, implements the state of health (SoH) block, and employs temperature feedback to assess accumulated damage in each leg's power module. In contrast, various methods, including electro-thermal models (ETMs), rely on the observation of electrical parameter changes in components, which can be employed in feedback – such as the MOSFET's on state resistance and gate threshold voltage [24] to estimate junction temperature and determine accumulated damage.

Nevertheless, this approach requires additional voltage sensors, increasing converter cost and complexity. The same applies to the indirect methods [25], including Coffin-Manson's and Bayere's model and their derivatives [4], [22], [26], [27], which estimate the thermally caused degradation upon mathematical lifetime models and built-in SoH block, which includes the counting method and lifetime model. The input to the SoH block is the estimated junction temperature of PM components from ETM and power losses from operating conditions.

The control strategies mentioned above, such as active gate control, modulation frequency adjustment, and power level techniques, aim to manage thermal stress by tracking the junction temperature of power module components. While this may be efficient for steady-state thermal management, it raises concerns about dynamic performance. Namely, the lagged thermal response of T_j could lead to dangerous current mismatches during dynamic load profiles, potentially exceeding operational boundaries and jeopardizing the converter's reliability. It becomes imperative, therefore, to address and mitigate such dangerous current mismatches during dynamic operation to safeguard the system from undesirable consequences.

Overall, the limitations highlighted in the literature review include the scarcity of comprehensive paper reviews addressing power-sharing control methods simultaneously with their broad impacts, the common practice of asymmetric power sharing between phases, and in some cases, the non-objective evaluation of control goals comparing the simulation-based and experimental results, i.e., evaluating the junction versus case/heatsink temperature [28]. This is a result of exclusive reliance on thermography-based temperature measurement, which may not fully capture the dynamic performance of the converters. Thus, the majority of active control concepts are validated only under steady-state load conditions, even though dynamic performance is addressed in research [27], [29], [30], [31], [32], [33].

Rather than using junction temperature as the feedback parameter, our research proposes the utilization factors (energy-related utilization factor $\lambda_{E,n}$ and current-related utilization factor $\lambda_{I,n}$ as feedback control parameters in the proposed interleaved converter control. While the first directly correlates with the losses dissipated on the individual switch, the second one indirectly affects the switch as it merely relates to the part of the output power routed through the individual converter's phases. Thus, both factors could be essential in estimating the accumulative thermal stress and achieving a balance in switch utilization under a dynamic load profile. The paper thoroughly evaluates their impact in combination with symmetrical and asymmetrical power distribution algorithms, aiming to enhance the control strategies for thermal stress management and aging in

Component	Value	Unit
U_S	450	V
R_S	0,369	Ω
R_L	[7-24]	Ω
$L_{1,2,3}$	86	μH
C_{in}	30	μF
C_{out}	500	μF

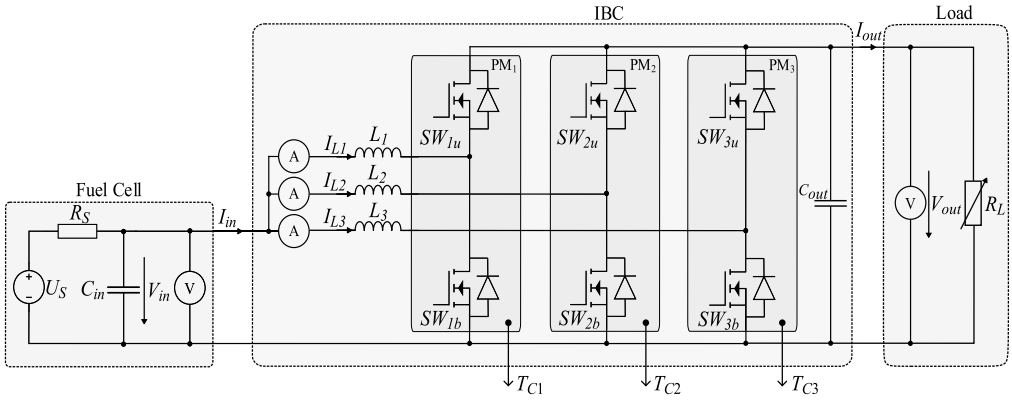

FIGURE 1. Power plant schematic and IBC's key simulation parameters.

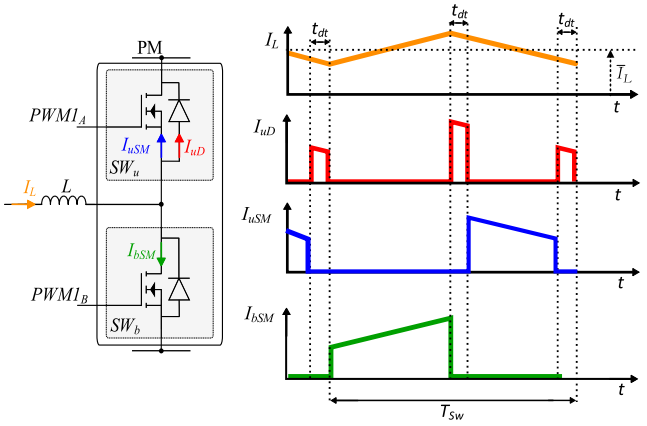

FIGURE 2. Transistor leg currents in CCM.

interleaved multi-phase converters. By utilizing these factors as feedback parameters, we additionally seek to explore a more straightforward approach that relies on the current-related factor to achieve an applicable switch utilization balance. This approach should not compromise the overall performance of the converter but rather reduce control effort and decrease algorithm execution times.

The feasibility study of different control structures is performed with the hardware-in-the-loop (HiL), enabling simulations to be carried out with decreased development costs and time.

II. THE INTERLEAVED BOOST CONVERTER

The analyzed system consists of an interleaved boost converter (IBC) that connects a fuel cell (FC) to the high-voltage DC bus of the drive, represented as a load in Fig. 1. The main function of the IBC is to regulate the unidirectional power flow from the FC to the load, ensuring a constant bus voltage (V_{out}) regardless of variations in V_{in}. The IBC is composed of three identical phases, denoted by $n = \{1, 2, 3\}$. Each phase includes an inductor (L_n) and upper and bottom switches integrated into a power module (PM_n). Each power module's case temperature ($T_{C,n}$) is monitored using a single sensor.

A phase-shifting technique is employed to minimize losses in the input and output capacitors, specifically reducing their current ripple. The phase currents ($I_{L,n}$) are intentionally phase shifted by 360/n, while their average values ($\bar{I}_L$) are maintained equal in the conventional control structure [14], [34]. However, when the values of the phase currents become too small, the respective phase is deactivated to enhance overall conversion efficiency. Consequently, each phase of the converter generally operates in continuous conduction mode (CCM). Accordingly, during the switching interval T_{sw}, individual components' average (denoted as $\bar{I}$) and RMS current differ substantially, as the waveforms in Fig. 2 reveal, leading to different conduction and switching losses.

The losses generated in the upper SiC MOSFET (P_{uSM}) and its Schottky body diode (P_{uD}) are

$$P_{uSM} = R_{DS,on}(T_{juSM}) \cdot I^2_{uSM,rms} \tag{1}$$

$$P_{uD} = V_{T0}(T_{juD}) \cdot \bar{I}_{uD} + R_D(T_{juD}) \cdot I^2_{uD,rms}, \tag{2}$$

where the $R_{DS,on}$, and R_D are the resistances of the MOSFET and its body diode in the conduction state, both being dependent on their junction temperatures. The temperature also impacts the diode's turn-on voltage (V_{T0}).

In the bottom SiC MOSFET (P_{bSM}), the switching losses must be considered as well

$$P_{bSM} = \underbrace{R_{DS,on}(T_{jbSM}) \cdot I^2_{bSM,rms}}_{\text{Conduction losses}} + \underbrace{E_{on+off}(V_{bSM}) \cdot f_{sw}}_{\text{Switching losses}}. \tag{3}$$

Namely, the operation of the upper and bottom MOSFETs in the power module (PM) differs significantly. The bottom MOSFET operates in hard-switching mode, characterized by high-magnitude overlapping transitions of current and voltage. In contrast, the upper switch experiences transition at a much lower voltage level, specifically the forward voltage V_F of the diode. As a result, the switching losses of the upper SiC MOSFET can be disregarded in (1). Similarly, if only the continuous conduction mode (CCM) is maintained, the losses in the bottom body diode can also be neglected.

The derived losses (1), (2), and (3) result in varying junction temperatures for different components within the PM, even when they possess identical junction-to-case resistance. Therefore, direct methods that provide access to each junction temperature (T_j) within the PM are necessary. However, these

methods are impractical due to their expensive and complex hardware requirements. On the other hand, methods based on the equivalent thermal model (ETM) are preferred. Although they involve offline modeling and a slightly higher computational burden during operation, they offer a more feasible approach.

In the subsequent sections, the measures aimed at extending the lifespan address the power module as a whole rather than focusing on specific discrete components of the transistor leg. Additionally, it is assumed that the thermal behavior of input inductors and I/O capacitors, which are thermally decoupled from the power module, is negligible and therefore disregarded.

III. THE PROPOSED ELECTRO-THERMAL-BASED AGING CONTROL IMPLEMENTED IN POWER CONTROLLER-LEVEL

In this paragraph, we initially describe the conventional digital dual-loop control, which consists of an outer voltage- and an inner current-control loop. As illustrated in Fig. 3, the first contains the current controller (CC) for each phase and PWM logic (PWML), which governs the subsidiary analog-to-digital converter and PWM modules integrated into the MCU. The controller adjusts the average inductor current $\bar{I}_L$ in each phase by modifying duty cycle D generated in a PWML.

One of the main distinctions between the conventional control structure and the proposed one lies in how a PI-type voltage controller (VC) handles the reference values ($\bar{I}^*_{in}$) along with the inner current controllers, which are responsible for controlling the converter's output voltage (V_{out}). The proposed control structure offers a significant departure from the conventional structure by allowing the magnitude of the reference value of the individual phase to be freely adjusted. This introduces additional control over power flow, granting flexibility in managing the system's behavior.

In the conventional approach, the power distribution module (PDM) enhances power flow efficiency through the remaining phases by shutting down one or two phases and simultaneously increasing the ratio share of the current reference value ($\bar{I}^*_{in}$) from one-third to one-half. Consequently, in the conventional structure, the power flow distribution is solely determined by the magnitude of the $\bar{I}^*_{in}$ value, limiting the control options available compared to the proposed structure.

By harnessing a higher degree of control and its modification, it becomes feasible to significantly extend the lifespan of the power module (PM). This progress involves estimating the junction temperature of a specific PM, which relies on accurate power loss calculations and considering the thermal properties of the device's cooling path. To accomplish this, the thermal model incorporates the power losses of the PM, utilizing the derived losses (1), (2), and (3). Utilization factors are then calculated to quantify the cumulative thermal stress experienced by the PM. These functionalities are handled within the proposed thermal model (TM) and power loss model (PLM), which are combined to form an enhanced electro-thermal model (ETM), being an integral part of the power distribution module (PDM).

A. THERMAL MODEL OF THE PM

The most cost-effective approach to indirectly monitor junction temperature relies upon the Foster equivalent thermal model [35], [36]. This model illustrates in Fig. 4 that each MOSFET and body diode integrated into the power module (PM) consists of seven sub-circuits, one for each layer. The thermal path of each layer contains a thermal resistance (R_{th}) and a thermal capacitance (C_{th}), both connected in parallel. These coefficients were obtained from the application manual [37], which guarantees an accurate representation for practical purposes. Note that thermal cross-coupling between adjacent components has not been considered to ensure simplicity and focus on the overall PM behavior.

Consequently, the heat generated inside the individual component's junction transfers directly to the PM's case. It is predicted that a more complex thermal model is not required since a single temperature sensor per PM is attached to its case for control purposes in the actual design. In order to determine the junction temperatures (T_j) required for the power loss model (PLM), calculations are performed based on the input power losses of specific components and the corresponding measured case temperature (T_C).

B. POWER LOSS MODEL OF THE PM

The losses in a particular transistor leg, i.e., PM, are calculated in power loss model (PLM). The average and RMS values of currents required in (1), (2), and (3) can be easily determined from a measured current waveform (refer to Fig. 2), which illustrates the steady-state continuous conduction mode (CCM) operation. Specifically, the average current $\bar{I}_{uD}$ flowing through the diode is directly proportional to the inductor current and the duty cycle D_{DT}, which corresponds to the dead-time interval

$$\bar{I}_{uD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_{uD}(t)dt = 2\bar{I}_L \cdot D_{DT}. \tag{4}$$

By neglecting the current ripple, the RMS values of the upper and bottom SiC MOSFETs ($I_{uSM,rms}$ and $I_{bSM,rms}$) are determined in the same way

$$I_{uSM,rms} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i^2_{uSM}(t)dt} = \bar{I}_L \cdot \sqrt{1 - (D - D_{DT})} \tag{5}$$

$$I_{bSM,rms} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i^2_{bSM}(t)dt} = \bar{I}_L \cdot \sqrt{D - D_{DT}}, \tag{6}$$

where the $\bar{I}_L$ is effortlessly obtained during the operation by sampling the measured current in the middle of PWM's t_{on} and t_{off} intervals. While the D_{DT} is predetermined through

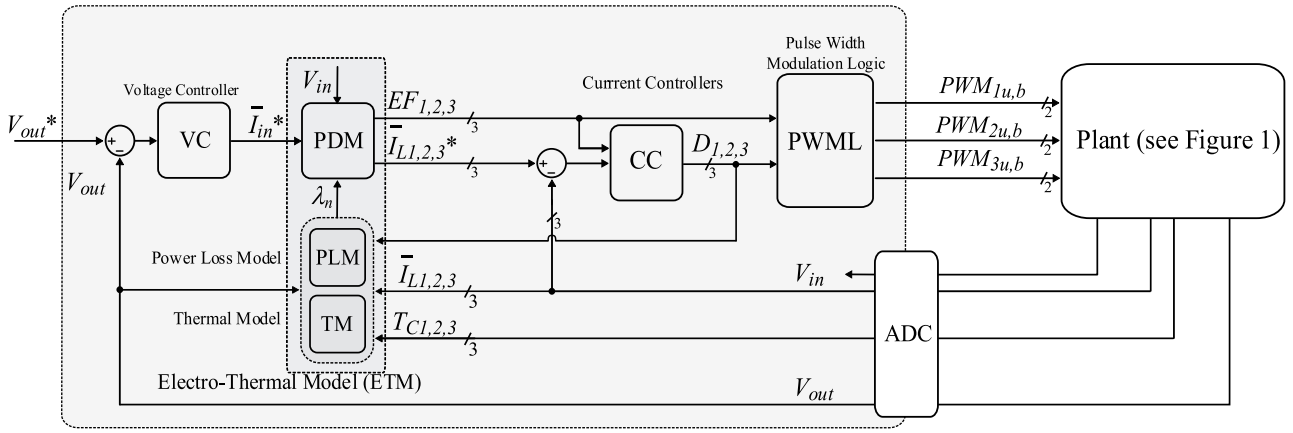

FIGURE 3. Schematic of three phase IBC controller.

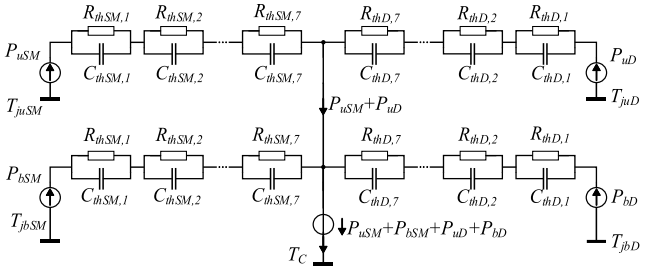

FIGURE 4. Power module's Foster thermal model.

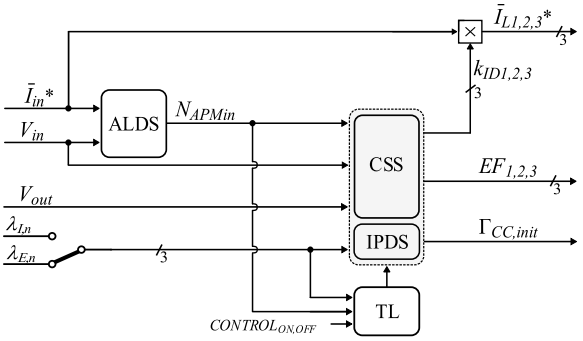

FIGURE 5. Power distribution module.

design, the duty cycle D varies during operation. Thus, both D_{DT} and D are known and utilized to calculate (4), (5), and (6).

However, additional effort was necessary to determine the impact of junction temperature on the $V_{T0}(T_{jD})$ and $R_D(T_{jD})$. Both relationships were extrapolated for arbitrary junction temperature from the forward body diode characteristic $V_F = f\ (I_F)$, which was previously interpolated from linearized characteristics obtained for two specific temperatures (25 °C, 175 °C) from the datasheet of the device being analyzed [30]. Likewise, the output characteristics of the SiC MOSFET, represented by $V_{DS} = f\ (I_D)$, were subjected to a similar process. In both cases, the interpolated data points, within the temperature range of 25 °C to 175 °C, were then utilized to derive the coefficients of the polynomial functions $V_{T0}(T_{jD})$ and $R_D(T_{jD})$, and $R_{DS,on}(T_{jSM})$ employed in the calculation algorithm.

Similarly, more effort was required to derive E_{on+off} (V_{SM}, I_{SM}) for the PM, as the manufacturer provided only measured energy values at 600 V and in graphical form. These values were then scaled to the desired voltage by applying scaling factors obtained through specific requests. To obtain the polynomial function E_{on+off} (V_{SM}, I_{SM}) suitable for execution within the algorithm, a generalized interpolation and extrapolation procedure was implemented. However, for the sake of simplicity, the overvoltage across the MOSFET was neglected during this process.

C. POWER DISTRIBUTION MODEL

Thermal and power loss models are seamlessly integrated into the electro-thermal model (ETM) and incorporated into the overall control scheme of the applied interleaved converter. The ETM calculates utilization factors for each transistor leg, which are then inputted into the power distribution model (PDM) shown in Fig. 5. To ensure equalization of the PM's aging process, the utilization (λ_n) of each PM is evaluated by monitoring the accumulated current stress $(\lambda_{I,n})$ or dissipated energy $(\lambda_{E,n})$ over its entire lifetime.

The computation of the latter follows the power loss explanation in section II. It's important to note that the inductor current sampling occurs in each T_{sw} interval, while the control algorithm routines occur in multiples of T_{sw}. For example, the current control loop is executed every $T_{CCL} = 10T_{sw}$, while the power loss model is calculated every $100T_{sw}$. Within the same time window (T_{PLM}), the power losses (P_n) are recalculated using the power loss model and added to the energy sum of the previous (n-1) events

$$\lambda_{E,n} = \lambda_{E,n-1} + P_n T_{PLM}. \tag{7}$$

Meanwhile, the accumulated current stress $(\lambda_{I,n})$ is determined within the T_{CCL} interval using the same approach but with more outstanding promptness, as the average value of

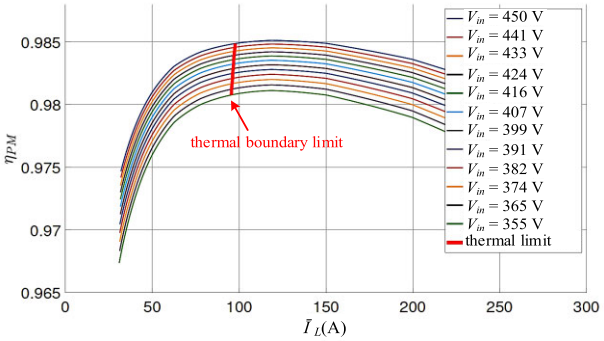

FIGURE 6. Estimated efficiency plot of a single PM with indicated boundary limit.

the inductor current is inherently obtained in the middle of each t_{on} interval

$$\lambda_{I,n} = \lambda_{I,n-1} + \bar{I}_{L,n} T_{CCL}. \tag{8}$$

Irrespective of which factor is selected as a control parameter (see Fig. 5), the power distribution module (PDM) regulates the power flow by adjusting two main parameters: *i*) the inductor current references ($\bar{I}^*_{L,n}$), i.e., the load factor ($k_{ID,n}$) for each transistor leg, and *ii*) the operating duration of each leg, achieved through controlling their active/inactive status or a combination of both.

The PDM's subordinate objective is to ensure high efficiency across the entire power range while enabling smooth transitions in response to input voltage or load power changes.

Fig. 5 provides a detailed schematic of the PDM, illustrating its four submodules and their respective functionalities. The active leg determination submodule (ALDS) adjusts the number of active legs (N_{APMin}) to maximize overall efficiency for a specific load ($V^*_{in} I^*_{in}$). This selection is based on an individual PM's estimated efficiency $\eta_{PM,n}$, as shown in Fig. 6. The efficiency is calculated using an offline Matlab script that utilizes the input parameters discussed in Section III-A.

Section II shows that the bottom transistor in the power module experiences the highest losses compared to other components. In order to prevent its potential failure, its maximum allowable junction temperature (150 °C) must not be exceeded. Thus, keeping the inductor current below a thermal boundary limit indicated by the red line in the diagram is crucial. This thermal boundary limit serves two purposes: *i*) it identifies the maximum achievable efficiency per power module, and *ii*) it restricts the highest allowed average inductor current ($\bar{I}_{Lmax}$), and thus the load factor (k_{ID}) for specified maximum temperature and voltage conditions. A first-order polynomial function was employed to approximate the relationship between the maximum average inductor current ($\bar{I}_{Lmax}$) and the input voltage (V_{in}) to facilitate control implementation. This approximation is valid within the input voltage range of {355 V, 450 V}.

Once the $\bar{I}_{Lmax}$ is identified, the current split submodule (CSS) calculates the N_{APMin} and selects the specific legs to minimize uneven aging processes among them. This selection

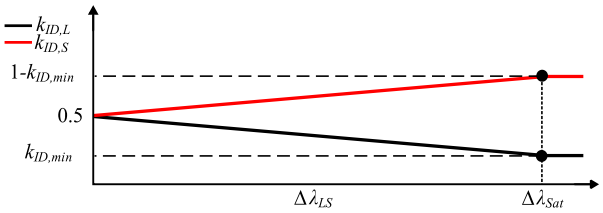

FIGURE 7. Load factors $k_{ID,L}$ and $k_{ID,S}$ as a function of $\Delta\lambda_{LS}$.

is accomplished by setting the individual enable flags EF_n based on the estimated legs utilization (λ_n). Additionally, the CSS determines load factors ($k_{ID,n}$) that govern the reference current in each leg

$$\bar{I}^*_{L,n} = \bar{I}^*_{in} \cdot k_{ID,n}. \tag{9}$$

Furthermore, the CSS considers the number of active legs, which can vary depending on the preferred power flow.

1) OPERATION WITH ONE ACTIVE LEG

In scenarios where a single transistor leg can handle the desired power flow, the leg with the lowest utilization is chosen. In this case, the load factor of the selected leg is set to "1," regardless of its utilization.

2) OPERATION WITH TWO ACTIVE LEGS

As the power flow increases, two legs are activated to handle the load. In this situation, the load factors of the selected legs are determined based on the difference ($\Delta\lambda_{LS} = \lambda_L$ - λ_S) between the leg with the largest λ_L and the smallest λ_S. If a difference exists, the load factor ($k_{ID,L}$) of the most utilized (λ_L) leg should be decreased according to

$$k_{ID,L} = {}^1\!/_n - \frac{{}^1\!/_n - k_{ID\,\min}}{\lambda_{sat}} \cdot \Delta\lambda_{LS};\ n = \{2, 3\}. \tag{10}$$

On the other hand, the load factor ($k_{ID,S}$) of the leg with the smallest utilization (λ_S) should be increased, ensuring that the load factors of the selected legs sum up to one, as illustrated in Fig. 7.

It is important to note that the load factors for the selected legs are subject to thermal boundary limits. Even when the difference ($\Delta\lambda_{LS}$) exceeds the pre-set saturation point ($\Delta\lambda_{sat}$), the minimum and maximum load factor values should never surpass these limits, ensuring efficient and safe operation.

3) OPERATION WITH THREE ACTIVE LEGS

In this case, the CSS must determine the load factor ($k_{ID,M}$) for the middle utilized leg. The process begins with finding the leg that satisfies the condition set in (10) with $n = 3$, meaning the one with the largest utilization ($k_{ID,L}$). The load factors in the remaining legs ($k_{ID,M}$ and $k_{ID,S}$) must satisfy

$$k_{ID,M} + k_{ID,S} = 1 - k_{ID,L}(\Delta\lambda_{LS}). \tag{11}$$

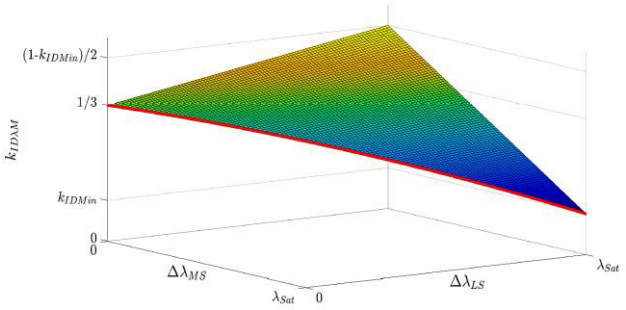

FIGURE 8. Load factor $k_{ID,M}$ as a function of $\Delta\lambda_{LS}$ and $\Delta\lambda_{MS}$.

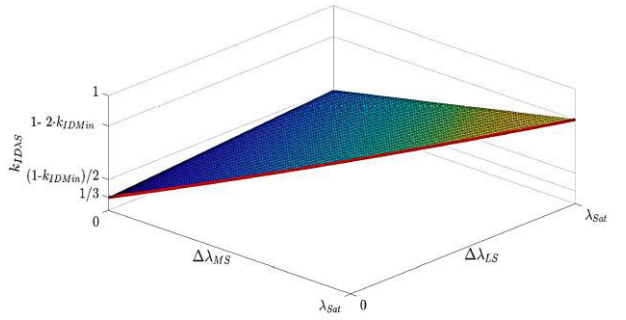

FIGURE 9. Load factor $k_{ID,S}$ as a function of $\Delta\lambda_{LS}$ and $\Delta\lambda_{MS}$.

Depending on the $\Delta\lambda_{LS}$, the sum (11) falls within 2/3 and $1 - k_{ID,\min}$. Additionally, $\Delta\lambda_{MS}$ is introduced as the difference between the medium-utilized leg and the leg with the smallest utilization. Generally, $\Delta\lambda_{MS}$ can be smaller or equal to the $\Delta\lambda_{LS}$. Assuming that the utilization difference $\Delta\lambda_{LS}$ is equal to the pre-set saturation point $\Delta\lambda_{sat}$, the $k_{ID,M}$ varies with $\Delta\lambda_{MS}$ according to

$$k_{ID,M}\big|_{\Delta\lambda_{LS}=\lambda_{sat}} = \frac{1 - k_{ID,\min}}{2} + \frac{k_{ID,\min} - 1}{2\lambda_{sat}} \cdot \Delta\lambda_{MS}. \tag{12}$$

The expression (11) that determines the load factor ($k_{ID,M}$) for a range of $\Delta\lambda_{LS}$ and $\Delta\lambda_{MS}$ values, graphically illustrated in Fig. 8, was obtained as a product between the expression given in (12) and the load factor $k_{ID,S}(\Delta\lambda_{LS})$

$$k_{ID,M} = \left[\frac{1 - k_{ID,\min}}{2} + \frac{k_{ID,\min} - 1}{2\lambda_{sat}}\Delta\lambda_{MS}\right] \cdot k_{ID,S}(\Delta\lambda_{LS}). \tag{13}$$

Once the $k_{ID,L}$, and $k_{ID,M}$ is known, the load factor ($k_{ID,S}$) of the smallest utilization leg can be calculated as

$$k_{ID,S} = 1 - k_{ID,L}(\Delta\lambda_{LS}) - k_{ID,M}(\Delta\lambda_{LS}, \Delta\lambda_{MS}). \tag{14}$$

Fig. 9 shows its value within the specified range $\{0, \lambda_{sat}\}$ of $\Delta\lambda_{LS}$ and $\Delta\lambda_{MS}$.

It is noteworthy that when utilization differences $\Delta\lambda_{LS}$ and $\Delta\lambda_{MS}$ reach or surpass the saturated utilization difference $\Delta\lambda_{sat}$, the maximum value of load factor ($k_{ID,S}$) for the leg with the smallest utilization is limited to

$$k_{ID,S}\big|_{\Delta\lambda_{LS}=\lambda_{sat},\,\Delta\lambda_{MS}=\lambda_{sat}} = 1 - 2 \cdot k_{ID,\min}. \tag{15}$$

The red curves in Fig. 8 and Fig. 9 represent the load factors ($k_{ID,M}$, $k_{ID,S}$) required under the condition of having identical utilization differences ($\Delta\lambda_{LS}$, $\Delta\lambda_{MS}$). It can also be deduced that when the utilization difference $\Delta\lambda_{LS}$ is at its saturated value and $\Delta\lambda_{MS}$ is zero, the legs with the smallest and middle utilization operate with equal load factors ($k_{ID,M}$, $k_{ID,S}$)

$$k_{ID,M}\big|_{\Delta\lambda_{LS}=\lambda_{sat},\,\Delta\lambda_{MS}=0} = \frac{1 - 2 \cdot k_{ID,\min}}{2}. \tag{16}$$

Nevertheless, to ensure the desired dynamics of the power balancing process, careful selection of the pre-set saturation point $\Delta\lambda_{sat}$, is crucial.

The trigger logic (TL) and integral part determination submodule (IPDS) coordinate the work of modules. In steady-state operation, both modules have negligible impact on PDM operation. In contrast, they ensure a smoother controller response and prevent overcurrent when leg status changes due to input voltage, load, or leg utilization variations.

IV. HiL TESTBENCH OF THE PLANT

In order to assess accumulated-based approaches of thermal stress on the aging process, we built a HiL-based model of the plant. The behavior of the analyzed power plant, including the fuel cell (FC), IBC, and load, was entirely emulated with a simulation model built into a HiL402 platform using the Typhoon Schematic Editor.

A. MODELLING OF THE INPUT SOURCE

The complex behavior of the fuel cell stack is modeled as a serial connection between the constant voltage source U_S and the resistor R_S. Both coefficients originate from the specimen fuel cell stack's polarization characteristic. Since the objective of this work was to analyze the plant behavior merely in the linear portion of the polarization curve, its dynamic properties have been neglected.

B. MODELLING OF THE LOAD

The load is modeled as a controlled resistor R_L that varies according to the predefined load profile $P_L(t)$ shown in Fig. 10. The data corresponds to the load profile obtained at the international student competition [38] with noticeable dynamics and peak power exceeding 80 kW.

C. MODELLING OF IBC POWER STAGE

The SiC MOSFET current-dependant parameters obtained from datasheets, such as *i*) the drain-source voltage (V_{DS}) and body diode's forward voltage V_F at two specific junction temperatures (T_j), and *ii*) the SiC MOSFET's turn-on and turn-off switching energies (E_{on}, E_{off})) provided for two specific bus voltages (V_{out}), were included in the plant model using Look-up tables to obtain the model's most representative responses.

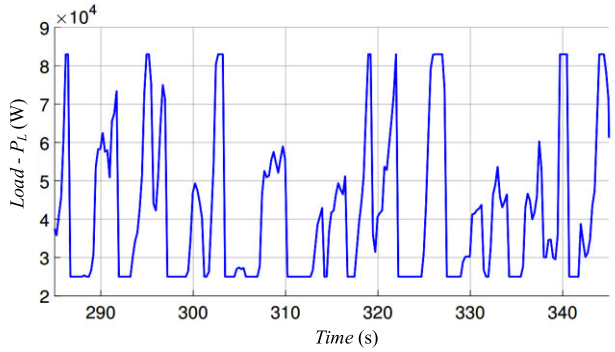

FIGURE 10. Loading profile $P_L(t)$ – shown in part.

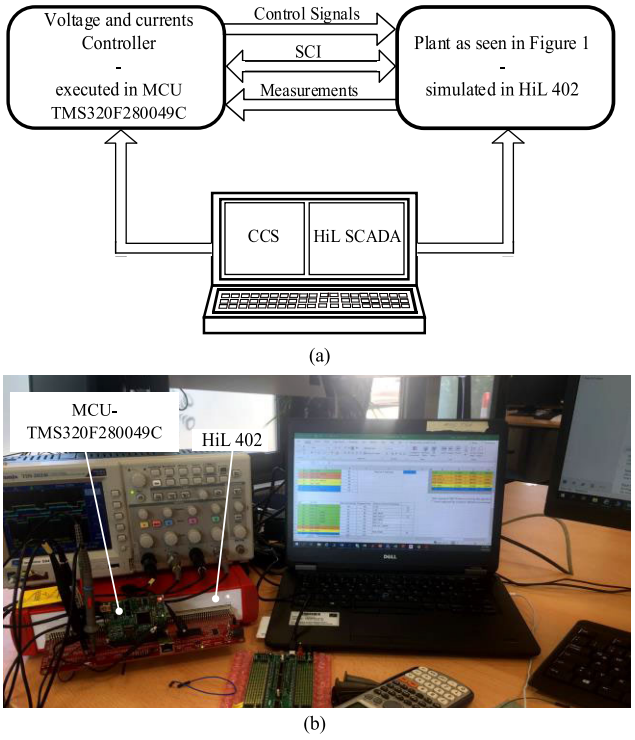

FIGURE 11. The analyzed power plant in HiL: (a) block view, (b) test bench setup.

Other coefficients of the HiL model were obtained from plant data sheets and not identified by measurements. To simplify the simulation and the interpretation of its results, all coefficients were assumed to be time-invariant. The fundamental simulation parameters are listed in Fig. 1.

In addition to the plant model, the test setup includes a designated MCU (Fig. 11), which executes the control algorithms based on the essential information obtained from the simulated plant via input-output pins. In this way, the plant behavior and the controller's functionality can be equivalently verified in a closed-loop manner without using vast and costly plant hardware.

The laptop served to program and monitor the HiL402 and MCU operation. The latter was accessed and controlled in debug mode, using Texas Instrument's Code Composer Studio (CCS), which additionally flashed the controller's software code. The Simulink Embedded Coder, integrated

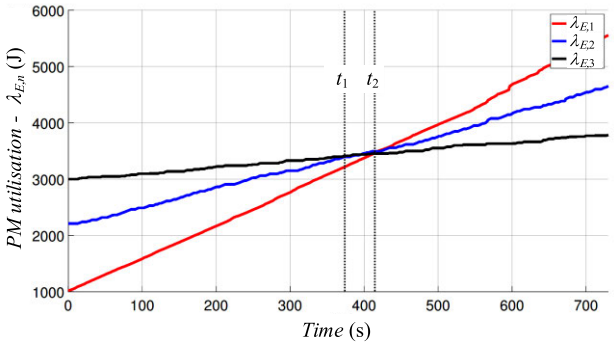

FIGURE 12. Utilization divergence due to the basic PDM functionality.

into Matlab Simulink, was used to build the controller code based on its Simulink model.

The fact that the converter plant is emulated inside the HiL device where the T_C can be initially pre-set to arbitrary value through the HiL SCADA panel substantially alleviates the experimentation and its duration.

V. RESULTS AND DISCUSSION

In multi-phase DC/DC converters, conventional controllers employ simple PDM techniques to distribute power flow symmetrically among the legs by equalizing the inductor currents. However, these controllers do not consider the past stress experienced by individual components. Additionally, when reducing power flow or shutting down a specific leg, the decision is made without considering the previous operational stress of that particular component. As a result, the same legs tend to be deactivated whenever the assessed N_{APMin} falls below a value of 3.

The impact of this behavior can be observed in Fig. 12, where the basic PDM functionality leads to divergence in utilization. To validate the concept, different initial values were intentionally assigned to the energy utilization factors ($\lambda_{E,n}$). Throughout the test, the load of the converter and the assessed N_{APMin} varied according to the profile described in Section IV-B. Until t_2, when the utilization indicators eventually converged, the first leg, which initially had the lowest utilization, exhibited the highest rising rate. Despite the power flow level, this leg remains active. However, after t_2, the same reason that kept the first leg active hindered the balanced operation as it prevented the energy utilization factors ($\lambda_{E,n}$) from increasing at the same rate.

The following subsections demonstrate the superiority of the proposed thermal-based aging control, which ensures a more balanced operation by considering the cumulative stress.

A. AGING CONTROL BASED ON ASSESSED $\lambda_{E,N}$ AND SYMMETRICAL LOAD DISTRIBUTION

Fig. 13 shows an operation with symmetrical power flow between the legs. The number of legs (N_{APMin}) and their active flags are determined based on temporary utilization factors and varying load profile.

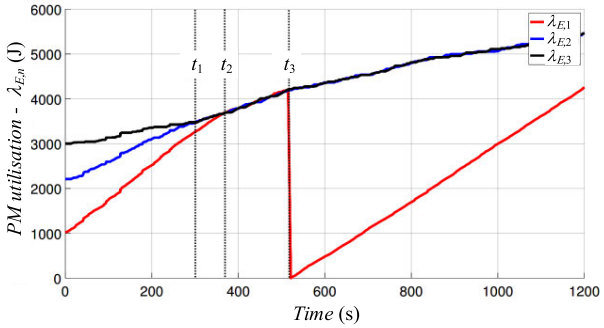

FIGURE 13. PDM's response considering prolonged test duration.

Consequently, in contrast to the conventional control concept, the utilization factors are actively regulated by manipulating their operational time, i.e., active status. The impact over an extended simulation period is depicted in Fig. 13.

At the start of the simulation, the utilization factors ($\lambda_{E,n}$) are initialized to the same values as shown in Fig. 12. Because the utilization factor (Fig. 13) is the smallest in the first leg ($\lambda_{E,1}$), the CSS keeps it active throughout the time interval $\{0, t_2\}$. On the other hand, the second and third legs become active only when the N_{APMin} increases to two or three. As a result, $\lambda_{E,1}$ experiences the greatest increase, whereas $\lambda_{E,3}$, grows at a slower rate. At time t_1, the second and third legs become equally utilized ($\lambda_{E,2} = \lambda_{E,3}$), whereas the $\lambda_{E,1}$ remains below both. Therefore, CSS keeps the first leg active regardless of the N_{APMin} until time t_2, when the utilization factors match. In the interval $\{t_2, t_3\}$, the utilization factors ($\lambda_{E,n}$) increase at a similar pace as the CSS continuously evaluates their values and decides which leg to turn on or off to minimize the difference. At time t_3, the $\lambda_{E,1}$ is intentionally changed to zero to examine the PDM's dynamic. The CSS promptly reacts to this change by keeping the first leg active as long as the $\lambda_{E,1} \leq (\lambda_{E,2}, \lambda_{E,3})$.

To gain further insight, Fig. 14 presents observations over a shorter duration starting at an arbitrary instant chosen in Fig. 13 when the utilization factors differ, as shown in Fig. 14-d. It additionally reveals (Fig. 14-b) that all three legs operate with the same magnitude of inductor currents, indicating that the PDM sets the same load factors ($k_{ID,n}$). Consequently, the individual $\lambda_{E,n}$ increases at a rate that differs from others, indicating the presence of a difference between PM junction temperatures. This operation continues until time t_A, when the converter load decreases by approximately 50 kW (Fig. 14-a). This change initiates new leg operational states (Fig. 14-c) based on their $\lambda_{E,n}$. Consequently, the assessed number of active legs N_{APMin} decreases from 3 to 1. By time t_A, the PM_1 reaches the lowest utilization value ($\lambda_{E,n}$) and remains active, whereas the remaining legs turn off. As a result, the $\lambda_{E,1}$ steadily increases, whereas the $\lambda_{E,2}$ and $\lambda_{E,3}$ persist at their attained levels (Fig. 14-d).

The converter continues its designated operation until t_B, when the converter's load increases again (Fig. 14-a), leading to an increase in N_{APMin} from 1 to 2. Consequently, the CSS

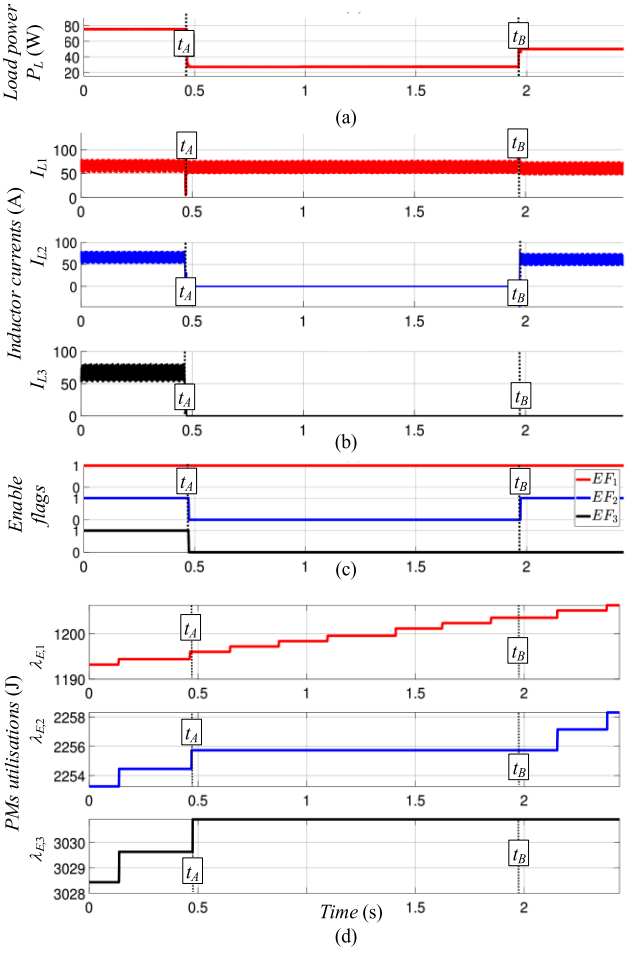

FIGURE 14. A detailed view of PDM response based on assessed $\lambda_{E,n}$ and symmetrical load distribution: (a) power load profile, (b) inductor currents, (c) enable flags, (d) legs' utilization.

re-activates the second leg of the converter as its utilization factor $\lambda_{E,2}$ is smaller than $\lambda_{E,3}$. The third leg remains inactive, indicated by cleared status EF_3. In addition, following the target goal, both load factors, i.e., inductor currents, are refreshed to a new equal steady-state value.

B. AGING CONTROL BASED ON ASSESSED $\lambda_{I,N}$ AND ASYMMETRICAL LOAD DISTRIBUTION

The asymmetrical load distribution splits the reference current unevenly among the active legs of the converter. This division is achieved through the power distribution routine, which manipulates the load factors described in Section III-C. In contrast to the approach in Section V-A, the distribution in this section is controlled according to the PMs' current-related utilization factors ($\lambda_{I,n}$).

According to the power level in Fig. 15-a, the PDM keeps all legs active, imposing different load factors ($k_{ID,n}$) to each individual current loop (Fig. 15-b). The first leg, the one with the smallest utilization ($\lambda_{I,1}$), operates with the highest load factor, i.e., the inductor current, while the third delivers the smallest portion of power to the load. Their load factors are thus calculated according to the (10), (13), and (14),

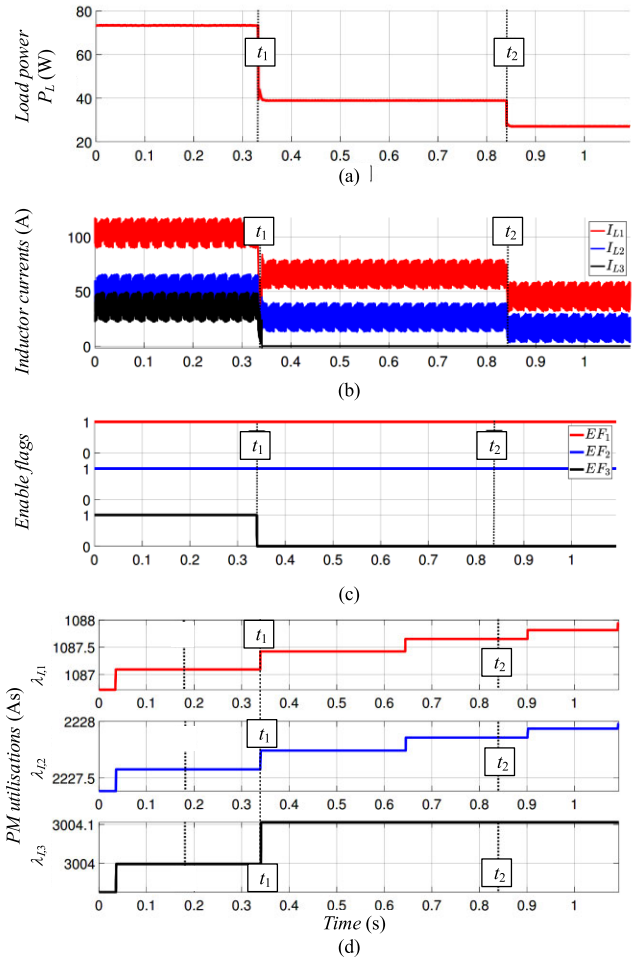

FIGURE 15. A detailed view of PDM response based on assessed $\lambda_{I,n}$ and asymmetrical load distribution: (a) power load profile, (b) inductor currents, (c) enable flags, (d) legs' utilization.

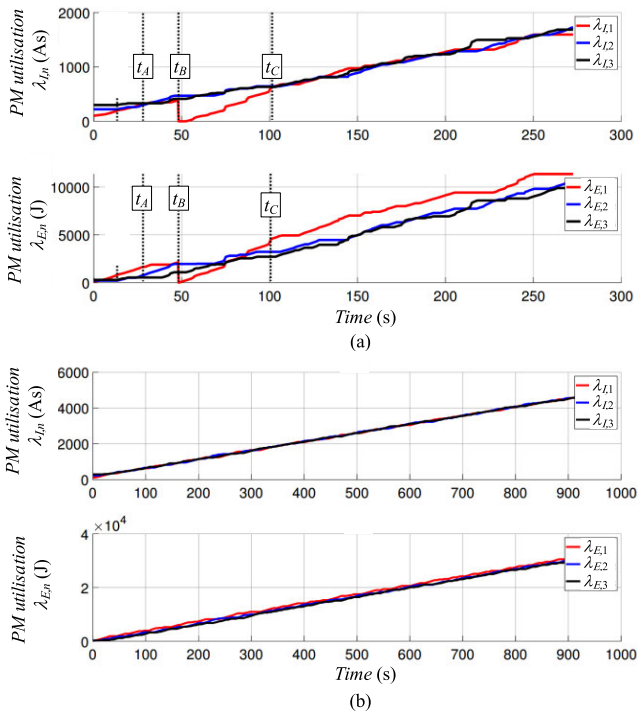

FIGURE 16. Comparison of utilizations achieved with $\lambda_{I,n}$ implementation in the controller: (a) shorter versus (b) longer simulation interval.

assuming $n = 3$. During the simulation, the minimum current distribution coefficient $k_{ID,M}$ was set to 0.2, and the saturated utilization difference $\Delta\lambda_{Sat}$ was set to 2000 As.

The load factors ($k_{ID,n}$) remain the same until t_1 when the load rapidly decreases. At the same time, the CSS clears the enable flag EF_3 for the third leg (Fig. 15-e) to ensure the superior efficiency of the converter. Additionally, CSS determines new values of $k_{ID,n}$. The $k_{ID,2}$ for the most utilized active leg, is determined using (10). The $k_{ID,1}$ of the smallest utilized active leg, is calculated as 1- $k_{ID,2}$.

A broader insight into the control algorithm (Fig. 16) presents a comparison of the control efficiency implemented with $\lambda_{I,n}$ during two different simulation intervals, considering both the current-related utilization ($\lambda_{I,n}$) and the energy-related utilization ($\lambda_{E,n}$). The test was conducted using the same load profile as in the scenario seen in Fig. 13. At the beginning of the simulation (Fig. 16-a), the CSS activates all legs but assigns different load factors ($k_{ID,n}$) to each individual current loop. The first leg, the one with the smallest utilization, operates with the highest load factor, i.e., the inductor current, while the third delivers the smallest portion of power to the load. Consequently, due to substantial differences in power losses across PMs, the energy-related ($\lambda_{E,n}$) utilization factors diverge at a different rate. Although the current-related utilization factors ($\lambda_{I,n}$) are appropriately matched between t_A and t_B, the energy-related factors continue to diverge.

At time t_B, the $\lambda_{I,1}$ and $\lambda_{E,1}$ are intentionally changed to zero to examine the PDM's response. The CSS promptly responds to this change by assigning the highest load factor to the first leg $\lambda_{I,1}$, successfully causing the $\lambda_{I,n}$ to converge again at t_C. The difference that occurs at that moment between $\lambda_{E,1}$ and the other two energy-related ($\lambda_{E,n}$) factors persist continuously, but it does not increase even when the system is exposed to a longer testing interval, as demonstrated in Fig. 16-b.

The results in Fig. 17 provide further insight into the operation of the control algorithm based on $\lambda_{E,n}$ with different load distributions applied, emphasizing the response triggered by an intentional change in utilization. The figure shows how the individual PM's energy dissipation ($\lambda_{E,n}$) accumulates during a test interval in the case of asymmetric and symmetric load distribution. The initial values of PMs energy dissipation $\lambda_{E,n}$ are at the beginning set at the same values as they were applied in Fig. 13. At instant t_1, after all $\lambda_{E,n}$ have converged, the $\lambda_{E,1}$ is manually set to zero. The time interval ($t_1 \rightarrow t_2$) required for the dissipation of the legs to match again is approximately 608 s in the case of asymmetric load distribution (Fig. 17-b). Comparing this response with the symmetrical one reveals that the latter requires more time to attain balanced operation.

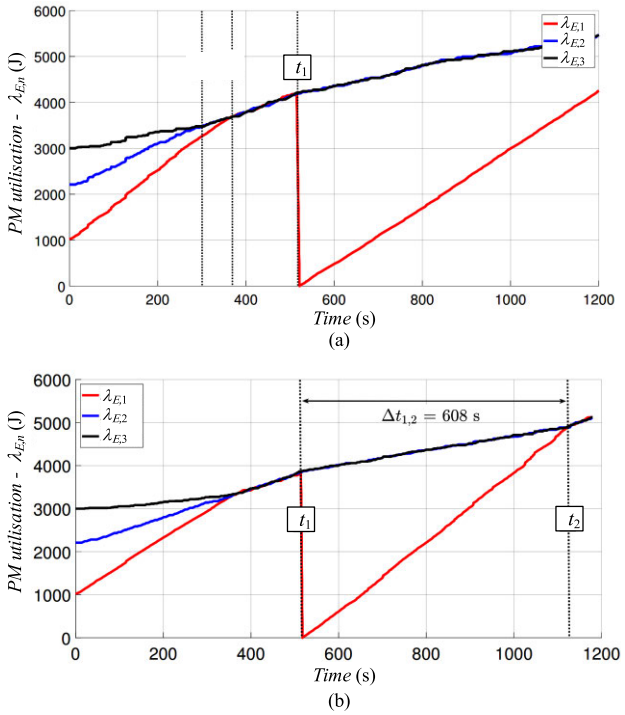

FIGURE 17. PDM response based on $\lambda_{E,n}$ control implementation combined with: (a) symmetrical versus (b) asymmetrical load distribution.

C. DISCUSSION

It can be easily deduced that implementing PM lifetime control based on ($\lambda_{E,n}$) consumes more processing time and requires more effort than ($\lambda_{I,n}$) in the initial stage. Namely, building the ETM model requires deriving PM parameters and considering their temperature and voltage dependence for the MCU implementation beforehand. Additionally, determining the thermal boundary condition relies on estimating the distribution of losses between switches in the PM.

When using the current utilization ($\lambda_{I,n}$) as the control parameter (selected with the switch in Fig. 5) combined with the asymmetrical load distribution, the comparison in Fig. 16 reveals that achieving balanced PM stress evaluated by $\lambda_{E,n}$ poses a challenge. Nevertheless, it remains feasible if the PM imbalance is acceptable and causes no premature failure. This imbalance is assumed to be particularly undesirable when discrete switch components with the same number of temperature sensors (T_C) in a larger layout are used instead of PMs, leading to potentially larger discrepancies in $\lambda_{E,n}$.

However, when using the energy utilization ($\lambda_{E,n}$) as the control parameter, both utilization factors converge similarly under symmetrical and asymmetrical load distribution scenarios, as shown in Fig. 17. Notably, the converged value of $\lambda_{E,n}$ is smaller with asymmetric load distribution, indicating less energy dissipation in the converter overall. This finding contradicts the misleading assumption that prioritizing operation with the highest possible efficiency in all active legs simultaneously, i.e., attaining symmetric load sharing, automatically guarantees optimal energy conversion in the whole. On the contrary, asymmetrical load operation proves to be preferable in terms of efficiency and achieving a balanced PM lifespan. Moreover, asymmetrical load distribution enables quicker equalization of PM utilization after sudden changes, such as replacing a damaged power module, potentially leading to more efficient and stable operation.

Although the results were obtained with constant thermal model coefficients for all three PMs, their practicality is still validated through successful convergence of the control algorithms during HiL testing, even when utilization indicators are deliberately changed. However, accounting for the temperature dependence of PMs in the thermal model could further refine the accuracy of the control algorithms.

VI. CONCLUSION

In this paper, we propose a superior approach to assess the efficacy of the aging controller by using cumulative indicators. This departure from the conventional validation, which relies on measuring temperature differences between case or junction temperatures of power modules as commonly done in previous studies, introduces significant enhancements. Notably, these improvements can be implemented with minimal adjustments to the conventional solution [14], [34].

Although this paper does not present experimental results on the physical hardware, we believe the HiL-based comparison of proposed cumulative indicators and their control implementation is illustrative enough to contribute to further research in this field. It aims to identify the most descriptive indicator suitable for interleaved converters, particularly in cases where the device's temperature fails to provide a strong indication during extended intervals when individual phases are idle.

We hope this and future investigations will provide more accurate and informative indicators to assess the aging of power modules in interleaved converters, ultimately leading to improved control strategies and enhanced performance in practical applications.

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