IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 13 August 2023, accepted 1 September 2023, date of publication 4 September 2023,
date of current version 13 September 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3312016

RESEARCH ARTICLE

Impact of Displacement Defect Owing to Cosmic Rays on Three-Nanometer-Node Nanosheet FET 6T Static Random Access Memory

JONGHYEON HA[1], MINJI BANG[1], GYEONGYEOP LEE[1], MINKI SUH[1], CHONG-EUN KIM[2], (Member, IEEE), AND JUNGSIK KIM[1], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Gyeongsang National University (GNU), Jinju 52828, Republic of Korea
[2]Department of Railroad Electrical and Electronic Engineering, Korea National University of Transportation, Uiwang 16106, Republic of Korea

Corresponding authors: Jungsik Kim (jungsik@gnu.ac.kr) and Chong-Eun Kim (cekim@ut.ac.kr)

This work was supported in part by the Electronic Design Automation (EDA) Tool Program of the IC Design Education Center (IDEC); in part by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (Ministry of Science and ICT (MSIT)), Republic of Korea, under Grant 2020R1Gs1A1099554; and in part by the "Leaders in INdustry-university Cooperation 3.0" Project funded by the Ministry of Education and National Research Foundation (NRF) of Korea.

ABSTRACT In this work, the effect of displacement defect (DD) owing to cosmic rays on six-transistor (6T) static random access memory (SRAM) with a 3 nm node nanosheet field-effect transistor (NSFET) is investigated using technology computer-aided design (TCAD) simulation. In order to comprehensively study the uncertainty of the radiation of NSFET 6T SRAM, the shape of the DD cluster cross-section and the transistor damaged by the DD in 6T SRAM are considered. Read static noise margin (RSNM) degradation (19 %) is the highest when the rectangular cross-section of the DD cluster (rectangular-DD cluster) is located in the pull-down1 (PD1) transistor. To mitigate the rectangular-DD cluster damage, we studied the variation in the DD cluster influence on the sheet shape and the source/drain (S/D) overlap length fluctuation. The sheet shape resulted in 2.3 % lower RSNM degradation in NS compared with nanowire (NW). Under the worst conditions (PD1 transistor damaged rectangular-DD cluster, NW structure), the S/D underlap structure showed 3.7 % lower RSNM degradation than the S/D overlap structure.

INDEX TERMS Displacement defect (DD), radiation effects, reliability, nanosheet FET (NSFET), static random access memory (SRAM), technology computer-aided design simulation (TCAD).

I. INTRODUCTION

Static random access memory (SRAM), which acts as a cache between the CPU and memory, has evolved alongside CPU development technology. Logic field-effect transistor (FET) such as FinFET is aggressively scaled down for large cache memory capacity and fast operation speed. A nanosheet FET (NSFET) was developed to replace the FinFET, which reached the scaling-down limit. NSFET, which consists of a surrounding gate, has higher gate controllability than FinFET. As a result, NSFET strongly suppresses the short-channel effect (SCE) compared with FinFET [1], [2], [3]. Although NSFET has the advantage such as high integration rate in a limited cell area, various issues remain. These issues included device process-related problems (such as point defects owing to ion implantation) and neutrons of cosmic rays that cause displacement defect (DD) in silicon [4], [5], [6], [7], [8]. The critical point at which a DD occurs in silicon is 50 keV. For example, when a silicon die of 1 cm^2 cross-section was exposed at sea level in New York, one event rate of DD occurred after 21 days [9], [10], [11]. One DD event is negligible for the bulk planar MOSFET. However, the aggressively decreased channel volume became comparable to the DD, and the DD effect is inescapable. The DD creates a recombination and trapping center within the silicon energy bandgap. The recombination center induced to recombine the minority carrier, and the trapping center captured the majority carrier [12], [13]. Owing to the carrier-trapping mechanism,

The associate editor coordinating the review of this manuscript and approving it for publication was Jiajie Fan.

TABLE 1. NSFET 6T SRAM geometry and doping parameters.

Symbol	Quantity	Value
L_g	Physical gate length	12 nm
L_{eff}	Effective gate length	12 nm
CPP	Contact poly pitch	48 nm
W_{sheet}	Sheet width	20 nm
T_{sheet}	Sheet Thickness	5 nm
L_{sp}	Spacer length	8 nm
$L_{overlap}$	Overlap distance of the source and drain doping in the channel	0 nm
EOT	Equivalent oxide thickness	1.4 nm
N_{sd}	Doping concentration of source and drain	1×10^{20} cm^{-3}
N_{ch}	Doping concentration of the channel	1×10^{15} cm^{-3}
N_{body}	Doping concentration of body	1×10^{18} cm^{-3}
WFn	Gate metal work function in the NMOS	4.51 eV
WFp	Gate metal work function in the PMOS	4.76 eV

the channel resistance increased, the carrier transfer characteristics and the current degraded. Cosmic rays cause single event transient (SET) and total ionizing dose (TID) effects, excluding DD. SET, induced by alpha-particle penetration, generates electron-hole pair (EHP) in the channel and substrate of the semiconductor. Carriers of EHP transport to drain region due to drain bias. An unexpected overcurrent in the logic device leads to a data flip of the device [14], [15]. TID effect by gamma rays occurs interface trap and oxide trap in the SiO_2. Both traps reduce SiO_2 quality, decreasing gate controllability and generating leakage current in the channel and shallow trench isolation (STI) regions. Consequently, the TID effect degrades electrical characteristics such as I_{on}, I_{off}, V_{th}, and SS. Unlike the TID and SET, DD caused permanent damage [16], [17]. Therefore, it is necessary to identify the device structure that is the most sensitive to radiation, and to fabricate a device structure that can minimize the effect of radiation.

In this study, we studied the degradation of the electrical characteristics (I_{on}, I_{off}, and static noise margin (SNM)) of NSFET six-transistor (6T) SRAM according to variations in the shape (square and rectangular) of the DD cluster cross-section and fluctuation of the transistors damaged by DD in SRAM (pass-gate1 (PG1), pull-down1 (PD1), pull-up1 (PU1), PG1 with PG2 (PG1-2), PD1 with PD2 (PD1-2), and PU1 with PU2 (PU1-2)). In addition, we analyzed the degradation tendency when the sheet shape and source/drain (S/D) doping overlap ($L_{overlap}$), which is the length of the overlapped S/D doping at between the nitride (spacer) and gate, fluctuated under the worst DD conditions.

II. SIMULATION AND MODELING METHODOLOGY

The Synopsys technology computer-aided design (TCAD) tool was used to simulate NSFET 6T SRAM (**Fig. 1**) [18]. In the device structure, NSFET collocated a certain distance (0.031 μm^2). Geometry (L_g, L_{eff},CPP, W_{sheet}, T_{sheet}, L_{sp}, $L_{overlap}$,and EOT), and the doping (N_{sd}, N_{ch},and N_{body}) parameters were fitted in accordance with those of a previous study [1]. The sub-band of silicon is discontinuous in the channel owing to device scale-down. In order to describe quantum confinement of the inversion and transportation of carriers in the sub-band, a modified local density approximation (MLDA) model was used [19], [20], [21]. Auger recombination models, a Shockley–Read–Hall model with doping dependence, and Hurkx band-to-band tunneling were adopted to consider gate-induced drain leakage (GIDL) in the short channel [22], [23], [24]. Inversion and accumulation layer mobility (IALMob) was used to consider carrier mobility model in the inversion layer of channel and accumulation region of source/drain (S/D) doping extension [22]. The I_d-V_g curve of **Fig. 2** was calibrated to approximate the reference measurement using the device's geometry, doping parameters (Table 1), and fitted simulation physics model.

Primary knock-on atom (PKA), a displaced silicon atom by the neutron, knocked out the silicon atom while penetrating the silicon die, creating vacancies and interstitials. A high density of vacancies and interstitials formed where PKA passed, creating a DD cluster. In this research, the DD cluster was set as cuboid by referring to other research references [11], [17], [25], [26]. The DD cluster used the acceptor-like trap energy level at $E_c - 0.4$ eV in NMOS and the donor-like trap energy level at $E_v + 0.2$ eV in PMOS [27], [28]. The position of the DD cluster in the X, Y, and Z directions is at the top of the sheet (**Fig. 1 (a)**, middle of the channel (**Fig. 1 (b)**, channel of the top sheet), and center of sheet (**Fig. 1 (c)**, channel of the top sheet), respectively, for the worst on-current degradation due to the DD cluster [11], [29]. Two types of cuboid DD clusters had the following structure, i.e., those with a rectangular cross-section (XZ plane, 9 nm length (L_g direction), 10 nm width (W_{sheet} direction), and 4 nm height (T_{sheet} direction)), and those with a square cross-section (XZ plane, 9 nm length, 5 nm width, and 5 nm height). The degradation of the electrical characteristics is expressed as follows: (|I_{on} (I_{off} or SNM) of the degraded device – I_{on} (I_{off} or SNM) of virgin device|)/ I_{on} (I_{off} or SNM) of virgin device $\times$ 100.

III. RESULT AND DISCUSSION

Fig. 3 shows the current degradation owing to the change in the cross-sectional area of the DD cluster in the PG1, PD1, and PU1 transistors of the NSFET 6T SRAM. In **Fig. 4**, the cross-sectional area of the DD cluster is either rectangular (rectangular-DD) or square (square-DD). In the PG1, PD1, and PU1 transistors, the rectangular-DD cluster causes a larger on-current reduction than the square-DD cluster. The rectangular-DD cluster occupies a wider high-electron-density profile ($>1 \times 10^{18}$/cm^3) of the NS channel cross-section (**Fig. 4**) than the square-DD cluster. Therefore, the charge captured by the rectangular-DD cluster was larger than that captured by the square-DD cluster. This means that the electron density in the channel is lower, and the

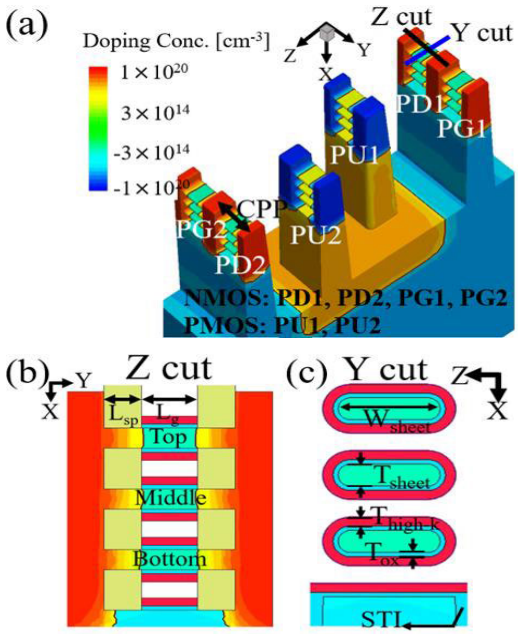

FIGURE 1. (a) Structure of NSFET 6T SRAM. (b) X-Y cross-section of NMOS at the Z-cut. (c) X-Z cross-section of NMOS at the Y-cut.

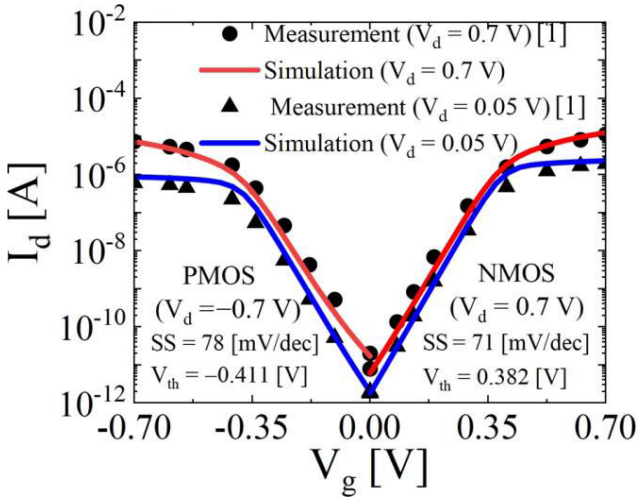

FIGURE 2. Simulated I_d–V_g transfer characteristics at V_d = 0.05 V and 0.7 V compared with measurement data.

channel resistance is higher for the rectangular-DD cluster than for the square-DD cluster. Furthermore, the mobility of the free carrier in the channel is reduced compared with that of the square-DD cluster because the rectangular-DD cluster contains more fixed charges. Consequently, the on-current is further degraded in the rectangular-DD cluster.

When DD is generated in the channel, the gate-induced drain leakage (GIDL) effect induces a high off-leakage current [28]. However, when a trapping center forms in the channel of the control device (NSFET 6T SRAM), it is difficult to tunnel the carrier on the source side through the trapping center owing to the undoped channel and low-density drain (LDD). Therefore, the off-currents of PG1, PD1, and PU1 are diminished by DD [11].

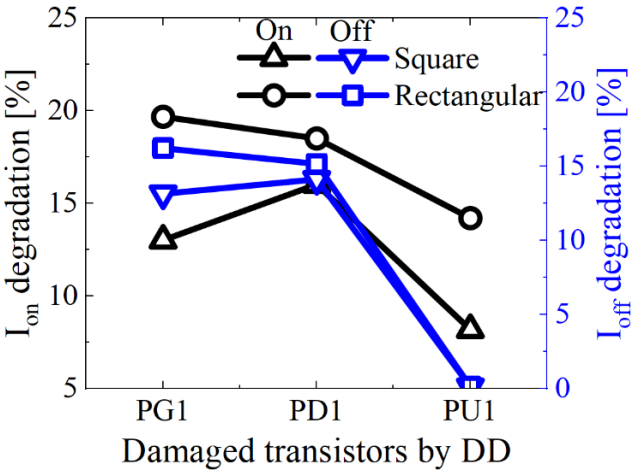

FIGURE 3. Current degradation of on and off state in the PG1, PD1, and PU1 damaged by DD cluster in the NSFET 6T SRAM transistors.

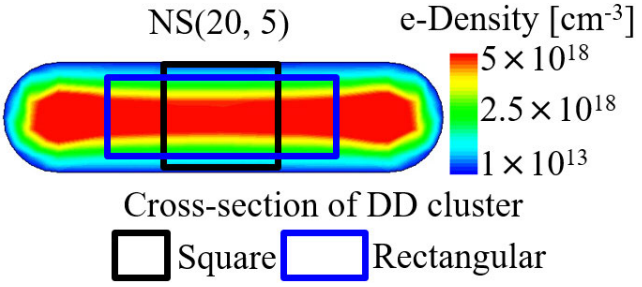

FIGURE 4. Electron density profile of NS shape (Y cut of Fig. 1 (a)) with different DD cluster cross-sections (square and rectangular).

Unlike PG1 and PD1, PU1 shows less than 1 % off-current degradation. For PU1, the Fermi level of the channel is above the DD's trap energy level (donor-like trap, E_v+ 0.2 eV) in the off-gate bias. This means that the carrier is not completely filled in the trapping center [11]. Consequently, the off-current degradation of the donor-like trap, which has a shallow trap-energy level, was even lower than that of the acceptor-like trap, which has a deep trap-energy level.

Fig. 5 (a) shows the extent to which the ability of the SNM of the SRAM to read and write operations is degraded by transistors damaged by the rectangular-DD cluster. In the read operation, when the PD1 transistor is damaged (PD1 transistor condition), the rate of the largest reduction in the read SNM (RSNM (19 %)) occurs. The read operation is sensitive to external noise because the sensing amplifier measures a tiny voltage difference between the bit-line (BL) and bit-line-bar (BLB) in **Fig. 5 (c)**. Activating the WL in the read operation, the voltage of the internal storage node (V_{out}) is slightly increased from zero by the voltage division between the PG1 and PD1 transistors. When V_{out} increases close to the critical voltage of the adjacent PD2 transistor (V_{th} of PD2 transistor), the SRAM has a higher probability of reversing the state, leading to the failure of the read operation. To prevent a sufficient external noise margin and voltage rise of the V_{out} node, a high drive current is required of the PD transistors compared with that of

the PG transistors. The RSNM, proportional to the β-ratio, increases when the I_{PD} transistor is higher than I_{PG}. In the PD1 transistor condition, a higher RSNM reduction occurred than in the other transistors. **Fig. 5 (b)** and **Fig. 5 (c)** illustrate the reduction in the RSNM in detail. The butterfly curve in **Fig. 5 (b)** shows the combined VTC curves for the left and right inverters. The colors indicate the conditions of the transistor damaged by the rectangular-DD cluster. The filled and open symbols of the VTC curve indicate flipping of the left and right inverters, respectively. An RSNM was extracted from the closed butterfly curve after $V_{in} =$ 0.35 V was applied. In the PD1 transistor condition shown in **Fig. 5 (b)**, the VTC curve of the left inverter (FlipL) overlaps with the no-DD condition. However, the VTC of the right inverter (FlipR) generates a higher V_{out} after $V_{in} =$ 0.35 V than that observed in the no-DD case. WL, V_{in}, BL, and BLB were applied at 0.7 V to determine the process of the flipped inverters, as shown in **Fig. 5 (c)**. When V_{in} is 0.7 V, V_{out} increases owing to the reduction of I_{PD1} by the rectangular-DD cluster. In the range from 0.35 V to 0.7 V, V_{out} is maintained higher than the no-DD condition. The FlipR of the PD1 transistor shifts positively until the gate voltage of PD1 decreases below 0.35 V. The RSNM of the PD1 transistor condition is lower than the no-DD butterfly curve beyond $V_{in} = 0.35$ V. In the PD1-2 transistor condition, the RSNM reduction was 7 % lower than in the PD1 transistor condition. The FlipL of the PD1-2 transistor condition moves in a positive direction at a high voltage of V_{out}, similar to the FlipR of the PD1 transistor condition. The FlipL and FlipR curves of the PD1-2 transistor condition moved in both directions. Only FlipR moves in a positive direction under the PD1 transistor conditions, resulting in an imbalance in the trip point. However, less mismatch occurred under the PD1-2 transistor condition than under the PD1 transistor condition, resulting in a lower RSNM reduction than under the PD1 transistor condition. In the PG transistor conditions, the β-ratio (I_{PD}/I_{PG}) increases because the rectangular-DD cluster degrades the I_{PG}, and the voltage of the V_{out} or V_{in} node decreases compared with the no-trap condition. Then, the RSNM increased with increasing β-ratio. However, the speed of the read operation was reduced. Since PU transistors do not directly affect the RSNM, an RSNM reduction of approximately 1 % occurs.

The write operation shows the highest write SNM (WSNM) decrease (0.28 %) in the PG1 transistor (**Fig. 5 (a)**). **Fig. 5 (d)** shows that the write operation activates WL, applies 0 V to BLB and 0.7 V to BL, sends a "0" signal to the V_{in} node and a "1" signal to the V_{out} node, and writes the data "1" to SRAM. When applying a signal to a node and flipping the data, the I_{PG} is stronger than the I_{PU}. This implies that the WSNM proportional to the γ-ratio (I_{PG}/I_{PU}) increases when the I_{PG} is higher than the I_{PU}. Consequently, the PG1 transistor condition exerts a greater influence on the WSNM than the other conditions. However, because the primary function of the write operation is to change the voltage state of the storage node (V_{in} or V_{out}), the circuit is designed to overcome slight changes in the voltage level and set an accurate voltage at the storage node. The WSNM reduction was less than 1 %.

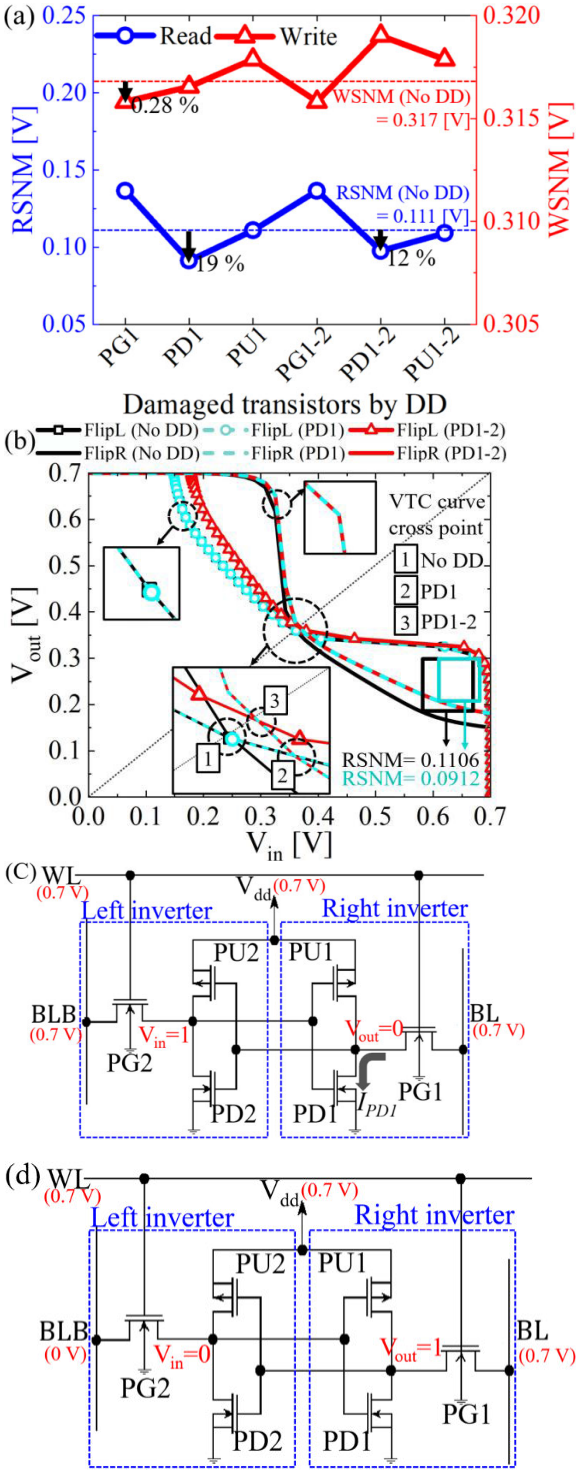

FIGURE 5. (a) In the NS structure, the rate of the read and write static noise margin (RSNM and WSNM) degradation by the single transistor (PD1, PG1, PU1) and coupled transistor (PD1-2, PG1-2, PU1-2) at the location of the rectangular-DD cluster. (b) Butterfly curves (Flip-R and Flip-L) in damaged PD1 (cyan line) and PD1-2 (red line) transistors, and no-DD (black line) conditions. (c) Reading and (d) writing operation under the worst-case conditions in which the rectangular-DD cluster is generated in the PD1 and PG1 transistor.

RSNM degradation has a fatal effect on the read operations. To minimize RSNM degradation in environments where radiation damage is unavoidable, it is important to develop device structures that are insensitive to DD effects. Therefore, the rectangular-DD cluster impact variation owing to sheet shape and S/D doping overlap length fluctuations were analyzed under the worst DD conditions (rectangular-DD cluster in the PD1 transistor).

Fig. 6 (a) and **Fig. 6 (b)** show the on-current and RSNM degradation owing to the rectangular-DD cluster in the FinFET, NS, and nanowire (NW) structures. The rectangular DD cluster of the FinFET, which is calibrated 10 nm node technology FinFET [30], is equal to the total volume of the rectangular DD cluster of the NS and is located at the top of the Fin and PD1 transistor. NS had 2 % and 6 % lower on-current and RSNM degradation than FinFET. Because the NS, unlike the FinFET, has a GAA structure that suppresses the rise in the conduction energy band caused by the DD cluster, reducing the impact of the DD cluster. NS exhibits 6.6 % and 2.5 % lower degradation than NW in terms of the current and RSNM, respectively. In the channel cross-section of the NS, the proportion of rectangular-DD cluster occupying the sheet-width direction of the NS was 30 % lower than the NW. The ratio of rectangular-DD cluster occupying the channel cross-sectional area of the NS and NW in the sheet-width direction is as follows: NS condition (10 nm of rectangular-DD cluster width / 20 nm of NS width $\times$ 100 $=$ 50 %) and NW condition (10 nm of rectangular-DD cluster width / 12.5 nm of NW width $\times$ 100 $=$ 80 %). This means that the influence of the fixed charge on the carrier is reduced because the space for electrons to move to the side of the rectangular-DD cluster in the NS is larger than in the NW. On the other hand, the rectangular-DD cluster accounted for the majority of the NW channel cross-sectional area. Thus, the fixed charge of the rectangular-DD cluster further reduces the carrier mobility in the NW channel.

We analyzed the variation in the impact of the rectangular-DD cluster by varying the S/D overlap on the NW structure with the worst DD conditions. Based on the control device ($L_{overlap} = 0$ nm), an overlap device ($L_{overlap} = 2$ nm) and an underlap device ($L_{overlap} = -2$ nm), as shown in **Fig. 6 (c)**, were produced. **Fig. 6 (a)** and **Fig. 6 (b)** reveal that the underlap structure undergoes less degradation in the device's electrical characteristics than the overlap structure owing to the rectangular-DD cluster. As the effective gate length of the underlap is longer than the physical gate length, the underlap has less SCE influence than the overlap and effectively controls the influence of the rectangular-DD cluster. The effect variation of the rectangular-DD cluster owing to the $L_{overlap}$ fluctuation can be more specifically determined through the channel's conduction band modulation by the gate field shown in **Fig. 6 (d)**. The gate electric field strongly suppresses the channel conduction band raised by the rectangular-DD cluster in the underlap. However, the overlap structure has a stronger SCE effect than the underlap structure, reducing the influence of the gate electrical field.

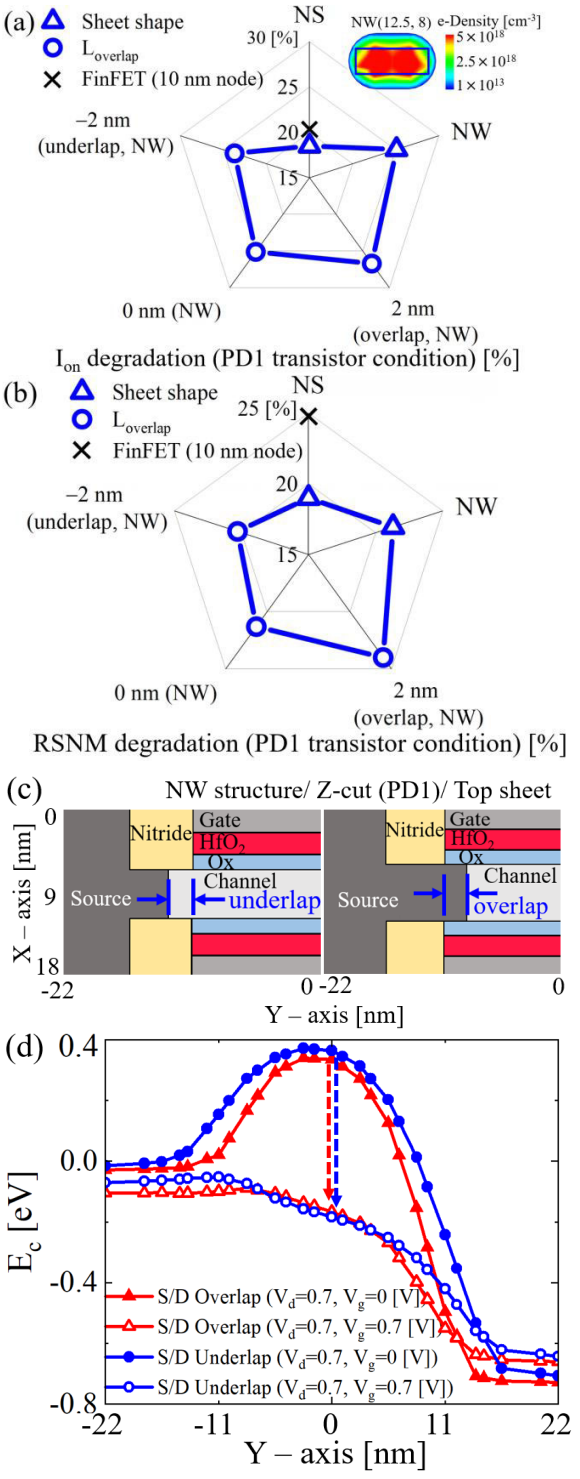

FIGURE 6. (a) Comparison of on-current and (b) RSNM degradation of NS, NW, FinFET, and $L_{overlap}$ variation under PD1 transistor condition (description of NW's electron profile in the upper left of Fig. 6(a)). (c) Illustration of underlap and overlap in the top sheet X-Y cross-sectional area of NWFET. (d) Conduction band at 2 nm and –2 nm of $L_{overlap}$ (off state ($V_d = 0.7$ [V], $V_g = 0$ [V]), and on state ($V_d = V_g = 0.7$ [V])).

Consequently, the underlap structure undergoes 2 % current deterioration and 3.7 % RSNM deterioration compared with the overlap structure.

IV. CONCLUSION

In this study, we explored the variation in the DD effect of various device geometries in NSFET 6T SRAM. When the cross-section of the DD cluster is rectangular, the on-current degradation is higher than that of the square cross-section. The region where the rectangular-DD cluster occupies the NS's high electron density is wider than the square-DD cluster, so the impact of the rectangular-DD cluster on the devices increased. The RSNM is proportional to the cell ratio of I_{PD1}/I_{PG1}, degraded the most when the rectangular-DD cluster damaged PD1 transistors. Owing to the further mismatch of the butterfly curve in the PD1 transistor condition than in the PD1-2 transistor condition, the PD1 transistor condition led to higher RSNM degradation than the PD1-2 transistor condition. We varied the sheet shape and $L_{overlap}$ to determine how to minimize SRAM SNM degradation in the worst DD conditions (i.e., rectangular-DD cluster and PD1 transistor damaged). In NS, lower on-current and RSNM degradation occur compared with NW, in which most of the high-electron-density area is occupied. When $L_{overlap}$ is decreased, the SCE effect in the channel is weaker than the overlap structure, and the energy barrier of the channel raised by the rectangular-DD is effectively suppressed through the gate bias field. Consequently, I_{on} and RSNM degradation in the S/D underlap device were lower than the S/D overlap device. Therefore, to enhance immunity to DD, NS structure with S/D underlap structure is excellent.

REFERENCES

[1] N. Loubet, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T230–T231, doi: 10.23919/VLSIT.2017.7998183.

[2] S.-D. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M.-H. Na, "Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2015, pp. 1–3, doi: 10.1109/S3S.2015.7333521.

[3] D. Jang, D. Yakimets, G. Eneman, P. Schuddinck, M. G. Bardon, P. Raghavan, A. Spessot, D. Verkest, and A. Mocuta, "Device exploration of NanoSheet transistors for sub-7-nm technology node," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2707–2713, Jun. 2017, doi: 10.1109/TED.2017.2695455.

[4] H.-J.-L. Gossmann, A. Agarwal, T. Parrill, L. M. Rubin, and J. M. Poate, "On the FinFET extension implant energy," *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 285–290, Dec. 2003, doi: 10.1109/TNANO.2003.820783.

[5] T. B. Hook, J. Brown, P. Cottrell, E. Adler, D. Hoyniak, J. Johnson, and R. Mann, "Lateral ion implant straggle and mask proximity effect," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1946–1951, Sep. 2003, doi: 10.1109/TED.2003.815371.

[6] A. Nylandsted Larsen, "Epitaxial growth of Ge and SiGe on Si substrates," *Mater. Sci. Semicond. Process.*, vol. 9, nos. 4–5, pp. 454–459, Aug. 2006, doi: 10.1016/j.mssp.2006.08.039.

[7] T. David, J.-N. Aqua, K. Liu, L. Favre, A. Ronda, M. Abbarchi, J.-B. Claude, and I. Berbezier, "New strategies for producing defect free SiGe strained nanolayers," *Sci. Rep.*, vol. 8, no. 1, p. 2891, Feb. 2018, doi: 10.1038/s41598-018-21299-9.

[8] J. R. Srour, C. J. Marshall, and P. W. Marshall, "Review of displacement damage effects in silicon devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, 612, pp. 653-670, Jun. 2003.

[9] V. A. J. van Lint, R. E. Leadon, and J. F. Colwell, "Energy dependence of displacement effects in semiconductors," *IEEE Trans. Nucl. Sci.*, vol. NS-19, no. 6, pp. 181–185, Dec. 1972.

[10] J. Ziegler and W. Lanford, "The effect of sea level cosmic rays on electronic devices," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 23, Feb. 1980, pp. 70–71, doi: 10.1109/ISSCC.1980.1156060.

[11] J. Kim, J.-S. Lee, J.-W. Han, and M. Meyyappan, "Caution: Abnormal variability due to terrestrial cosmic rays in scaled-down FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1887–1891, Apr. 2019, doi: 10.1109/TED.2019.2899056.

[12] A. N. Larsen, A. Mesli, K. B. Nielsen, H. K. Nielsen, L. Dobaczewski, J. Adey, R. Jones, D. W. Palmer, P. R. Briddon, and S. Öberg, "ECenter in silicon has a donor level in the band gap," *Phys. Rev. Lett.*, vol. 97, no. 10, Sep. 2006, Art. no. 106402.

[13] J. Adey, R. Jones, D. W. Palmer, P. R. Briddon, and S. Öberg, "Theory of boron-vacancy complexes in silicon," *Phys. Rev. B, Condens. Matter*, vol. 71, no. 16, Apr. 2005, Art. no. 165211, doi: 10.1103/PhysRevB.71.165211.

[14] J. Kim, J.-S. Lee, J.-W. Han, and M. Meyyappan, "Single-event transient in FinFETs and nanosheet FETs," *IEEE Electron Device Lett.*, vol. 39, no. 12, pp. 1840–1843, Dec. 2018, doi: 10.1109/LED.2018.2877882.

[15] J.-W. Han, J. Kim, D.-I. Moon, J.-S. Lee, and M. Meyyappan, "Soft error in saddle fin based DRAM," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 494–497, Apr. 2019, doi: 10.1109/LED.2019.2897685.

[16] T. D. Haeffner, R. F. Keller, R. Jiang, B. D. Sierawski, M. W. Mccurdy, E. X. Zhang, R. W. Mohammed, D. R. Ball, M. L. Alles, R. A. Reed, R. D. Schrimpf, and D. M. Fleetwood, "Comparison of total-ionizing-dose effects in bulk and SOI FinFETs at 90 and 295 k," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 6, pp. 911–917, Jun. 2019.

[17] M. G. Esposito, J. E. Manuel, A. Privat, T. P. Xiao, D. Garland, E. Bielejec, G. Vizkelethy, J. Dickerson, J. Brunhaver, A. A. Talin, D. Ashby, M. P. King, H. Barnaby, M. Mclain, and M. J. Marinella, "Investigating heavy-ion effects on 14-nm process FinFETs: Displacement damage versus total ionizing dose," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 724–732, May 2021.

[18] *Sentaurus Device User Guide, Version N-2017.09*, Synopsys, San Jose, CA, USA, 2017.

[19] V. Moroz, J. Huang, and R. Arghavani, "Transistor design for 5nm and beyond: Slowing down electrons to speed up transistors," in *Proc. 17th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2016, pp. 278–283, doi: 10.1109/ISQED.2016.7479214.

[20] L. Smith, M. Choi, M. Frey, V. Moroz, A. Ziegler, and M. Luisier, "FinFET to nanowire transition at 5nm design rules," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices (SISPAD)*, Sep. 2015, pp. 254–257.

[21] M. Choi, V. Moroz, L. Smith, and J. Huang, "Extending drift-diffusion paradigm into the era of FinFETs and nanowires," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices (SISPAD)*, Sep. 2015, pp. 242–245.

[22] J.-W. Han, H. Y. Wong, D.-I. Moon, N. Braga, and M. Meyyappan, "Stringer gate FinFET on bulk substrate," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3432–3438, Sep. 2016, doi: 10.1109/TED.2016.2586607.

[23] J. Kim, J.-W. Han, and M. Meyyappan, "Reduction of variability in junctionless and inversion-mode FinFETs by stringer gate structure," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 470–475, Feb. 2018, doi: 10.1109/TED.2017.2786238.

[24] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992, doi: 10.1109/16.121690.

[25] F. Häonniger, "Radiation damage in silicon," Ph.D. dissertation, Dept. Phys., Univ. Hamburg, Hamburg, Germany, 2007.

[26] J. R. Srour and J. W. Palko, "Displacement damage effects in irradiated semiconductor devices," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1740–1766, Jun. 2013.

[27] G. D. Watkins, "Intrinsic defects in silicon," *Mater. Sci. Semiconduct. Process.*, vol. 3, no. 1, pp. 227–235, 2000, doi: 10.1016/S1369-8001(00)00037-8.

[28] J. Kim, J.-W. Han, and M. Meyyappan, "The impact of a single displacement defect on tunneling field-effect transistors," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4765–4769, Nov. 2020, doi: 10.1109/TED.2020.3022004.

[29] S.-G. Jung, J.-K. Kim, and H.-Y. Yu, "Analytical model of contact resistance in vertically stacked nanosheet FETs for sub-3-nm technology node," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 930–935, Mar. 2022, doi: 10.1109/TED.2022.3143473.

[30] C. Auth, "A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects," in *IEDM Tech. Dig.*, Dec. 2017, p. 29, doi: 10.1109/IEDM.2017.8268472.

JONGHYEON HA received the B.S. degree in electrical engineering from Gyeongsang National University, in 2023, where he is currently pursuing the master's degree in electrical engineering. His main research interest includes modeling of logic FET using TCAD simulation.

MINJI BANG received the B.S. degree in electrical engineering from Gyeongsang National University, in 2022, where she is currently pursuing the master's degree in electrical engineering. Her main research interest includes modeling of logic FET using TCAD simulation.

GYEONGYEOP LEE received the B.S. degree in electrical engineering from Gyeongsang National University, in 2021, where he is currently pursuing the master's degree in electrical engineering. His main research interest includes the modeling and reliability of silicon channel FET.

MINKI SUH received the B.S. degree in electrical engineering from Gyeongsang National University, in 2022, where he is currently pursuing the master's degree in electrical engineering. His main research interest includes the modeling and reliability of silicon channel FET.

CHONG-EUN KIM (Member, IEEE) received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 2001, and the M.S. and Ph.D. degrees in power electronics from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2003 and 2008, respectively.

JUNGSIK KIM (Senior Member, IEEE) received the Ph.D. degree in IT convergence engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2016. From February 2016 to March 2018, he was with SK-Hynix, for the modeling of 96-stacks VNAND. From April 2018 to March 2019, he was a Visiting Scholar with the NASA Ames Research Center, for reliability due to the radiation effect in silicon devices. From April 2019 to February 2020, he was with Samsung Electronics, for compact modeling of 1a-node DRAM. He is currently an Assistant Professor with the Department of Electrical Engineering, Gyeongsang National University, Jinju, South Korea. His research interest includes the modeling and reliability of nano-scale devices based on technical computer-aided simulation and measurement.