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RESEARCH ARTICLE

A Novel Current Limiting Protection Control Strategy by Power MOSFET Thermal Management for Solid-State Power Controller

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ABSTRACT This paper combines real-time temperature detection of MOSFETs inside solid-state switches with a temperature field model, and proposes a current limiting protection control strategy based on real-time heat management of MOSFETs. This strategy can avoid the unreasonable setting of current limiting protection time in solid-state switches during short circuit faults, leading to overheating and failure of MOSFET, and thus causing faults in HVDC power distribution system. Firstly, we analyzed the protection characteristics and shortcomings of solid-state switches such as solid-state power controller(SSPC) and solid-state circuit breakers (SSCB). Secondly, we optimized the circuit design of the solid-state power controller and the conversion relationship under different operating conditions, and elaborate on the implementation method of this control strategy in detail. Thirdly, we established a heat dissipation model for the MOSFET of SSPC, conduct theoretical and simulation analysis, and obtain the temperature field distribution of the MOSFET; Finally, the temperature of the MOSFET core is calculated by collecting the temperature of the position through the solid-state power controller temperature sensor, achieving accurate measurement. This paper also developed a prototype of a solid-state power controller with a rated current of 20A at 270V DC, and conducted short-circuit current limiting protection tests at 5 times the rated current; Experiments have shown that this control strategy can effectively prevent the overheating failure of the MOSFET.

INDEX TERMS SSPC, power distribution system, current limiting protection, thermal management.

NOMENCLATURE

SSPC	Solid-state power controller.
SSCB	Solid-state circuit breaker.
ASAAC	Allied standard avionics architecture council.
R_{on}	On-resistance of the SSPC.
I_M	Maximum load current.
I_O	Maximum over current.
I_R	Load rated current.
I_S	Short-circuit current.
U_S	Power supply voltage.
R_W	line resistance.
V_{GS}	Gate-source voltage.
V_{DS}	Drain-source voltage.
U_S	Power supply voltage.
K_1, K_2	Constant of the loop current equation.
t	Trip protection time.
Q	Heat.
q	Heat flow density fluctuation.
P_D	MOSFET power consumption load-rated current.
T	Temperature.
K	Constant.

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I. INTRODUCTION

Since the 21st century, human society has been facing more severe challenges such as fossil energy shortages, environmental pollution, climate change, and sustainable development. Especially in the field of transportation, people are paying more attention to factors such as safety, comfort, energy conservation, and environmental protection [1]. In the design of more/all electric aircraft, electrical energy replaces hydraulic, mechanical, and pneumatic energy as the main secondary energy source in the system [2]. Under the new system energy architecture, a large number of electrical load devices have been added to the distribution system [3]. In addition, in order to reduce line losses in the distribution system, the bus voltage has been increased in the distribution system (onboard DC 270V system, onboard DC 540V system, etc.). With the increase of system bus voltage, traditional electromechanical short circuities and relays cannot meet the requirements of fault isolation and load switching due to factors such as arc [4], [5]. New solid-state switches such as solid-state power controllers (SSPCs) and solid-state circuit breakers (SSCBs) have been widely used in electrical systems such as new aircraft due to their high reliability, small size, low loss, remote control, power-on built-in test, and continuous built-in test [6]. SSCB is used to replace traditional mechanical circuit breakers, while SSPC is used to replace the combination of electromechanical relays (contactors) and mechanical circuit breakers. It is a key component in the new distribution system [5].

With the development of semiconductor technology, power devices such as silicon based MOSFETs, IGBT, GTO, ITO, and IGCT are widely used as output devices for intelligent solid-state switches such as SSPC and SSCB [7]. In recent years, SiC and GaN based wide bandgap power devices have also been applied to intelligent solid-state switches [8], [9], [10]. Microprocessors such as MCU, DSP, and FPGA are used to achieve functions such as inverse time protection, remote control, status detection, and fault diagnosis [11], [12], [13]. In addition, researchers have optimized the control strategies of SSPC and SSCB to improve their adaptability to capacitive loads, such as selecting a more optimal current trajectory based on the safety operation area (SOA) of power MOSFETs to avoid damage to MOSFETs caused by surge currents when capacitive loads are turned on [4] and [14]; In addition, the current limiting protection methods and control strategies of SSPC and SSCB during load short circuits have also been a research hotspot in recent years. Some studies have achieved current limiting protection during load short circuits by changing the V_{GS} voltage of MOSFETs to operate from saturation to amplification region [15], [16]. By adding a BUCK circuit, it is an effective method to improve the suppression ability of SSPC against short circuit currents in all electrical systems, while also improving its capacitance and adaptability to motor loads [16].

However, with the increase in the number and power of electrical loads in all electrical systems such as fully electric aircraft, there are some shortcomings in the current control strategies of intelligent solid-state switches such as SSPC and SSCB for short-circuit conditions. By controlling the power output device to work in the amplification zone or combining PWM circuits with BUCK circuits, current limiting protection is achieved during load short-circuit, allowing the power output device to work in the amplification zone for a long time.The generated heat can easily cause thermal damage to the success rate devices, even leading to a decrease in lifespan or failure, leading to a decrease in the reliability of the distribution system [17]. A reliability research report on power electronic systems shows that power devices have the highest failure efficiency in converter systems, with a proportion of about 34% [18]. This paper proposes a short-circuit current-limiting protection control strategy for FET based on the heat dissipation model of a solid-state power controller. The real-time temperature of the FET inside the solid-state power controller is deduced based on its heat dissipation model, so as to determine the length of its short-circuit current-limiting protection operating time, and to avoid the thermal breakdown of the field-effect transistor due to the solid-state power controller.Firstly, this paper improves the accuracy and real-time performance of temperature, current, and voltage parameter acquisition by optimizing the circuit design of the SSPC; Then, by establishing the three-dimensional structure model of SSPC and FET, the heat dissipation model of FET is obtained using the thermodynamic law, and the temperature field distribution of FET when it is working is obtained using the finite element simulation calculation, so as to obtain the temperature distribution relationship between the inside and outside of FET; Finally, a control strategy is obtained to determine the current limiting protection time based on the real-time temperature value inside the field-effect transistor, in order to prevent the overheating and burning of the field-effect transistor caused by inaccurate current limiting protection time. The paper also applies the control strategy to the design of the Allied Standard Avionics Architecture Council (ASAAC) standard SSPC board in the DC 270V distribution system, develops experimental samples, and verifies the effectiveness and correctness of the control strategy through experiments.

II. CHARACTERISATION OF SOLID STATE DISTRIBUTION SYSTEMS

In traditional solid state power distribution system, SSPC uses inverse time protection algorithm to protect the load overcurrent condition, and has weak ability to isolate short circuit fault. This chapter analyzes the protection characteristics of traditional solid-state switches, establishes the circuit model under short-circuit fault conditions, and analyzes the limitations of inverse time protection algorithm.

A. ANALYSIS OF THE OVERCURRENT AND SHORT CIRCUIT PROTECTION CHARACTERISTICS OF CONVENTIONAL SOLID STATE SWITCHES

SSPC overcurrent protection is based on the principle that heat is generated by current flowing through the conductors,

and heat accumulation occurs during circuit overcurrent. When the heat accumulation reaches the trip protection threshold, the power switching device is driven to shut down and achieve trip protection [7]. Overcurrent protection is carried out according to the inverse time protection characteristic, and the mathematical model of inverse time protection commonly used in DC 270V distribution systems is [21]:

$$\begin{cases} I_m = 0.88 \times \left(\dfrac{4.71}{\mathrm{t}} - 0.47\right)^{0.8} + 10, & 0.04 \le t \le 10, \\ I_o = 4.57 \times \left(\dfrac{75.62}{\mathrm{t}} - 0.25\right)^{0.73} + 24, & 1.6 \le t \le 300. \end{cases} \tag{1}$$

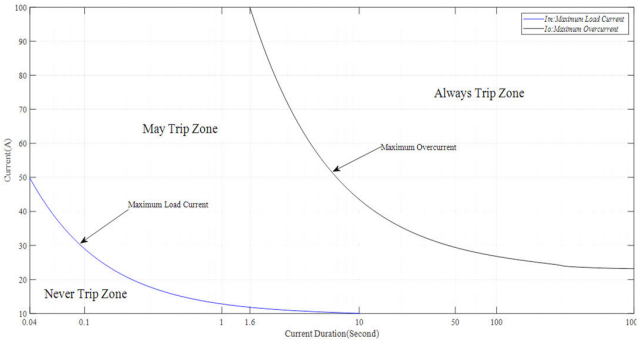

FIGURE 1. Inverse time limit protection curve.

As shown in Fig. 1, I_m is the maximum load curve and I_o is the maximum overcurrent curve. This shows that the protection characteristics of the SSPC are mainly for load overcurrents greater than several times the rated current and overcurrent protection times longer than 40ms. If the model is used for short-circuit protection, then solid-state switching devices such as power field-effect tubes in the SSPC need to be capable of over-current for tens of milliseconds under short-circuit conditions. The circuit parameters for a SSPC with bus voltages of 28V and 270V DC and rated currents of 50A and 20A respectively are shown in Table 1.

TABLE 1. Short-circuit condition circuit parameters.

Parameters	SSPC1(28V)	SSPC2(270V)
Bus Voltage(V_{Bus})	28Vd.c.	270Vd.c.
Rated current(I_R)	50A	20A
On-resistance(R_{on})	5mΩ	10mΩ
Line Resistance(R_w)	30mΩ	30mΩ
Short-circuit Current(I_S)	400A(single)	3375A(single)
Pulsed Drain Current(I_{DM})	1280A	250A
Exceeding SOA(Y/N)	N	Y
Use of Power MOSFET	In parallel	In parallel

Notes: The IRFP4368 power FET is used in 28V SSPC, and the ASC100N1200MT4 SiC power FET is used in 270V SSPC.

As can be seen from Table 1, in the line resistance R_W with 30mΩ in the secondary distribution circuit, bus voltage for DC 28V secondary distribution system when a short-circuit fault occurs, the circuit theoretical short-circuit current of about 400A, not beyond the pulse drain current I_{DM} of the field-effect tube, will not lead to field-effect tube damage. Bus voltage for DC 270V secondary distribution system when a short-circuit fault occurs. If the current rise rate is not suppressed, the circuit theoretical short-circuit current will quickly reach 3375A, beyond the pulse drain current I_{DM} of the field-effect tube, then resulting in field-effect tube damage or secondary power supply power failure, illustrate in Fig.2.

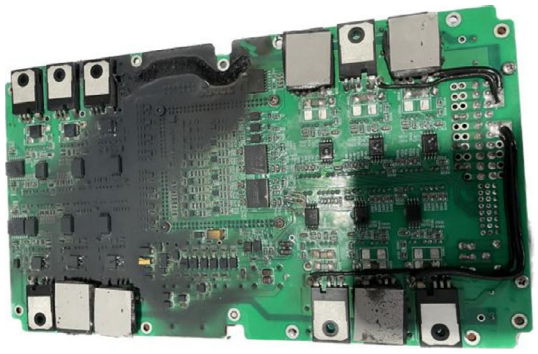

FIGURE 2. Load short circuit causes the MOSFET and peripheral circuit to burn out.

The key circuit of a generic SSCB are gate driver circuit, power semiconductor device, current sampling circuit, voltage simpling circuit, temperature sensor, conditioning circuit, cooling system, voltage clamping circuit, trip control circuit, and power supply. The schematic block diagram can be seeing in Fig. 3.

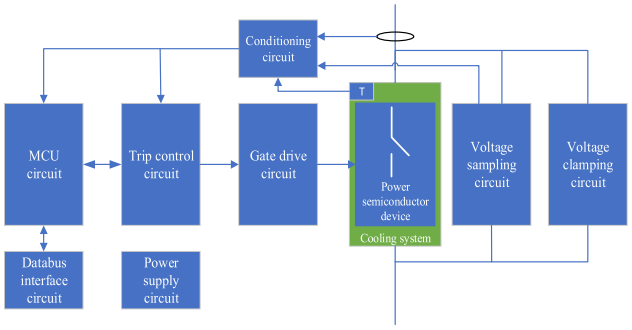

FIGURE 3. Functional block diagram of SSCB.

SSCBs detect the circuit current in real time through a current sensor and trigger the gate drive circuit to control the power switching device to shut down when the fault current reaches the trip protection point to achieve fault current breaking and trip protection [21]. Solid-state circuit breakers are mainly based on the circuit short-circuit fault current size, and the breaking capacity is enhanced by selecting solid-state switching devices with higher overload capacity, such as IGBTs, IGCTs and GTOs. The Fig.4 shows a solid

state circuit breaker short circuit protection test for a distribution circuit with a load rating of 8.75A, where the circuit short circuit current is close to 15 times the rated current. As the SSCB requires a large current overload capability, it requires a power semiconductor device with a high continuous gate current; the power consumption of this type of semiconductor device itself is high, making the SSCB structure design require additional auxiliary cooling measures such as air or liquid cooling, resulting in a relatively large size and weight. Therefore, SSCBs are not suitable for high voltage secondary power distribution systems for airborne and satellite platforms, which require high volume and weight specifications.

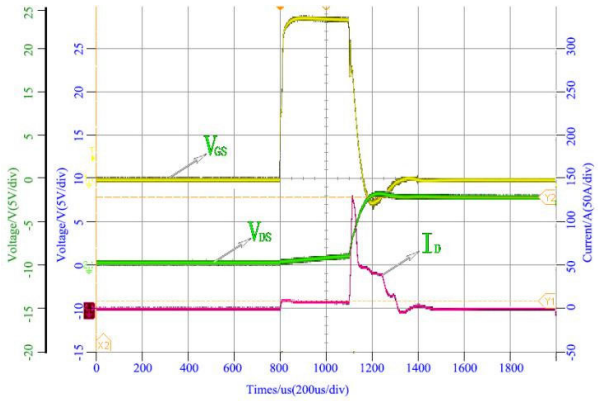

FIGURE 4. Short circuit protection test of SSCB.

B. LIMITATIONS OF INVERSE TIME PROTECTION

There are two main international standards for inverse time protection characteristics: IEEE StdC37.112-1996 and IEC 60255-3 (1989 - 05). The inverse time model is given in the standard, with a mathematical model of the current protection time as:

$$t = \frac{KM}{(I/I_p)^r - 1} \quad (2)[12]$$

where t is the trip protection time. K is design constants and r is determined according to thermal conditions, which contain three recommended parameters: general inverse time, extraordinary inverse time and extreme inverse time. M is the rectification factor, determined according to the size of the allowed current fluctuations in the circuit. I is the rated current of the load. I_p is the rectified current value, which is a multiple of the rated current.

The theory of inverse time protection has been derived in paper [20] in conjunction with the first law of thermodynamics. The main protection mechanism is: when current flows through a conductor, the conductor heats up and radiates heat to the surroundings by conduction, convection and radiation. When the rated current flows through the conductor, the accumulation and distribution of heat from the conductor is balanced. When the load is overcurrent, the conductor will flow at a higher current and the inverse time protection circuit comes into play, sending a trip signal to shut down the power tube after a corresponding delay according to the multiplier of the overload.

Combined with the above analysis, it can be seen that the inverse time protection is mainly applicable to the trip protection of the transmission circuit overheating caused by load overcurrent. For low-voltage solid-state power controllers, when the load has a large rate of overcurrent or short circuit, due to the power FET work in the saturation zone, the on-state resistance is small, the thermal power consumption is small, the temperature rise within the inverse time trip protection time will not lead to thermal breakdown of the FET. While for high-voltage solid-state power controllers, due to the FET and other solid-state switching devices on-state resistance is large, a large rate of overcurrent or short circuit, will lead to the FET thermal Power consumption is high, which can easily lead to thermal breakdown failure. With a load voltage of 270V DC and a rated current of 20A, the solid-state power controller is connected in parallel with two tubes, with an on-state resistance of about 10mΩ.

TABLE 2. Power consumption of FET under overcurrent.

Overcurrent ratio	Load resistance (Ω)	Load current (A)	FET power consumption (w)
I_R	13.5	20	4
$2I_R$	7	40	16
$3I_R$	4.5	60	36
$6I_R$	2.25	120	144
$10I_R$	1.35	200	400

As can be seen from Table 1 and Table 2 above, in more than 10 times overcurrent or short-circuit conditions, the thermal power consumption of the field-effect tube will lead to a rapid rise in SSPC temperature, which may even exceed the maximum power consumption allowed for the field-effect tube, and will easily lead to thermal breakdown and failure. Hence, the inverse time protection algorithm is not fully applicable to the tripping protection of the SSPC under large overcurrent or short circuit conditions in the DC high voltage secondary distribution system.

C. ANALYSIS OF CIRCUIT CHARACTERISTICS DURING LOAD SHORT CIRCUIT

The addition of a BUCK circuit to the SSPC circuit, which reduces the rate of change of the circuit current during a short circuit by adding an inductor to the distribution path. It allows the control circuit to be safely switched off within the SOA of the power FET and is an effective measure to improve the isolation of the SSPC against short circuit faults. When the secondary distribution path load short-circuit, the circuit in [16] can be equated to a circuit as shown in Fig.5 (a), where R_{on} is the on-state resistance of the MOSFET, R_L is the load resistance, R_{line} is the line resistance, L is the

inductor, L_{line} is the line distribution inductance, C_{line} is the distribution capacitance; ignoring the distribution parameters in the circuit, it can be simplified to Fig.5 (b) shown, where R is the sum of the on-state resistance of the MOSFET and the line resistance in the line.

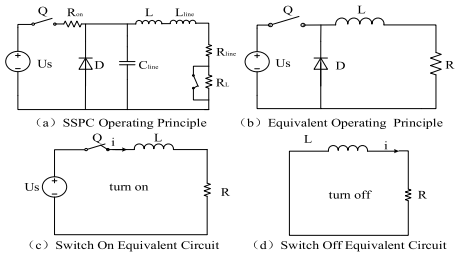

FIGURE 5. Load short circuit equivalent circuit.

When the SSPC controlled MOSFET Q is on, the load R_L is equivalently shorted and the equivalent circuit is shown in Fig.5(c)the following equations can be obtained:

$$U_S = L\frac{di}{dt} + iR. \tag{3}$$

The solution i of (3) is

$$i(t) = \frac{U_S}{R} + K_1 e^{-\frac{Rt}{L}}. \tag{4}$$

When the SSPC controls the MOSFET Q off, ignoring the voltage drop across the diode, the equivalent circuit is shown in Fig.5(d), the following equations can be obtained:

$$L\frac{di}{dt} + iR = 0. \tag{5}$$

The solution i of (5) is determined as

$$i(t) = K_2 e^{-\frac{Rt}{L}}. \tag{6}$$

Based on the initial state characteristics of the circuit, $K_1 = 6730$ and $K_2 = 100$ can be found.

III. OPTIMAL CONTROL OF SECONDARY POWER DISTRIBUTION

The studies in [20] showed that junction overheating and wide thermal cycling are the two main causes of power device failures such as power FETs. In this paper, heat loop control is added to the SSPC control strategy to calculate the heat generation by measuring the V_{DS} voltage and I_{DS}current of the power FET in real time; calculating the heat dissipation according to the heat dissipation model of the power FET to obtain the real-time surface temperature and junction temperature of the power FET; determining the load characteristics and operating conditions according to the dV_{DS}/dt of the MOSFET, and setting a reasonable heat threshold by Determine the current limit protection time of the SSPC under short circuit conditions and the inverse time protection curve threshold under normal conditions.

A. CIRCUIT OPTIMIZATION DESIGN OF SSPC

In the paper, this paper adds a voltage detection circuit to the power MOSFET, a PWM Circuit and a BUCK circuit in our new SSPC design. It mainly consists of FPGA main control module, PWM circuit, ADC isolated sampling circuit, isolated drive circuit, threshold circuit, switch state detection, V_{DS} voltage clamp circuit, data storage circuit, temperature acquisition and isolated secondary power supply. Fig.7 is a circuit principle block diagram of a novel SSPC.

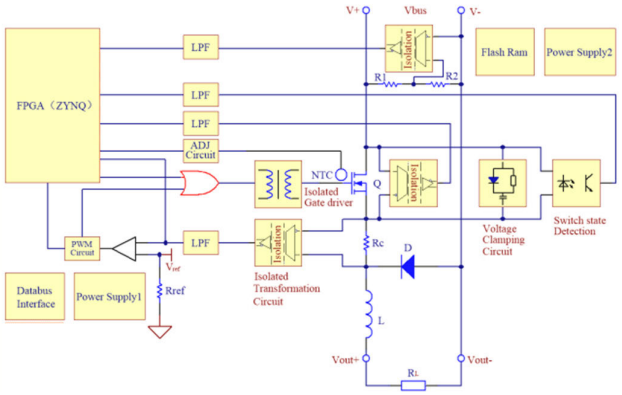

FIGURE 6. Circuit principle block diagram of the proposed SSPC.

The circuit uses an isolated op-amp sampling circuit instead of a Hall sensor to increase the sampling frequency of the bus voltage, power FET VDS voltage and output loop current, which is filtered by the LPF and sent to the voltage comparator and the ADC port of the FPGA. Due to the tens of milliseconds machine cycle of the FPGA processor, when there is a short circuit at the load side of the SSPC or when a large capacity capacitive load is connected, the inductor L in the circuit is used to reduce the di/dt in the loop. When the current is greater than the current limit threshold, the hardware PWM circuit is triggered to work with a fixed duty cycle and control the gate isolated driver circuit to drive the BUCK circuit to limit current. When the current is greater than the current limit threshold, the hardware PWM circuit is triggered to work with a fixed duty cycle and the gate isolation driver circuit is controlled to drive the BUCK circuit to limit the current; when the FPGA processor detects that the load is overcurrent, the I/O outputs the same control signal as the duty cycle of the hardware PWM circuit, and at the same time, the hardware PWM circuit is controlled to reset and the BUCK circuit is controlled by the Afterwards, the FPGA processor calculates the surface temperature and junction temperature (T_j) of the MOSFET according to the thermal model of the SSPC, and determines the control policy and protection time in combination with the load type diagnosed by the algorithm. Fig.7 shows a work logic block diagram of a novel SSPC.

B. OPTIMAL HEAT MANAGEMENT OF CONTROL STRATEGY FOR SSPC

In the previous introduction, the proposed SSPC has six operating states, namely On-State, Off-State, PCL-State,

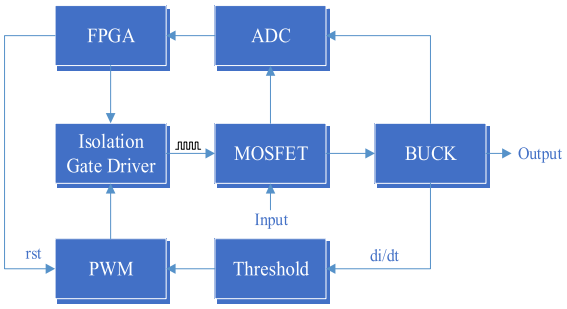

FIGURE 7. Work logic block diagram of the proposed SSPC.

ACL-State, CC-State and OC-State. SSPC operating in On-State, the load current does not exceed the maximum multiple of its rated current (such as $<1.25\ I_{\text{rate}}$), allowing the load to work for a long time; operating in Off-State, the SSPC's power FET is in a high resistance state, the output circuit only uA level leakage current flow; operating in PCL-State, because in the processor response cycle. Thus, when the current reaches the threshold current, the hardware PWM circuit is triggered to control the BUCK circuit to work in the current-limited protection state. As working in ACL-State, the output current increment does not exceed the safe operating region of the MOSFET due to the processor response cycle and the delay of the conditioning circuit. The FPGA generates PWM signals to control the BUCK circuit in the current-limited protection state. The FPGA controls the BUCK circuit instead of the hardware PWM circuit, converts the PCL-State to the ACL-State operating state, and resets the hardware PWM circuit. When operating in the CC-State, the FPGA determines that the load is a large-capacity When working in CC-State, the FPGA determines that the load is a high-capacity capacitive load and generates a PWM control signal to control the BUCK circuit to achieve slow charging; and when working in OC-State, the FPGA controls the MOSFET to achieve reverse-time overcurrent protection. Fig.8 shows Multi-Mod Control strategy for the proposed SSPC.

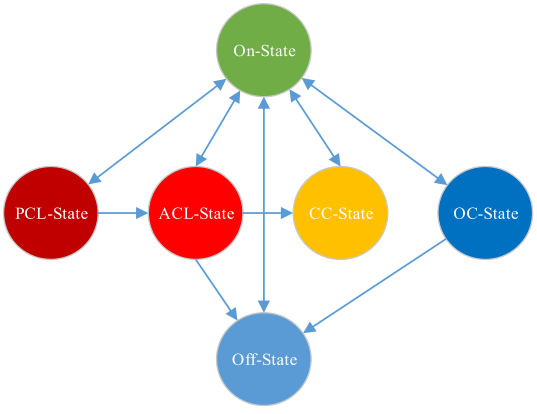

FIGURE 8. Multi-Mod Control strategy for the proposed SSPC.

When the SSPC works in different states, the transition between states is achieved according to the control flow shown in Fig. 8. When the SSPC receives a turn-on command via the data bus to control the MOSFET turn-on, it enters the On-State state; at the same time, the main control unit, with the FPGA as the core, continuously samples and monitors parameters such as load current and VDS voltage and maintains the On-State state. When there is an overcurrent in the output loop, e.g. di/dt is large and the current value exceeds the PCL current threshold during the response time interval of the main control unit, the hardware circuit is triggered to drive the PWM circuit to work with a fixed duty cycle, entering the PCL-State state and limiting the current to the set value; when the main control unit responds, the FPGA takes over the system and the system goes from PCL-State to ACL-State; when the output circuit is overcurrent and the current value does not exceed the PCL current threshold during the response time interval of the main control unit, it enters the ACL-State state; when the SSPC works in the ACL-State state, the main control unit judges the output as a capacitive load, short circuit or overcurrent condition by monitoring the V_{DS} voltage and dV_{DS}/dt; at the same time, considering the reliability and at the same time, the maximum temperature rise of the power MOSFET is 0.7 Tjmax, and the heat dissipation model calculates the real-time heat of the MOSFET and conFig.9 the slow-charge current curve, the short-circuit protection curve and the inverse-time overcurrent protection curve for each of the three operating conditions.

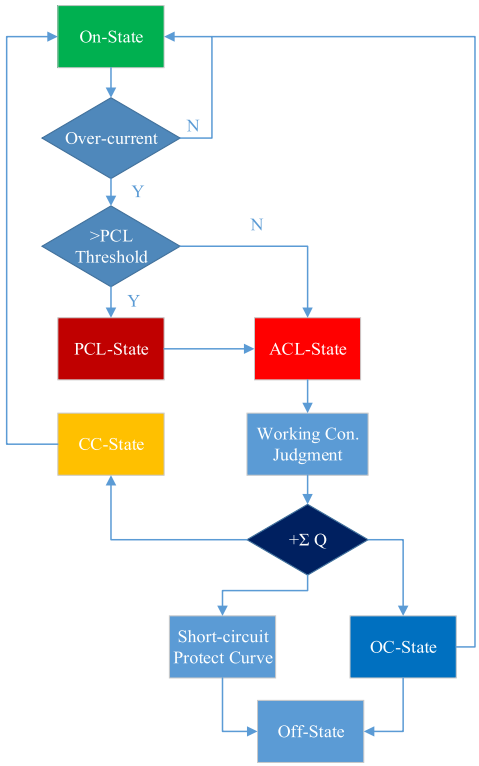

FIGURE 9. Control flow for the proposed SSPC.

C. CURRENT LIMIT PROTECTION CONTROL AND SIMULATION

The ASAAC standard board structure DC 270V SSPC performance parameters designed in this paper are shown in Table 1,

the load supply US is 270V, the short circuit is circuit resistance R is 40mΩ as shown in Fig.6, and the inductance of inductor L is 4.7mH. According to the control flow shown in Fig.8, the short circuit current limit threshold is set to 5 times the rated current I_R, which is 100A. When the circuit is short-circuited, the current rises to 100A, the gate drive circuit turns off the FET; when the current drops to the rated current, the gate drive circuit turns on the FET. According to the circuit response characteristics, and the parameters into formula (4) and formula (6), the period T is calculated as 190.405ms, the turn-on time t_1 is 1.405ms, the turn-off time t_2 is 189.000ms, the mathematical model is as follows.

$$i(t) = \begin{cases} \dfrac{U_S}{R} + K_1 e^{-\frac{Rt}{L}} & [nT, nT + t_1), \\ K_2 e^{-\frac{Rt}{L}} & [nT - t_1, nT + t_2), \end{cases} \tag{7}$$

where n is a non-negative integer. When the load is short-circuited in the rated operation of the SSPC, the simulation waveform of the current rise is shown in Fig.12; when the load short-circuit current rises to 5 times the rated operating current, the simulation waveform after the SSPC is switched off is shown in Fig. 11; when the SSPC is in the current-limited protection state, the simulation waveform of the loop current is shown in Fig. 12.

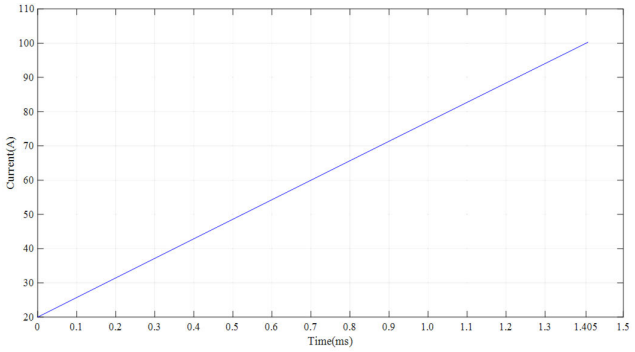

FIGURE 10. Current simulation waveform after short circuit.

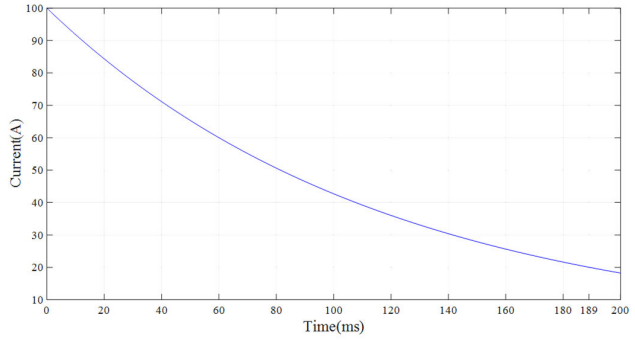

FIGURE 11. Current simulation waveform after SSPC switching off.

IV. THERMAL DESIGN AND SIMULATION ANALYSIS OF SSPC

ASAAC structure is a typical structure of SSPC module in secondary power distribution system, which is convenient for maintenance and replacement and enables the system to reach LRM level maintenance level. This section mainly describes the heat dissipation design method of SSPC module FET with ASAAC structure, and carries out theoretical and simulation analysis.

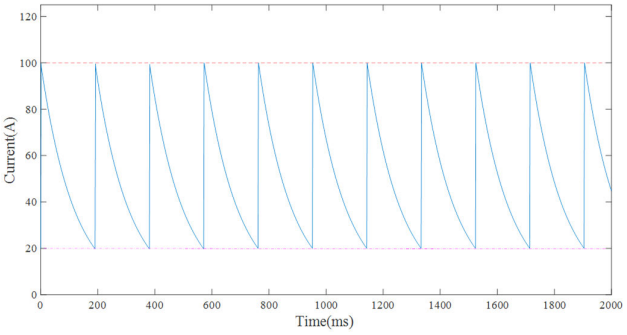

FIGURE 12. Current limiting protection simulation waveform.

A. THERMAL DESIGN AND THEORETICAL ANALYSIS

The structural design of the SSPC takes into account not only the fixation of the MOSFET, but also the rapid conduction of heat to the outside world. Aluminum alloy is a commonly used material for structural components, with the advantages of light weight, good machinability and high thermal conductivity, and is widely used in the design of SSPC structures. The SSPC model of the ASAAC standard board structure is shown in Fig.13.

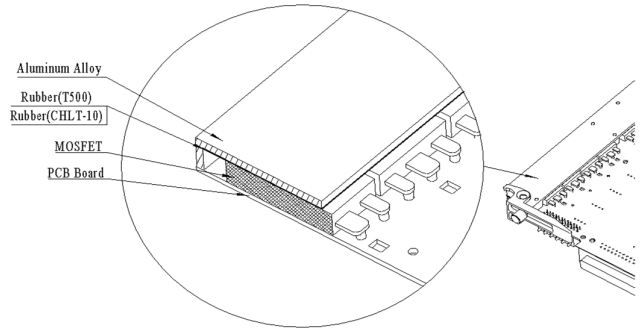

FIGURE 13. SSPC 3D structural model.

According to the first law of thermodynamics:

$$Q - W = \Delta U + \Delta KE + \Delta PE \tag{8}$$

where Q is the heat, W is the work done, U is the internal energy of the system, KE is the kinetic energy of the system and PE is the potential energy of the system. For the SSPC thermal analysis problem, $\Delta KE + \Delta PE = 0$, ignoring the work done by heat, i.e. $W = 0$, then

$$Q = \Delta U. \tag{9}$$

In transient thermal analysis, the heat flow rate is equal to the change in internal energy of the system.

$$\varphi = \frac{\mathrm{d}Q}{\mathrm{d}t} = \frac{\mathrm{d}U}{\mathrm{d}t}. \tag{10}$$

According to the principle of conservation of energy, the energy balance equation can be expressed as

$$[C(T)]\left\{\dot{T}\right\} + [K(T)]\{T\} = \{\varphi(T)\}. \tag{11}$$

where C is the specific heat matrix, K is the heat transfer matrix, T is the nodal temperature vector and φ is the nodal heat flow rate vector.

In steady-state thermal analysis, the heat flowing into and out of the system is equal and the nodal temperature vectors do not vary with time, $\left\{\dot{T}\right\} = 0$, The energy balance equation for the steady state thermal analysis is therefore:

$$[K(T)]\{T\} = \{\varphi(T)\}. \tag{12}$$

where K contains the thermal conductivity, convection coefficient, emissivity and shape factor. the SSPC heat transfer modes are mainly heat conduction and heat convection, and the expressions are:

$$\begin{aligned} q &= -k\frac{dT}{dx}, \\ q &= h(T_S - T_B). \end{aligned} \tag{13}$$

where, q is the heat flow density, k is the thermal conductivity, h is the convective heat transfer coefficient, T_S is the solid surface temperature and T_B is the surrounding fluid temperature.

B. MOSFET THERMAL POWER CONSUMPTION CALCULATION AND HEAT DISSIPATION SIMULATION

1) THERMAL POWER CALCULATION

SSPC current limiting protection work process, due to the FET distribution parameters, the gate drive circuit in the control of the FET turn-on shutdown process through the amplification area, generating a lot of heat. As shown in Fig. 12, the SSPC in the process of current limiting protection work, let the MOSFET drain and source voltage V_{DS}, its thermal power consumption is P_D, then there are the following equations.

$$P_D = \int V_{DS}(t)i(t)dt. \tag{14}$$

Substituting (12) into (13) the thermal power consumption generated by the FET during the SSPC current limiting protection can be calculated.

2) THERMAL SIMULATION

As shown in Fig. 7, by adjusting the SSPC gate and drain capacitance C_{DG}, the gate drive circuit control FET turn-on turn-off time is designed to 50us. according to (14) formula can be calculated to get the single tube thermal power consumption of about 200W, and then according to the above on the DC 270V ASAAC standard board heat dissipation principle, the finite element simulation analysis of the SSPC designed in this paper, in the ambient temperature The maximum internal temperature of the FET is 136.1°C and the maximum external surface temperature is 117.92°C, as shown in Fig. 14-16. It can be seen from the simulation, due to the SSPC shell and thermal insulation materials exist thermal resistance, the surface of the FET and the peripheral materials there is a certain temperature difference.

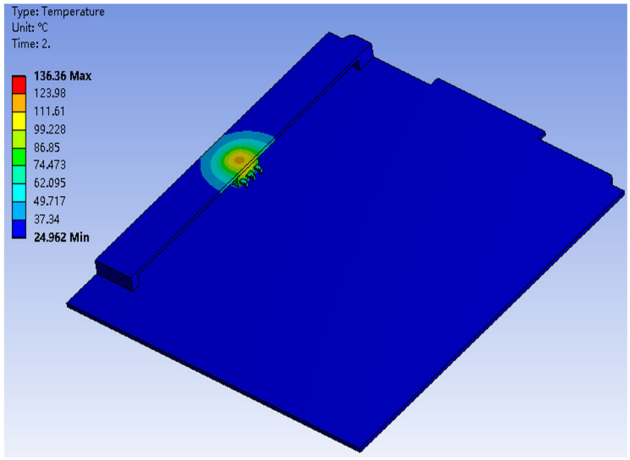

FIGURE 14. Thermal simulation of SSPC.

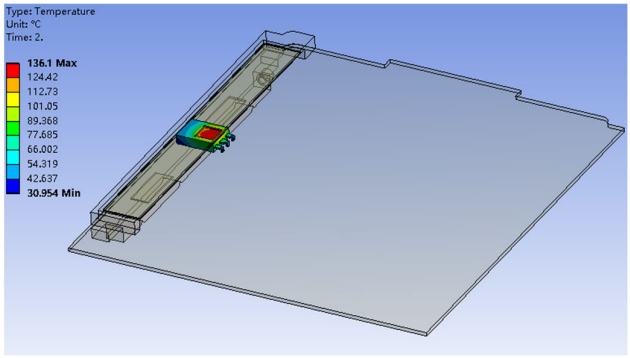

FIGURE 15. Thermal simulation of MOSFET.

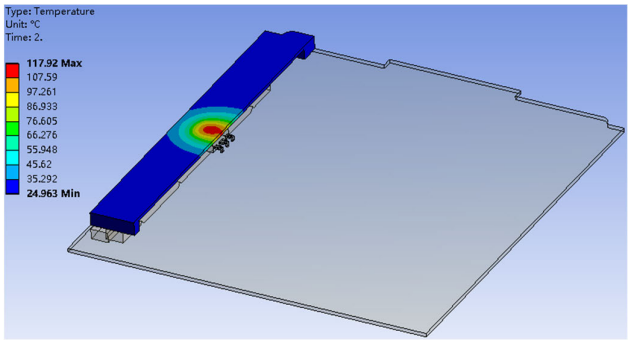

FIGURE 16. Temperature Field Distribution of MOSFETs.

V. EXPERIMENTAL RESULTS

A. PROTOTYPE DEVELOPMENT

The circuit design and structural design of the SSPC was carried out according to the circuit principle shown in Fig. 7 and the relevant structural dimensional requirements of the ASAAC standard, and a prototype was developed as shown below.

FIGURE 17. Printed board assembly of SSPC.

FIGURE 18. ASSAC standard SSPC module.

B. PROTOTYPE TESTS

Prototype verification tests were carried out according to the bus voltage and load characteristics of an all-electric aircraft DC 270 V secondary distribution system. The equivalent resistance of the load impedance R_L at the rear end of the SSPC was 13.5Ω and the rated current was 20 A. High power contactor contacts were connected in parallel at both ends of the load to simulate a load short circuit by controlling the contactor on. As shown in Fig. 19, U_S is the power supply, Q is the SSPC, K is the contactor and R_L is the load.

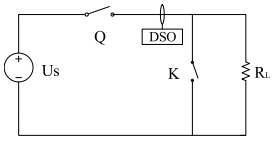

FIGURE 19. Schematic diagram of load test circuit.

The short-circuit current-limit protection test platform is shown in Fig. 20, setting the rated current of the SSPC to 20A and setting the current-limit protection current limit to 5 times the rated current. Use the upper computer to send control commands to control the SSPC to turn on one way solid state switch output with rated operating current of 20A; then control the contactor K to turn on and short circuit the load R_L, the SSPC current limit protection output for 2s, the test results are shown in Fig. 21 and Fig. 22 below.The temperature cloud around the solid-state power control FET was tested using an infrared scanner, and as shown in Figure 23, the maximum

FIGURE 20. Current limiting protection test platform of SSPC.

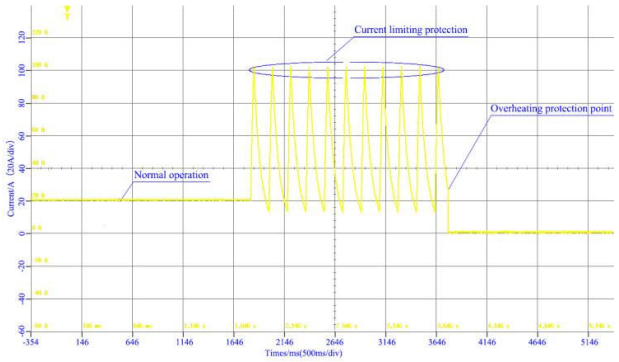

FIGURE 21. Current limiting protection test.

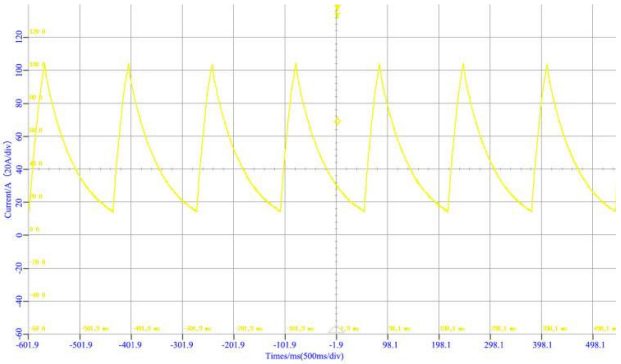

FIGURE 22. Current limiting protection waveform.

temperature at the surface of the FET was 120.2°C, with the heat sink and wires at higher temperatures due to low thermal resistance.

C. ANALYSIS OF TEST RESULTS

The theoretical analysis, simulation and test show that the control strategy based on the steady-state heat management of power FETs can effectively prevent the failure of FETs due to thermal breakdown under short-circuit conditions. This paper elaborates on the optimization of the SSPC circuit, the optimization of the control flow, and establishes a power FET heat dissipation model using the ASAAC standard board structure. A comparison of the simulation calculations and

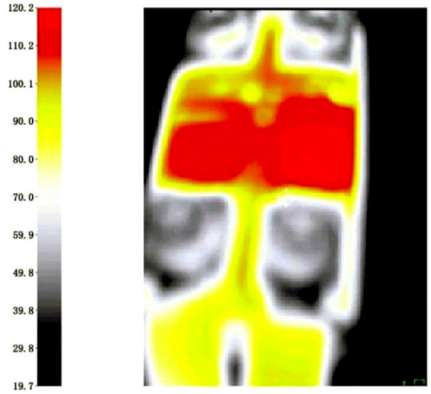

FIGURE 23. MOSFET temperature monitoring of SSPC.

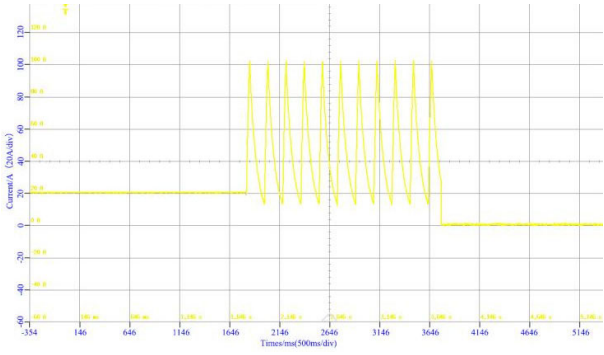

FIGURE 24. Current limiting protection time.

test data is shown in Table 3. Based on the above comparative analysis, it can be deduced that the error is mainly caused by the existence of an air gap between the field effect and the thermally conductive insulation material, resulting in errors in the thermal resistance, as well as measurement errors and other factors.

TABLE 3. Simulation and test result Comparison for maximum surface temperature of MOSFET.

parametersPRM Test details	Current limiting protection time（setting, ms）	Maximum surface temperature of FET（°C）	Temperature deviation between test and simulation（°C）
Simulation	2000	117.92	--
Test 1	2000	120.20	2.28
Test 2	2000	116.90	1.02
Test 3	2000	117.80	0.12

Using the control strategy shown in Fig. 9, set the overheat protection point on the outer surface of the FET to 120°C. Through the main control unit in the SSPC with the FPGA as the core, the temperature rise of the FET is calculated according to the heat dissipation model of the ASAAC module, and when the temperature rise of the FET reaches the protection threshold, the SSPC is controlled to trip the protection, and

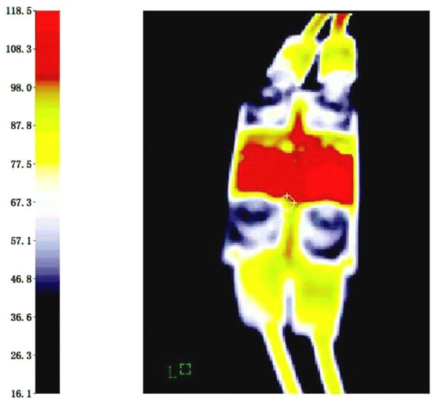

FIGURE 25. Temperature nephogram of MOSFET overheating protection.

the test conditions shown in Fig. 19 are used to test the current-limited protection waveform As shown in Fig. 24, the trip protection time is 1974*ms*; overheating protection instant, using infrared imaging instrument to measure the temperature cloud of the FET surface as shown in Fig. 25, the highest temperature point is 118.5°*C*. The above test results can prove the correctness of the control strategy and circuit optimization of the SSPC proposed in this paper.

VI. CONCLUSION

In this paper, a control strategy based on steady state heat management of power MOSFET is proposed by improving the circuit design of SSPC, optimizing the control flow and establishing the heat dissipation model of power MOSFET based on ASAAC standard board structure. Firstly, the principle and application scope of the traditional SSPC inverse time protection are analyzed. The circuit design is optimized to improve the SSPC voltage and current sampling rate, and improve the SSPC response speed and current suppression capability under load short circuit fault. Then the temperature field and temperature rise of power devices are simulated by establishing the SSPC heat dissipation model of ASAAC board structure. In addition, the optimal control algorithm is used to realize the optimal control of SSPC under short-circuit fault; Finally, the optimization design method and control strategy are applied to the design of the ASAAC standard board SSPC of a DC 270V distribution system of an all electric system. The SSPC prototype with a rated current of 20A is developed, and the short-circuit current limiting protection experiment with 5 times of the rated current is carried out. The test results verify the correctness of the optimization method and control strategy proposed in this paper. The reliability and safety of secondary distribution can be improved by using it in high-voltage DC distribution system.

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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