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SURVEY

Leveraging GaN for DC-DC Power Modules for Efficient EVs: A Review

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ABSTRACT Limitations of Silicon (Si)-based devices have compelled us to use alternative devices for modern power electronics applications. Material attributes of wide-band-gap devices (such as GaN and SiC) possess the ability to bridge these gaps. They can be used for higher power applications and provide high power-density, high efficiency and better thermal performance. GaN-based devices in electric vehicle power modules make the vehicle more efficient, achieving an extended range for the same battery size. Worldwide, researchers and engineers are working on GaN-based power-electronics modules. On the one hand, the utilisation of GaN switches in power modules eliminates a few existing design concerns. While it also introduces new challenges for designers. Mere replacing Si with GaN doesn't give the stipulated result. This article identifies the works related to GaN-based DC-DC converter modules to determine how researchers address the circuit design issues with GaN. This paper presents a detailed description of the material benefits of GaN and paves the path of future work by identifying the research gap in the field of GaN-based DC-DC converters.

INDEX TERMS Electric vehicle, Gallium nitride (GaN), high-frequency DC-DC converter, isolated converter, non-isolated converter, wide-band-gap devices.

I. INTRODUCTION

Alarming concerns of global warming, climate change, deplenishing oil reserves, and mounting oil prices have forced intellectuals, researchers and scientists to take concrete steps to save mother earth. Elevating the usage of alternate energy sources (like solar, wind, tidal etc.) and electric vehicles (EVs) are a few of them. Conventional vehicles, especially road transport ones, critically affect the environment by blowing out greenhouse gases (74.5% of global CO_2 emission by various transport sectors is accounted for by road transports [1]). Hence gas-guzzling vehicles are one of the major sources of global warming. In this regard, EVs are emerging as an option to replace conventional fuel vehicles. EVs are more efficient, safe, and reliable and have lesser maintenance and operating costs than conventional ones. However, accelerating towards EV adoption demands a few challenges to be addressed. Higher charging time, more capital cost (mainly because of high battery price), shorter driving range, reliability and lack of charging infrastructure are the challenges before automakers. To make EVs viable for customers, these challenges should be taken care of [2].

Charging time, for example, can be lowered by raising the power level of the on-board charger (OBC). The current trend is to increase the power level of OBC from 3.6 kW to 22 kW [3]. However, an increment in power level will add cost, weight and volume. In contrast, we require to have an OBC that must accommodate the given physical envelope of the vehicle with minimum to no increase in weight, volume and cost without impacting the driving ranges. So we need to increase the power-density to get a compact OBC.

Similarly, driving range can be increased by using large and bulky battery packs (which will put an economic burden) or improving the vehicle's energy efficiency. Better energy efficiency means lower energy consumption per km, i.e. lower losses. It is important to note that while we are trying to increase the power-density and get better energy efficiency, Si (silicon) cannot deliver the technical exigency because of its material limit. Here wide band-gap (WBG) devices come into the picture. Figure 1 demonstrates the comparative analysis of the energy efficiency of various EVs available in the market, their battery capacity and range [4], [5]. We can

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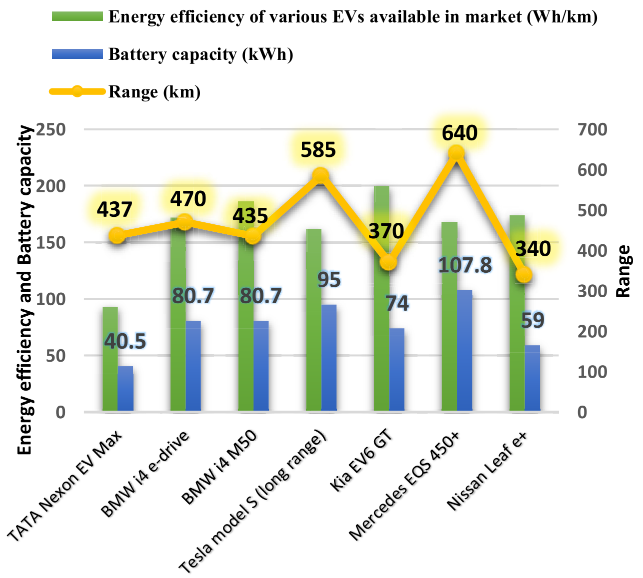

FIGURE 1. Comparative analysis of the energy efficiency, battery capacity and range of various EVs available in market.

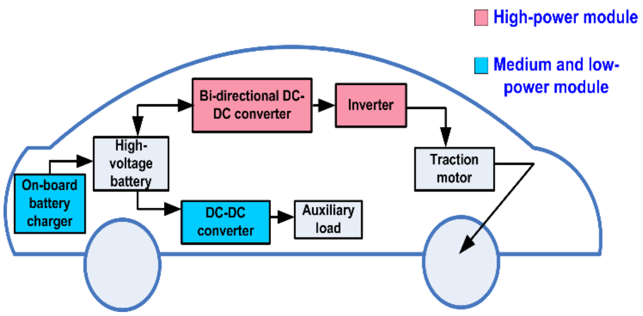

FIGURE 2. Powertrain of a BEV.

see that EV manufacturers are attempting to improve energy efficiency and reduce battery capacity for the same vehicle range. The values shown are based on the standard testing condition as per various testing agencies, which may vary depending on multiple factors, including driving style, route and weather conditions, vehicle equipment and payload [6].

Power electronics modules, essentially based on switch-mode power conversion, are an integrated part of EVs. Figure 2 shows the various power electronics modules used in a battery-electric-vehicle (BEV) powertrain. DC-DC converter finds its application in three main areas. The first one is a bi-directional high-power module (~80 kW), which converts the battery voltage (typically 200-400 V) to 650-800 V (to feed high-power traction inverter as well as to store back the regenerative energy to the battery). Without this converter, we would require a high-voltage battery with a rating that matches the traction inverter, which would raise the price of the battery. Hence DC-DC converter can be considered the core of energy management of EVs as it improves its performance and efficiency [7]. Another DC-DC converter module is low-power, which supplies 12 V EV loads from the battery. Finally, OBC, a medium-power module (~4 kW), is another place where DC-DC converters are used. A typical EV's OBC contains a power-factor-correction AC/DC stage followed by a DC-DC converter. This converter can be bi-directional in case, a vehicle to grid connectivity is required [8].

Passive components, which include inductors, capacitors, filters, heat sinks, and transformers, constitute a large chunk of power converters. Higher switching frequency reduces the size of passive components. However, it fundamentally increases the switching losses (as the number of times switches ON and OFF increases). Reduction in the size of power modules demands a decrement in power loss as well to keep the temperature of components constant [3]. Because the existing surface area is now tiny for heat ejection, this shows that higher power-density requires a simultaneous reduction in power losses. This is where Si stumbles to deliver the technical requirement. Si-based devices suffer from efficiency issues when used for switching frequencies beyond a few kHz, especially for high-power applications [9]. WBG devices such as Gallium nitride (GaN) and Silicon carbide (SiC) can go beyond the limit of Si and are capable of providing higher switching frequency, higher voltage operation, better thermal performance and lower losses.

This paper deals with WBG-GaN (devices and related power modules) only. The journey of GaN embarked in 1940 when Juza and Hanh passed ammonia over hot gallium [10]. Later the industry witnessed its applications in optoelectronics, such as blue and white light-emitting diodes (LEDs), LASER, ultraviolet-emitter, and microwaves [11], [12]. In the quest for higher voltage and frequency, GaN's application extended to power electronics. Figure 3 highlights the various milestones in the development of GaN [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. Although a long way has been covered, GaN is still an immature device. More advancements and significant efforts are still required to deal with the technical challenges in future.

This paper does a comprehensive analysis of the benefits of the material properties of GaN for efficient DC-DC converters and emphasises the design challenges of using GaN. This review article is composed of 7 sections. Following the introduction, section II of this paper describes why GaN is significant for today's power electronics converters. Section III presents the details of the material benefits of GaN. Section IV deals with the challenges of circuit-design on using GaN switches. Section V offers some illustrations of GaN's benefits in DC-DC converters. Section VI identifies and summarises those papers where GaN has been used for DC-DC converter. Finally, section VII gives a design example of a GaN-based buck converter and its superiority analysis over its counterpart.

II. PERTINENCY OF GaN FOR TODAY'S POWER ELECTRONICS

After serving the power electronics industry for decades, Si has reached its material limit and the desired performance of power electronics modules can't be achieved with Si-based

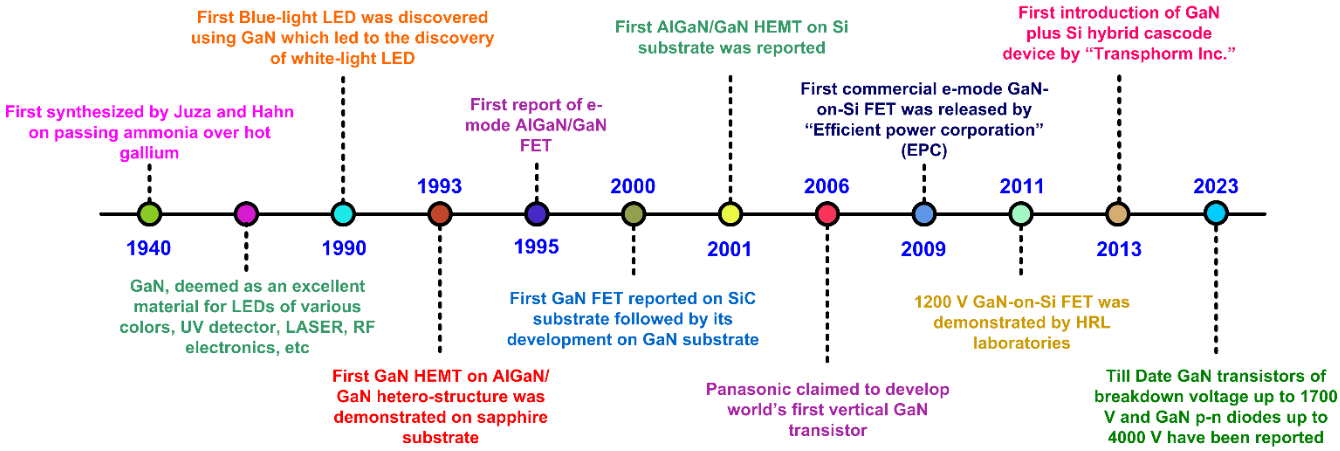

FIGURE 3. Milestones in the advancement of GaN devices.

devices even after enhancement in their structure or fabrication process [25], [26], [27]. As we approach high-power applications, Si-based devices (like MOSFET and IGBT) can't be switched ON or OFF beyond a few kHz because of their thermal limits or low permissible junction temperature. In other words, the switching frequency of Si based devices is limited because of the higher power losses associated with them at increased frequency.

Higher power loss results in higher device temperature, which they cannot bear due to the low thermal limit. This limitation forces the use of bulky cooling components, such as water-filled copper jackets [28]. The thermal management becomes more complex in the harsh ambient environment of EVs drivetrain, especially in hybrid electric vehicles (HEVs) where the temperature goes beyond 120° C in the surroundings of the engine and in the traction inverter, where the power level is more than 100 kW [29]. Moreover, extensive cooling pays off with vehicle weight, size and cost.

Si-based switches, hence, are primarily used at low switching frequencies resulting in increased size of passive components and filters; not desired for EVs application. Using GaN, the necessities of today's power electronics converters, which are characterised by higher operating frequency, higher power-density (lower weight and volume), lower losses, and lower cost, can be fulfilled [30].

To understand how power modules can leverage GaN for efficient EVs, we need to understand the material properties of GaN. Table 1 summarises the various material properties of GaN, SiC and Si [12], [31], [32], [33], [34], [35] and Figure 4 shows the resulting benefits because of the fundamental material properties of GaN.

As Table 1 shows, in comparison with Si, GaN possesses more than 10 times the breakdown electric field, almost 3 times band-gap energy, more than 33% electron mobility, and 10 times more electron drift velocity. These attributes effectively make GaN devices capable of operating at high breakdown voltage (because of wider energy-gap and higher breakdown electric field) and high switching speed (because of higher electron mobility and saturation drift velocity) (figure 4). The high electron mobility of the GaN device is because of the formation of two-dimensional electron gas (2DEG) at its hetero-junction. Higher mobility and breakdown field allow GaN to shrink the die size for a given current and voltage capability [36], [37]. Smaller die size results in lower gate and output capacitance, which further contributes to high switching frequency.

Moreover, the higher breakdown field helps GaN to be optimised with a thin drift-region, which gives lower ON-state resistance ($Rds_{(ON)}$). Higher mobility also helps to achieve lower $Rds_{(ON)}$ and hence increased frequency.

Table 1 also indicates that although GaN excels Si-devices, it lags behind SiC in thermal performance. SiC boasts more than three times better thermal conductivity than GaN, making it suitable for high-temperature and high-power applications (in the range of 100 kW), such as traction inverters and three-phase converters [38]. Moreover, the temperature coefficient of $Rds_{(ON)}$ of GaN is more than that of SiC, i.e. with the rise in operating temperature, GaN shows more variation in $Rds_{(ON)}$. This increases the losses in GaN devices at high temperatures. Better thermal performance (of SiC) positively impacts the size of cooling components and hence the cost. The thermal performance of SiC also indicates that, theoretically, it can serve at a higher power-density than GaN or Si [39], [40]. In this aspect, the relatively poor thermal performance of GaN devices challenges their heat management design.

However, GaN outperforms SiC devices with higher electron mobility (which makes GaN 10 times faster than SiC), higher band-gap energy, lower $Rds_{(ON)}$ (lower conduction loss), and lower junction capacitance (lower switching loss) [41], [42]. In addition, the GaN device has zero reverse recovery (because of no body diode) and lower dead-time loss than SiC devices [38]. The high switching frequency of GaN also helps to reduce passive components' size and hence to gain high power-density, making the converter scalable. It means that for the given power rating, we need a smaller footprint to design a converter. Reducing size demands decrement in power losses to keep the converter temperature

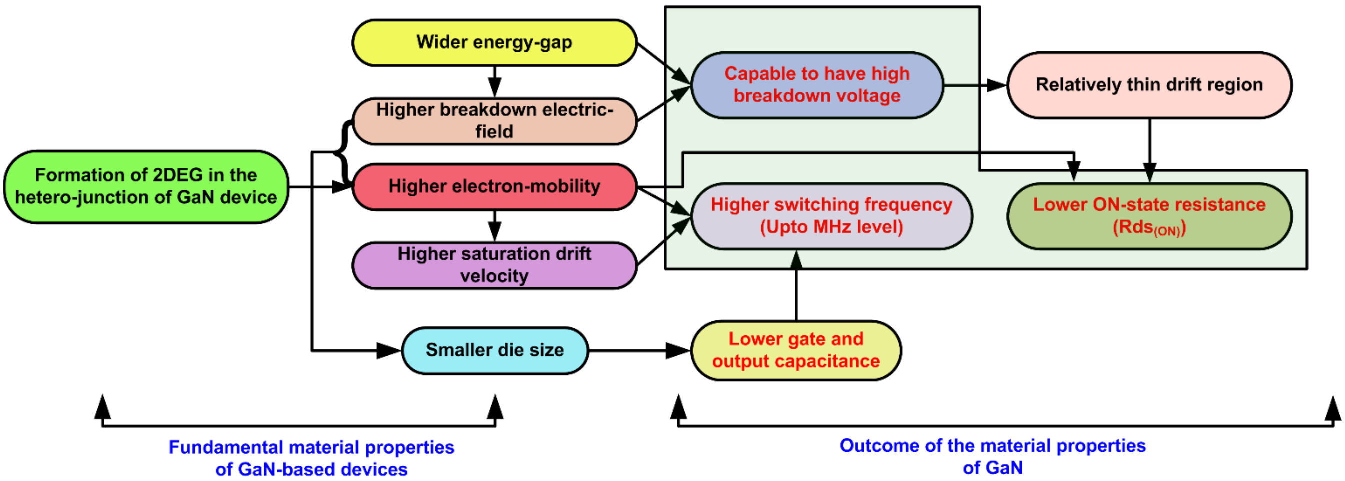

FIGURE 4. Fundamental material attributes of GaN devices.

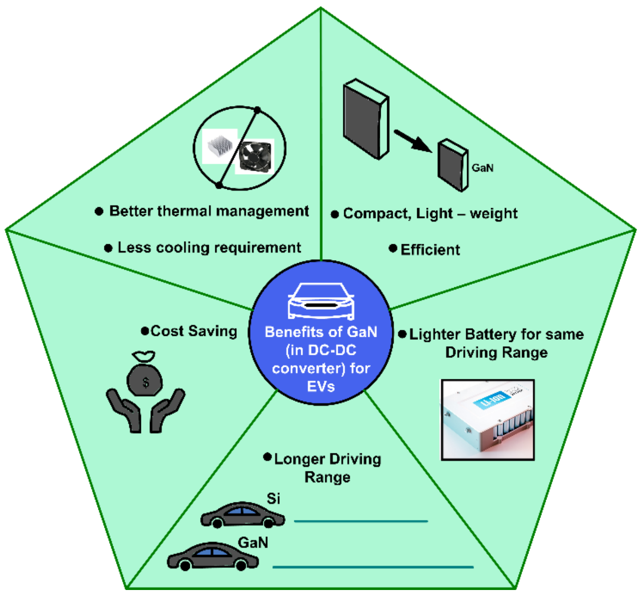

FIGURE 5. Benefits of GaN for electric vehicles.

TABLE 1. Comparison of GaN versus Si and SiC.

S. No	Characteristic	Unit	Semiconductor Material		
			Silicon (Si)	Silicon Carbide (SiC)	Gallium Nitride (GaN)
1.	Band Gap Energy	eV	1.12	3.26	3.4
2.	Breakdown electric field	V/cm	2×10^5	2.2×10^6	3.3×10^6
3.	Dielectric Constant		11.9	9.7	9.0
4.	Electron Mobility at T=300 K	cm^2/Vs	1360	900	2000
5.	Hole Mobility at T= 300 K	cm^2/Vs	480	120	<200
6.	Saturation Electron Drift Velocity	cm/s	8×10^6	2.7×10^7	2.8×10^7
7.	Intrinsic carrier concentration at T=300 K	$/cm^3$	1.5×10^{10}	1.1×10^8	1×10^{10}
8.	Thermal conductivity	W/cm K	1.5	4.56	< 1.5
9.	Max. Junction temp.	ºC	150	175	175
10.	Melting point	K	1.6×10^3	$>2.1\times10^3$	$>1.7\times10^3$

constant. Again, GaN meets the expectation with its lower switching and conduction loss, which further benefits with less cooling requirement and an efficient converter. With an efficient converter, we can have a longer driving range for the given battery capacity. Ultimately it saves the cost. Figure 5 pictorially summarises the benefits of employing GaN devices in the DC-DC converter of EVs. The use of GaN devices can satisfy the necessity of higher voltage, better efficiency, faster switching speed, and higher power-density, enhancing their performance and, subsequently, the performance of the whole vehicle.

III. DETAILED ANALYSIS OF THE MATERIAL BENEFITS OF GaN

GaN has superior material characteristics over Si and SiC, as mentioned in section II. This section gives a thorough explanation of those characteristics and how they contribute to ameliorating the circuit design.

A. LOWER GATE-CHARGE (Q_G) AND LOWER ON-STATE RESISTANCE ($Rds_{(ON)}$)

The time required to charge the parasitic capacitors, essential to turn-ON the MOSFET at a given operating voltage, is small if the gate charge is low. This reduces the switching loss and

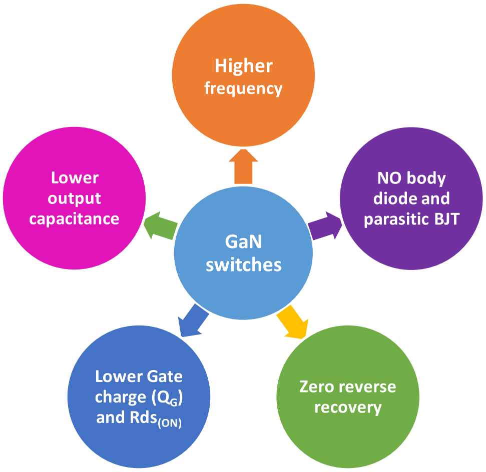

FIGURE 6. Advantages of GaN switches.

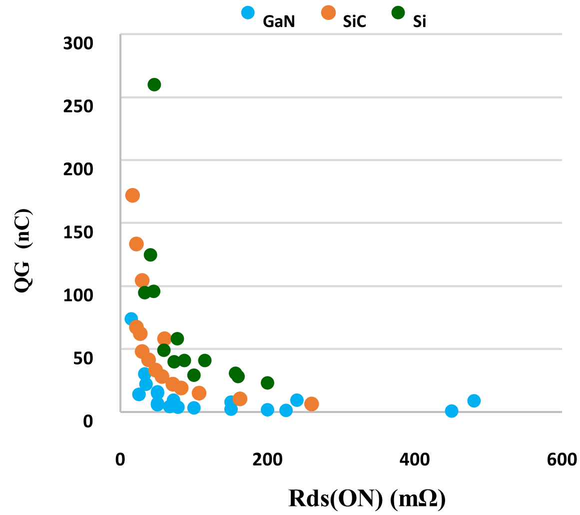

FIGURE 7. Gate-charge FOM comparison of 650 V power switches based on data sheets at 25°C.

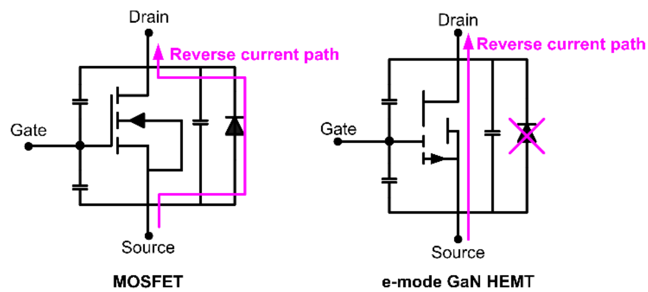

FIGURE 8. Reverse conduction in Si MOSFET and e-mode GaN HEMT [52].

contributes to achieving high switching capability. Smaller die sizes of GaN devices allow them to have lower input and output capacitances [36]. Hence, GaN devices possess lower gate charges compared to Si and SiC devices enabling them for faster-switching transients (faster rise and fall time) and lower switching losses.

However, there is a trade-off between the total gate charge and ON-state resistance. Usually, a smaller die size gives smaller Q_G, but it increases $Rds_{(ON)}$. In other words, since $Rds_{(ON)}$ has direct implications on conduction loss, there will be a conflicting relation between conduction and switching losses because of the smaller die size of GaN [43], [44].

Here come the excellent material properties of GaN devices. Because of the high breakdown field, GaN devices can be optimised with relatively thin drift regions, resulting in lower specific ON resistance. Moreover, its higher electron mobility also contributes to lower $Rds_{(ON)}$ [36]. Thus GaN switches possess lower gate charge as well as lower ON-state resistance resulting in reduced switching, conduction and gate driver losses along with higher switching speed. At a given breakdown voltage, GaN possesses the lowest $Rds_{(ON)}$ among Si, SiC and GaN.

$Rds_{(ON)} \times Q_G$, also known as gate charge figure of merit (FOM), is a common FOM that considers both on-state and switching behaviour. While analysing and comparing the switches of different semiconductor materials, this FOM is an essential tool for it is directly connected with system losses (This is to be noted that lower FOM is considered better) [45]. Figure 7 shows a FOM comparison of different semiconductor devices based on the datasheets of their manufacturers [46], [47], [48], [49], [50], [51]. As the figure depicts, GaN switches have ultra-low FOM showing faster switching and lower gate-drive loss.

B. NO BODY-DIODE, PARASITIC BJT, AND ZERO REVERSE RECOVERY

Like Si MOSFETs, GaN devices available don't have p-n doped body and drift regions (responsible for providing reverse conduction path in Si MOSFETs). Hence GaN devices (most notably, e-mode GaN high electron mobility transistors (HEMTs)) don't have intrinsic body diodes and parasitic BJT between drain and source [36], [52], [53]. However, they have the reverse conduction property the same as Si MOSFETs (as shown in Figure 8) when the gate-to-source voltage (V_{GS}) is zero or negative. The reason behind it lies in the symmetrical behaviour of this device. When the drain to source voltage (V_{DS}) is positive, the 2DEG channel gets turned ON if V_{GS} exceeds the threshold limit (V_{GS_TH}). Likewise, when V_{DS} is negative, the channel turns ON if the gate to drain voltage (V_{GD}) reaches its threshold limit (V_{GD_TH}). The negatively biased drain terminal causes a potential gradient in the channel. This, in turn, generates a negative electrical potential in the depletion region below the gate electrode, which is responsible for turning the device ON for reverse conduction [52]. This phenomenon is also called "self-commutation in reverse-conduction".

This is to be noted that V_{GD_TH} is approximately equal to the specified V_{GS_TH}. If the device is carrying the drain current I_D, the voltage drop in the reverse conduction mode (D_T) is given by

$$D_T = V_{GD\_TH} + (-V_{GS}) + I_D R_{DS\_REV} \tag{1}$$

where R_{DS_REV} represents the channel resistance during reverse conduction and is typically greater than $Rds_{(ON)}$.

Reverse conduction without a body diode gives some real advantages to GaN devices. No body-diode implies no reverse recovery charge (Q_{rr}). Zero Q_{rr} results in lower switching losses. It helps in fast switching as well as provides lower EMI noise (no noise of turning ON the body diode). This makes GaN fit for half-bridge applications with hard and soft switching (Zero Q_{rr} lowers the dead-time, necessary to ascertain zero voltage switching (ZVS)) [54]. There are added benefits of high *dv/dt* ruggedness and reliability. Si MOSFETs show a failure mechanism during reverse recovery [55]. In the absence of a body-diode, GaN HEMT is safe from such failure.

However, the downside is that GaN HEMT experiences a high voltage drop in reverse conduction (D_T), which can be as high as 3-5 V (greater than an equivalent drop in Si MOSFETs). Higher D_T can reduce efficiency by increasing losses in the dead time of a particular circuit. Reducing the dead time can suppress these losses.

C. LOWER OUTPUT CAPACITANCE (C_{OSS})

Output parasitic capacitance (C_{OSS}) of a MOSFET is given by $C_{OSS} = C_{DS} + C_{GD}$, where C_{DS} is the capacitance between the drain and source and C_{GD} is the capacitance between the gate and drain. It is an important parameter that directly impacts the soft-switching performance of a converter. While turning-ON the MOSFET, in the case of ZVS transition, C_{OSS} must be discharged before the switch is turned ON, bringing the drain to source voltage to zero [56]. Owing to the smaller die area, GaN devices offer smaller C_{OSS}. Lower C_{OSS} discharges quickly, leading to lower losses and better soft switching.

The time required to achieve ZVS is given by $t_{zvs} = \frac{Q_{oss}}{I_{zvs}}$, where Q_{OSS} is the output charge of MOSFET and I_{ZVS} is the current required to get ZVS [57]. Lower Q_{OSS} of GaN provides a shorter time to attain soft switching. This also leads to having a shorter delay time and helps in achieving a higher switching frequency.

This is to be noted that with the help of GaN, the switching frequency can be scaled up to MHz. But increased switching frequency comes with increased switching losses. This increases the operating temperature, and consequently, the heat sink size also increases. To overcome this barrier, soft-switching gets essential. Soft-switching provides an apparent reduction in switching losses. Moreover, the severe EMI issue during fast commutations at high frequency is suppressed by soft switching [58]. Which otherwise requires large filters. Lower C_{OSS} of GaN helps to attain better soft switching. So at the same time, we can have a higher frequency, lower switching losses and better EMI immunity.

D. HIGHER FREQUENCY

As discussed in section II of this article, GaN devices enable high-frequency operation, which is the key to shrink the passive components' size and to attain high power-density. Figure 9 shows that GaN devices can be used for frequencies up to 10MHz, which surpasses all other devices [38]. We can also observe that there is an overlapping region below the 10 kW application where Si, SiC and GaN can all be used. However, the maximum switching frequency is limited by losses associated with the devices. Si shows higher losses at higher frequencies; hence, GaN is the best choice for medium-power applications such as on-board chargers, DC-DC converters, etc. From Figure 9, it is also clear that keeping the power constant at around 10 kW, the switching frequency in GaN can be scaled up to MHz. This provides a significant reduction in the volume of transformers, inductors and capacitors saving system cost and space. At high frequencies, a smaller filter size can be achieved and the transformer can be replaced by PCB-based planar transformer with integrated leakage inductance [59]. It means at higher frequencies, the series inductor needed to achieve ZVS (such as in resonant converters) is very small. So by giving adequate air-gap between primary and secondary winding, the leakage inductor can be used as a series inductor [60]. Such integration reduces the volume of magnetic components as well as magnetic losses.

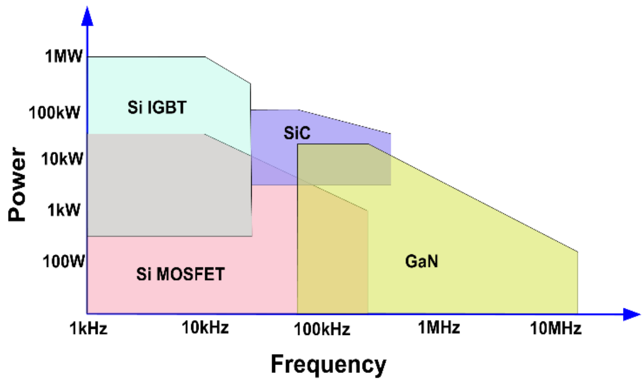

FIGURE 9. Power-level vs frequency mapping of various power devices [38].

Table 2 summarises the eminence of GaN over Si and SiC based on the data sheets of 650 V switches taken as an example.

IV. CHALLENGES IN THE CIRCUIT DESIGN WITH GaN SWITCHES

Although unique features of GaN devices provide a lot of benefits to circuit design engineers in terms of high power-density, lower losses etc., various design challenges arise because of using these new class of devices. There are multiple trade-offs and limitations between the achievable benefits and new drawbacks. These limitations have been classified here and summarized in Figure 10.

A. DEVICE-LEVEL CHALLENGES

The first limitation of the GaN device is regarding its voltage rating. GaN devices are commercially available up to 650 V

TABLE 2. **Comparison showing GaN's superiority based on values from data-sheets.**

Parameters		GaN [61]	Si [62]	SiC [63]	GaN's benefits
Drain-source voltage	V_{DS} ;V	650	650	650	
On-resistance	$R_{DS(ON)}$; mΩ	50	39	48	Comparable $R_{DS(ON)}$
Output capacitance	C_{OSS}; pF	65	885	156	Shorter dead time
Output Charge	Q_{OSS}; nC	57	575	103	Shorter turn-ON time and lower loss
Gate to drain charge	Q_{gd}; nC	1.8	23.5	6.2	Lower switching loss
Total gate charge	Q_g; nC	5.8	80	41	Lower gate-drive loss
Turn-OFF time	t_{off}; ns	2.52	89	68	Lower turn-OFF loss
Reverse-recovery charge	Q_{rr}; nC	0	4000	250	Lower turn-ON loss

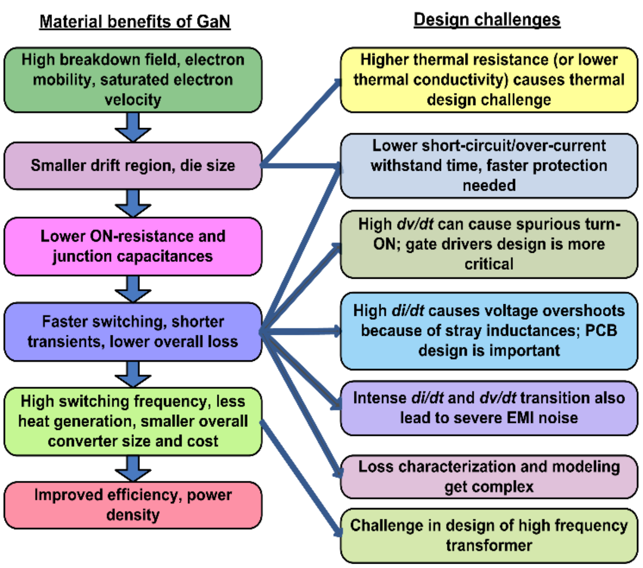

FIGURE 10. **Design challenges on using GaN switches.**

only [36], [64] and therefore, a 650V e-GaN device can't be applied easily in the conventional DC-DC converters of higher voltage rating. For a higher voltage rating, we have to go with the SiC device. This is to be noted that today, GaN transistor up to 1700 V and diode up to 4000 V breakdown voltage is available [65]. However, they are only for research purposes and their techniques are not suitable for large-scale production.

Another major limitation of GaN devices is the commercial non-availability of their vertical structure. The available lateral structure of GaN requires a large chip area [36], [64], [66], [67] if used for converters of high current rating, which also makes the overall area of the converter large. And therefore, it is cumbersome to manufacture the lateral GaN topology for high current and power demand.

B. CHALLENGES WITH THE GATE-DRIVER DESIGN

The high switching frequency and low gate-to-source threshold voltage (typically 1.5V) of the GaN device make the gate voltage of GaN HEMT extremely sensitive to *"miller current"*, parasitic inductance, and noise. Hence, the gate circuit design for high frequency remains an addressable issue in converter design with GaN [68]. There is a small margin between the recommended and maximum V_{GS} of GaN. For example, the typical V_{GS} to turn-ON a GaN FET is 5V, while the maximum V_{GS} is 6V. This shows that we need very precise and accurate V_{GS}, which is difficult to obtain for high-side switches by traditional bootstrapping supply [69], [70]. One of the ways to achieve a clean gate drive signal is to adjust the gate resistance for critical damping.

Another issue is, when GaN switches are used under high dv/dt, which causes unwanted charging of gate-source capacitance (C_{GS}) because of the 'Miller effect'. If the charges in C_{GS} goes beyond the threshold value, this may lead to a spurious turn-ON of the GaN device [71], [72]. Spurious turn-On can also happen if the voltage drop through the resistances of gate-drive loop exceeds the threshold limit of V_{GS} [73]. Therefore the selection of external gate resistance and minimization of the gate-loop parasitic inductance are crucial. A gate driver co-packaged with the switch will have positive impact in this case.

C. HIGH EMI NOISE

Owing to having a low gate charge (Q_G), a GaN FET has a shorter turn-ON time and hence its switching frequency is higher than that of a Si-based device. However, because of the shorter turn-ON time, the GaN devices face intense *di/dt* and *dv/dt* transition, which leads to severe EMI noise. EMI can be suppressed using an input filter, but this increases the overall system cost and volume [74]. Moreover, with the increase in switching frequency, the converter gets smaller and the components of the converter get closer. This equally creates EMI, a significant challenge for engineers to tackle.

D. CHALLENGES WITH THE DESIGN OF MAGNETICS

The design of an isolated DC-DC converter using GaN face the major difficulty in the design of a high-frequency transformer. At megahertz, phenomena like the skin effect and proximity effect come into play, which increases the AC losses [8], [54]. This can be mitigated by using improved core and winding materials and by the integrated design of the magnetic components.

E. PRINTED CIRCUIT BOARD (PCB) LAYOUT DESIGN AND DEVICE PACKAGING

Because of the high switching frequency of GaN devices, PCB layout and device packaging demand proper consideration while designing a power module to lower the associated parasitics. Otherwise they can create overshoot, ringing and EMI issues, overstressing the GaN switches. Good layout practice and technique are essential to maximize the benefits of GaN and converter performance. Moreover, a device with low package inductance enables low-inductance power-loops in PCB.

Common-source-inductance (CSI) is of the most critical parasitic elements. CSI is the summation of the source terminal's inductance (inside the package) and the inductance of lead of the package itself [75]. CSI shares the main current path (which carries the drain-source current) and loop of the gate driver (which carries the gate charging current). The voltage induced in CSI because of high di/dt in the drain-source path alters the effective V_{DS} and V_{GS}, impacting the switching performance, spurious switching and switching losses [76].

The ringing of V_{GS} can even cause gate-breakdown because of its low safety margin. In Si, we increase the gate resistance to dampen the ringing. However, in the case of GaN, such practice is not suggested, for the inherent fast switching of GaN will compromise. So a through-hole (like TO-220) package is not ideal for GaN. Surface-mount-device (SMD) package is better choice for GaN devices. However, thermal management is challenging, for SMD for they rely on PCB for heat transfer [77].

F. OTHER CHALLENGES

1) NECESSITY of SOFT-SWITCHING

A higher switching frequency of GaN devices helps to reduce the size of passive elements of the converter circuit. However, this leads to increased switching loss which is another major challenge. Moreover, the energy loss during turn-ON is more than that during turn-OFF, and hence soft switching is essential for GaN devices [77], [78]. In the absence of soft-switching, rapid transition during the commutation creates a serious EMI issue also.

This is to be noted that stored energy in C_{OSS} in GaN FETs can be recovered easily compared to Si-based MOSFETs. So it is advisable to use soft switching in high frequency application.

2) DEAD-BAND OPTIMIZATION

GaN devices possess a higher voltage drop in reverse-conduction in comparison with that of Si or SiC devices as discussed in section III of this article; the dead-band should be optimized while designing a converter.

3) DRAIN-VOLTAGE RATING

Practically, majority of GaN switches are avalanche-incapable by design [77]. So it is crucial to consider sufficient margin in device voltage rating. Even while transient, the maximum transient voltage should not exceed the rated device voltage. For example, a device with voltage rating 600V is typically sufficient for 480V bus voltage in H- bridge topologies.

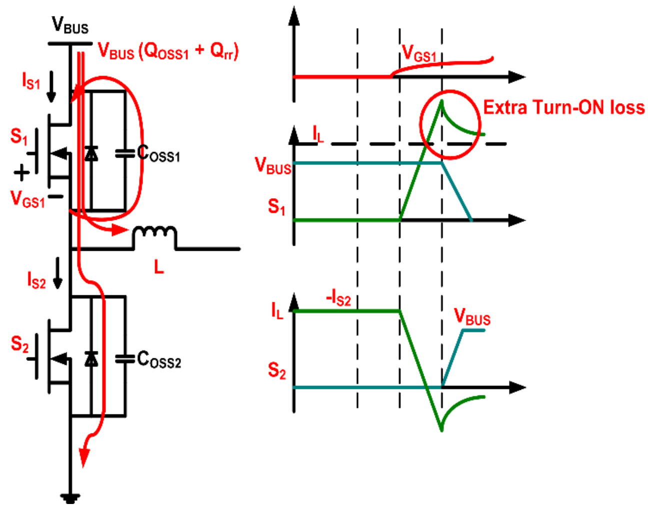

FIGURE 11. Turn-ON loss in SBC because of Qrr.

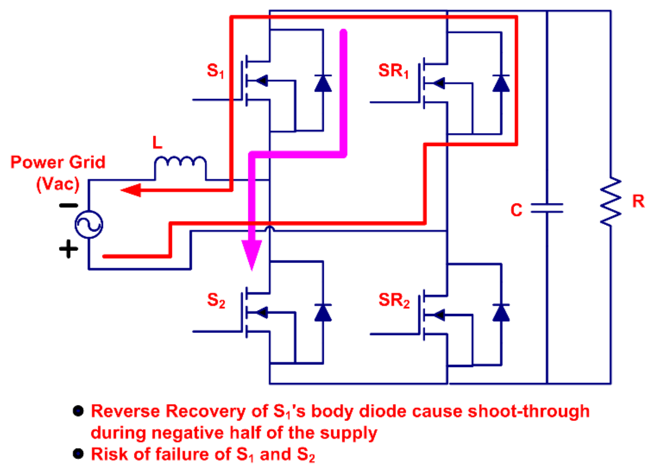

FIGURE 12. Bridgeless Totem-pole PFC circuit.

V. ILLUSTRATIONS OF THE BENEFITS OF GaN SWITCHES IN DC-DC CONVERTER TOPOLOGIES

Application of GaN-switches in DC-DC converter circuits gives advantages to the design engineers. It overcomes a few design barriers which were not possible earlier with the help of Si-based switches. It also enables new topologies, such as totem-pole power-factor correction (PFC) circuits. This section presents few examples of DC-DC converter circuits where the use of GaN solves existing issues to get an efficient and improved converter.

A. SYNCHRONOUS BUCK CONVERTER (SBC)

Two phenomena happen simultaneously when switch S1 is turned ON and S2 is turned OFF at hard-switching. First, C_{OSS1} is discharged, as shown in Figure 11 and energy is lost. Second, a reverse current flows to recover switch S_2. Hence during turning ON switch S_1, there is an overshoot in current flowing through S_1, which creates additional power loss. The total energy lost during this particular period in switch S_1 is [$E = V_{BUS}$ $(Q_{OSS1} + Q_{rr})$], where Q_{OSS1} is the charge stored in the output capacitance of switch S_1 [79]. In the case of

TABLE 3. Summary of GaN-based non-isolated DC-DC converters.

Author	Topology	Switching frequency	Power rating	Efficiency	Power-density	Problem addressed/ Main work	Features	Limitations and drawbacks
Ahmadi et al. [87]	Bi-directional, buck/boost	-	600 W	97.6%	-	Work on a novel topology with soft switching	✓ Zero-voltage-transition for all switches. ✓ Voltage spikes and current stress on switches reduced. ✓ Low conduction losses. ✓ Can be used for wide power range.	✓ More number of switches as compared to conventional buck/boost converter
Huang et al. [88]	Interleaved, bi-directional buck/boost	1 MHz	1.2 kW	98.5%	-	Benefits of GaN switches and improved inductor design	✓ Analysis of the advantages of Inverse-Coupled-Inductor (ICI) on critical-current-mode interleaved buck/boost converter. ✓ Improved soft-switching range and reduced circulating energy during resonance, using ICI.	
Ke et al. [74]	Buck converter	10 MHz	6 W	85.5% (max)	-	Reduction of EMI noise and suppression of switch voltage ringing	✓ Spurious-noise-compression scheme is used to reduce EMI noise ✓ A tri-slope gate-driver is designed for slew rate control and switch-voltage ringing suppression.	✓ Converter becomes more complex and efficiency reduces slightly.
Moradpour et al. [89]	Interleaved, bi-directional boost converter	10 kHz	40 kW	98.2%	-	A high power, two-phase converter design using lateral GaN	✓ To overcome the power rating limitation of lateral GaN, a two-phase converter (one phase with GaN and another with SiC switches) is proposed. ✓ Proposed work gives better efficiency than a converter, using the same topology and all-SiC switches.	✓ Circulating current flows because of unequal sharing of current in two phases, leading additional losses.
Elsayad et al. [90]	Boost converter	100 kHz	1.3 kW	94.6% (max)	-	Novel topology for fuel cell vehicle	✓ Enhanced voltage-gain with wide range ✓ Reduced switch-voltage stress and input current ripple	
Faraji et al. [91]	3-port boost converter	100 kHz	125 W	97%	-	Novel topology with soft switching	✓ Soft-switching is achieved for all the switches using an active-clamp-circuit. ✓ Reduction in the voltage ringing and stress across switches using clamp-circuit	
Agrawal et al. [92]	Buck converter	1 MHz	1 kW	96%	7.8 kW/L (forced air cooling)	Novel soft-switching method	✓ A variable-frequency critical-soft-switching method is presented. ✓ Boundary condition for critical-soft-switching is derived. ✓ Improvement in efficiency of the converter.	
Cui et al. [93]	Synchronous buck converter	-	-	-	-	Integration of gate-driver with half-bridge GaN IC	✓ A half-bridge power stage is monolithically integrated with a gate-driver in smaller die area. ✓ Reduced voltage overshoot. ✓ Reduced ringing due to parasitic inductance. ✓ High thermal stability up to 250 °C	✓ The converter is tested for an input voltage of 15 V to 25 V only.
Moradisizkoohi et al. [94]	Quasi-resonant half-bridge converter	100 kHz	1 kW	97.5%	-	Modular topology with soft switching	✓ Reduced voltage stress of the switches. ✓ Reduced current stress because of parallel modules. ✓ Optimized PCB design to reduce voltage ringing because of parasitic inductor.	✓ Increased number of switches which make design expensive.
Li et al. [59]	6-phase interleaved buck/boost converter	700 kHz	3.5 kW	97.5% (max)	8.7 kW/L (with heatsink)	Improved circuit design	✓ Six-phase interleaved connection is used to obtain high power. ✓ PCB winding negative-coupled inductor is used which provides high power-density.	✓ Controlling of six-phase connection is a challenge.

GaN switches, there is no reverse recovery and Qrr is zero. Hence the said loss is because of Q_{OSS} only [80]. Moreover, GaN switches have lower Q_{OSS} values. This provides less EMI noise and high efficiency. This is worth noting that Q_{rr} worsens with higher temperature, current, voltage rating and faster switching. Hence, GaN switches are best fit for lowering the losses of reverse recovery charges.

B. BRIDGELESS TOTEM-POLE PFC (BTPFC) CIRCUIT

Excellent reverse recovery of GaN (Zero Q_{rr}) enables a new topology of power factor correction, known as a bridgeless totem-pole circuit. This circuit is more efficient and has less switches count than the conventional boost-PFC.

A BTPFC circuit is shown in Figure 12. For power factor correction, switches S_1 and S_2 must be operated at a higher frequency (in the kHz range), while switches SR_1 and SR_2 are operated at line frequency. For the positive and negative half of the AC input, switches S_1 and S_2 are operated respectively for a specific duty cycle (D). For the positive half, when switch S_2 is ON, current flows through L, S_2 and the body diode of SR_2. For the same positive half, when S_2 is OFF, current flows through L, the body diode of S_1, load and body diode of SR_2. A similar operation happens during the negative half, except the switches S_2 and SR_2 are replaced by S_1 and SR_1, respectively.

The inherent issue with the BTPFC circuit is that when the AC input changes from the positive to the negative half, the body diode of the high-side switch S_1 goes under reverse recovery. In the case of Si switches, slow reverse recovery of the body diode results in large current spikes. Therefore, in BTPFC, the high-frequency switches (S_1 and S_2) must have zero or very low reverse recovery [81], [82]. Otherwise, there will be shoot-through and associated power loss. Hence designers don't find Si-MOSFET fit for BTPFC circuits.

TABLE 4. Summary of GaN-based isolated DC-DC converters.

Author	Topology	Switching frequency	Power rating	Efficiency	Power-density	Problem addressed/ Main work	Features	Limitations and drawbacks
Guan et al. [95]	Half-bridge resonant CLCL converter	1 MHz	25 W	88.7%	0.33 kW/L (no cooling used)	Magnetic design and soft-switching	✓ Soft-switching is used both for turn-ON and turn-OFF. ✓ Planar magnetics is used for inductor and transformer.	✓ In the resonant circuit, two planar inductors have been used, which don't allow the power-density to go high. Magnetic integration can be used instead. ✓ Bi-directional power flow is not possible with given converter.
He et al. [8]	Full-bridge resonant CLLC converter	1 MHz	3.3 kW	97%	9.22 kW/L (forced air cooling)	High-frequency magnetic design, magnetic integration and ZVS switching	✓ Skin and proximity losses in high frequency transformer are quantified. ✓ PCB based planar transformer with magnetic-integration is used.	✓ At light load condition efficiency drops and secondary current gets discontinuous.
Liu et al. [96]	Two-stage converter	500 kHz	6.6kW	96%	37 W/in^3 (no cooling used)	Soft-switching range extension, novel topology and novel control strategy	✓ First stage of the design is an interleaved totem-pole boost converter while the second stage is a resonant converter. ✓ To handle high current, parallel channels are used in secondary side of transformer.	✓ Variable DC-link is used, which makes the control strategy complex.
Li et al. [97]	Two-stage converter	500 kHz	6.6 kW	96%	37 W/in^3 (no cooling used)	Magnetic design	✓ For first stage of the converter, PCB winding based positive-coupled inductor is used. ✓ For second stage (dc/dc) a transformer based on PCB winding and EI shaped core is used with leakage integration.	✓ For high-power, magnetic design gets challenging and complex when magnetic integration is used.
Wang et al. [98]	Multi-CLLC resonant converter	1 MHz	400 W	94.3%	53 W/in^3 (no cooling used)	Novel topology	✓ 3 parallel braches are used in the low-voltage side of converter to lower current stress. ✓ PCB based planar transformer is used.	✓ 3 parallel branches in low-voltage side need 3 transformers, affecting efficiency.
Matsumori et al. [99]	Two-stage LLC converter	300 kHz	500 W	~92%	10 W/cm^3	Improved circuit design	✓ A two stage converter including a LLC resonant converter and a boost converter is used to deal the voltage fluctuations. ✓ Soft-switching is achieved using synchronous conduction mode control for entire load range.	✓ MOSFETs used in the design is of higher $Rds_{(ON)}$, which creates high losses.
Ammar et al. [100]	CLLC resonant converter	500 kHz	1 kW	95.7%	-	Novel topology	✓ An additional LC tank is used in the secondary side of transformer. ✓ The input bus voltage range is kept limited to operate the converter at resonant frequency. ✓ Resonant inductances are realized with leakage inductance of transformer.	✓ Reverse conduction of GaN switches in the secondary side account for 33% of total losses. Which is high enough.
Zhang et al. [71]	Stacked bridge LLC converter	1 MHz	3 kW	96.2%	107 W/in^3 (water cooling for secondary side)	Novel topology, improved circuit design for high *dv/dt* issue	✓ This topology uses stacked-bridge arrangement which reduces the voltage-stress of the switches to half. This helps to select a switch with low rating and reduces *dv/dt*. ✓ Matrix transformer used in the topology provides primary series and secondary parallel technique to deal high voltage and current respectively. ✓ Problems because of parasitic capacitance and displacement-current is addressed. To overcome this the resonant tank is split into two parts.	✓ This topology uses 10 switches. So the switch-counts are even more than full-bridge LLC converter.
Abramson et al. [83]	Double-stacked active bridge converter	175 kHz	300 W	97% (max)	-	Novel topology addressing the limitation of DAB converter	✓ This topology uses a double-stacked bridge in the primary side of transformer. Which reduces the voltage stress to one fourth to that in full bridge. ✓ Lower-rating switch has lower output-capacitance, so ZVS can be extended for light load.	✓ Three-winding single-core transformer design and control scheme for the converter is complex.
Jafari et al. [101]	DAB converter	300 kHz	1kW	97.4%	10 kW/L	Enhanced magnetic design	✓ A quasi planar matrix transformer with adjustable tap-changing is used. Which extends the soft-switching range over wide voltage gain.	
Zhang et al. [102]	DAB converter	1 MHz	1.2 kW	97.51 % (peak)	-	Novel approach for magnetic integration	✓ 3 parallel H-Bridge are connected in the low-voltage side of the converter. This reduces the current stress of the switches. ✓ A novel transformer with 3 leg core geometry is designed which replaces 3 discrete transformer.	✓ Because of higher magnetic field, EMI issue will be there, which has not been analysed by the author.
Xue et al. [103]	DAB converter	500 kHz	1 kW	-	-	Improved circuit design	✓ To reduce the size of DC-link capacitor, idea of sinusoidal charging is proposed. ✓ Sinusoidal charging allows a portion or ripple power to go into the battery, reducing the ripple going to the capacitor. So the size of DC-link capacitor is reduced.	✓ Ripple makes the battery get heated. ✓ Output current fluctuates because of sinusoidal charging.
Ramchandran et al. [104]	Full-bridge converter	50 kHz	2.4 kW	98.5%	7 kW/L	Loss modelling of the converter	✓ An ultra-high efficient converter using GaN switches has been demonstrated.	
Cong et al. [105]	Full bridge converter	2 MHz	250 W	90.2%	-	Novel approach of dead-time control for soft switching	✓ To ensure seamless ZVS operation, adequate dead-time is mandatory. A novel approach for dead-time control has been developed.	✓ It improves efficient but the circuit gets complex.
Xue et al. [106]	Flyback converter	280 kHz	45 W	94.5% (peak)	25 W/in^3	Soft-switching method	✓ A resonance in the secondary side is achieved instead of primary for soft-switching. ✓ This shapes the waveform of primary current and its rms value is reduced.	

TABLE 4. *(Continued.)* **Summary of GaN-based isolated DC-DC converters.**

Fu et al. [107]	Two stage converter	1 MHz	200 W	95.1%	130 W/in³	Improved circuit design	✓ A two stage converter is design using interleaved buck in first stage and LLC in the second stage. ✓ For ZVS of buck converter critical current control is used.	✓ Digital controller used for the work gives slow response affecting transient.
Ren et al. [108]	Three level converter	1 MHz	1.5 kW	97.8% (peak)	-	Novel topology	✓ A 3-level converter with 2 output port is designed. ✓ It can work either buck converter or LLC converter. ✓ For LLC a matrix transformer handles the high current	✓ This architecture doesn't provide simultaneous power from both output ports.
Sarkar et al. [109]	Flyback converter	600 kHz	40 W	86.9%	20 W/in³	Improved circuit design	✓ Poor cross regulation of conventional multi-output flyback converter is improved using the reverse conduction of GaN switch.	✓ Converter efficiency is still low.
Sarkar et al. [110]	Multiple-output flyback converter	540 kHz	40 W	88.22%	51 W/in³	Modified circuit to minimise reverse-conduction loss in GaN	✓ A modified PWM is presented, in which by shortening the conduction time and the reverse current in GaN, reverse conduction loss is decreased.	
Bu et al. [111]	Matrix Converter	-	-	-	-	Filter design to mitigate high *dv/dt* issue in GaN	✓ A gate driver circuit is proposed to get high transient-immunity. ✓ Emphasis on PCB design is given to reduce parasitic inductances. ✓ Moreover a *dv/dt* filter is designed	

TABLE 5. **Specifications for Si and GaN-based buck converters.**

SPECIFICATIONS	Si	GaN
1. Load range	50 W to 200 W	50 W to 200 W
2. Input voltage	40 V	40 V
3. Output voltage (V_o)	30 V	30 V
4. Frequency	100 kHz	350kHz
5. ΔV_c (voltage ripple)	1% of V_o	1% of V_o
6. ΔI_L (current ripple)	15% of I_o (Output current)	15% of I_o
7. Inductor value	100μH	25μH
8. Capacitor value	10μF	3.3μF
9. Selected switch	BUK9219-55A	EPC2001
10. Selected diode	MBR745	MBR745
11. Duty ratio	0.75	0.75

Given no body-diode and zero Qrr, GaN is the best fit for BTPFC.

C. DUAL ACTIVE BRIDGE (DAB) CONVERTER

The main downside of a DAB converter is the loss of soft-switching in light-load conditions. Under light-load, in case of higher C_{OSS}, the leakage-inductor current is not sufficient to get the required charging and discharging to obtain ZVS in a given dead time. For DAB, the minimum current required to ascertain the full voltage-transition in C_{OSS} within a specific dead time is given by $I_{l,min} = 2C_{OSS}\left(dV_C/dt\right)$ [83]. Where dV_C is the change in switch capacitance-voltage and dt is the dead time.

Possible solutions for this drawback are to use switches with lower C_{OSS} or to extend and provide enough dead time letting inductor current ramp up. However, the latter results in increased conduction loss. GaN switches, because of their low C_{OSS}, help to get better ZVS and the soft-switching range can also be extended.

TABLE 6. **Loss-breakdown of buck converter.**

	Losses in switch			Loss in diode	Inductor loss	Efficiency
	Conduction loss	Switching loss	Gate drive loss			
Si	51.12 mW	2.103 W	24 mW	17.94 mW	147.21 mW	93.25 %
GaN	15.85 mW	160.56 mW	17.5 mW	15.09 mW	52.64 mW	96.61 %

VI. GaN-BASED DC-DC CONVERTERS

Replacing Si with a GaN device in the given circuit topology invites multiple challenges from a circuit-design point of view, as discussed in the previous section. Worldwide, many researchers are working on GaN-based DC-DC converters for EV applications. To address the design challenges, researchers are working on novel, innovative topologies, improved transformer and inductor designs (such as magnetic integration), and new magnetic materials. As well as they are working on a modified design of PCB, gate drivers, soft-switching circuits etc. This section of the article identifies those works to understand the existing approaches and solutions implemented by the various authors using GaN switches. The converters have been reviewed on the basis of their various features, such as topology structure, characteristics, operation, merits, and demerits. For the sake of clarity this work has been divided into isolated and non-isolated DC-DC converters in Table 3 and 4, respectively.

VII. DESIGN EXAMPLE OF A BUCK CONVERTER USING GaN SWITCHES

To authenticate the superiority of GaN switches over Si, a design example of a buck converter is presented in this section. A comparative analysis of power losses and efficiency is done after the design and simulation of a buck converter in LTspice. Specifications of both converters are presented in Table 5. An e-GaN FET (EPC2001) [84] and a Si MOSFET (BUK9219-55A) [85] are selected for the analysis based on the specifications. The switching frequency is taken as 100 kHz and 350 kHz for Si and GaN switches, respectively. Table 5 clearly indicates the benefits of the higher switching frequency of e-GaN FET in terms of reduction in the size of the inductor and capacitor.

Losses and efficiency calculations of both the converters are done based on standard equations [86]. Loss-breakdown is shown in Table 6. While the Si-based buck converter shows an efficiency of 93.25%, the one based on e-GaN FET boosts the efficiency to 96.61%. The major power loss component in the converter is switching loss and losses in passive elements. Losses in passive components are because of their equivalent series resistance. Table 6 identifies the lower switch losses in e-GaN FET because of the lower on-state resistance and lower gate charge of GaN switches.

VIII. CONCLUSION AND FUTURE ASPECTS

The elementary motive of this review paper is to come out with the updated research status of the GaN-based DC-DC converter circuits and the research gap, primarily for EV applications. The use of electric vehicles is the need of today's time because of the threat of climate change and the hike in oil prices. Researchers and engineers are working towards the performance enhancement of converters, which is an essential part of EVs. Converters based on GaN devices inherently obtain higher power density and efficiency than converters based on Si devices. On the contrary, we have to compromise with the cost of GaN devices and there are numerous other challenges. Therefore, to have optimum benefits, we need to consider the topology, the devices, and the magnetic materials used in the converter altogether. Since the GaN power switch has not reached its maturity stage, future research work should be focused to optimize the characteristics of GaN switches. On the one hand, we need to continue exploring the new topologies of the converter, while on the other hand, there are opportunities in improving the performance of the converter by adopting new materials and designs for the transformer and inductor, including magnetic integration. Future research should also focus on power train integration in EVs in order to reduce the part counts. For this, one of the ideas is to develop such topologies which can have both AC and DC outputs or which can have DC voltages at two different levels to be used in EVs at two different voltage buses. EMI remains a major issue that arises because of the high frequency caused by the use of GaN switches, which need to be addressed thoroughly. As the number of accessories in EVs is increasing with time, power converters with high power ratings should be the desired goal. Eventually, as renewable energy is being integrated with EVs and EVs are being integrated with the grid, critical research work should be carried out to improve reliability, power quality, cost, and efficiency.

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